AD7837/AD7847–SPECIFICATIONS[1] (V_{DD} = +15 V ± 5%, V_{SS} = –15 V ± 5%, AGNDA = AGNDB = DGND = 0 V. V_{REFA} = V_{REFB} = +10 V, R_L = 2 kΩ, C_L = 100 pF [V_{OUT} connected to R_{FB} AD7837]. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version	B Version	S Version	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[2]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[2]	±1	±1	±1	LSB max	Guaranteed Monotonic
Zero Code Offset Error[2]					
@ +25°C	±2	±2	±2	mV max	DAC Latch Loaded with All 0s
T_{MIN} to T_{MAX}	±4	±3	±4	mV max	Temperature Coefficient = ±5 µV/°C typ
Gain Error[2]					
@ +25°C	±4	±2	±4	LSB max	DAC Latch Loaded with All 1s
T_{MIN} to T_{MAX}	±5	±3	±5	LSB max	Temperature Coefficient = ±2 ppm of FSR/°C typ
REFERENCE INPUTS					
V_{REF} Input Resistance	8/13	8/13	8/13	kΩ min/max	Typical Input Resistance = 10 kΩ
V_{REFA}, V_{REFB} Resistance Matching	±2	±2	±2	% max	Typically ±0.25%
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current	±1	±1	±1	µA max	Digital Inputs at 0 V and V_{DD}
Input Capacitance[3]	8	8	8	pF max	
ANALOG OUTPUTS					
DC Output Impedance	0.2	0.2	0.2	Ω typ	
Short Circuit Current	11	11	11	mA typ	V_{OUT} Connected to AGND
POWER REQUIREMENTS[4]					
V_{DD} Range	14.25/15.75	14.25/15.75	14.25/15.75	V min/max	
V_{SS} Range	–14.25/–15.75	–14.25/–15.75	–14.25/–15.75	V min/max	
Power Supply Rejection					
$\Delta Gain/\Delta V_{DD}$	±0.01	±0.01	±0.01	% per % max	V_{DD} = 15 V ± 5%, V_{REF} = –10 V
$\Delta Gain/\Delta V_{SS}$	±0.01	±0.01	±0.01	% per % max	V_{SS} = –15 V ± 5%, V_{REF} = +10 V
I_{DD}	8	8	8	mA max	Outputs Unloaded. Inputs at Thresholds. Typically 5 mA
I_{SS}	6	6	6	mA max	Outputs Unloaded. Inputs at Thresholds. Typically 3 mA
AC CHARACTERISTICS[2, 3]					
Voltage Output Settling Time	3	3	3	µs typ	Settling Time to Within ±1/2 LSB of Final Value. DAC Latch Alternately Loaded with All 0s and All 1s
	5	5	5	µs max	
Slew Rate	11	11	11	V/µs typ	
Digital-to-Analog Glitch Impulse	10	10	10	nV secs typ	1 LSB Change Around Major Carry
Channel-to-Channel Isolation					
V_{REFA} to V_{OUTB}	–95	–95	–95	dB typ	V_{REFA} = 20 V p-p, 10 kHz Sine Wave. DAC Latches Loaded with All 0s
V_{REFB} to V_{OUTA}	–95	–95	–95	dB typ	V_{REFB} = 20 V p-p, 10 kHz Sine Wave. DAC Latches Loaded with All 0s
Multiplying Feedthrough Error	–90	–90	–90	dB typ	V_{REF} = 20 V p-p, 10 kHz Sine Wave. DAC Latch Loaded with All 0s
Unity Gain Small Signal BW	750	750	750	kHz typ	V_{REF} = 100 mV p-p Sine Wave. DAC Latch Loaded with All 1s
Full Power BW	175	175	175	kHz typ	V_{REF} = 20 V p-p Sine Wave. DAC Latch Loaded with All 1s
Total Harmonic Distortion	–88	–88	–88	dB typ	V_{REF} = 6 V rms, 1 kHz. DAC Latch Loaded with All 1s
Digital Crosstalk	1	1	1	nV secs typ	Code Transition from All 0s to All 1s and Vice Versa
Output Noise Voltage @ +25°C					See Typical Performance Graphs
(0.1 Hz to 10 Hz)	2	2	2	µV rms typ	Amplifier Noise and Johnson Noise of R_{FB}
Digital Feedthrough	1	1	1	nV secs typ	

NOTES
[1]Temperature ranges are as follows: A, B Versions, –40°C to +85°C; S Version, –55°C to +125°C.
[2]See Terminology.
[3]Guaranteed by design and characterization, not production tested.
[4]The Devices are functional with V_{DD}/V_{SS} = ±12 V (See typical performance graphs.).

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2, 3] (V_{DD} = +15 V ± 5%, V_{SS} = –15 V ± 5%, AGNDA = AGNDB = DGND = 0 V)

Parameter	Limit at T_{MIN}, T_{MAX} (All Versions)	Unit	Conditions/Comments
t_1	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	30	ns min	$\overline{WR}$ Pulsewidth
t_4	80	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5	0	ns min	Data Valid to $\overline{WR}$ Hold Time
t_6[4]	0	ns min	Address to $\overline{WR}$ Setup Time
t_7[4]	0	ns min	Address to $\overline{WR}$ Hold Time
t_8[4]	50	ns min	$\overline{LDAC}$ Pulsewidth

NOTES
[1]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 3 and 5.
[3]Guaranteed by design and characterization, not production tested.
[4]AD7837 only.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND, AGNDA, AGNDB . . . . . –0.3 V to +17 V
V_{SS}[1] to DGND, AGNDA, AGNDB . . . . . +0.3 V to –17 V
V_{REFA}, V_{REFB} to AGNDA, AGNDB
. . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
AGNDA, AGNDB to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
V_{OUTA}[2], V_{OUTB}[2] to AGNDA, AGNDB
. . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
R_{FBA}[3], R_{FBB}[3] to AGNDA, AGNDB
. . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
Digital Inputs to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Commercial/Industrial (A, B Versions) . . . –40°C to +85°C
Extended (S Version) . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . 300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTES
[1]If V_{SS} is open circuited with V_{DD} and either AGND applied, the V_{SS} pin will float positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode connected between V_{SS} and AGND (cathode to AGND) ensures the Maximum Ratings will be observed.
[2]The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.
[3]AD7837 only.

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Package Option[2]
AD7837AN	–40°C to +85°C	±1 LSB	N-24
AD7837BN	–40°C to +85°C	±1/2 LSB	N-24
AD7837AR	–40°C to +85°C	±1 LSB	R-24
AD7837BR	–40°C to +85°C	±1/2 LSB	R-24
AD7837AQ	–40°C to +85°C	±1 LSB	Q-24
AD7837BQ	–40°C to +85°C	±1/2 LSB	Q-24
AD7837SQ	–55°C to +125°C	±1 LSB	Q-24
AD7847AN	–40°C to +85°C	±1 LSB	N-24
AD7847BN	–40°C to +85°C	±1/2 LSB	N-24
AD7847AR	–40°C to +85°C	±1 LSB	R-24
AD7847BR	–40°C to +85°C	±1/2 LSB	R-24
AD7847AQ	–40°C to +85°C	±1 LSB	Q-24
AD7847BQ	–40°C to +85°C	±1/2 LSB	Q-24
AD7847SQ	–55°C to +125°C	±1 LSB	Q-24

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number.
[2]N = Plastic DIP; Q = Cerdip; R = SOIC.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

Relative Accuracy (Linearity)
Relative accuracy, or endpoint linearity, is a measure of the maximum deviation of the DAC transfer function from a straight line passing through the endpoints. It is measured after allowing for zero and full-scale errors and is expressed in LSBs or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB or less over the operating temperature range ensures monotonicity.

Zero Code Offset Error
Zero code offset error is the error in output voltage from V_{OUTA} or V_{OUTB} with all 0s loaded into the DAC latches. It is due to a combination of the DAC leakage current and offset errors in the output amplifier.

Gain Error
Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded. It does not include offset error.

Total Harmonic Distortion
This is the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental, expressed in dBs.

Multiplying Feedthrough Error
This is an ac error due to capacitive feedthrough from the V_{REF} input to V_{OUT} of the same DAC when the DAC latch is loaded with all 0s.

Channel-to-Channel Isolation
This is an ac error due to capacitive feedthrough from the V_{REF} input on one DAC to V_{OUT} on the other DAC. It is measured with the DAC latches loaded with all 0s.

Digital Feedthrough
Digital feedthrough is the glitch impulse injected from the digital inputs to the analog output when the data inputs change state, but the data in the DAC latches is not changed.

For the AD7837, it is measured with $\overline{LDAC}$ held high. For the AD7847, it is measured with $\overline{CSA}$ and $\overline{CSB}$ held high.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one converter due to a change in digital code on the DAC latch of the other converter. It is specified in nV secs.

Digital-to-Analog Glitch Impulse
This is the voltage spike that appears at the output of the DAC when the digital code changes, before the output settles to its final value. The energy in the glitch is specified in nV secs and is measured for a 1 LSB change around the major carry transition (0111 1111 1111 to 1000 0000 0000 and vice versa).

Unity Gain Small Signal Bandwidth
This is the frequency at which the small signal voltage output from the output amplifier is 3 dB below its dc level. It is measured with the DAC latch loaded with all 1s.

Full Power Bandwidth
This is the maximum frequency for which a sinusoidal input signal will produce full output at rated load with a distortion less than 3%. It is measured with the DAC latch loaded with all 1s.

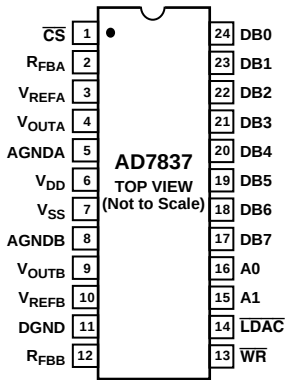
AD7837 PIN FUNCTION DESCRIPTION (DIP AND SOIC PIN NUMBERS)

Pin	Mnemonic	Description
1	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
2	R_{FBA}	Amplifier Feedback Resistor for DAC A.
3	V_{REFA}	Reference Input Voltage for DAC A. This may be an ac or dc signal.
4	V_{OUTA}	Analog Output Voltage from DAC A.
5	AGNDA	Analog Ground for DAC A.
6	V_{DD}	Positive Power Supply.
7	V_{SS}	Negative Power Supply.
8	AGNDB	Analog Ground for DAC B.
9	V_{OUTB}	Analog Output Voltage from DAC B.
10	V_{REFB}	Reference Input Voltage for DAC B. This may be an ac or dc signal.
11	DGND	Digital Ground. Ground reference for digital circuitry.
12	R_{FBB}	Amplifier Feedback Resistor for DAC B.
13	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CS}$, A0 and A1 to write data to the input latches.
14	$\overline{LDAC}$	DAC Update Logic Input. Data is transferred from the input latches to the DAC latches when $\overline{LDAC}$ is taken low.
15	A1	Address Input. Most significant address input for input latches (see Table II).
16	A0	Address Input. Least significant address input for input latches (see Table II).
17–20	DB7–DB4	Data Bit 7 to Data Bit 4.
21–24	DB3–DB0	Data Bit 3 to Data Bit 0 (LSB) or Data Bit 11 (MSB) to Data Bit 8.

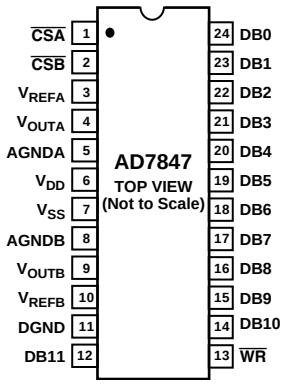
AD7847 PIN FUNCTION DESCRIPTION (DIP AND SOIC PIN NUMBERS)

Pin	Mnemonic	Description
1	$\overline{CSA}$	Chip Select Input for DAC A. Active low logic input. DAC A is selected when this input is low.
2	$\overline{CSB}$	Chip Select Input for DAC B. Active low logic input. DAC B is selected when this input is low.
3	V_{REFA}	Reference Input Voltage for DAC A. This may be an ac or dc signal.
4	V_{OUTA}	Analog Output Voltage from DAC A.
5	AGNDA	Analog Ground for DAC A.
6	V_{DD}	Positive Power Supply.
7	V_{SS}	Negative Power Supply.
8	AGNDB	Analog Ground for DAC B.
9	V_{OUTB}	Analog Output Voltage from DAC B.
10	V_{REFB}	Reference Input Voltage for DAC B. This may be an ac or dc signal.
11	DGND	Digital Ground.
12	DB11	Data Bit 11 (MSB).
13	$\overline{WR}$	Write Input. $\overline{WR}$ is a positive edge triggered input which is used in conjunction with $\overline{CSA}$ and $\overline{CSB}$ to write data to the DAC latches.
14–24	DB10–DB0	Data Bit 10 to Data Bit 0 (LSB).

AD7837 PIN CONFIGURATION
DIP AND SOIC



AD7847 PIN CONFIGURATION
DIP AND SOIC



AD7837/AD7847–Typical Performance Graphs

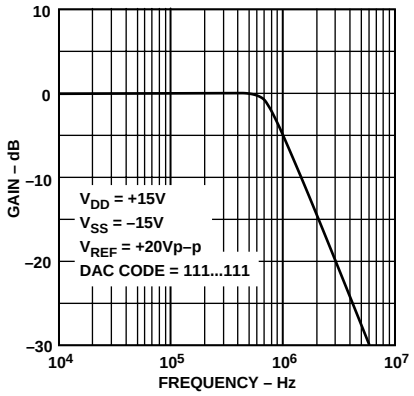


Figure 1. Frequency Response

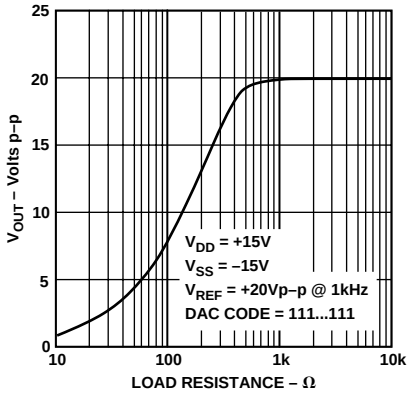


Figure 2. Output Voltage Swing vs. Resistive Load

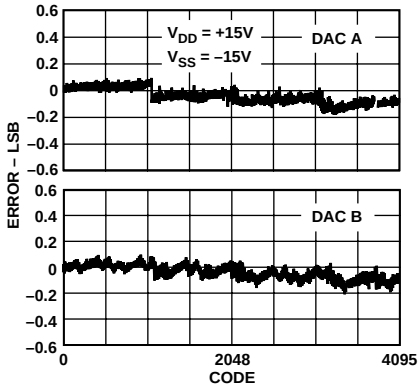


Figure 3. DAC-to-DAC Linearity Matching

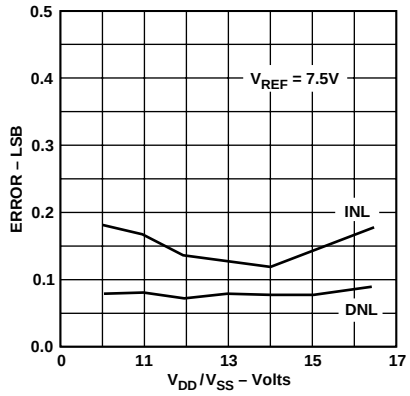


Figure 4. Linearity vs. Power Supply

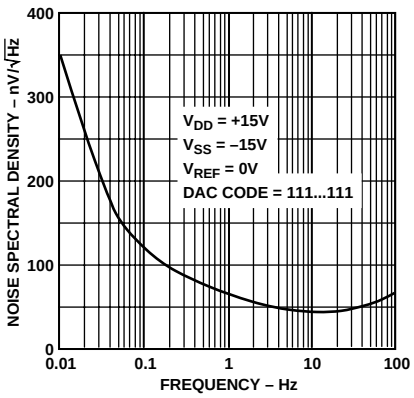


Figure 5. Noise Spectral Density vs. Frequency

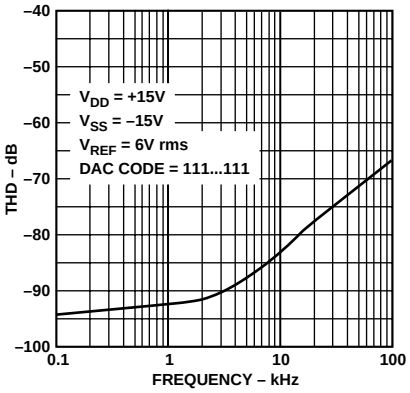


Figure 6. THD vs. Frequency

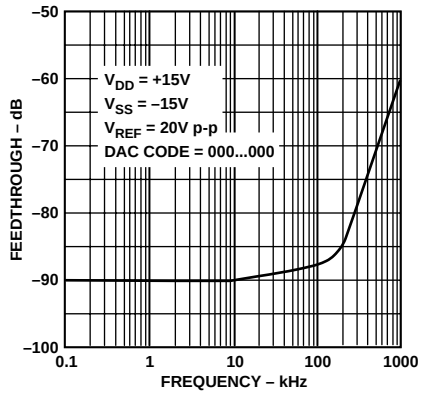


Figure 7. Multiplying Feedthrough Error vs. Frequency

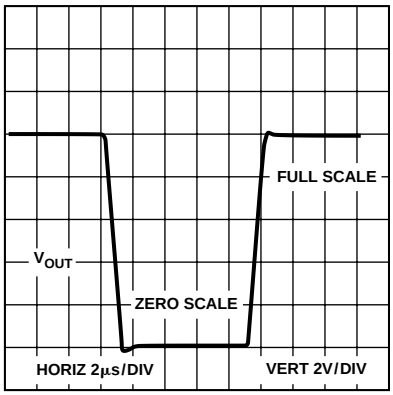


Figure 8. Large Signal Pulse Response

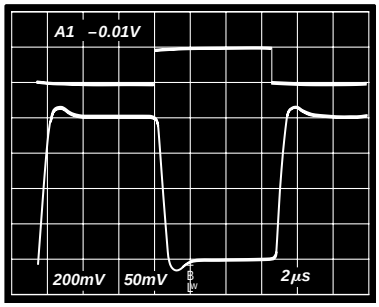


Figure 9. Small Signal Pulse Response

CIRCUIT INFORMATION

D/A SECTION

A simplified circuit diagram for one of the D/A converters and output amplifier is shown in Figure 10.

A segmented scheme is used whereby the 2 MSBs of the 12-bit data word are decoded to drive the three switches A-C. The remaining 10 bits drive the switches (S0–S9) in a standard R-2R ladder configuration.

Each of the switches A–C steers 1/4 of the total reference current with the remaining 1/4 passing through the R-2R section.

The output amplifier and feedback resistor perform the current to voltage conversion giving

$$V_{OUT} = -D \times V_{REF}$$

where D is the fractional representation of the digital word. (D can be set from 0 to 4095/4096.)

The output amplifier can maintain ±10 V across a 2 kΩ load. It is internally compensated and settles to 0.01% FSR (1/2 LSB) in less than 5 µs. Note that on the AD7837, V_{OUT} must be connected externally to R_{FB}.

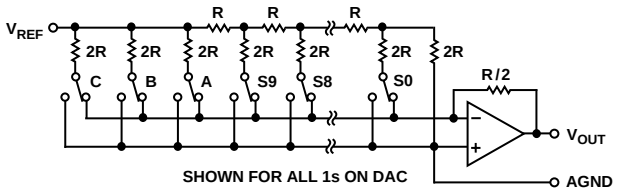


Figure 10. D/A Simplified Circuit Diagram

INTERFACE LOGIC INFORMATION—AD7847

The input control logic for the AD7847 is shown in Figure 11. The part contains a 12-bit latch for each DAC. It can be treated as two independent DACs, each with its own $\overline{CS}$ input and a common $\overline{WR}$ input. $\overline{CSA}$ and $\overline{WR}$ control the loading of data to the DAC A latch, while $\overline{CSB}$ and $\overline{WR}$ control the loading of the DAC B latch. The latches are edge triggered so that input data is latched to the respective latch on the rising edge of $\overline{WR}$. If $\overline{CSA}$ and $\overline{CSB}$ are both low and $\overline{WR}$ is taken high, the same data will be latched to both DAC latches. The control logic truth table is shown in Table I, while the write cycle timing diagram for the part is shown in Figure 12.

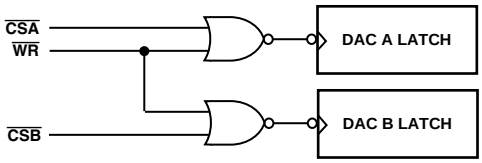


Figure 11. AD7847 Input Control Logic

Table I. AD7847 Truth Table

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	Function
X	X	1	No Data Transfer
1	1	X	No Data Transfer
0	1	↓	Data Latched to DAC A
1	0	↓	Data Latched to DAC B
0	0	↓	Data Latched to Both DACs
↓	1	0	Data Latched to DAC A
1	↓	0	Data Latched to DAC B
↓	↓	0	Data Latched to Both DACs

X = Don't Care. ↓ = Rising Edge Triggered.

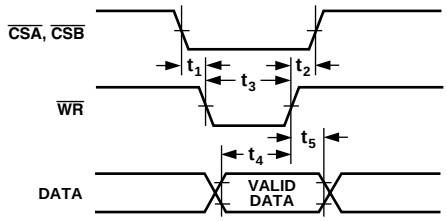


Figure 12. AD7847 Write Cycle Timing Diagram

INTERFACE LOGIC INFORMATION—AD7837

The input loading structure on the AD7837 is configured for interfacing to microprocessors with an 8-bit-wide data bus. The part contains two 12-bit latches per DAC—an input latch and a DAC latch. Each input latch is further subdivided into a least-significant 8-bit latch and a most-significant 4-bit latch. Only the data held in the DAC latches determines the outputs from the part. The input control logic for the AD7837 is shown in Figure 13, while the write cycle timing diagram is shown in Figure 14.

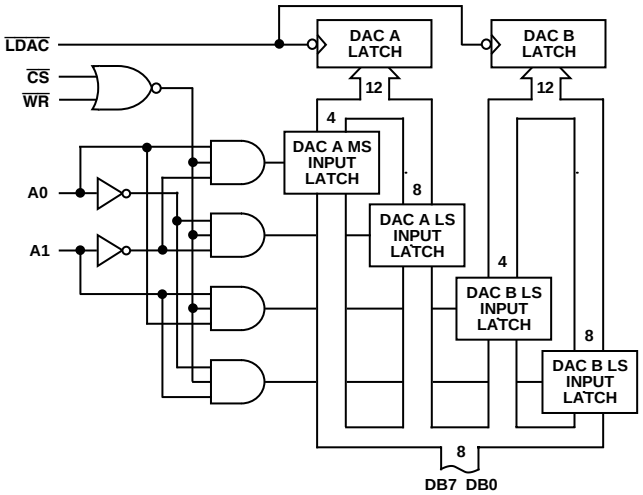


Figure 13. AD7837 Input Control Logic

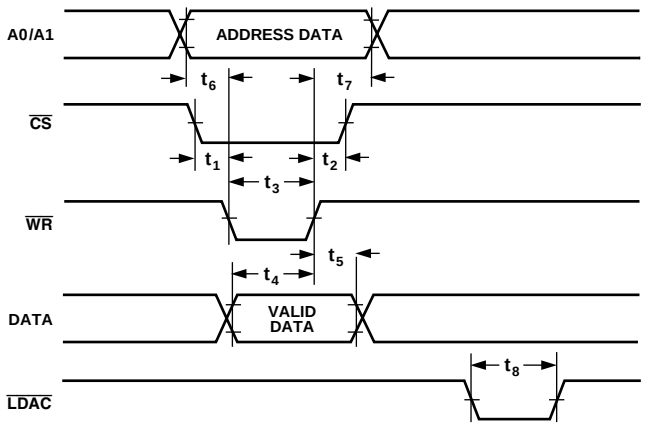


Figure 14. AD7837 Write Cycle Timing Diagram

$\overline{CS}$, $\overline{WR}$, A0 and A1 control the loading of data to the input latches. The eight data inputs accept right-justified data. Data can be loaded to the input latches in any sequence. Provided that $\overline{LDAC}$ is held high, there is no analog output change as a result of loading data to the input latches. Address lines A0 and A1 determine which latch data is loaded to when $\overline{CS}$ and $\overline{WR}$ are low. The control logic truth table for the part is shown in Table II.

Table II. AD7837 Truth Table

$\overline{CS}$	$\overline{WR}$	A1	A0	$\overline{LDAC}$	Function
1	X	X	X	1	No Data Transfer
X	1	X	X	1	No Data Transfer
0	0	0	0	1	DAC A LS Input Latch Transparent
0	0	0	1	1	DAC A MS Input Latch Transparent
0	0	1	0	1	DAC B LS Input Latch Transparent
0	0	1	1	1	DAC B MS Input Latch Transparent
1	1	X	X	0	DAC A and DAC B DAC Latches Updated Simultaneously from the Respective Input Latches

X = Don't Care.

The $\overline{LDAC}$ input controls the transfer of 12-bit data from the input latches to the DAC latches. When $\overline{LDAC}$ is taken low, both DAC latches, and hence both analog outputs, are updated at the same time. The data in the DAC latches is held on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ input is asynchronous and independent of $\overline{WR}$. This is useful in many applications especially in the simultaneous updating of multiple AD7837s. However, care must be taken while exercising $\overline{LDAC}$ during a write cycle. If an $\overline{LDAC}$ operation overlaps a $\overline{CS}$ and $\overline{WR}$ operation, there is a possibility of invalid data being latched to the output. To avoid this, $\overline{LDAC}$ must remain low after $\overline{CS}$ or $\overline{WR}$ return high for a period equal to or greater than t_8, the minimum $\overline{LDAC}$ pulsewidth.

UNIPOLAR BINARY OPERATION

Figure 15 shows DAC A on the AD7837/AD7847 connected for unipolar binary operation. Similar connections apply for DAC B. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication. The code table for this circuit is shown in Table III. Note that on the AD7847 the feedback resistor R_{FB} is internally connected to V_{OUT}.

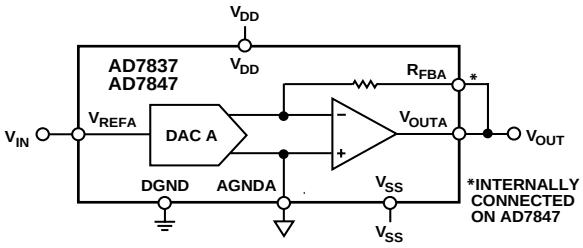


Figure 15. Unipolar Binary Operation

Table III. Unipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$-V_{IN} \times \left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN} \times \left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000 0000 0001	$-V_{IN} \times \left(\frac{1}{4096}\right)$
0000 0000 0000	0 V

Note 1 LSB = $\frac{V_{IN}}{4096}$.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 16 shows the AD7837/AD7847 connected for bipolar operation. The coding is offset binary as shown in Table IV. When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication. To maintain the gain error specifications, resistors R1, R2 and R3 should be ratio matched to 0.01%. Note that on the AD7847 the feedback resistor R_{FB} is internally connected to V_{OUT}.

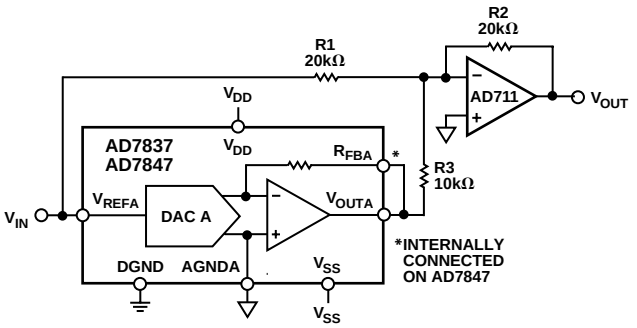


Figure 16. Bipolar Offset Binary Operation

Table IV. Bipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{IN} \times \left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN} \times \left(\frac{1}{2048}\right)$
1000 0000 0000	0 V
0111 1111 1111	$-V_{IN} \times \left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN} \times \left(\frac{2048}{2048}\right) = -V_{IN}$

Note 1 LSB = $\frac{V_{IN}}{2048}$.

APPLICATIONS

PROGRAMMABLE GAIN AMPLIFIER (PGA)

The dual DAC/amplifier combination along with access to R_{FB} make the AD7837 ideal as a programmable gain amplifier. In this application, the DAC functions as a programmable resistor in the amplifier feedback loop. This type of configuration is shown in Figure 17 and is suitable for ac gain control. The circuit consists of two PGAs in series. Use of a dual configuration provides greater accuracy over a wider dynamic range than a single PGA solution. The overall system gain is the product of the individual gain stages. The effective gains for each stage are controlled by the DAC codes. As the code decreases, the effective DAC resistance increases, and so the gain also increases.

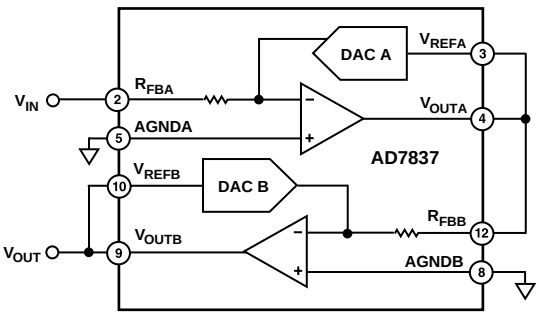


Figure 17. Dual PGA Circuit

The transfer function is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_{EQA}}{R_{FBA}} \times \frac{R_{EQB}}{R_{FBB}} \quad (1)$$

where R_{EQA}, R_{EQB} are the effective DAC resistances controlled by the digital input code:

$$R_{EQ} = \frac{2^{12} R_{IN}}{N} \quad (2)$$

where R_{IN} is the DAC input resistance and is equal to R_{FB} and N = DAC input code in decimal.

The transfer function in (1) thus simplifies to

$$\frac{V_{OUT}}{V_{IN}} = \frac{2^{12}}{N_A} \times \frac{2^{12}}{N_B} \quad (3)$$

where N_A = DAC A input code in decimal and N_B = DAC B input code in decimal.

N_A, N_B may be programmed between 1 and (2^{12}–1). The zero code is not allowed as it results in an open loop amplifier response. To minimize errors, the digital codes N_A and N_B should be chosen to be equal to or as close as possible to each other to achieve the required gain.

ANALOG PANNING CIRCUIT

In audio applications it is often necessary to digitally "pan" or split a single signal source into a two-channel signal while maintaining the total power delivered to both channels constant. This may be done very simply by feeding the signal into the V_{REF} input of both DACs. The digital codes are chosen such that the code applied to DAC B is the two's complement of that applied to DAC A. In this way the signal may be panned between both channels as the digital code is changed. The total power variation with this arrangement is 3 dB.

For applications which require more precise power control the circuit shown in Figure 18 may be used. This circuit requires the AD7837/AD7847, an AD712 dual op amp and eight equal value resistors.

Again both channels are driven with two's complementary data. The maximum power variation using this circuit is only 0.5 dBs.

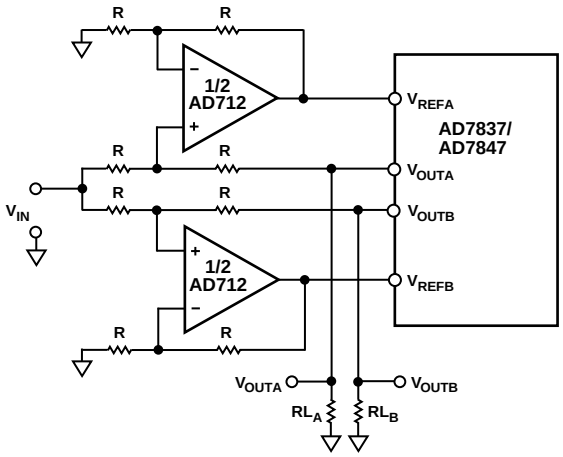


Figure 18. Analog Panning Circuit

The voltage output expressions for the two channels are as follows:

$$V_{OUTA} = -V_{IN}\left(\frac{N_A}{2^{12}+N_A}\right)$$

$$V_{OUTB} = -V_{IN}\left(\frac{N_B}{2^{12}+N_B}\right)$$

where N_A = DAC A input code in decimal ($1 \leq N_A \leq 4095$)

and N_B = DAC B input code in decimal ($1 \leq N_B \leq 4095$)

with N_B = 2s complement of N_A.

The two's complement relationship between N_A and N_B causes N_B to increase as N_A decreases and vice versa.

Hence $N_A + N_B = 4096$.

With N_A = 2048, then N_B = 2048 also; this gives the balanced condition where the power is split equally between both channels. The total power variation as the signal is fully panned from Channel B to Channel A is shown in Figure 19.

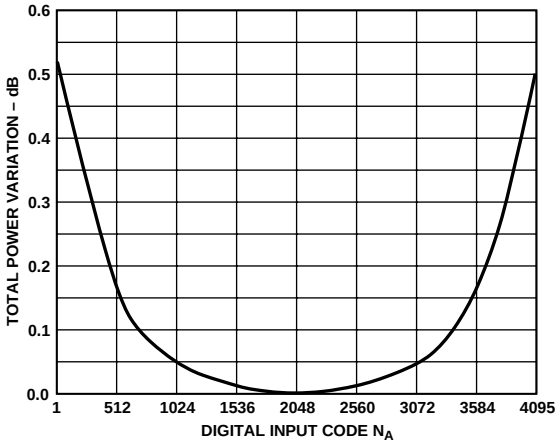


Figure 19. Power Variation for Circuit in Figure 9

APPLYING THE AD7837/AD7847

General Ground Management

AC or transient voltages between the analog and digital grounds i.e., between AGNDA/AGNDB and DGND can cause noise injection into the analog output. The best method of ensuring that both AGNDs and DGND are equal is to connect them together at the AD7837/AD7847 on the circuit board. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AGND and DGND pins (1N914 or equivalent).

Power Supply Decoupling

In order to minimize noise it is recommended that the V_{DD} and the V_{SS} lines on the AD7837/AD7847 be decoupled to DGND using a 10 µF in parallel with a 0.1 µF ceramic capacitor.

Operation with Reduced Power Supply Voltages

The AD7837/AD7847 is specified for operation with V_{DD}/V_{SS} = ±15 V ± 5%. The part may be operated down to V_{DD}/V_{SS} = ±10 V without significant linearity degradation. See typical performance graphs. The output amplifier however requires approximately 3 V of headroom so the V_{REF} input should not approach within 3 V of either power supply voltages in order to maintain accuracy.

MICROPROCESSOR INTERFACING–AD7847

Figures 20 to 22 show interfaces between the AD7847 and three popular 16-bit microprocessor systems, the 8086, MC68000 and the TMS320C10. In all interfaces, the AD7847 is memory-mapped with a separate memory address for each DAC latch.

AD7847–8086 Interface

Figure 20 shows an interface between the AD7847 and the 8086 microprocessor. A single MOV instruction loads the 12-bit word into the selected DAC latch and the output responds on the rising edge of $\overline{WR}$.

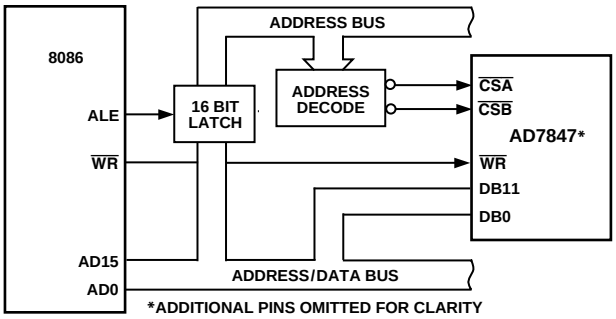


Figure 20. AD7847 to 8086 Interface

AD7847–MC68000 Interface

Figure 21 shows an interface between the AD7847 and the MC68000. Once again a single MOVE instruction loads the 12-bit word into the selected DAC latch. $\overline{CSA}$ and $\overline{CSB}$ are AND-gated to provide a $\overline{DTACK}$ signal when either DAC latch is selected.

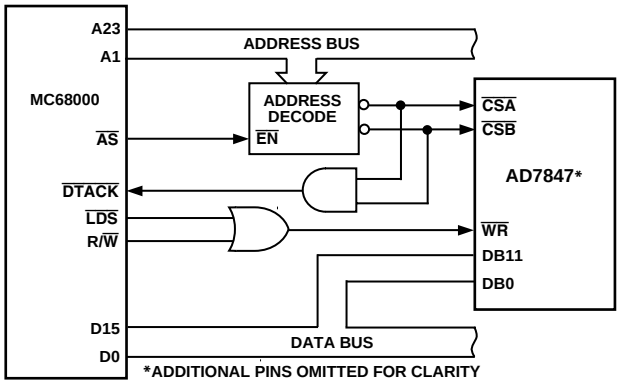


Figure 21. AD7847 to MC68000 Interface

AD7847–TMS320C10 Interface

Figure 22 shows an interface between the AD7847 and the TMS320C10 DSP processor. A single OUT instruction loads the 12-bit word into the selected DAC latch.

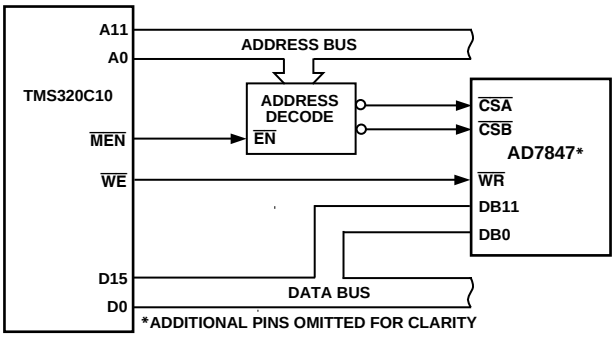


Figure 22. AD7847 to TMS320C10 Interface

MICROPROCESSOR INTERFACING–AD7837

Figures 23 to 25 show the AD7837 configured for interfacing to microprocessors with 8-bit data bus systems. In all cases, data is right-justified and the AD7837 is memory-mapped with the two lowest address lines of the microprocessor address bus driving the A0 and A1 inputs of the AD7837. Five separate memory addresses are required, one for the each MS latch and one for each LS latch and one for the common $\overline{LDAC}$ input. Data is written to the respective input latch in two write operations. Either high byte or low byte data can be written first to the input latch. A write to the AD7837 $\overline{LDAC}$ address transfers the data from the input latches to the respective DAC latches and updates both analog outputs. Alternatively, the $\overline{LDAC}$ input can be asynchronous and can be common to several AD7837s for simultaneous updating of a number of voltage channels.

AD7837–8051/8088 Interface

Figure 23 shows the connection diagram for interfacing the AD7837 to both the 8051 and the 8088. On the 8051, the signal $\overline{PSEN}$ is used to enable the address decoder while $\overline{DEN}$ is used on the 8088.

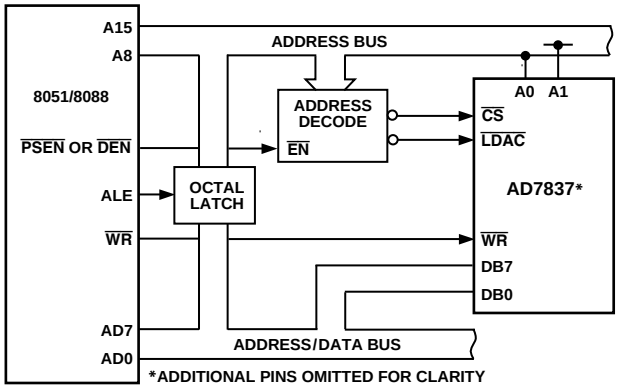


Figure 23. AD7837 to 8051/8088 Interface

AD7837–MC68008 Interface

An interface between the AD7837 and the MC68008 is shown in Figure 24. In the diagram shown, the $\overline{LDAC}$ signal is derived from an asynchronous timer but this can be derived from the address decoder as in the previous interface diagram.

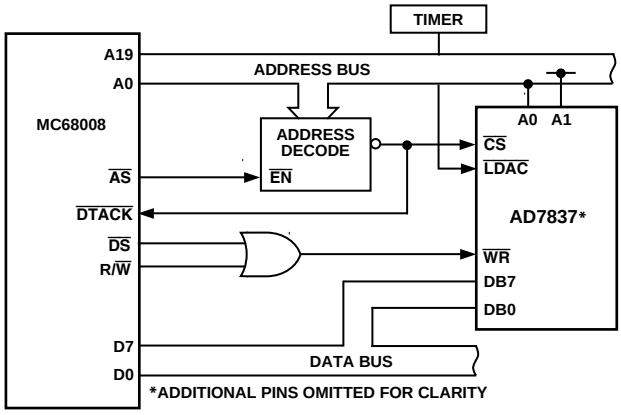


Figure 24. AD7837 to 68008 Interface

AD7837–6502/6809 Interface

Figure 25 shows an interface between the AD7837 and the 6502 or 6809 microprocessor. For the 6502 microprocessor, the ϕ2 clock is used to generate the $\overline{WR}$, while for the 6809 the E signal is used.

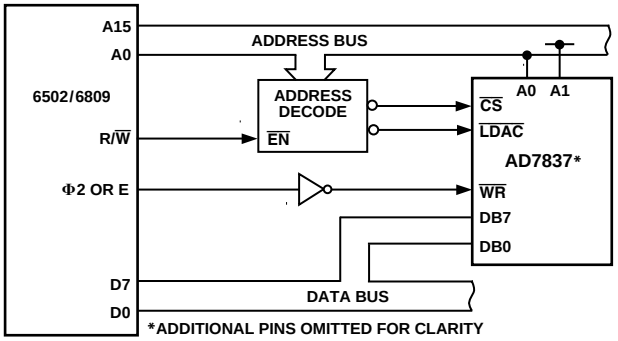
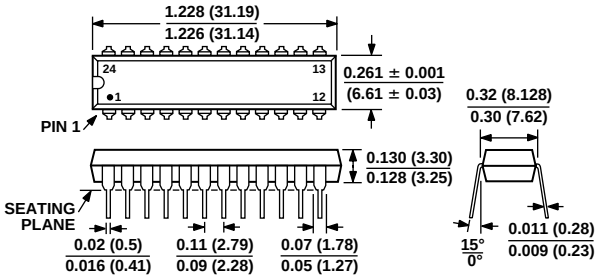


Figure 25. AD7837 to 6502/6809 Interface

OUTLINE DIMENSIONS

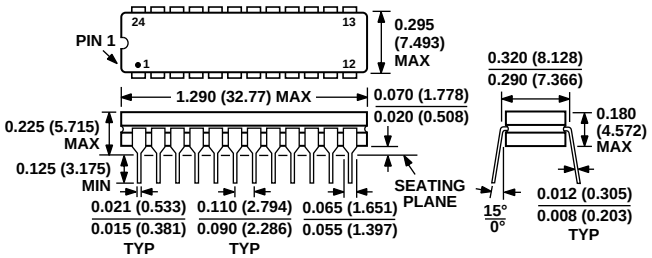
Dimensions shown in inches and (mm).

24-Lead Plastic DIP (N-24)



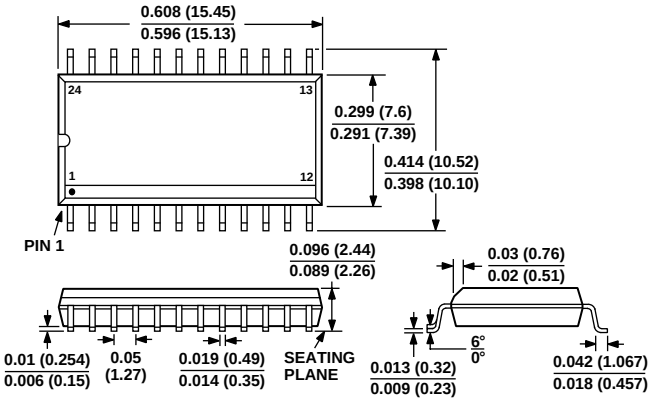
1. LEAD NO. 1 IDENTIFIED BY A DOT OR NOTCH.
2. PLASTIC LEADS WILL EITHER BE SOLDER DIPPED OR TIN LEAD PLATED. IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Lead Cerdip (Q-24)



1. LEAD NO. 1 IDENTIFIED BY A DOT OR NOTCH.
2. CERDIP LEADS WILL EITHER BE TIN PLATED OR SOLDER DIPPED. IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

24-Lead SOIC (R-24)



1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. SOIC LEADS WILL EITHER BE TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

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