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- UG-079: Evaluation Board for the AD7781 20-Bit, Pin-Programmable, Low Power, Sigma-Delta ADC

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- AD7780 IIO Low Power Sigma-Delta ADC Linux Driver
- AD7781 Evaluation Board Software
- AD7781 Evaluation Software Labview Source Code

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- Sigma-Delta ADC Tutorial

REFERENCE DESIGNS

- CN0108

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Test & Instrumentation Solutions Bulletin, Volume 10, Issue 3

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- MS-2210: Designing Power Supplies for High Speed ADC

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REVISION HISTORY

5/09—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = 2.7 V to 5.25 V, V_{REF} = AV_{DD}, DV_{DD} = 2.7 V to 5.25 V, GND = 0 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL					
Output Update Rate (f_{ADC})		10		Hz	FILTER = 1, settling time = 3/f_{ADC}
		16.7		Hz	FILTER = 0, settling time = 2/f_{ADC}
No Missing Codes[2]	20			Bits	
Resolution, Peak-to-Peak					See Table 7 and Table 8
RMS Noise					See Table 7 and Table 8
Integral Nonlinearity		±6		ppm FSR	
Offset Error		±6		µV	Gain = 128 with FILTER = 1
		±200		µV	Gain = 1 with FILTER = 1
		±1		µV	Gain = 128 with FILTER = 0
		±10		µV	Gain = 1 with FILTER = 0
Offset Error Drift vs. Temperature		±10		nV/°C	Gain = 128
		±150		nV/°C	Gain = 1 with FILTER = 1
		±10		nV/°C	Gain = 1 with FILTER = 0
Full-Scale Error		±0.25		% of FS	
Gain Drift vs. Temperature		±2		ppm/°C	
Power Supply Rejection		100		dB	Gain = 128, FILTER = 1, AIN = 7.81 mV
		120		dB	Gain = 128, FILTER = 0, AIN = 7.81 mV
Normal Mode Rejection[2]					
50 Hz, 60 Hz	63	75		dB	50 Hz ± 1 Hz, 60 Hz ± 1 Hz, f_{ADC} = 16.7 Hz
	72	90		dB	50 Hz ± 1 Hz, 60 Hz ± 1 Hz, f_{ADC} = 10 Hz
Common-Mode Rejection					
DC		90		dB	Gain = 1, AIN = 1 V
		90		dB	Gain = 128, AIN = 7.81 mV
50 Hz, 60 Hz		110		dB	50 Hz ± 1 Hz, 60 Hz ± 1 Hz
ANALOG INPUTS					
Differential Input Voltage Range		±V_{REF}/gain		V	V_{REF} = REFIN(+) − REFIN(−), gain = 1 or 128
Absolute AIN Voltage Limits[2]	GND + 100 mV		AV_{DD} − 100 mV	V	Gain = 1
	GND + 450 mV		AV_{DD} − 1.1	V	Gain = 128, FILTER = 0
	GND + 1.1		AV_{DD} − 1.1	V	Gain = 128, FILTER = 1, AV_{DD} ≤ 3.6 V
	GND + 1.5		AV_{DD} − 1.5	V	Gain = 128, FILTER = 1, AV_{DD} > 3.6 V
Average Input Current		±1		nA	Gain = 1
		±250		pA	Gain = 128
Average Input Current Drift		±3		pA/°C	
REFERENCE					
External REFIN Voltage		AV_{DD}		V	REFIN = REFIN(+) − REFIN(−)
Reference Voltage Range[2]	0.5		AV_{DD}	V	
Absolute REFIN Voltage Limits[2]	GND − 30 mV		AV_{DD} + 30 mV	V	
Average Reference Input Current		400		nA/V	
Average Reference Input Current Drift		±0.15		nA/V/°C	
Normal Mode Rejection					Same as for analog inputs
Common-Mode Rejection		110		dB	
BRIDGE POWER-DOWN SWITCH (BPDSW)					Controlled via the $\overline{PDRST}$ pin
R_{ON}			9	Ω	
Allowable Current[2]			30	mA	Continuous current

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INTERNAL CLOCK					
Frequency	64 – 3%		64 + 3%	kHz	
Duty Cycle		50:50		%	
LOGIC INPUTS					
SCLK, FILTER, GAIN, $\overline{PDRST}$[2]					
Input Low Voltage, V_{INL}			0.4	V	DV_{DD} = 3 V
			0.8	V	DV_{DD} = 5 V
Input High Voltage, V_{INH}	1.8			V	DV_{DD} = 3 V
	2.4			V	DV_{DD} = 5 V
SCLK (Schmitt-Triggered Input)					
Hysteresis[2]		100		mV	DV_{DD} = 3 V
		140		mV	DV_{DD} = 5 V
Input Currents		±2		µA	V_{IN} = DV_{DD} or GND
Input Capacitance		10		pF	All digital inputs
LOGIC OUTPUT (DOUT/$\overline{RDY}$)					
Output High Voltage, V_{OH}[2]	DV_{DD} – 0.6			V	DV_{DD} = 3 V, I_{SOURCE} = 100 µA
	4			V	DV_{DD} = 5 V, I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}[2]			0.4	V	DV_{DD} = 3 V, I_{SINK} = 100 µA
			0.4	V	DV_{DD} = 5 V, I_{SINK} = 1.6 mA
Floating-State Leakage Current		±2		µA	
Floating-State Output Capacitance		10		pF	
Data Output Coding		Offset binary			
POWER REQUIREMENTS[3]					
Power Supply Voltage					
AV_{DD} to GND	2.7		5.25	V	
DV_{DD} to GND	2.7		5.25	V	
Power Supply Currents					
I_{DD} Current					
Gain = 1		115		µA	AV_{DD} = 3 V
		130	160	µA	AV_{DD} = 5 V
Gain = 128 (B Grade)		300		µA	AV_{DD} = 3 V
		350	400	µA	AV_{DD} = 5 V
Gain = 128 (C Grade)		330		µA	AV_{DD} = 3 V
		420	500	µA	AV_{DD} = 5 V
I_{DD} (Power-Down/Reset Mode)		10		µA	

[1] Temperature range is –40°C to +105°C.
[2] This specification is not production tested but is supported by characterization data at initial product release.
[3] Digital inputs are equal to DV_{DD} or GND.

TIMING CHARACTERISTICS

AV_{DD} = 2.7 V to 5.25 V, DV_{DD} = 2.7 V to 5.25 V, GND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = DV_{DD}, unless otherwise noted.

Table 3.

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Test Conditions/Comments
Read[2]			
t_1	100	ns min	SCLK high pulse width
t_2	100	ns min	SCLK low pulse width
t_3[3]	0	ns min	SCLK active edge to data valid delay[4]
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_4	10	ns min	SCLK inactive edge to DOUT/$\overline{RDY}$ high
	130	ns max	
Reset			
t_5	100	ns min	$\overline{PDRST}$ low pulse width
t_6[5]			FILTER/GAIN change to data valid delay
	120	ms typ	Update rate = 16.7 Hz
	300	ms typ	Update rate = 10 Hz

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.
[2] See Figure 3.
[3] The values of t_3 are measured using the load circuit of Figure 2 and are defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[4] SCLK active edge is falling edge of SCLK.
[5] The $\overline{PDRST}$ high to data valid delay is typically 1 ms longer than t_6 because the internal oscillator requires time to power up and settle.

Circuit and Timing Diagrams

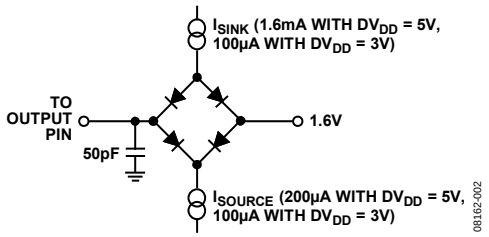


Figure 2. Load Circuit for Timing Characterization

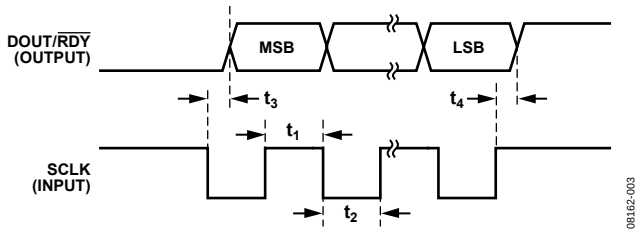


Figure 3. Read Cycle Timing Diagram

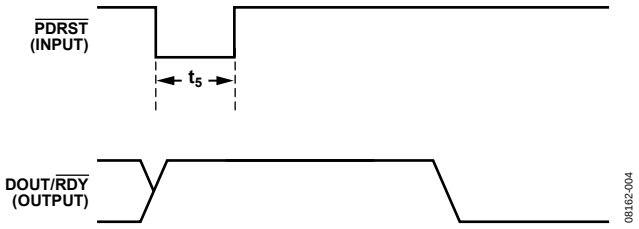


Figure 4. Resetting the AD7781

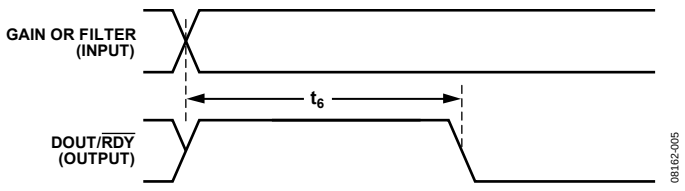


Figure 5. Changing Gain or Filter Option

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
AV_{DD} to GND	−0.3 V to +7 V
DV_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
AIN/Digital Input Current	10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature, Soldering Reflow	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5.

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead SOIC	104.5	42.9	°C/W
16-Lead TSSOP	150.4	27.6	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

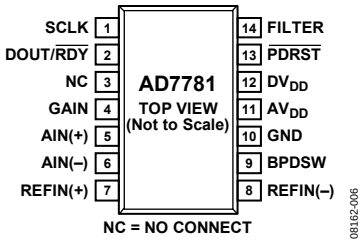


Figure 6. SOIC Pin Configuration

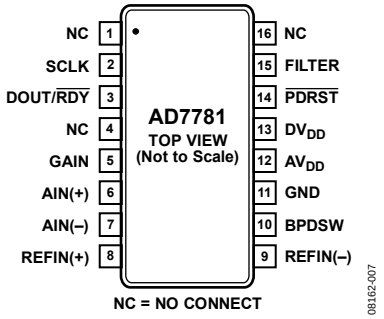


Figure 7. TSSOP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.			
SOIC	**TSSOP**	**Mnemonic**	**Description**
1	2	SCLK	Serial Clock Input. This serial clock input is for data transfers from the ADC. The SCLK pin has a Schmitt-triggered input. The serial clock can be active only when transferring data from the AD7781. The data from the AD7781 can be read as a continuous 32-bit word. Alternatively, SCLK can be noncontinuous during the data transfer, with the information being transmitted from the ADC in smaller data batches.
2	3	DOUT/$\overline{\text{RDY}}$	Serial Data Output/Data Ready Output. DOUT/$\overline{\text{RDY}}$ serves a dual purpose: as a data ready pin, going low to indicate the completion of a conversion, and as a serial data output pin to access the data register of the ADC. Eight status bits accompany each data read (see Figure 22). The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, indicating that new data is available. If the data is not read after the conversion, the pin goes high before the next update occurs. The serial interface is reset each time that a conversion is available. Therefore, the user must ensure that any conversions being transmitted are completed before the next conversion is available.
3	1, 4, 16	NC	No Connect. This pin can be left floating.
4	5	GAIN	Gain Select Pin. When GAIN is low, the gain is set to 128. When GAIN is high, the gain is set to 1.
5	6	AIN(+)	Analog Input. AIN(+) is the positive terminal of the differential analog input pair, AIN(+)/AIN(–).
6	7	AIN(–)	Analog Input. AIN(–) is the negative terminal of the differential analog input pair, AIN(+)/AIN(–).
7	8	REFIN(+)	Positive Reference Input. An external reference can be applied between REFIN(+) and REFIN(–). The nominal reference voltage (REFIN(+) – REFIN(–)) is 5 V, but the part can function with a reference of 0.5 V to AV_{DD}.
8	9	REFIN(–)	Negative Reference Input.
9	10	BPDSW	Bridge Power-Down Switch to GND. When $\overline{\text{PDRST}}$ is high, the bridge power-down switch is closed. When $\overline{\text{PDRST}}$ is low, the switch is opened.
10	11	GND	Ground Reference Point.
11	12	AV_{DD}	Supply Voltage, 2.7 V to 5.25 V.
12	13	DV_{DD}	Digital Interface Supply Voltage. The logic levels for the serial interface pins and the digital control pins are related to this supply, which is between 2.7 V and 5.25 V. The DV_{DD} voltage is independent of the voltage on AV_{DD}; therefore, AV_{DD} can equal 5 V with DV_{DD} at 3 V or vice versa.
13	14	$\overline{\text{PDRST}}$	Power-Down/Reset. When this pin is low, the ADC is placed in power-down mode, and the low-side power switch is opened. All the logic on the chip is reset, and the DOUT/$\overline{\text{RDY}}$ pin is tristated. When $\overline{\text{PDRST}}$ is high, the ADC is taken out of power-down mode. The on-chip clock powers up and settles, and the ADC continuously converts. In addition, the low-side power switch is closed. The internal clock requires approximately 1 ms to power up.
14	15	FILTER	Filter Select Pin. When FILTER is low, the fast settling filter is selected. The update rate is set to 16.7 Hz, which gives a filter settling time of 120 ms. When FILTER is high, the high rejection filter is selected. The update rate is set to 10 Hz, which gives a filter settling time of 300 ms. With this filter, the stop-band (higher than f_{ADC}) attenuation is better than −45 dB.

TYPICAL PERFORMANCE CHARACTERISTICS

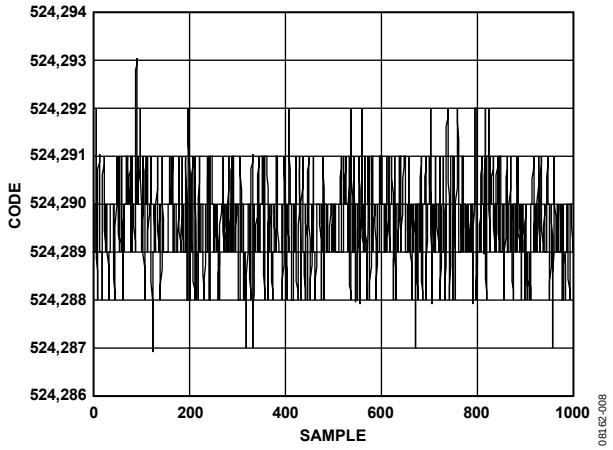


Figure 8. C Grade Noise (V_{REF} = AV_{DD}, Update Rate = 16.7 Hz, Gain = 128)

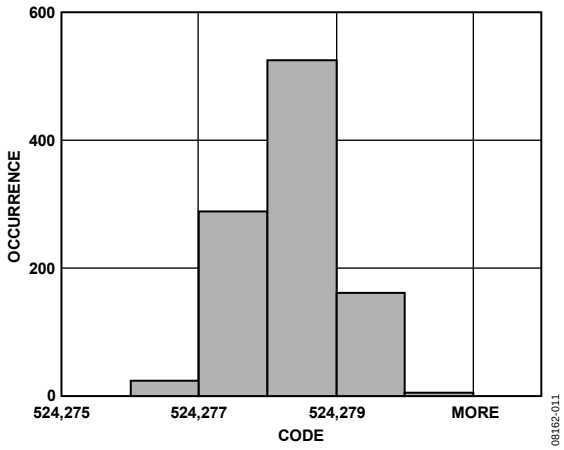


Figure 11. C Grade Noise Distribution Histogram (V_{REF} = AV_{DD}, Update Rate = 10 Hz, Gain = 128)

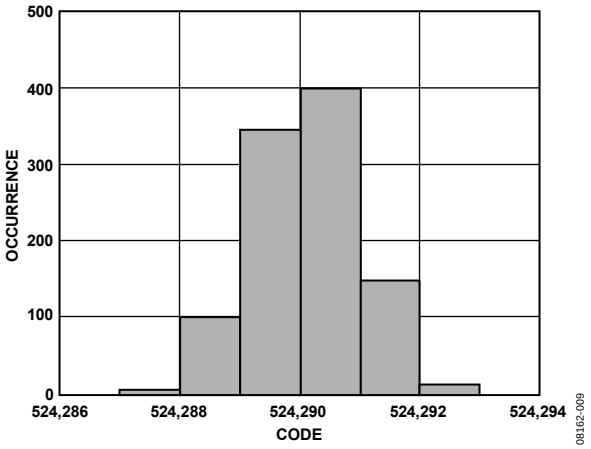


Figure 9. C Grade Noise Distribution Histogram (V_{REF} = AV_{DD}, Update Rate = 16.7 Hz, Gain = 128)

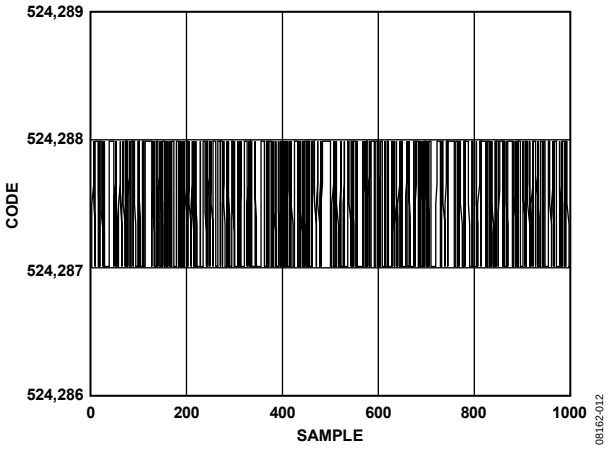


Figure 12. Noise (V_{REF} = AV_{DD}, Update Rate = 16.7 Hz, Gain = 1)

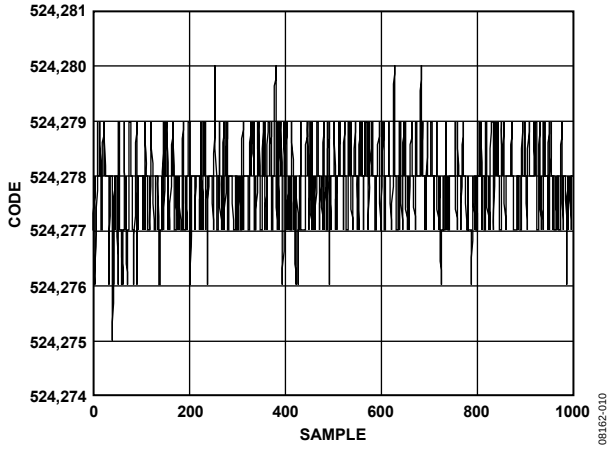


Figure 10. C Grade Noise (V_{REF} = AV_{DD}, Update Rate = 10 Hz, Gain = 128)

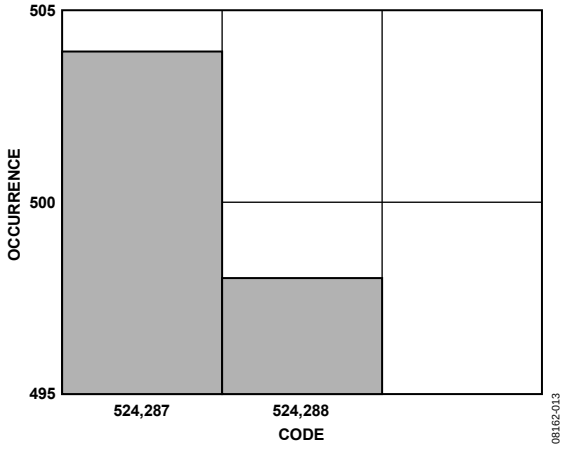


Figure 13. Noise Distribution Histogram (V_{REF} = AV_{DD}, Update Rate = 16.7 Hz, Gain = 1)

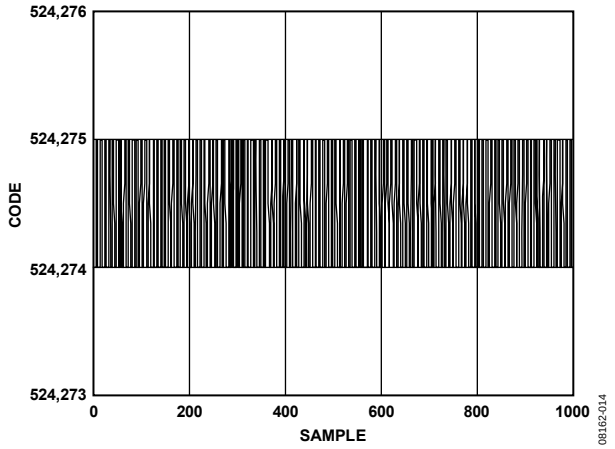


Figure 14. Noise (V_{REF} = AV_{DD}, Update Rate = 10 Hz, Gain = 1)

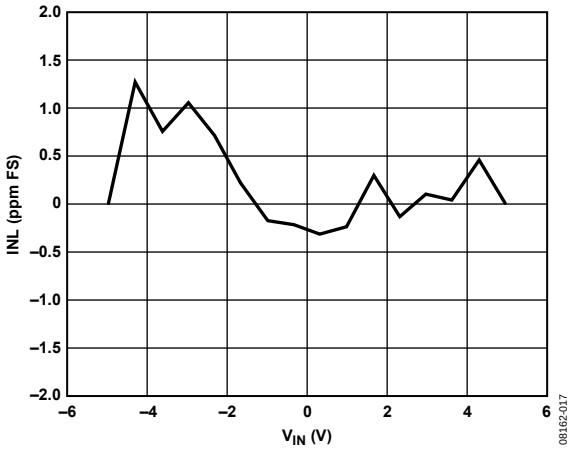


Figure 17. Integral Nonlinearity (V_{REF} = AV_{DD}, Gain = 1)

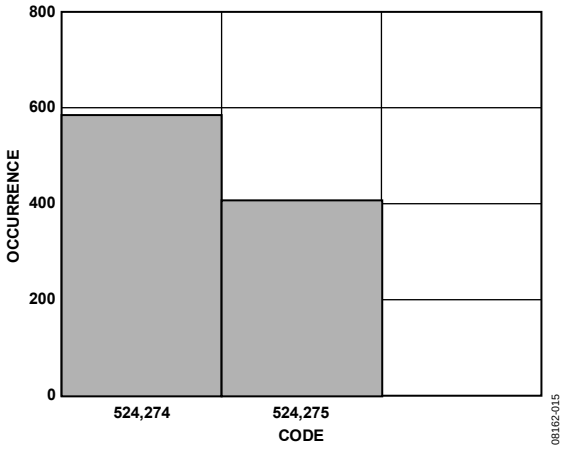


Figure 15. Noise Distribution Histogram
(V_{REF} = AV_{DD}, Update Rate = 10 Hz, Gain = 1)

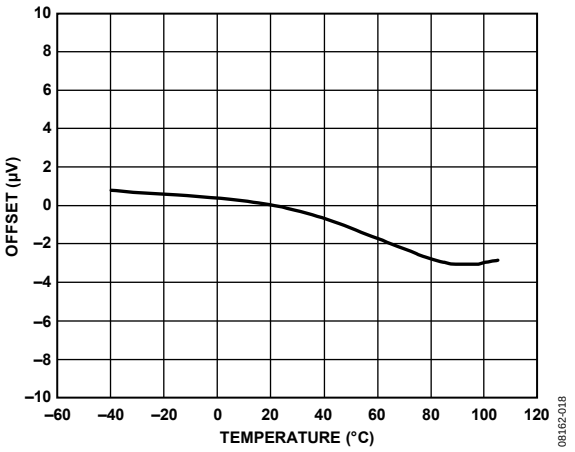


Figure 18. Offset vs. Temperature (Gain = 128)

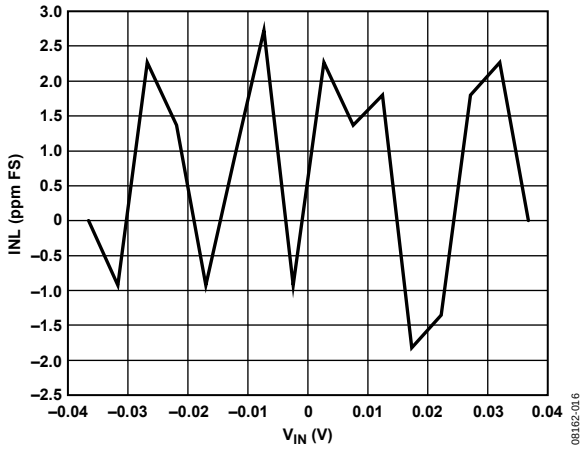


Figure 16. Integral Nonlinearity (V_{REF} = AV_{DD}, Gain = 128)

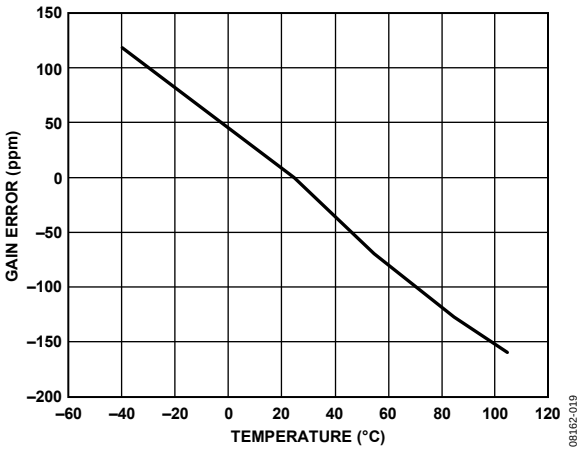


Figure 19. Gain Error vs. Temperature (Gain = 128)

OUTPUT NOISE AND RESOLUTION

Table 7 and Table 8 show the rms noise of the AD7781 for the two output data rates and gain settings when using a 3 V and a 5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. The peak-to-peak (p-p) resolution is also listed. The p-p resolution represents the resolution for which there is no code flicker. These numbers are typical.

Table 7. RMS Noise and Peak-to-Peak Resolution When AV_{DD} = 3 V and V_{REF} = 3 V

Parameter	Gain = 128		Gain = 1	
Update Rate	10 Hz	16.7 Hz	10 Hz	16.7 Hz
RMS Noise				
C Grade	44 nV	65 nV	2.4 µV	2.7 µV
B Grade	55 nV	90 nV	2.4 µV	2.7 µV
P-P Resolution				
C Grade	17.6	17.1	18.8	18.7
B Grade	17.3	16.6	18.8	18.7

Table 8. RMS Noise and Peak-to-Peak Resolution When AV_{DD} = 5 V and V_{REF} = 5 V

Parameter	Gain = 128		Gain = 1	
Update Rate	10 Hz	16.7 Hz	10 Hz	16.7 Hz
RMS Noise				
C Grade	49 nV	69 nV	3.0 µV	2.7 µV
B Grade	60 nV	90 nV	3.0 µV	2.7 µV
P-P Resolution				
C Grade	18.2	17.7	19.3	19.4
B Grade	17.9	17.3	19.3	19.4

THEORY OF OPERATION

The AD7781 is a low power ADC that incorporates a precision, 20-bit, Σ-Δ modulator; a PGA; and an on-chip digital filter intended for measuring wide dynamic range, low frequency signals. The part provides a complete front-end solution for bridge sensor applications such as weigh scales and pressure sensors.

The device has an internal clock and one buffered differential input. It offers a choice of two update rates (10 Hz or 16.7 Hz) and two gain settings (1 or 128). These functions are controlled using dedicated pins, which makes the interface easy to configure. A 2-wire interface simplifies data retrieval from the AD7781.

FILTER, DATA RATE, AND SETTLING TIME

The AD7781 has two filter options. When the FILTER pin is low, the 16.7 Hz filter is selected; when the FILTER pin is high, the 10 Hz filter is selected. When the polarity of the FILTER pin is changed, the AD7781 modulator and filter are reset immediately. DOUT/$\overline{\text{RDY}}$ is set high, and the ADC begins conversions using the selected filter response. The first conversion requires the total settling time of the filter. Subsequent conversions occur at the selected update rate. The settling time of the 10 Hz filter is 300 ms (three conversion cycles), and the settling time of the 16.7 Hz filter is 120 ms (two conversion cycles).

When a step change occurs on the analog input, the AD7781 requires several conversion cycles to generate a valid conversion. If the step change occurs synchronous to the conversion period, the settling time of the AD7781 must be allowed to generate a valid conversion. If the step change occurs asynchronous to the end of a conversion, an extra conversion must be allowed to generate a valid conversion. The data register is updated with all the conversions, but, for an accurate result, the user must allow for the required time.

Figure 20 and Figure 21 show the filter response for each filter. The 10 Hz filter provides more than −45 dB of rejection in the stop band. The only external filtering required on the analog inputs is a simple R-C filter to provide rejection at multiples of the master clock. A 1 kΩ resistor in series with each analog input, a 0.01 µF capacitor from each input to GND, and a 0.1 µF capacitor from AIN(+) to AIN(−) are recommended.

When the filter is changed, DOUT/$\overline{\text{RDY}}$ goes high and remains high until the appropriate settling time for that filter elapses (see Figure 5). Therefore, the user should complete any read operations before changing the filter. Otherwise, 1s are read back from the AD7781 because the DOUT/$\overline{\text{RDY}}$ pin is set high following the filter change.

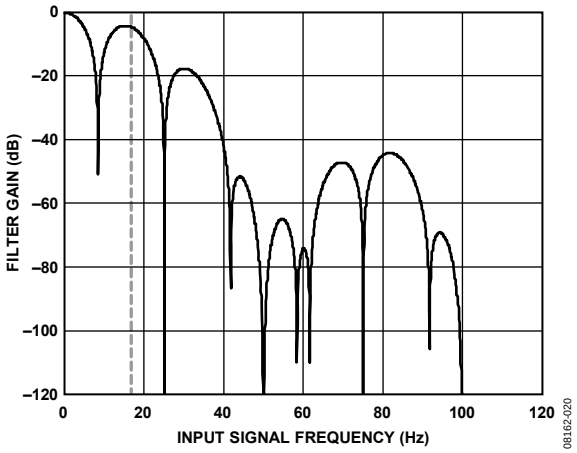


Figure 20. Filter Profile with Update Rate = 16.7 Hz (FILTER = 0)

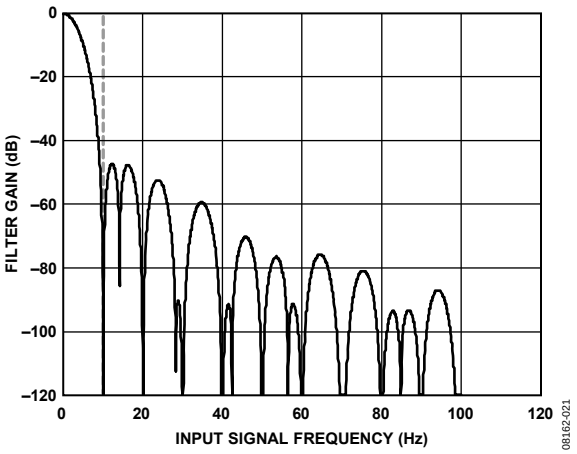


Figure 21. Filter Profile with Update Rate = 10 Hz (FILTER = 1)

GAIN

The AD7781 has two gain options: gain = 1 and gain = 128. When the GAIN pin is low, the gain is set to 128; when the GAIN pin is high, the gain is set to 1. The acceptable analog input range is $\pm V_{REF}$/gain. Thus, with V_{REF} = 5 V, the input range is ±5 V when GAIN is high and ±39 mV when GAIN is low.

When the polarity of the GAIN pin is changed, the AD7781 modulator and filter are reset immediately. DOUT/$\overline{\text{RDY}}$ is set high, and the ADC begins conversions. DOUT/$\overline{\text{RDY}}$ remains high until the appropriate settling time for the filter elapses (see Figure 5). Therefore, the user should complete any read operations before changing the gain. Otherwise, 1s are read back from the AD7781 because the DOUT/$\overline{\text{RDY}}$ pin is set high following the gain change. The total settling time of the selected filter is required to generate the first conversion after the gain change; subsequent conversions occur at the selected update rate.

POWER-DOWN/RESET (PDRST)

The PDRST pin functions as a power-down pin and a reset pin. When PDRST is taken low, the AD7781 is powered down. The entire ADC is powered down (including the on-chip clock), the low-side power switch is opened, and the DOUT/RDY pin is tristated. The circuitry and serial interface are also reset, which resets the logic, the digital filter, and the analog modulator. PDRST must be held low for 100 ns minimum to initiate the reset function (see Figure 4).

When PDRST is taken high, the AD7781 is taken out of power-down mode. When the on-chip clock has powered up (1 ms, typically), the modulator begins sampling the analog input. The low-side power switch is closed, and the DOUT/RDY pin becomes active.

A reset is automatically performed on power-up.

ANALOG INPUT CHANNEL

The AD7781 has one differential analog input channel. The input channel feeds into a high impedance input stage of the amplifier. Therefore, the input can tolerate significant source impedances and is tailored for direct connection to external resistive-type sensors such as strain gages.

The absolute input voltage range is restricted to a range between GND + 450 mV and AV_{DD} − 1.1 V. Care must be taken in setting up the common-mode voltage to avoid exceeding these limits. Otherwise, there is degradation in linearity and noise performance.

The low noise in-amp means that signals of small amplitude can be amplified within the AD7781, which still maintains excellent noise performance. The amplifier can be configured to have a gain of 128 or 1, using the GAIN pin. The analog input range is equal to $\pm V_{REF}$/gain. The common-mode voltage (AIN(+) + AIN(−))/2 must be ≥0.5 V.

BIPOLAR CONFIGURATION

The AD7781 accepts a bipolar input range. A bipolar input range does not imply that the part can tolerate negative voltages with respect to system GND. Signals on the AIN(+) input are referenced to the voltage on the AIN(−) input. For example, if AIN(−) is 2.5 V, the analog input range on the AIN(+) input is 2.46 V to 2.54 V for a gain of 128.

DATA OUTPUT CODING

The AD7781 uses offset binary coding. Thus, a negative full-scale voltage results in a code of 000...000, a zero differential input voltage results in a code of 100...000, and a positive full-scale input voltage results in a code of 111...111.

The output code for any analog input voltage can be represented as

$$Code = 2^{N-1} \times [(AIN \times Gain/V_{REF}) + 1]$$

where:
AIN is the analog input voltage.
Gain is 1 or 128.
N = 20.

REFERENCE

The AD7781 has a fully differential input capability for the channel. The common-mode range for these differential inputs is GND to AV_{DD}. The reference input is unbuffered; therefore, excessive R-C source impedances introduce gain errors. The reference voltage of REFIN (REFIN(+) − REFIN(−)) is AV_{DD} nominal, but the AD7781 is functional with reference voltages of 0.5 V to AV_{DD}. In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source is removed because the application is ratiometric. If the AD7781 is used in a nonratiometric application, a low noise reference should be used.

Recommended 2.5 V reference voltage sources for the AD7781 include the ADR381 and ADR391, which are low noise, low power references. These references have low output impedances and are, therefore, tolerant to decoupling capacitors on REFIN(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor means that the reference input sees a significant external source impedance. External decoupling on the REFIN pins is not recommended in this type of circuit configuration.

BRIDGE POWER-DOWN SWITCH

The bridge power-down switch (BPDSW) is useful in battery-powered applications where the optimization of system power consumption is essential. A 350 Ω load cell typically consumes 15 mA when excited with a 5 V power supply. To minimize current consumption, the load cell is disconnected when it is not being used. The bridge power-down switch can be included in series with the load cell. When PDRST is high, the bridge power-down switch is closed, and the load cell measures the strain. When PDRST is low, the bridge power-down switch is opened so no current flows through the load cell. Therefore, the current consumption of the system is minimized. The bridge power-down switch has an on resistance of 9 Ω maximum. The switch is capable of withstanding 30 mA of continuous current.

DIGITAL INTERFACE

The serial interface of the AD7781 consists of two signals: SCLK and DOUT/$\overline{RDY}$. SCLK is the serial clock input for the device, and data transfers occur with respect to the SCLK signal. The DOUT/$\overline{RDY}$ pin is dual purpose: it functions as a data ready pin and as a data output pin. DOUT/$\overline{RDY}$ goes low when a new data-word is available in the output register. A 32-bit word is placed on the DOUT/$\overline{RDY}$ pin when sufficient SCLK pulses are applied. This word consists of a 20-bit conversion result followed by four 0s to generate a 24-bit word. Following this, status bits are output. Figure 22 shows the status bits, and Table 9 describes the status bits and their functions.

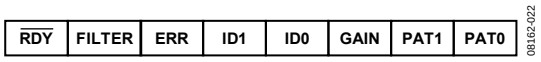


Figure 22. Status Bits

DOUT/$\overline{RDY}$ is reset high when the conversion has been read. If the conversion is not read, DOUT/$\overline{RDY}$ goes high prior to the data register update to indicate when not to read from the device. This ensures that a read operation is not attempted while the register is being updated. Each conversion can be read only once. The data register is updated for every conversion.

When a conversion is complete, the serial interface is reset, and the new conversion is placed in the data register. Therefore, the user must ensure that the complete word is read before the next conversion is complete.

When $\overline{PDRST}$ is low, the DOUT/$\overline{RDY}$ pin is tristated. When $\overline{PDRST}$ is taken high, the internal clock requires approximately 1 ms to power up. Following power-up, the ADC continuously converts. The first conversion requires the total settling time (see Figure 4). DOUT/$\overline{RDY}$ goes high when $\overline{PDRST}$ is taken high and returns low only when a conversion is available. The ADC then converts continuously, and subsequent conversions are available at the selected update rate. Figure 3 shows the timing for a read operation from the AD7781.

When the filter response is changed (using the FILTER pin) or the gain is changed (using the GAIN pin), the modulator and filter are reset immediately (see Figure 5). DOUT/$\overline{RDY}$ is set high. The ADC then begins conversions using the selected filter response/gain setting. DOUT/$\overline{RDY}$ remains high until the appropriate settling time for that filter has elapsed. Therefore, the user should complete any read operations before changing the gain or update rate. Otherwise, 1s are read back from the AD7781 because the DOUT/$\overline{RDY}$ pin is set high following the gain/filter change.

Table 9. Status Bit Functions

Bit Name	Description		
$\overline{RDY}$	Ready bit. 0: a conversion is available.		
FILTER	Filter bit. 1: 10 Hz filter is selected. 0: 16.7 Hz filter is selected.		
ERR	Error bit. 1: an error occurred during conversion. (An error occurs when the analog input is out of range.)		
ID1, ID0	ID bits.		
	ID1	**ID0**	**Function**
	0	0	Indicates the ID number for the AD7781.
GAIN	Gain bit. 1: gain = 1. 0: gain = 128.		
PAT1, PAT0	Status pattern bits. When the user reads data from the AD7781, a pattern check can be performed.		
	PAT1	**PAT0**	**Function**
	0	1	Indicates that the serial transfer from the ADC was performed correctly (default).
	0	0	Indicates that the serial transfer from the ADC was not performed correctly.
	1	x	Indicates that the serial transfer from the ADC was not performed correctly.

APPLICATIONS INFORMATION

The AD7781 provides a low cost, high resolution analog-to-digital function. Because the analog-to-digital function is provided by a Σ-Δ architecture, the part is more immune to noisy environments, making it ideal for use in sensor measurement and industrial and process control applications.

WEIGH SCALES

Figure 23 shows the AD7781 being used in a weigh scale application. The load cell is arranged in a bridge network and gives a differential output voltage between its OUT+ and OUT– terminals. Assuming a 5 V excitation voltage, the full-scale output range from the transducer is 10 mV when the sensitivity is 2 mV/V. The excitation voltage for the bridge can be used to directly provide the reference for the ADC because the reference input range includes the supply voltage.

A second advantage of using the AD7781 in transducer-based applications is that the bridge power-down switch (BPDSW) can be fully utilized in low power applications. The bridge power-down switch is connected in series with the low side of the bridge. In normal operation, the switch is closed and measurements can be taken. In applications where power is of concern, the AD7781 can be placed in power-down mode, significantly reducing the power consumed in the application. In addition, the bridge power-down switch is opened while in power-down mode, thus avoiding unnecessary power consumption by the front-end transducer. When the part is taken out of power-down mode and the bridge power-down switch is closed, the user should ensure that the front-end circuitry is fully settled before attempting to read from the AD7781.

The load cell has an offset, or tare, associated with it. This tare is the main component of the system offset (load cell + ADC) and is similar in magnitude to the full-scale signal from the load cell. For this reason, calibrating the offset and gain of the AD7781 alone is not sufficient for optimum accuracy; a system calibration that calibrates the offset and gain of the ADC, plus the load cell, is required. A microprocessor can be used to perform the calibrations. The offset error (the conversion result from the AD7781 when no load is applied to the load cell) and the full-scale error (the conversion result from the ADC when the maximum load is applied to the load cell) must be determined. Subsequent conversions from the AD7781 are then corrected, using the offset and gain coefficients that were calculated from these calibrations.

AD7781 PERFORMANCE IN A WEIGH SCALE SYSTEM

If the load cell has a sensitivity of 2 mV/V and a 5 V excitation voltage is used, the full-scale signal from the load cell is 10 mV. When the AD7781 (C grade) operates with a 10 Hz output data rate and the gain is set to 128, the device has a p-p resolution of 18.2 bits when the reference is equal to 5 V. Postprocessing the data from the AD7781 using a microprocessor increases the p-p resolution. For example, an average by 4 in the microprocessor increases the accuracy by 2 bits. The noise-free counts value is equal to

$$Noise\text{-}Free\ Counts = (2^{Effective\ Bits}) \times (FS_{LC}/FS_{ADC})$$

where:
Effective Bits = 18.2 bits (AD7781) + 2 bits (due to postprocessing in the microprocessor).
FS_{LC} is the full-scale signal from the load cell (10 mV).
FS_{ADC} is the full-scale input range when gain = 128 and V_{REF} = 5 V (78 mV).

The noise-free counts is equal to

$$(2^{18.2+2}) \times (10\ mV/78\ mV) = 154{,}422$$

This example shows that with a 5 V supply, 154,422 noise-free counts can be achieved with the AD7781.

EMI RECOMMENDATIONS

For simplicity, the EMI filters are not included in Figure 23. However, an R-C antialiasing filter should be included on each analog input. This filter is needed because the on-chip digital filter does not provide any rejection around the master clock or multiples of the master clock. Suitable values are a 1 kΩ resistor in series with each analog input, a 0.1 μF capacitor from AIN(+) to AIN(–), and 0.01 μF capacitors from AIN(+)/AIN(–) to GND.

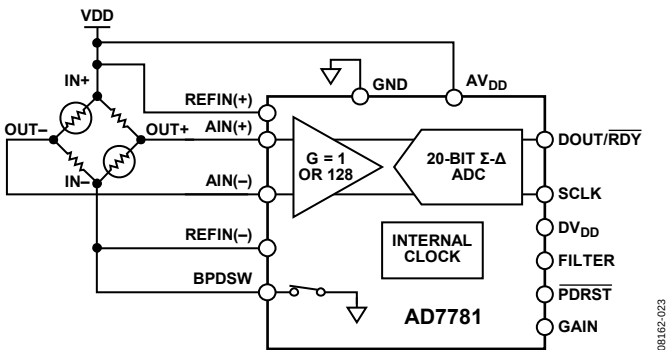


Figure 23. Weigh Scales Using the AD7781

GROUNDING AND LAYOUT

Because the analog input and reference input of the ADC are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part removes common-mode noise on these inputs. The digital filter provides rejection of broadband noise on the power supply, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD7781 is more immune to noise interference than conventional high resolution converters. However, because the resolution of the AD7781 is so high and the noise levels from the AD7781 are so low, care must be taken with regard to grounding and layout.

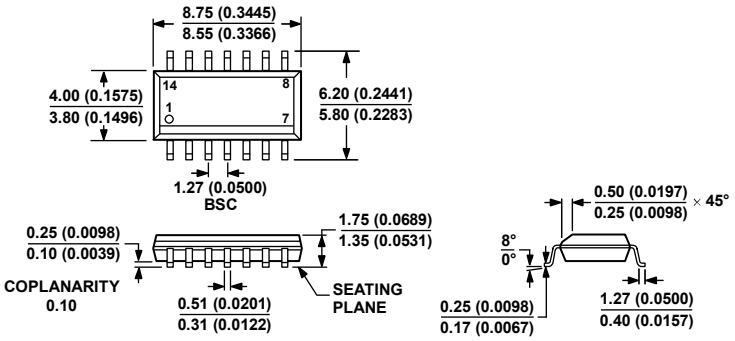
The printed circuit board (PCB) that houses the AD7781 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it gives the best shielding.

It is recommended that the GND pin of the AD7781 be tied to the AGND plane of the system. In any layout, pay attention to the flow of currents in the system and ensure that the return paths for all currents are as close as possible to the paths that the currents took to reach their destinations. Avoid forcing digital currents to flow through the AGND sections of the layout.

The ground plane of the AD7781 should be allowed to run under the AD7781 to prevent noise coupling. The power supply lines to the AD7781 should use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, and the signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. AV_{DD} should be decoupled with 10 µF tantalum capacitors in parallel with 0.1 µF capacitors to GND. DV_{DD} should be decoupled with 10 µF tantalum capacitors in parallel with 0.1 µF capacitors to GND, with the system's AGND to DGND connection being close to the AD7781. To achieve the best results from these decoupling components, place them as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 µF ceramic capacitors to DGND.

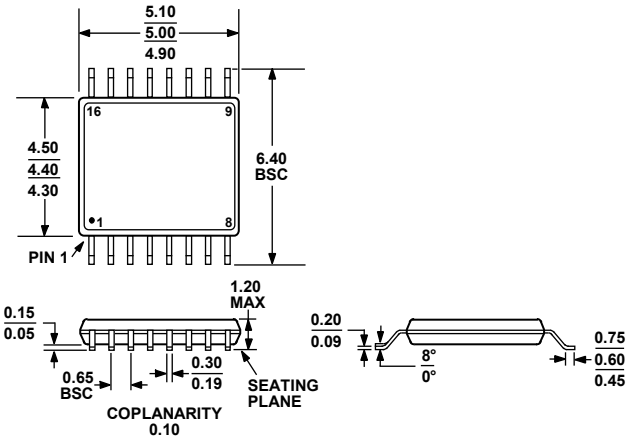
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 24. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 25. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7781BRZ[1]	−40°C to +105°C	14-Lead SOIC_N	R-14
AD7781BRZ-REEL[1]	−40°C to +105°C	14-Lead SOIC_N	R-14
AD7781BRUZ[1]	−40°C to +105°C	16-Lead TSSOP	RU-16
AD7781BRUZ-REEL[1]	−40°C to +105°C	16-Lead TSSOP	RU-16
AD7781CRZ[1]	−40°C to +105°C	14-Lead SOIC_N	R-14
AD7781CRZ-REEL[1]	−40°C to +105°C	14-Lead SOIC_N	R-14
AD7781CRUZ[1]	−40°C to +105°C	16-Lead TSSOP	RU-16
AD7781CRUZ-REEL[1]	−40°C to +105°C	16-Lead TSSOP	RU-16

[1] Z = RoHS Compliant Part.

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