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1/2015—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, resistive load (R_L) = 2 kΩ, capacitive load (C_L) = 200 pF, all specifications T_A = −40°C to +125°C, unless otherwise noted.

Table 2.

	A Grade			B Grade				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
STATIC PERFORMANCE[1]								
Resolution	16			16			Bits	
Relative Accuracy/Integral Nonlinearity (INL)[2]		±1.8	±8		±1.8	±3	LSB	Gain = 1
		±1.7	±8		±1.7	±3	LSB	Gain = 2
Differential Nonlinearity (DNL)[2]		±0.7	±1		±0.7	±1	LSB	Gain = 1
		±0.5	±1		±0.5	±1	LSB	Gain = 2
Zero Code Error[2]		0.8	4		0.8	1.6	mV	Gain = 1 or gain = 2
Offset Error[2]		−0.75	±6		−0.75	±2	mV	Gain = 1
		−0.1	±4		−0.1	±1.5	mV	Gain = 2
Full-Scale Error[2]		−0.018	±0.28		−0.018	±0.14	% of full-scale range (FSR)	Gain = 1
		−0.013	±0.14		−0.013	±0.07	% of FSR	Gain = 2
Gain Error[2]		+0.04	±0.24		+0.04	±0.12	% of FSR	Gain = 1
		−0.02	±0.12		−0.02	±0.06	% of FSR	Gain = 2
TUE		±0.03	±0.3		±0.03	±0.18	% of FSR	Gain = 1
		±0.006	±0.25		±0.006	±0.14	% of FSR	Gain = 2
Offset Error Drift[2]		±1			±1		µV/°C	
DC Power Supply Rejection Ratio (PSRR)[2]		0.25			0.25		mV/V	DAC code = midscale, V_{DD} = 5 V ± 10%
DC Crosstalk[2]		±2			±2		µV	Due to single channel, full-scale output change
		±3			±3		µV/mA	Due to load current change
		±2			±2		µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS								
Output Voltage Range	0		V_{REF}	0		V_{REF}	V	Gain = 1
	0		$2 \times V_{REF}$	0		$2 \times V_{REF}$	V	Gain = 2
Output Current Drive (I_{OUT})			15			15	mA	
Capacitive Load Stability		2			2		nF	$R_L = \infty$
		10			10		nF	R_L = 1 kΩ
Resistive Load[3]	1			1			kΩ	
Load Regulation		183			183		µV/mA	V_{DD} = 5 V ± 10%, DAC code = midscale, −30 mA ≤ I_{OUT} ≤ +30 mA
		177			177		µV/mA	V_{DD} = 3 V ± 10%, DAC code = midscale, −20 mA ≤ I_{OUT} ≤ +20 mA
Short-Circuit Current[4]		40			40		mA	
Load Impedance at Rails[5]		25			25		Ω	
Power-Up Time		2.5			2.5		µs	Exiting power-down mode, V_{DD} = 5 V
REFERENCE INPUT								
Reference Input Current		398			398		µA	$V_{REF} = V_{DD} = V_{LOGIC}$ = 5.5 V, gain = 1
		789			789		µA	$V_{REF} = V_{DD} = V_{LOGIC}$ = 5.5 V, gain = 2
Reference Input Range	1		V_{DD}	1		V_{DD}	V	Gain = 1
	1		$V_{DD}/2$	1		$V_{DD}/2$	V	Gain = 2
Reference Input Impedance		14			14		kΩ	Gain = 1
		7			7		kΩ	Gain = 2

Parameter	A Grade			B Grade			Unit	Test Conditions/Comments
	Min	Typ	Max	Min	Typ	Max		
LOGIC INPUTS								
Input Current			±1			±1	μA	Per pin
Input Voltage								
Low, V_{IL}			0.3 × V_{LOGIC}			0.3 × V_{LOGIC}	V	
High, V_{IH}	0.7 × V_{LOGIC}			0.7 × V_{LOGIC}			V	
Pin Capacitance		3			3		pF	
LOGIC OUTPUTS (SDA)								
Output Voltage								
Low, V_{OL}			0.4			0.4	V	I_{SINK} = 200 μA
High, V_{OH}	V_{LOGIC} − 0.4			V_{LOGIC} − 0.4			V	I_{SOURCE} = 200 μA
Floating State Output Capacitance		4			4		pF	
POWER REQUIREMENTS								
V_{LOGIC}	1.62		5.5	1.62		5.5	V	
V_{LOGIC} Supply Current (I_{LOGIC})			3			3	μA	Power-on, −40°C to +105°C
			3			3	μA	Power-on, −40°C to +125°C
			3			3	μA	Power-down, −40°C to +105°C
			3			3	μA	Power-down, −40°C to +125°C
V_{DD}	2.7		5.5	2.7		5.5	V	Gain = 1
	V_{REF} + 1.5		5.5	V_{REF} + 1.5		5.5	V	Gain = 2
V_{DD} Supply Current, I_{DD}								$V_{IH} = V_{DD}$, V_{IL} = GND, V_{DD} = 2.7 V to 5.5 V
Normal Mode[6]		1.1	1.26		1.1	1.26	mA	−40°C to +85°C
		1.1	1.3		1.1	1.3	mA	−40°C to +125°C
All Power-Down Modes[7]		1	1.7		1	1.7	μA	Tristate to 1 kΩ, −40°C to +85°C
		1	1.7		1	1.7	μA	Power-down to 1 kΩ, −40°C to +85°C
		1	2.5		1	2.5	μA	Tristate to 1 kΩ, −40°C to +105°C
		1	2.5		1	2.5	μA	Power-down to 1 kΩ, −40°C to +105°C
		1	5.5		1	5.5	μA	Tristate to 1 kΩ, −40°C to +125°C
		1	5.5		1	5.5	μA	Power-down to 1 kΩ, −40°C to +125°C

[1] DC specifications tested with the outputs unloaded, unless otherwise noted. Upper dead band = 10 mV and exists only when $V_{REF} = V_{DD}$ with gain = 1, or when $V_{REF}/2 = V_{DD}$ with gain = 2. Linearity calculated using a reduced code range of 256 to 65,280.
[2] See the Terminology section.
[3] Together, Channel 0, Channel 1, Channel 2, and Channel 3 can source or sink 40 mA. Similarly, together, Channel 4, Channel 5, Channel 6, and Channel 7 can source or sink 40 mA up to a junction temperature of 125°C.
[4] V_{DD} = 5 V. The AD5675 includes current limiting to protect the device during temporary overload conditions. Junction temperature can be exceeded during current limit. Operation above the specified maximum operation junction temperature can impair device reliability.
[5] When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV.
[6] Interface inactive. All DACs active. DAC outputs unloaded.
[7] All DACs powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, all specifications T_A = −40°C to +125°C, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage Settling Time[1]		5	8	µs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		0.8		V/µs	
Digital-to-Analog Glitch Impulse[1]		1.4		nV-sec	1 LSB change around major carry (gain = 1)
Digital Feedthrough[1]		0.13		nV-sec	
Digital Crosstalk[1]		0.1		nV-sec	
Analog Crosstalk[1]		−0.25		nV-sec	Gain = 1
		−1.3		nV-sec	Gain = 2
DAC-to-DAC Crosstalk[1]		−2.0		nV-sec	Gain = 2
Total Harmonic Distortion (THD)[1, 2]		−80		dB	T_A = 25°C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Output Noise Spectral Density (NSD)[1]		80		nV/√Hz	DAC code = midscale, bandwidth = 10 kHz, gain = 1 and 2
Output Noise		6		µV p-p	0.1 Hz to 10 Hz, gain = 1
Signal-to-Noise Ratio (SNR)		90		dB	T_A = 25°C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Spurious-Free Dynamic Range (SFDR)		83		dB	T_A = 25°C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Signal-to-Noise-and-Distortion Ratio (SINAD)		80		dB	T_A = 25°C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz

[1] See the Terminology section.
[2] Digitally generated sine wave (f_{OUT}) at 1 kHz.

TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, all specifications −40°C to +125°C, unless otherwise noted.

Table 4.

Parameter[1]	Min	Max	Unit	Description
t_1	2.5		µs	SCL cycle time
t_2	0.6		µs	t_{HIGH}, SCL high time
t_3	1.3		µs	t_{LOW}, SCL low time
t_4	0.6		µs	$t_{HD,STA}$, start/repeated start hold time
t_5	100		ns	$t_{SU,DAT}$, data setup time
t_6[2]	0	0.9	µs	$t_{HD,DAT}$, data hold time
t_7	0.6		µs	$t_{SU,STA}$, repeated start setup time
t_8	0.6		µs	$t_{SU,STO}$, stop condition setup time
t_9	1.3		µs	t_{BUF}, bus free time between a stop condition and a start condition
t_{10}[3]	0	300	ns	t_R, rise time of SCL and SDA when receiving
t_{11}[3]	20 + 0.1C_B		ns	t_F, fall time of SCL and SDA when transmitting/receiving
t_{12}	20		ns	$\overline{\text{LDAC}}$ pulse width
t_{13}	400		ns	SCL rising edge to $\overline{\text{LDAC}}$ rising edge
t_{14}	8		ns	$\overline{\text{RESET}}$ minimum pulse width low, 1.62 V ≤ V_{LOGIC} ≤ 2.7 V
	10		ns	$\overline{\text{RESET}}$ minimum pulse width low, 2.7 V ≤ V_{LOGIC} ≤ 5.5 V
t_{15}	90		ns	$\overline{\text{RESET}}$ activation time, 1.62 V ≤ V_{LOGIC} ≤ 2.7 V
	90		ns	$\overline{\text{RESET}}$ activation time, 2.7 V ≤ V_{LOGIC} ≤ 5.5 V
t_{SP}[4]	0	50	ns	Pulse width of suppressed spike
C_B[4]		400	pF	Capacitive load for each bus line

[1] See Figure 2 and Figure 3.
[2] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the minimum V_{IH} of the SCL signal) to bridge the undefined region of the SCL falling edge.
[3] t_R and t_F are measured from 0.3 × V_{DD} to 0.7 × V_{DD}.
[4] Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns.

Timing Diagrams

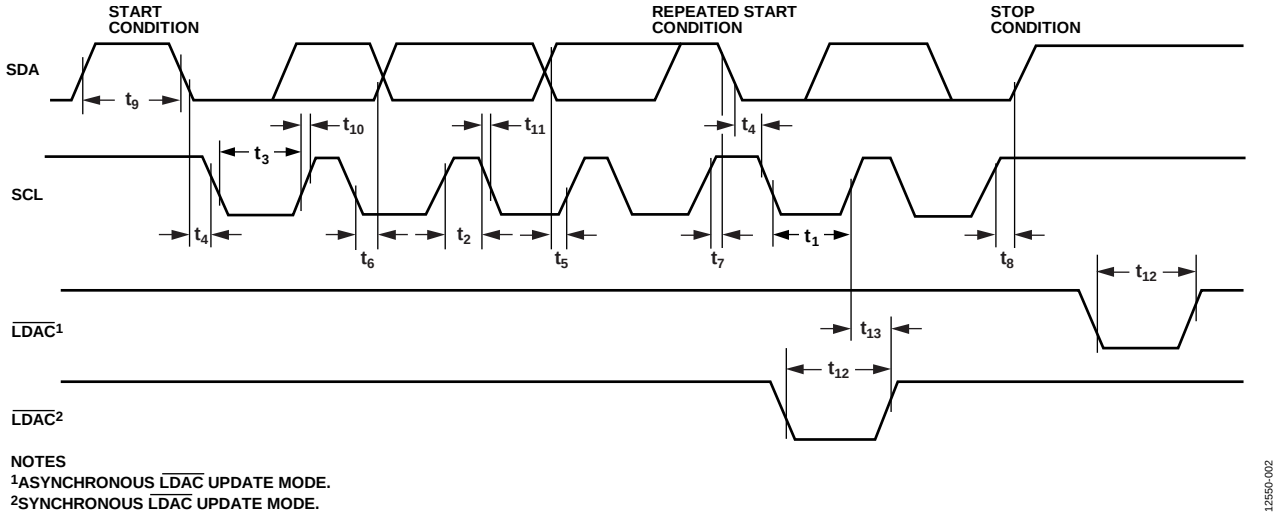


Figure 2. Two-Wire Serial Interface Timing Diagram

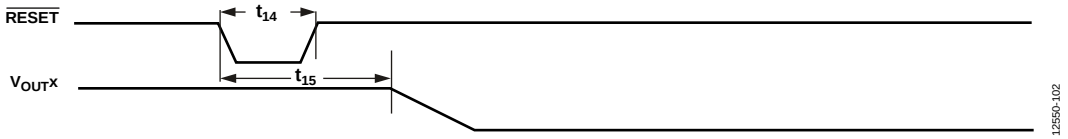


Figure 3. RESET Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{LOGIC} to GND	−0.3 V to +7 V
$V_{OUT}x$ to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	125°C
Reflow Soldering Peak Temperature, Pb-Free (J-STD-020)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}	Unit
20-Lead TSSOP (RU-20)[1]	98.65	44.39	17.58	1.77	43.9	°C/W
20-Lead LFCSP (CP-20-8)[2]	82	16.67	32.5	0.43	22	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD51

[2] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with nine thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

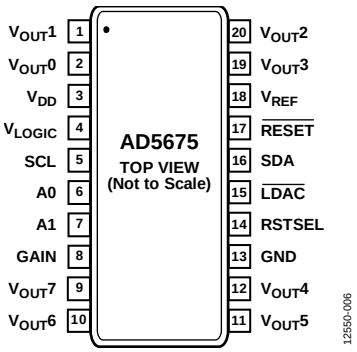


Figure 4. TSSOP Pin Configuration

Table 7. TSSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{OUT}1$	Analog Output Voltage from DAC 1. The output amplifier has rail-to-rail operation.
2	$V_{OUT}0$	Analog Output Voltage from DAC 0. The output amplifier has rail-to-rail operation.
3	V_{DD}	Power Supply Input. The AD5675 operates from 2.7 V to 5.5 V. Decouple the V_{DD} supply with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	V_{LOGIC}	Digital Power Supply. The voltage on this pin ranges from 1.62 V to 5.5 V.
5	SCL	Serial Clock Line. This pin is used in conjunction with the SDA line to clock data into or out of the 24-bit input shift register.
6	A0	Address Input. This pin sets the first LSB of the 7-bit slave address.
7	A1	Address Input. This pin sets the second LSB of the 7-bit slave address.
8	GAIN	Span Set. When this pin is tied to GND, all eight DAC outputs have a span from 0 V to V_{REF}. If this pin is tied to V_{LOGIC}, all eight DACs output a span of 0 V to 2 × V_{REF}.
9	$V_{OUT}7$	Analog Output Voltage from DAC 7. The output amplifier has rail-to-rail operation.
10	$V_{OUT}6$	Analog Output Voltage from DAC 6. The output amplifier has rail-to-rail operation.
11	$V_{OUT}5$	Analog Output Voltage from DAC 5. The output amplifier has rail-to-rail operation.
12	$V_{OUT}4$	Analog Output Voltage from DAC 4. The output amplifier has rail-to-rail operation.
13	GND	Ground Reference Point for All Circuitry on the Device.
14	RSTSEL	Power-On Reset. Tie this pin to GND to power up all eight DACs to zero scale. Tie this pin to V_{LOGIC} to power up all eight DACs to midscale.
15	$\overline{\text{LDAC}}$	Load DAC. $\overline{\text{LDAC}}$ operates in two modes, asynchronously and synchronously. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data, which allows all DAC outputs to update simultaneously. This pin can also be tied permanently low.
16	SDA	Serial Data Input. This pin is used in conjunction with the SCL line to clock data into or out of the 24-bit input shift register. SDA is a bidirectional, open-drain data line that must be pulled to the supply with an external pull-up resistor.
17	$\overline{\text{RESET}}$	Asynchronous Reset Input. The $\overline{\text{RESET}}$ input is falling edge sensitive. When $\overline{\text{RESET}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{RESET}}$ is activated, the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin.
18	V_{REF}	Reference Input Voltage.
19	$V_{OUT}3$	Analog Output Voltage from DAC 3. The output amplifier has rail-to-rail operation.
20	$V_{OUT}2$	Analog Output Voltage from DAC 2. The output amplifier has rail-to-rail operation.

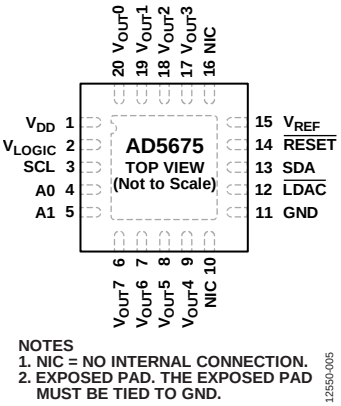


Figure 5. LFCSP Pin Configuration

Table 8. LFCSP Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. The AD5675 operates from 2.7 V to 5.5 V. Decouple the V_{DD} supply with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
2	V_{LOGIC}	Digital Power Supply. The voltage on this pin ranges from 1.62 V to 5.5 V.
3	SCL	Serial Clock Line. This pin is used in conjunction with the SDA line to clock data into or out of the 24-bit input shift register.
4	A0	Address Input. Sets the first LSB of the 7-bit slave address.
5	A1	Address Input. Sets the second LSB of the 7-bit slave address.
6	$V_{OUT}7$	Analog Output Voltage from DAC 7. The output amplifier has rail-to-rail operation.
7	$V_{OUT}6$	Analog Output Voltage from DAC 6. The output amplifier has rail-to-rail operation.
8	$V_{OUT}5$	Analog Output Voltage from DAC 5. The output amplifier has rail-to-rail operation.
9	$V_{OUT}4$	Analog Output Voltage from DAC 4. The output amplifier has rail-to-rail operation.
10, 16	NIC	No Internal Connection.
11	GND	Ground Reference Point for All Circuitry on the Device.
12	$\overline{LDAC}$	Load DAC. $\overline{LDAC}$ operates in two modes, asynchronously and synchronously. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data, which allows all DAC outputs to update simultaneously. This pin can also be tied permanently low.
13	SDA	Serial Data Input. This pin is used in conjunction with the SCL line to clock data into or out of the 24-bit input shift register. SDA is a bidirectional, open-drain data line that must be pulled to the supply with an external pull-up resistor.
14	$\overline{RESET}$	Asynchronous Reset Input. The $\overline{RESET}$ input is falling edge sensitive. When $\overline{RESET}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{RESET}$ is activated, the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin.
15	V_{REF}	Reference Input Voltage.
17	$V_{OUT}3$	Analog Output Voltage from DAC 3. The output amplifier has rail-to-rail operation.
18	$V_{OUT}2$	Analog Output Voltage from DAC 2. The output amplifier has rail-to-rail operation.
19	$V_{OUT}1$	Analog Output Voltage from DAC 1. The output amplifier has rail-to-rail operation.
20	$V_{OUT}0$	Analog Output Voltage from DAC 0. The output amplifier has rail-to-rail operation.
	EPAD	Exposed Pad. The exposed pad must be tied to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

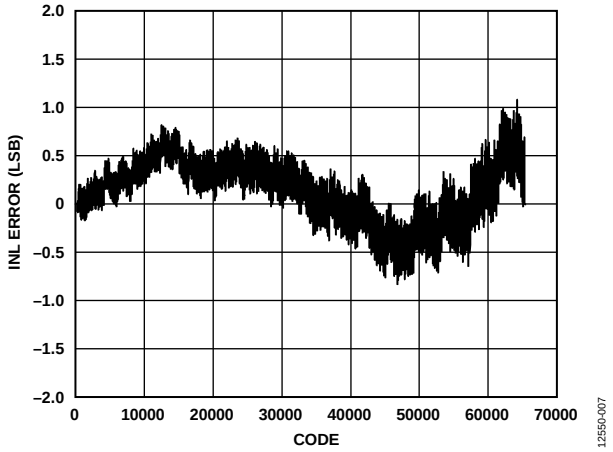


Figure 6. INL Error vs. Code

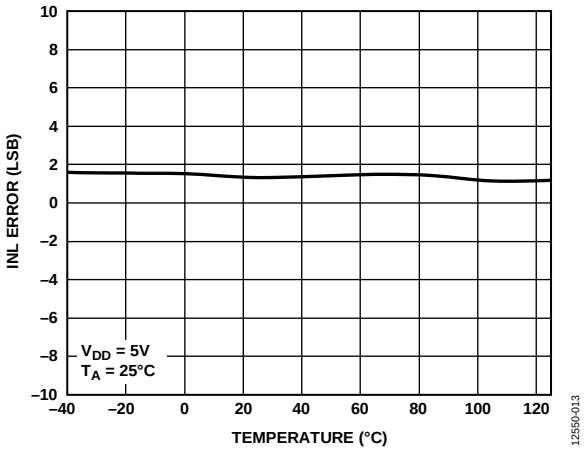


Figure 9. INL Error vs. Temperature

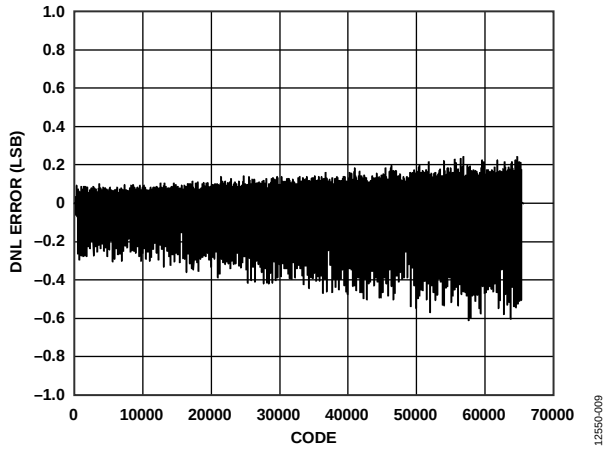


Figure 7. DNL Error vs. Code

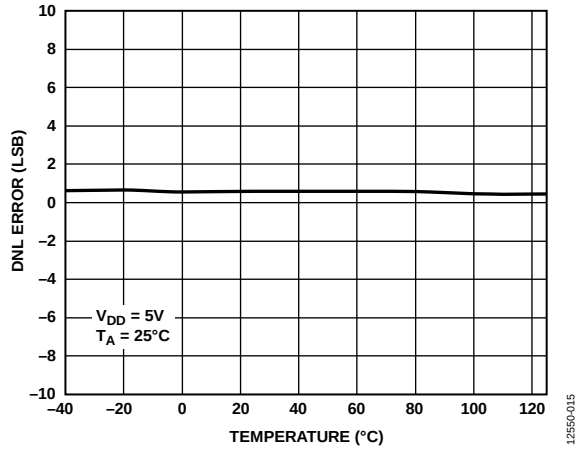


Figure 10. DNL Error vs. Temperature

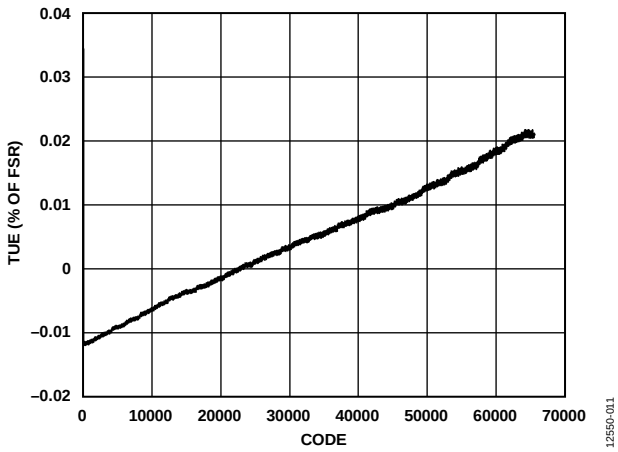


Figure 8. TUE vs. Code

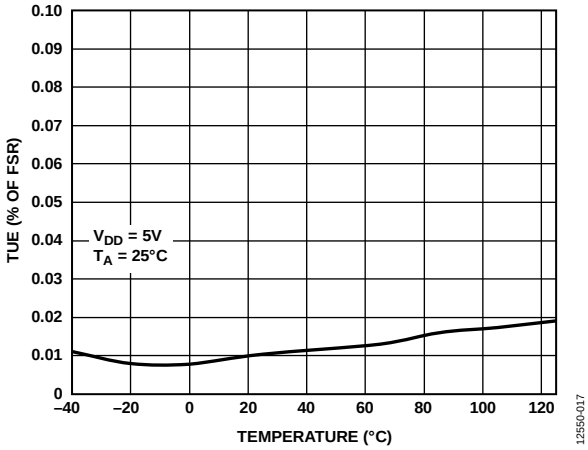


Figure 11. TUE vs. Temperature

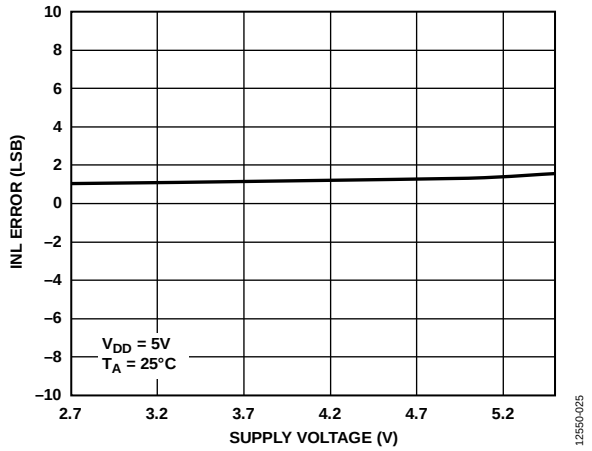


Figure 12. INL Error vs. Supply Voltage

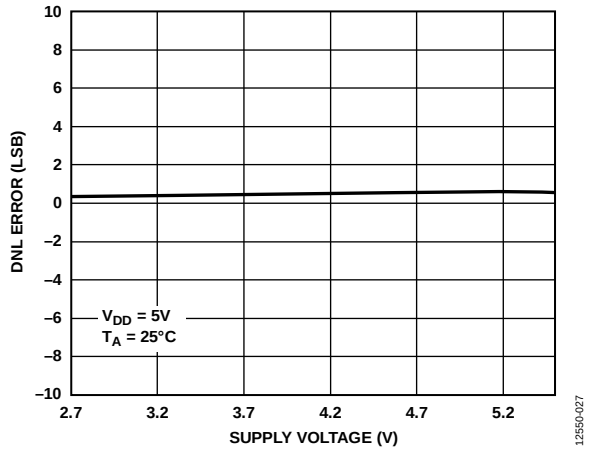


Figure 13. DNL Error vs. Supply Voltage

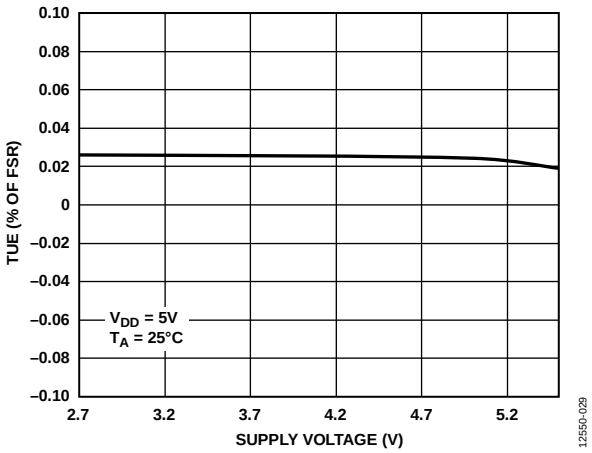


Figure 14. TUE vs. Supply Voltage

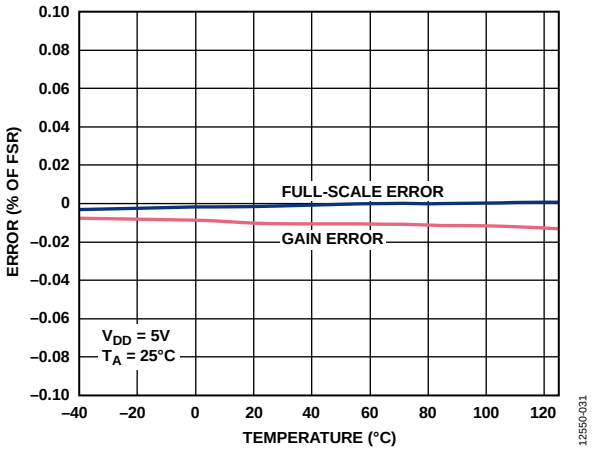


Figure 15. Gain Error and Full-Scale Error vs. Temperature

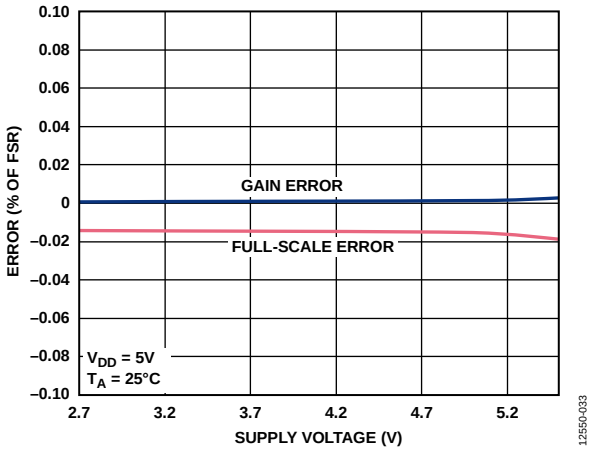


Figure 16. Gain Error and Full-Scale Error vs. Supply Voltage

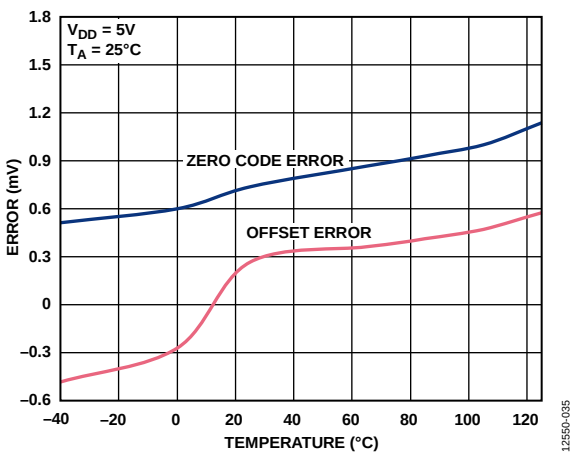


Figure 17. Zero Code Error and Offset Error vs. Temperature

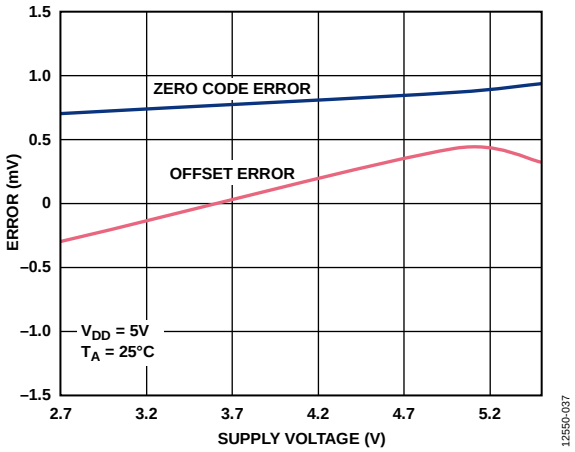


Figure 18. Zero Code Error and Offset Error vs. Supply Voltage

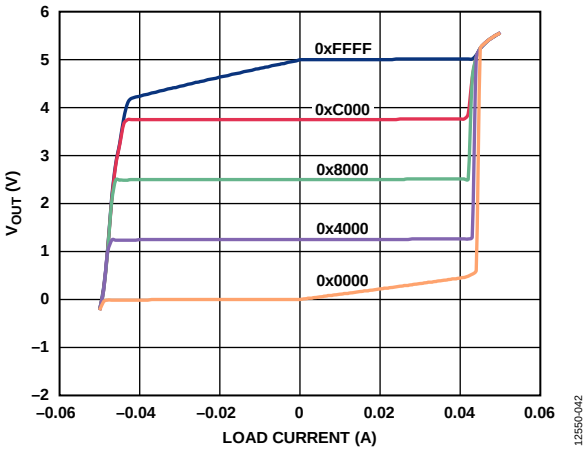


Figure 21. Source and Sink Capability at 5 V

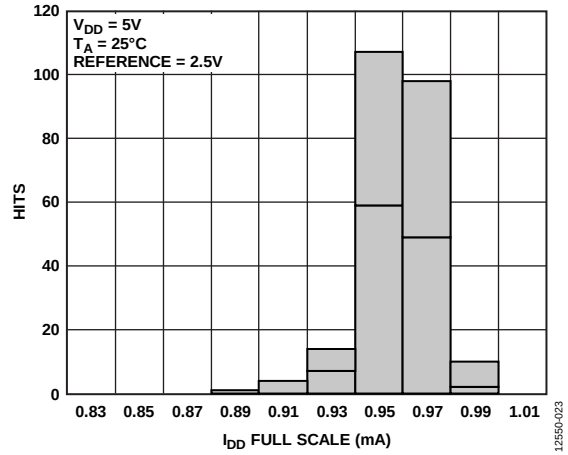


Figure 19. Supply Current (I_{DD}) Histogram

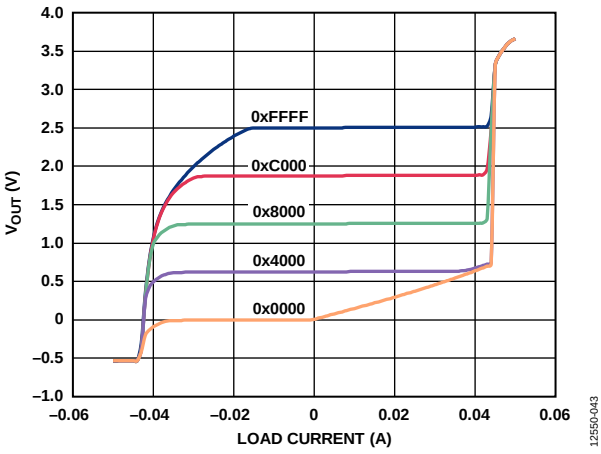


Figure 22. Source and Sink Capability at 3 V

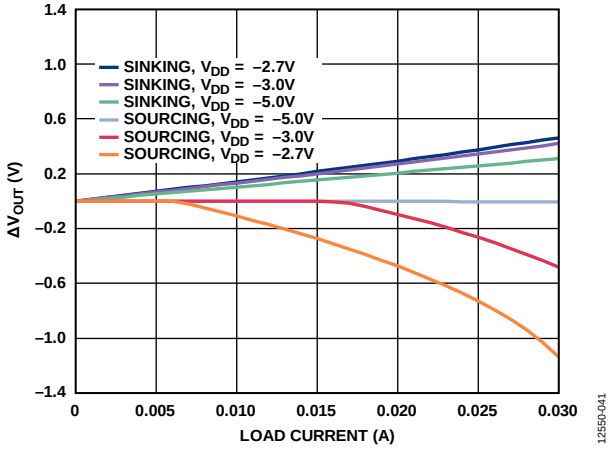


Figure 20. Headroom/Footroom (ΔV_{OUT}) vs. Load Current

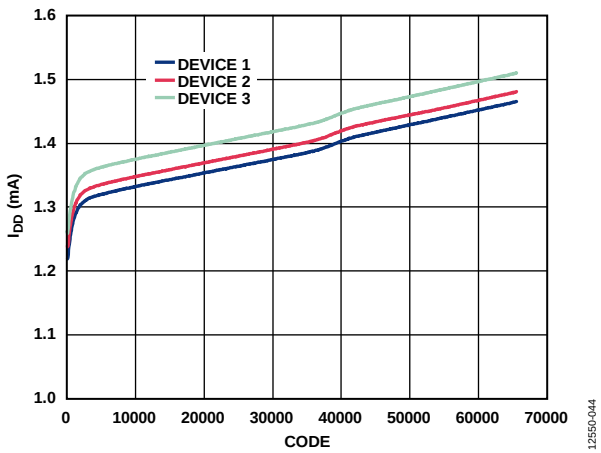


Figure 23. I_{DD} vs. Code

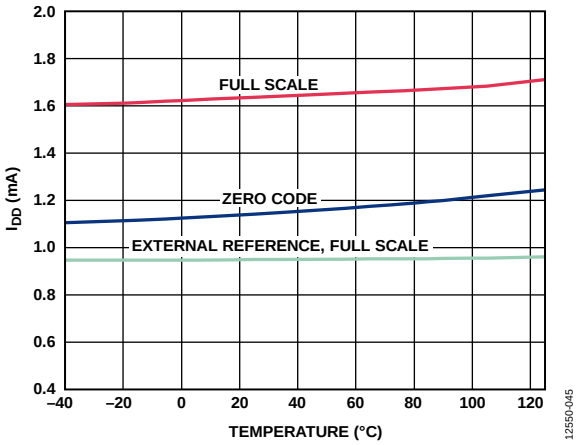


Figure 24. I_{DD} vs. Temperature

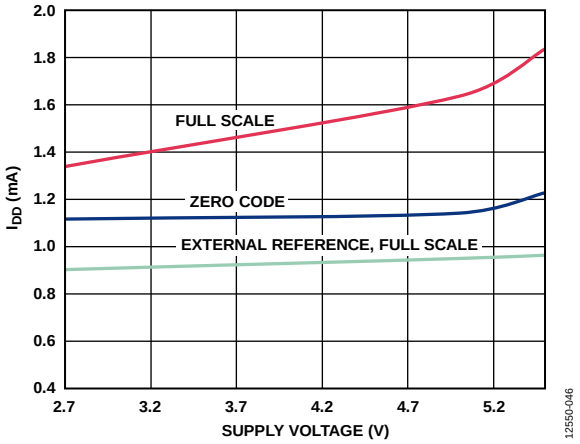


Figure 25. I_{DD} vs. Supply Voltage

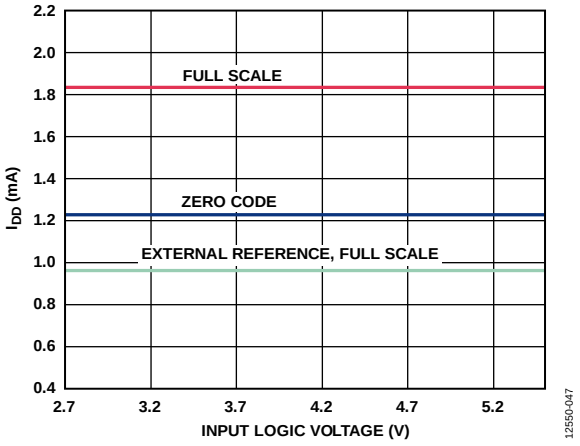


Figure 26. I_{DD} vs. Input Logic Voltage

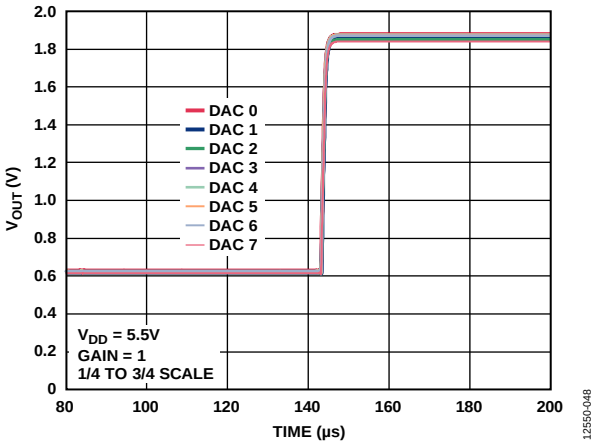


Figure 27. Full-Scale Settling Time

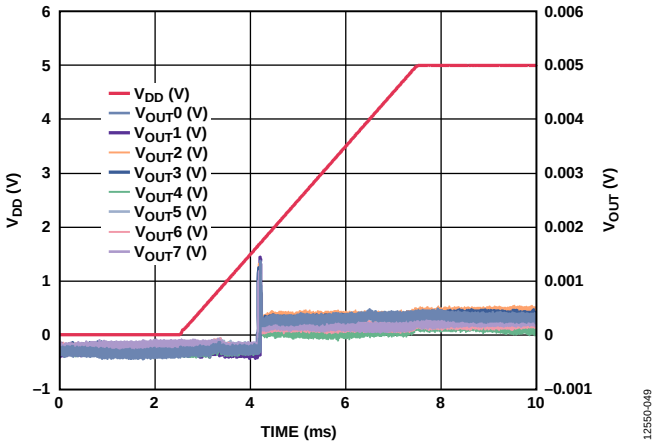


Figure 28. Power-On Reset to 0 V and Midscale

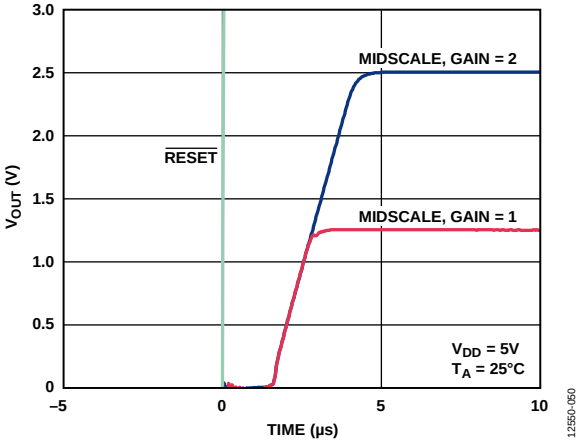


Figure 29. Exiting Power-Down to Midscale

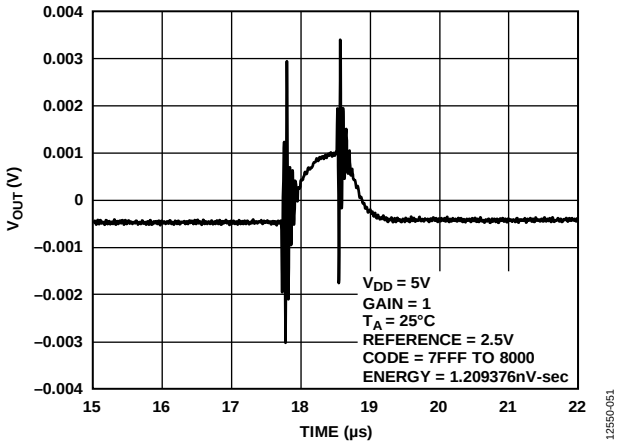


Figure 30. Digital-to-Analog Glitch Impulse

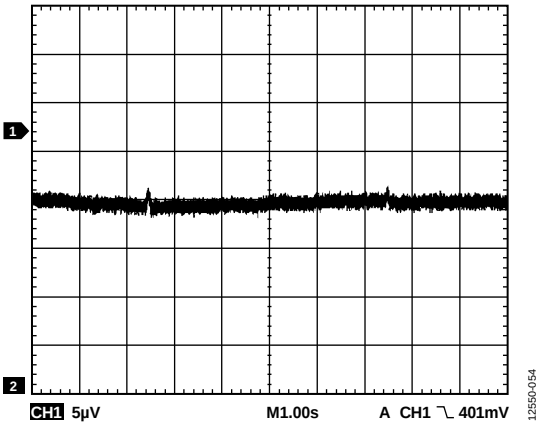


Figure 33. 0.1 Hz to 10 Hz Output Noise Plot

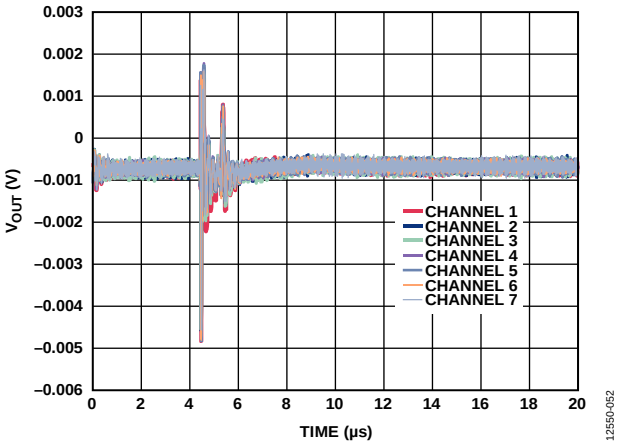


Figure 31. Analog Crosstalk

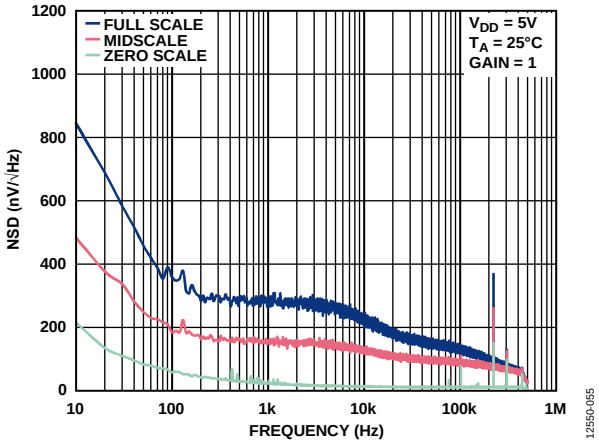


Figure 34. Noise Spectral Density (NSD)

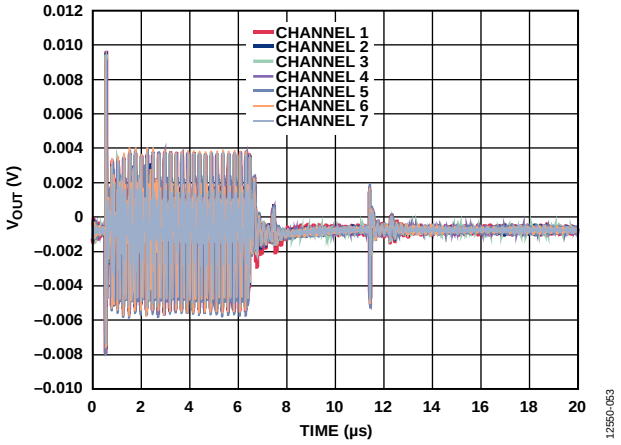


Figure 32. DAC-to-DAC Crosstalk

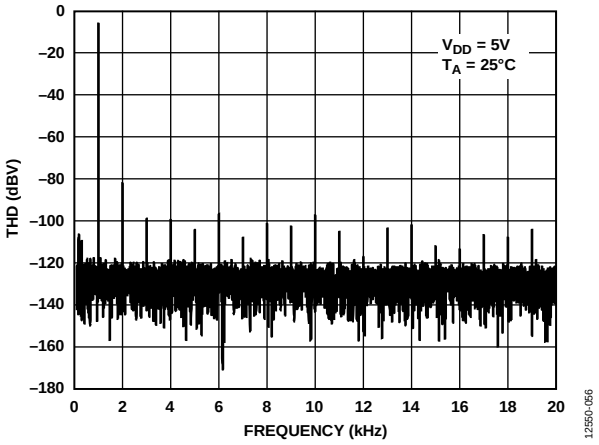


Figure 35. Total Harmonic Distortion (THD) at 1 kHz

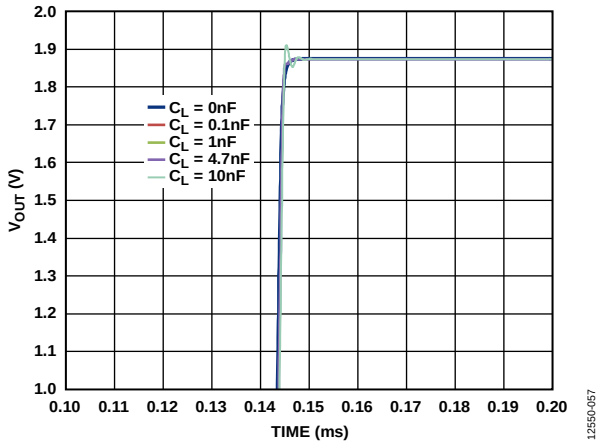


Figure 36. Settling Time at Various Capacitive Loads

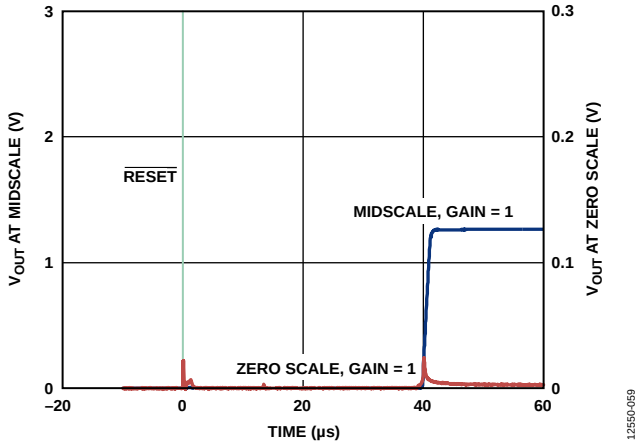


Figure 38. Hardware Reset

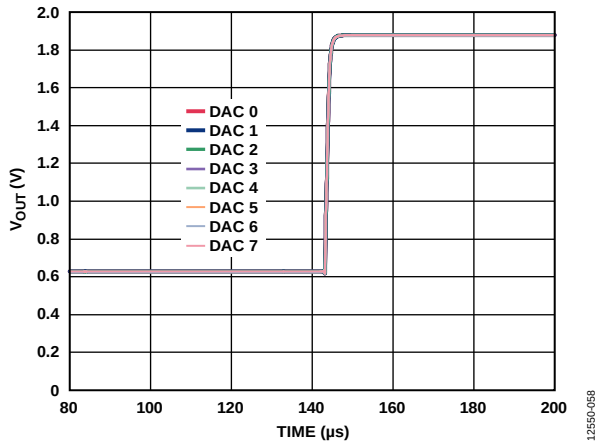


Figure 37. Settling Time, 5.5 V

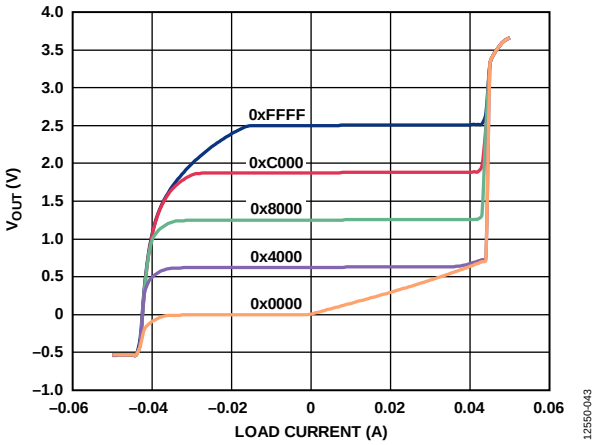


Figure 39. Multiplying Bandwidth

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For a DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design.

Zero Code Error
Zero code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. The ideal output is 0 V. The zero code error is always positive because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero code error is expressed in mV.

Full-Scale Error
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. The ideal output is V_{DD} − 1 LSB. Full-scale error is expressed in percent of full-scale range (% of FSR).

Gain Error
Gain error is a measure of the span error of a DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % of FSR.

Offset Error Drift
Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in µV/°C.

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured with Code 256 loaded in the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
The dc PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to the change in V_{DD} for the full-scale output of the DAC. It is measured in mV/V. V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
The output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Noise Spectral Density (NSD)
NSD is a measurement of the internally generated random noise. Random noise is characterized as spectral density (nV/√Hz). To measure NSD, load the DAC to midscale and measure the noise at the output. It is measured in nV/√Hz.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in µV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has on another DAC kept at midscale. It is expressed in µV/mA.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-sec.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. To measure analog crosstalk, first load one of the input registers with a full-scale code change (all 0s to all 1s and vice versa). Then, execute a software $\overline{\text{LDAC}}$ and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa), using the write to and update commands while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-sec.

Multiplying Bandwidth

The multiplying bandwidth is a measure of the finite bandwidth of the amplifiers within the DAC. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)

THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. THD is measured in dB.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5675 is an octal, 16-bit, serial input, voltage output DAC. The AD5675 operates from a supply voltage of 2.7 V to 5.5 V. Data is written to the AD5675 in a 24-bit word format via a 2-wire serial interface. The AD5675 incorporates a power-on reset circuit to ensure that the DAC output powers up to a known output state. The device also has a software power-down mode that reduces the typical current consumption to 1 μA.

TRANSFER FUNCTION

The gain of the output amplifier is set to ×1 or ×2 using the gain select pin (GAIN). When the gain select pin is tied to GND, all eight DAC outputs have a span from 0 V to V_{REF}. When the gain select pin is tied to V_{LOGIC}, all eight DACs output a span of 0 V to 2 × V_{REF}.

DAC ARCHITECTURE

The AD5675 implements a segmented string DAC architecture with an internal output buffer. Figure 40 shows the internal block diagram.

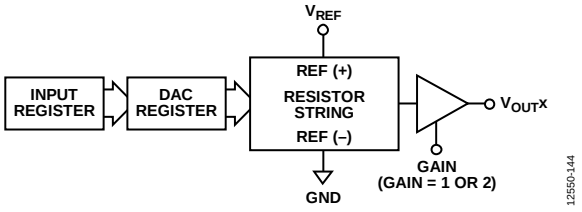


Figure 40. Single DAC Channel Architecture Block Diagram

The simplified segmented resistor string DAC structure is shown in Figure 41. The code loaded to the DAC register determines the node on the string where the voltage is tapped off and fed into the output amplifier. The voltage is tapped off by closing one of the switches and connecting the string to the amplifier. Because each resistance in the string has the same value, R, the string DAC is guaranteed monotonic.

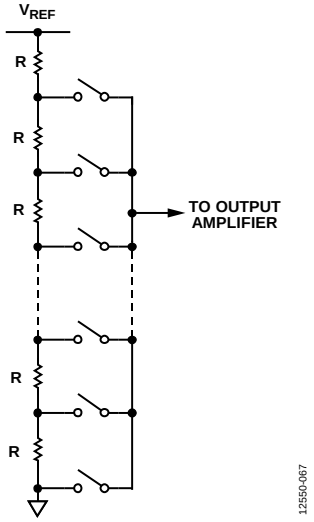


Figure 41. Resistor String Structure

Output Amplifier

The output buffer amplifier generates rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. The actual range depends on the value of V_{REF}, the GAIN pin, the offset error, and the gain error. The GAIN pin selects the gain of the output. If the GAIN pin is tied to GND, all eight outputs have a gain of 1, and the output range is 0 V to V_{REF}. If the GAIN pin is tied to V_{LOGIC}, all eight outputs have a gain of 2, and the output range is 0 V to 2 × V_{REF}.

This amplifier can drive a load of 1 kΩ in parallel with 10 nF to GND. The slew rate is 0.8 V/μs with a typical ¼ to ¾ scale settling time of 5 μs.

SERIAL INTERFACE

The AD5675 uses a 2-wire, I²C-compatible serial interface. The device can be connected to an I²C bus as a slave device under the control of the master devices. The AD5675 supports standard (100 kHz) and fast (400 kHz) data transfer modes. Support is not provided for 10-bit addressing and general call addressing.

Input Shift Register

The input shift register of the AD5675 is 24 bits wide. Data is loaded MSB first (DB23), and the first four bits are the command bits, C3 to C0 (see Table 9), followed by the 4-bit DAC address bits, A3 to A0 (see Table 10), and finally, the 16-bit data-word.

The data-word comprises a 16-bit input code (see Figure 42). These data bits are transferred to the input register on the 24 falling edges of SCL.

Commands execute on individual DAC channels, combined DAC channels, or on all DACs, depending on the address bits selected.

Table 9. Command Definitions

Command				
C3	C2	C1	C0	Description
0	0	0	0	No operation
0	0	0	1	Write to Input Register n (where n = 0 to 7, depending on the DAC selected from the address bits in Table 10, dependent on $\overline{LDAC}$)
0	0	1	0	Update DAC Register n with the contents of Input Register n
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up the DAC
0	1	0	1	Hardware $\overline{LDAC}$ mask register
0	1	1	0	Software reset (power-on reset)
0	1	1	1	Gain setup register (LFCSP package only)
1	0	0	0	Reserved
1	0	0	1	Set up the readback register (readback enable)
1	0	1	0	Update all channels of the input register simultaneously with the input data
1	0	1	1	Update all channels of the DAC register and input register simultaneously with the input data
1	1	0	0	Reserved
…	…	…	…	
1	1	1	1	Reserved

Table 10. Address Commands

Channel Address, Bits[3:0]				
A3	A2	A1	A0	Selected DAC Channel
0	0	0	0	DAC 0
0	0	0	1	DAC 1
0	0	1	0	DAC 2
0	0	1	1	DAC 3
0	1	0	0	DAC 4
0	1	0	1	DAC 5
0	1	1	0	DAC 6
0	1	1	1	DAC 7

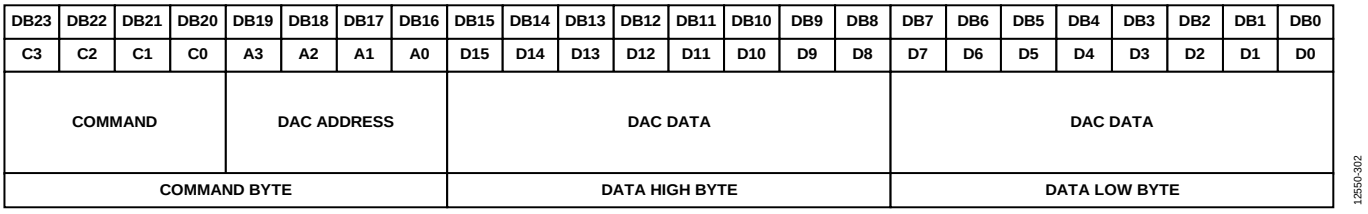


Figure 42. Input Shift Register Content

WRITE AND UPDATE COMMANDS

Write to Input Register n (Dependent on $\overline{\text{LDAC}}$)

Command 0001 allows the user to write to the dedicated input register of each DAC individually. When $\overline{\text{LDAC}}$ is low, the input register is transparent, if not controlled by the $\overline{\text{LDAC}}$ mask register.

Update DAC Register n with Contents of Input Register n

Command 0010 loads the DAC registers and outputs with the contents of the selected input registers and updates the DAC outputs directly. Data Bit D7 to Bit D0 determine which DACs have data from the input register transferred to the DAC register. Setting a bit to 1 transfers data from the input register to the appropriate DAC register.

Write to and Update DAC Channel n (Independent of $\overline{\text{LDAC}}$)

Command 0011 allows the user to write to the DAC registers and updates the DAC outputs directly. The DAC address bits are used to select the DAC channel.

I²C SLAVE ADDRESS

The AD5675 has a 7-bit I²C slave address. The five MSBs are 00011, and the two LSBs (A1 and A0) are set by the state of the A1 and A0 address pins. The ability to make hardwired changes to A1 and A0 allows the user to incorporate up to four AD5675 devices on one bus (see Table 11).

Table 11. Device Address Selection

A1 Pin Connection	A0 Pin Connection	A1	A0
GND	GND	0	0
GND	V_{LOGIC}	0	1
V_{LOGIC}	GND	1	0
V_{LOGIC}	V_{LOGIC}	1	1

SERIAL OPERATION

The 2-wire I²C serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition when a high to low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address.
2. The slave device with the transmitted address responds by pulling SDA low during the ninth clock pulse (this is called the acknowledge bit, or ACK). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its input shift register.
3. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). Transitions on the SDA line must occur during the low period of SCL; SDA must remain stable during the high period of SCL.
4. After all data bits are read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge (NACK) for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse, and then high again during the 10th clock pulse to establish a stop condition.

WRITE OPERATION

When writing to the AD5675, begin with a start command followed by an address byte (R/$\overline{\text{W}}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The AD5675 require two bytes of data for the DAC, and a command byte that controls various DAC functions. Three bytes of data must, therefore, be written to the DAC with the command byte followed by the most significant data byte and the least significant data byte, as shown in Figure 43. All these data bytes are acknowledged by the AD5675. A stop condition follows.

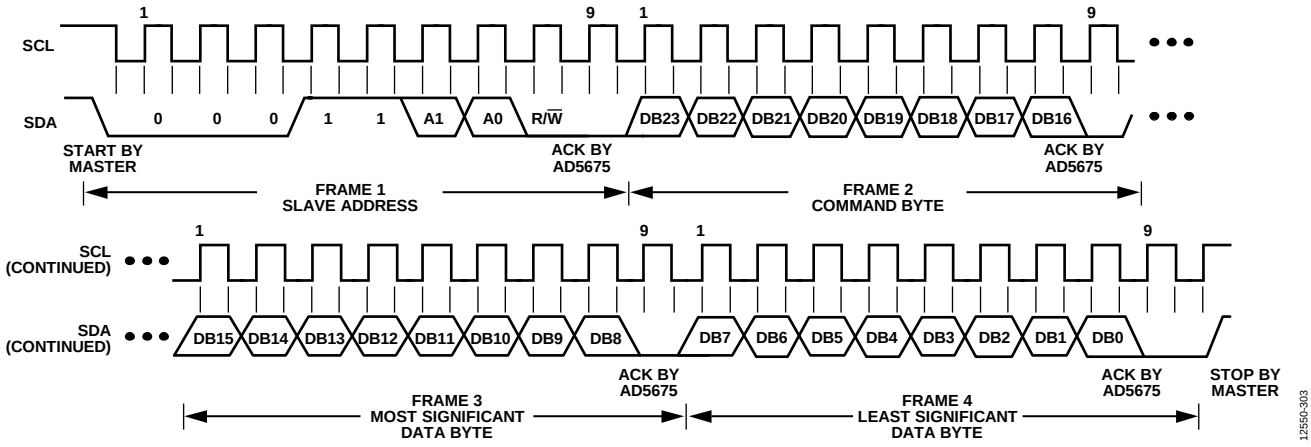


Figure 43. I²C Write Operation

READ OPERATION

When reading data back from the AD5675, begin with a start command followed by an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte must be followed by the command byte, which determines both the read command that is to follow and the pointer address to read from; the command byte is also acknowledged by the DAC. The user configures the channel to read back the contents of one or more DAC input registers and sets the readback command to active using the command byte.

Then, the master establishes a repeated start condition, and the address is resent with R/$\overline{W}$ = 1. This byte is acknowledged by the DAC, indicating that it is prepared to transmit data. Two bytes of data are then read from the DAC, as shown in Figure 44. A NACK condition from the master, followed by a stop condition, completes the read sequence. If more than one DAC is selected, DAC 0 is read back by default.

MULTIPLE DAC READBACK SEQUENCE

When reading data back from multiple AD5675 DACs, the user begins with an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte must be followed by the command byte, which is also acknowledged by the DAC. The user selects the first channel to read back using the command byte.

Following this sequence, the master establishes a repeated start condition, and the address is resent with R/$\overline{W}$ = 1. This byte is acknowledged by the DAC, indicating that it is prepared to transmit data. The first two bytes of data are then read from DAC Input Register n (selected using the command byte), MSB first, as shown in Figure 44. The next two bytes read back are the contents of DAC Input Register n + 1, and the next bytes read back are the contents of DAC Input Register n + 2. Data is read from the DAC input registers in this auto-incremented fashion until a NACK followed by a stop condition follows. If the contents of DAC Input Register 7 are read out, the next two bytes of data read are the contents of DAC Input Register 0.

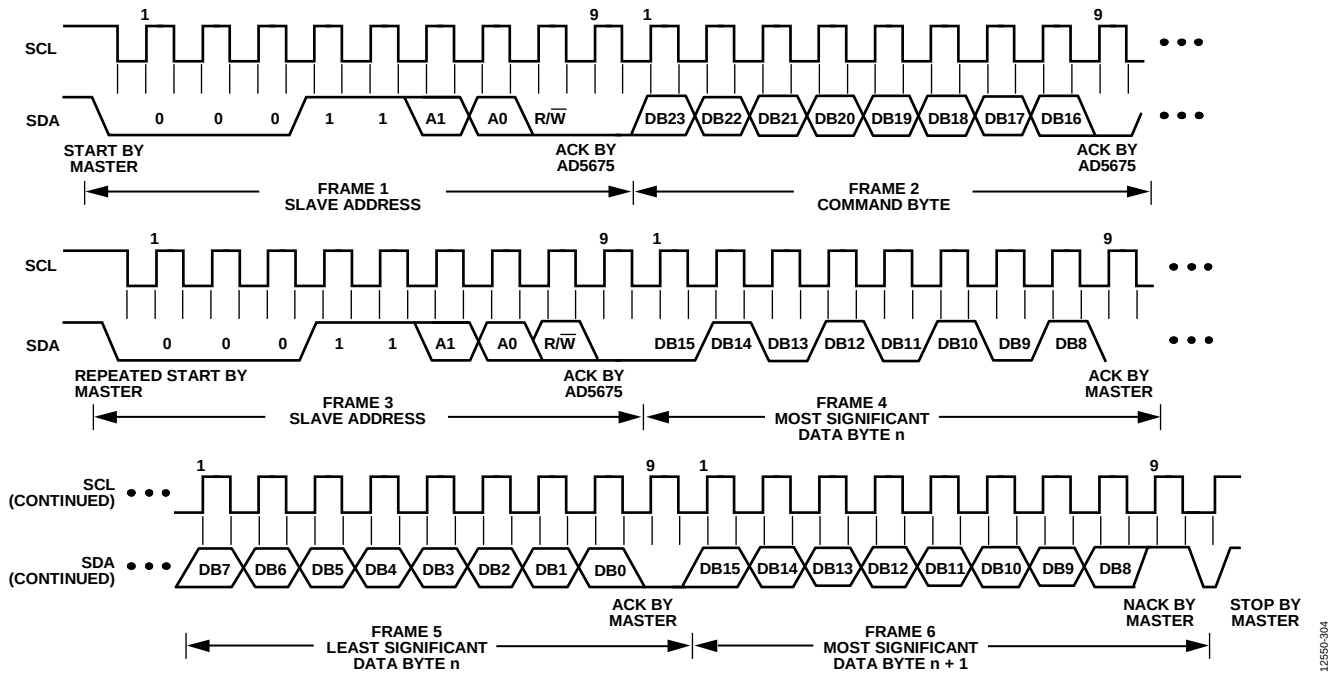


Figure 44. I²C Read Operation

POWER-DOWN OPERATION

The AD5675 contains two separate power-down modes. Command 0100 is designated for the power-down function (see Table 9). These power-down modes are software programmable by setting 16 bits, Bit DB15 to Bit DB0, in the input shift register. There are two bits associated with each DAC channel. Table 12 shows how the state of the two bits corresponds to the mode of operation of the device.

Any or all DACs (DAC 0 to DAC 7) power down to the selected mode by setting the corresponding bits. See Table 13 for the contents of the input shift register during the power-down/power-up operation.

Table 12. Modes of Operation

Operating Mode	PD1	PD0
Normal Operation	0	0
Power-Down Modes		
1 kΩ to GND	0	1
Tristate	1	1

When both Bit PD1 and Bit PD0 in the input shift register are set to 0, the device works normally with its normal power consumption of typically 1 mA at 5 V. However, for the two power-down modes, the supply current falls to typically 1 µA. In addition to this fall, the output stage switches internally from the amplifier output to a resistor network of known values. Therefore, the DAC channel output impedance is defined when the channel is powered down. There are two different power-down options. The output is connected internally to GND through either a 1 kΩ resistor, or it is left open circuited (tristate). The output stage is shown in Figure 45.

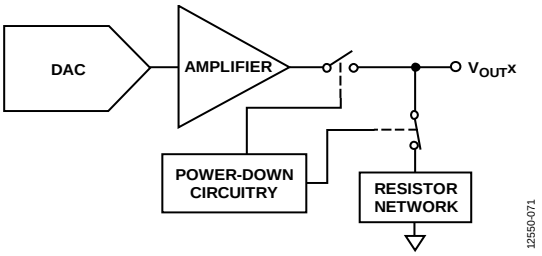


Figure 45. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry shut down when power-down mode is activated. However, the contents of the DAC registers are unaffected when in power-down mode. The DAC registers can be updated while the device is in power-down mode. The time required to exit power-down is typically 2.5 µs for V_{DD} = 5 V.

LOAD DAC (HARDWARE $\overline{\text{LDAC}}$ PIN)

The AD5675 DACs have a double buffered interface consisting of two banks of registers: input registers and DAC registers. The user can write to any combination of the input registers. Updates to the DAC registers are controlled by the $\overline{\text{LDAC}}$ pin.

Instantaneous DAC Updating ($\overline{\text{LDAC}}$ Held Low)

For instantaneous updating of the DACs, $\overline{\text{LDAC}}$ is held low while data is clocked into the input register using Command 0001. Both the addressed input register and the DAC register are updated on the 24th clock, and the output changes immediately.

Deferred DAC Updating ($\overline{\text{LDAC}}$ is Pulsed Low)

For deferred updating of the DACs, $\overline{\text{LDAC}}$ is held high while data is clocked into the input register using Command 0001. All DAC outputs are asynchronously updated by pulling $\overline{\text{LDAC}}$ low after the 24th clock. The update occurs on the falling edge of $\overline{\text{LDAC}}$.

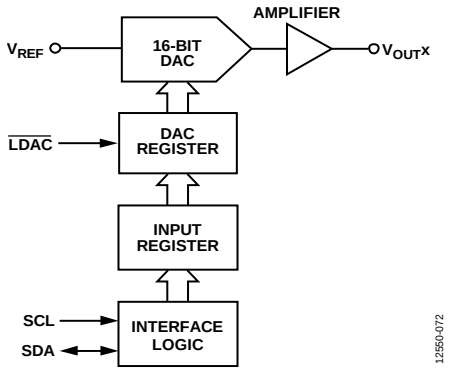


Figure 46. Simplified Diagram of Input Loading Circuitry for a Single DAC

Table 13. 24-Bit Input Shift Register Contents of Power-Down/Power-Up Operation

			DAC 7	DAC 6	DAC 5	DAC 4	DAC 3	DAC 2	DAC 1	DAC 0
[DB23:DB20]	DB19	[DB18:DB16]	[DB15:DB14]	[DB13:DB12]	[DB11:DB10]	[DB9:DB8]	[DB7:DB6]	[DB5:DB4]	[DB3:DB2]	[DB1:DB0]
0100	0	XXX[1]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]

[1] X means don't care.

$\overline{\text{LDAC}}$ MASK REGISTER

Command 0101 is reserved for this hardware $\overline{\text{LDAC}}$ function. The address bits are ignored. Writing to the DAC using Command 0101 loads the 8-bit $\overline{\text{LDAC}}$ register (DB7 to DB0). The default for each channel is 0, that is, the $\overline{\text{LDAC}}$ pin works normally. Setting the bits to 1 forces this DAC channel to ignore transitions on the $\overline{\text{LDAC}}$ pin, regardless of the state of the hardware $\overline{\text{LDAC}}$ pin. This flexibility is useful in applications where the user wants to select which channels respond to the $\overline{\text{LDAC}}$ pin.

The $\overline{\text{LDAC}}$ register gives the user extra flexibility and control over the hardware $\overline{\text{LDAC}}$ pin (see Table 15). Setting the $\overline{\text{LDAC}}$ bits (DB0 to DB7) to 0 for a DAC channel means that the update for this channel is controlled by the hardware $\overline{\text{LDAC}}$ pin.

Table 14. $\overline{\text{LDAC}}$ Overwrite Definition

Load $\overline{\text{LDAC}}$ Register		
$\overline{\text{LDAC}}$ Bits (DB7 to DB0)	**$\overline{\text{LDAC}}$ Pin**	**$\overline{\text{LDAC}}$ Operation**
00000000	1 or 0	Determined by the $\overline{\text{LDAC}}$ pin.
11111111	X[1]	DAC channels update and override the $\overline{\text{LDAC}}$ pin. DAC channels see $\overline{\text{LDAC}}$ as 1.

[1] X means don't care.

Table 15. Write Commands and $\overline{\text{LDAC}}$ Pin Truth Table[1]

Command	Description	Hardware $\overline{\text{LDAC}}$ Pin State	Input Register Contents	DAC Register Contents
0001	Write to Input Register n (dependent on $\overline{\text{LDAC}}$)	V_{LOGIC}	Data update	No change (no update)
		GND[2]	Data update	Data update
0010	Update DAC Register n with the contents of Input Register n	V_{LOGIC}	No change	Updated with input register contents
		GND	No change	Updated with input register contents
0011	Write to and update DAC Channel n	V_{LOGIC}	Data update	Data update
		GND	Data update	Data update

[1] A high to low hardware $\overline{\text{LDAC}}$ pin transition always updates the contents of the DAC register with the contents of the input register on channels that are not masked (blocked) by the $\overline{\text{LDAC}}$ mask register.
[2] When $\overline{\text{LDAC}}$ is permanently tied low, the $\overline{\text{LDAC}}$ mask bits are ignored.

HARDWARE RESET ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ pin is an active low reset that allows the outputs to be cleared to either zero scale or midscale. The clear code value is user selectable via the RSTSEL pin. Keep $\overline{\text{RESET}}$ low for a minimum of 2 µs to complete the operation (see Table 4). When the $\overline{\text{RESET}}$ signal is returned high, the output remains at the cleared value until a new value is programmed. While the $\overline{\text{RESET}}$ pin is low, the outputs cannot be updated with a new value. Any events on $\overline{\text{LDAC}}$ or $\overline{\text{RESET}}$ during power-on reset are ignored. If the $\overline{\text{RESET}}$ pin is pulled low at power-up, the device does not initialize correctly until the pin is released.

RESET SELECT PIN (RSTSEL)

The AD5675 contains a power-on reset circuit that controls the output voltage during power-up. By connecting the RSTSEL pin low, the output powers up to zero scale. Note that this power-up is outside the linear region of the DAC; by connecting the RSTSEL pin high, the $V_{OUT}x$ pins power up to midscale. The output remains powered up at this level until a valid write sequence is made to the DAC.

SOFTWARE RESET

A software executable reset function is also available, which resets the DAC to the power-on reset code. Command 0110 is designated for this software reset function. The DAC address bits must be set to 0x0 and the data bits set to 0x1234 for the software reset command to execute.

AMPLIFIER GAIN SELECTION ON LFCSP PACKAGE

The output amplifier gain setting for the LFCSP package is determined by the state of Bit DB2 in the gain setup register (see Table 16 and Table 17).

Table 16. Gain Setup Register

Bit	Description
DB2	Amplifier gain setting DB2 = 0; amplifier gain = 1 (default) DB2 = 1; amplifier gain = 2

Table 17. 24-Bit Input Shift Register Contents for Gain Setup Command

DB23 (MSB)	DB22	DB21	DB20	DB19 to DB3	DB2	DB1	DB0 (LSB)
0	1	1	1	Don't care	Gain	Reserved; set to 0	Reserved; set to 0

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The AD5675 is typically powered by the following supplies: V_{DD} = 3.3 V and V_{LOGIC} = 1.8 V.

The ADP7118 can be used to power the V_{DD} pin. The ADP160 can be used to power the V_{LOGIC} pin. This setup is shown in Figure 47. The ADP7118 can operate from input voltages up to 20 V. The ADP160 can operate from input voltages up to 5.5 V.

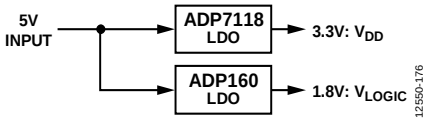


Figure 47. Low Noise Power Solution for the AD5675

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5675 is performed via a serial bus that uses a standard protocol that is compatible with DSP processors and microcontrollers. The communications channel requires a 2-wire interface consisting of a clock signal and a data signal.

AD5675 TO ADSP-BF531 INTERFACE

The I²C interface of the AD5675 is designed for easy connection to industry-standard DSPs and microcontrollers. Figure 48 shows the AD5675 connected to the Analog Devices, Inc., Blackfin® processor. The Blackfin processor has an integrated I²C port that can be connected directly to the I²C pins of the AD5675.

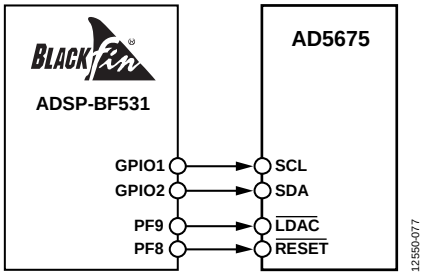


Figure 48. AD5675 to ADSP-BF531 Interface

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the PCB on which the AD5675 is mounted so that the device lies on the analog plane.

The AD5675 must have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

In systems where many devices are on one board, it is often useful to provide some heat sinking capability to allow the power to dissipate easily.

The GND plane on the device can be increased (as shown in Figure 49) to provide a natural heat sinking effect.

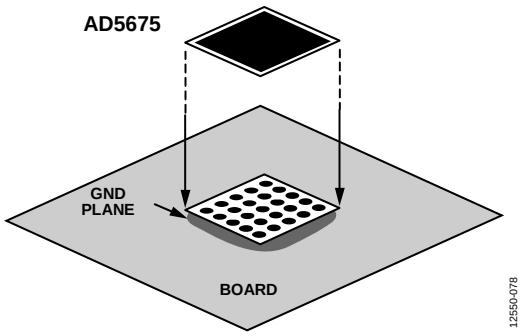


Figure 49. Pad Connection to Board

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. iCoupler® products from Analog Devices provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5675 makes the device ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 50 shows a 4-channel isolated interface to the AD5675 using an ADuM1251. For further information, visit www.analog.com/icoupler.

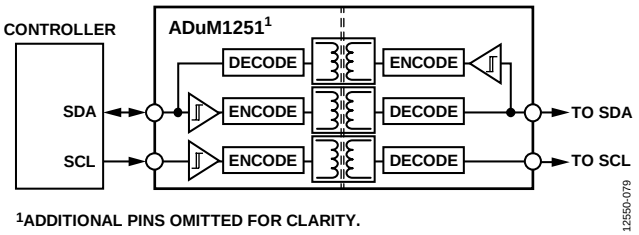
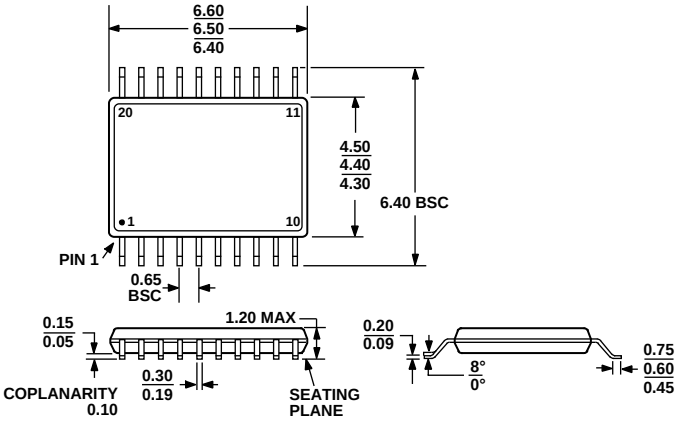


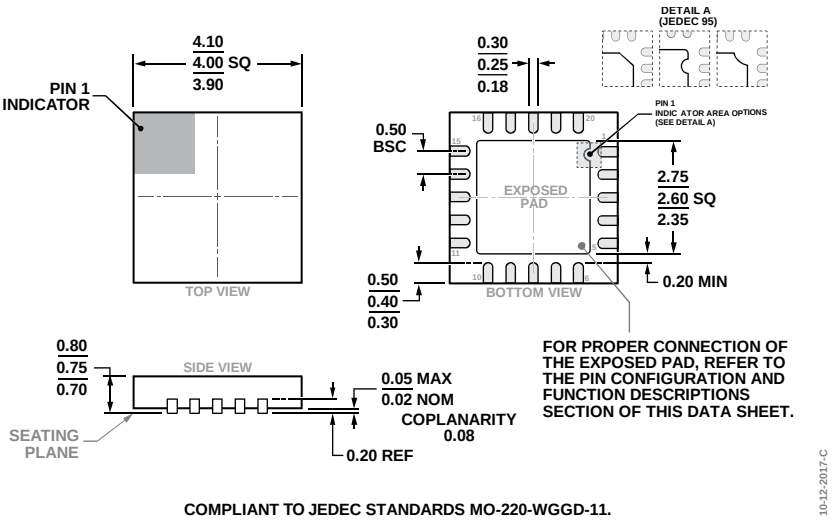
Figure 50. Isolated Interface

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 51. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-11.

Figure 52. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Resolution (Bits)	Temperature Range	Accuracy	Package Description	Package Option
AD5675ARUZ	16	−40°C to +125°C	±8 LSB INL	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5675ARUZ-REEL7	16	−40°C to +125°C	±8 LSB INL	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5675BRUZ	16	−40°C to +125°C	±3 LSB INL	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5675BRUZ-REEL7	16	−40°C to +125°C	±3 LSB INL	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5675ACPZ-REEL7	16	−40°C to +125°C	±8 LSB INL	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
AD5675ACPZ-RL	16	−40°C to +125°C	±8 LSB INL	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
AD5675BCPZ-REEL7	16	−40°C to +125°C	±3 LSB INL	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
AD5675BCPZ-RL	16	−40°C to +125°C	±3 LSB INL	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
EVAL-AD5675SDZ				Evaluation Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

D12550-0-4/18(C)