

1 Characteristics

Table 2. Absolute ratings (limiting values)

Symbol	Parameter	Test conditions		Value	Unit
$I_{T(RMS)}$	On-state RMS current (full sine wave)	$T_c = 112\text{ °C}$		3	A
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25 °C)	f = 50 Hz	$t_p = 20\text{ ms}$	20	A
		f = 60 Hz	$t_p = 16.7\text{ ms}$	21	
I^2t	I^2t value for fusing (T_j initial = 25 °C)	$t_p = 10\text{ ms}$		2.6	A ² s
di/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, $t_r = 100\text{ ns}$	f = 120 Hz	$T_j = 125\text{ °C}$	50	A/ μ s
$V_{PP}^{(1)}$	Non repetitive line peak mains voltage	$T_j = 25\text{ °C}$		2	kV
$P_{G(AV)}$	Average gate power dissipation	$T_j = 125\text{ °C}$		0.1	W
P_{GM}	Peak gate power	$t_p = 20\text{ }\mu$ s	$T_j = 125\text{ °C}$	10	W
I_{GM}	Peak gate current	$t_p = 20\text{ }\mu$ s	$T_j = 125\text{ °C}$	1.6	A
T_{stg}	Storage junction temperature range			-40 to +150	°C
T_j	Operating junction temperature range			-40 to +125	°C
T_L	Maximum lead temperature for soldering during 10 s			260	°C

1. according to test described by IEC 61000-4-5 standard (see [Figure 18](#)).

Table 3. Electrical characteristics

Symbol	Test conditions	Quadrant	T_j	Value		Unit
$I_{GT}^{(1)}$	$V_{OUT} = 12\text{ V}$, $R_L = 33\text{ }\Omega$	I - II - III	25 °C	Max.	10	mA
V_{GT}				Max.	1.1	V
V_{GD}	$V_{OUT} = V_{DRM}$, $R_L = 3.3\text{ k}\Omega$	I - II - III	125 °C	Min.	0.2	V
$I_H^{(2)}$	$I_{OUT} = 100\text{ mA}$		25 °C	Max.	20	mA
I_L	$I_G = 1.2 \times I_{GT}$	I - III	25 °C	Max.	25	mA
		II			35	
$dV/dt^{(2)}$	$V_{OUT} = 67\% V_{DRM}$, gate open		125 °C	Min.	1000	V/ μ s
$(di/dt)_c^{(2)}$	$(dV/dt)_c = 0.1\text{ V}/\mu$ s		125 °C	Min.	5	A/ms
$(di/dt)_c^{(2)}$	$(dV/dt)_c = 10\text{ V}/\mu$ s		125 °C	Min.	1	A/ms
$V_{CL}^{(2)}$	$I_{CL} = 0.1\text{ mA}$, $t_p = 1\text{ ms}$		25 °C	Min.	850	V

1. Minimum I_{GT} is guaranteed at 5% of I_{GT} max.

2. For both polarities of OUT pin referenced to COM pin

Table 4. Static characteristics

Symbol	Test conditions		Value		Unit
$V_{TM}^{(1)}$	$I_{TM} = 4.2 \text{ A}$, $t_p = 380 \mu\text{s}$	$T_j = 25 \text{ }^\circ\text{C}$	Max.	1.8	V
$V_{TO}^{(1)}$	Threshold voltage	$T_j = 125 \text{ }^\circ\text{C}$	Max.	0.9	V
$R_D^{(1)}$	Dynamic resistance	$T_j = 125 \text{ }^\circ\text{C}$	Max.	200	m Ω
I_{DRM} I_{RRM}	$V_{OUT} = V_{DRM} / V_{RRM}$	$T_j = 25 \text{ }^\circ\text{C}$	Max.	10	μA
		$T_j = 125 \text{ }^\circ\text{C}$		500	

1. For both polarities of OUT pin referenced to COM pin

Table 5. Thermal resistances

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (AC)		3	$^\circ\text{C/W}$
$R_{th(j-a)}$	Junction to ambient	$S_{Cu}^{(1)} = 0.5 \text{ cm}^2$	70	$^\circ\text{C/W}$

1. S_{Cu} = copper surface under tab

Figure 2. Maximum power dissipation versus RMS on-state current (full cycle)

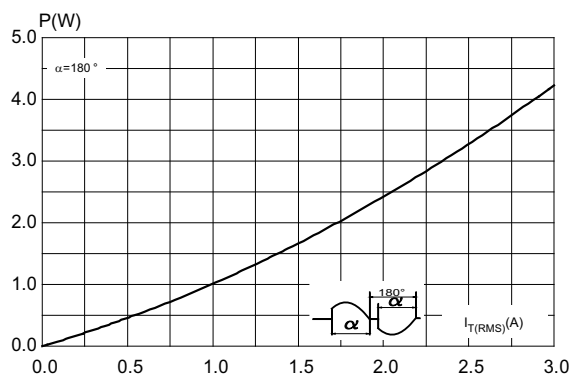


Figure 3. On-state RMS current versus case temperature

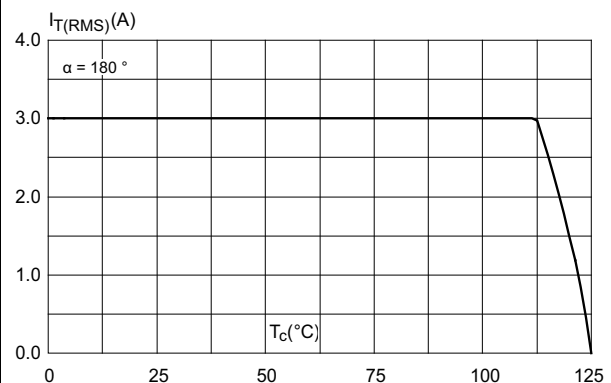


Figure 4. On-state RMS current versus ambient temperature (free air convection)

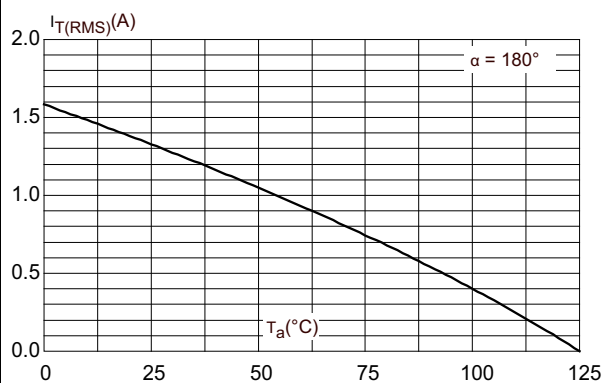


Figure 5. Relative variation of thermal impedance versus pulse duration

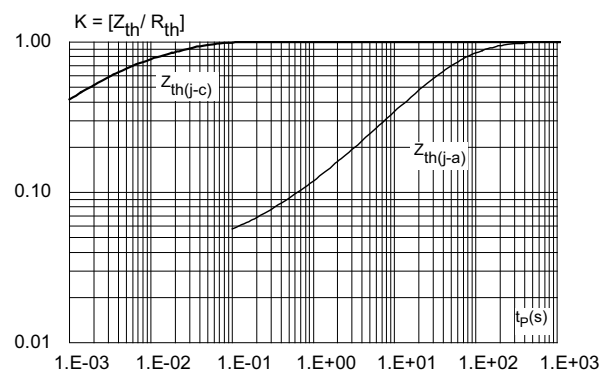


Figure 6. Non repetitive surge peak on-state current for a sinusoidal pulse with width: $t_p < 10ms$

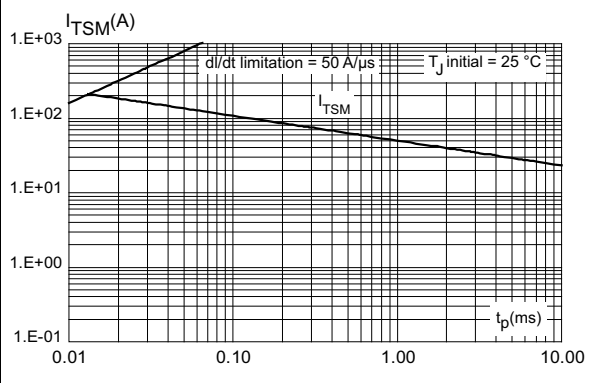


Figure 7. Surge peak on-state current versus number of cycles

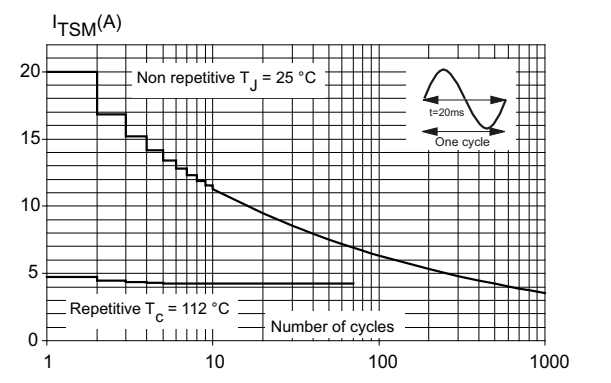


Figure 8. Relative variation of holding current and latching current versus junction temperature (typical values)

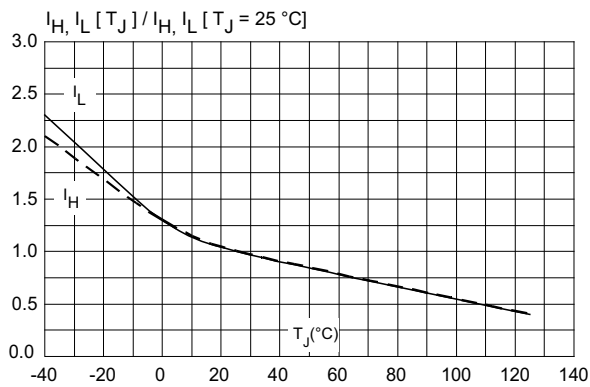


Figure 9. Relative variation of gate trigger current and gate trigger voltage versus junction temperature (typical values)

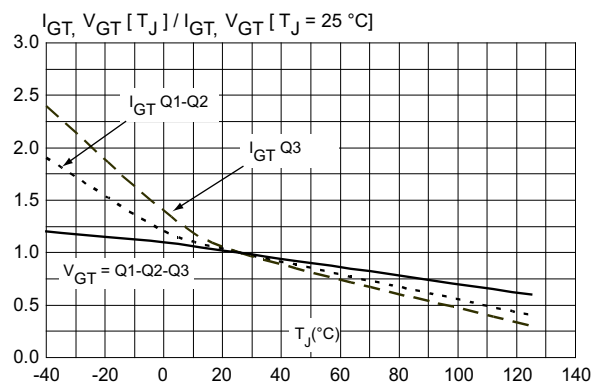


Figure 10. On-state characteristics (maximum values)

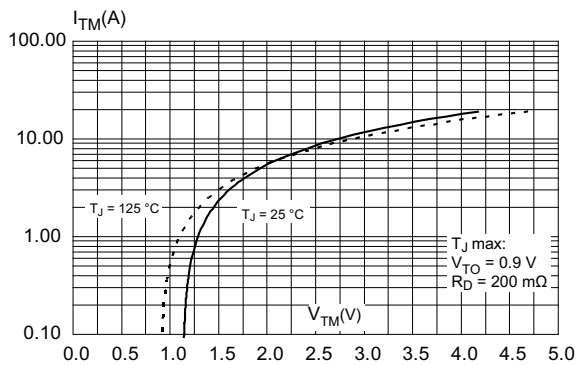


Figure 11. Relative variation of critical rate of decrease of main current versus junction temperature (typical values)

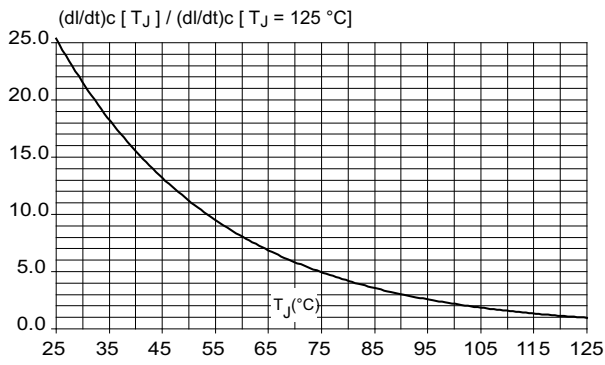


Figure 12. Relative variation of static dV/dt immunity versus junction temperature

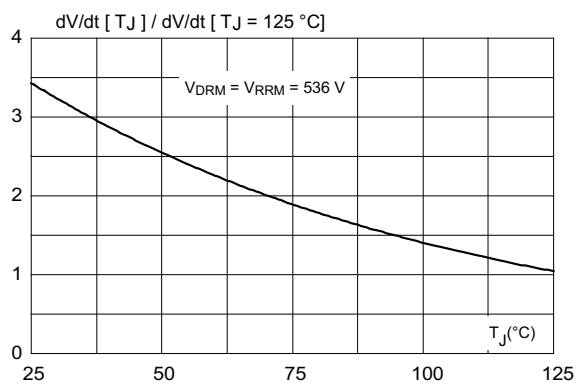


Figure 13. Relative variation of leakage current versus junction temperature (typical values)

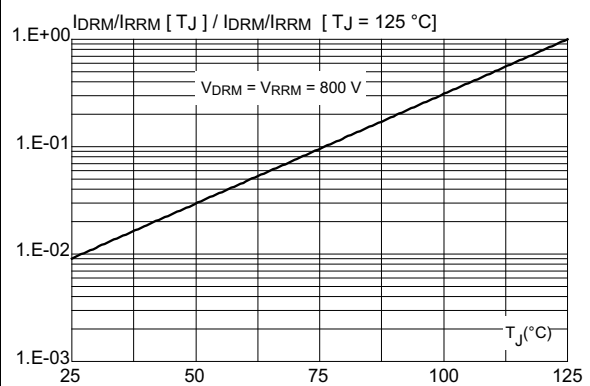


Figure 14. Relative variation of critical rate of decrease of main current versus reapplied (dV/dt) (typical value)

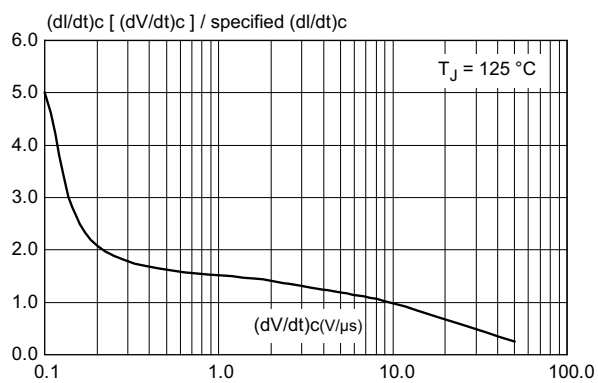
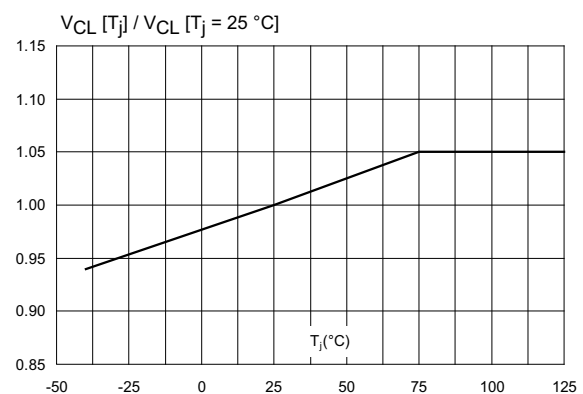


Figure 15. Relative variation of the maximal clamping voltage versus junction temperature (min. value)



2 Application information

2.1 Typical application description

The ACST310-8B device has been designed to switch on and off, or by phase angle control, highly inductive or resistive loads such as pump, valve, fan, or bulb lamps. Thanks to its high sensitivity ($I_{GT} \text{ max} = 10 \text{ mA}$), this device can be driven directly by logic level circuits through a resistor as shown on the typical application diagram ([Figure 16](#)).

Figure 16. Typical application schematic

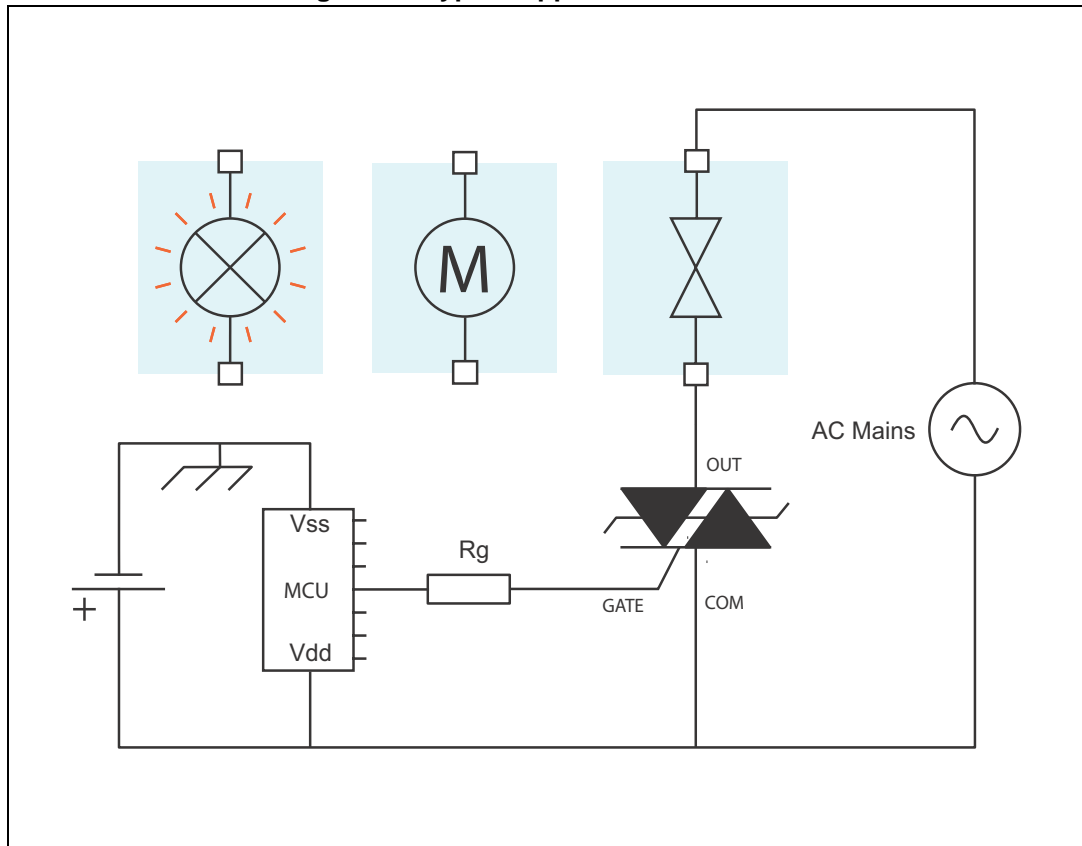
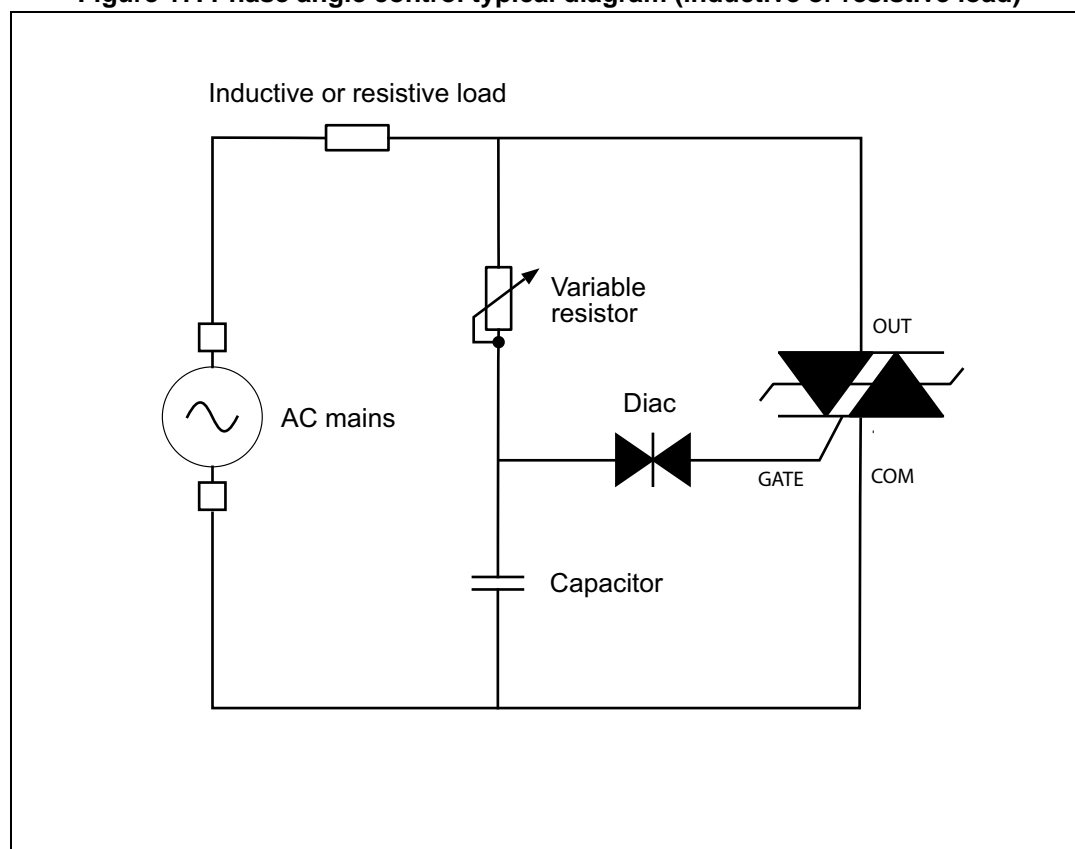


Figure 17. Phase angle control typical diagram (inductive or resistive load)

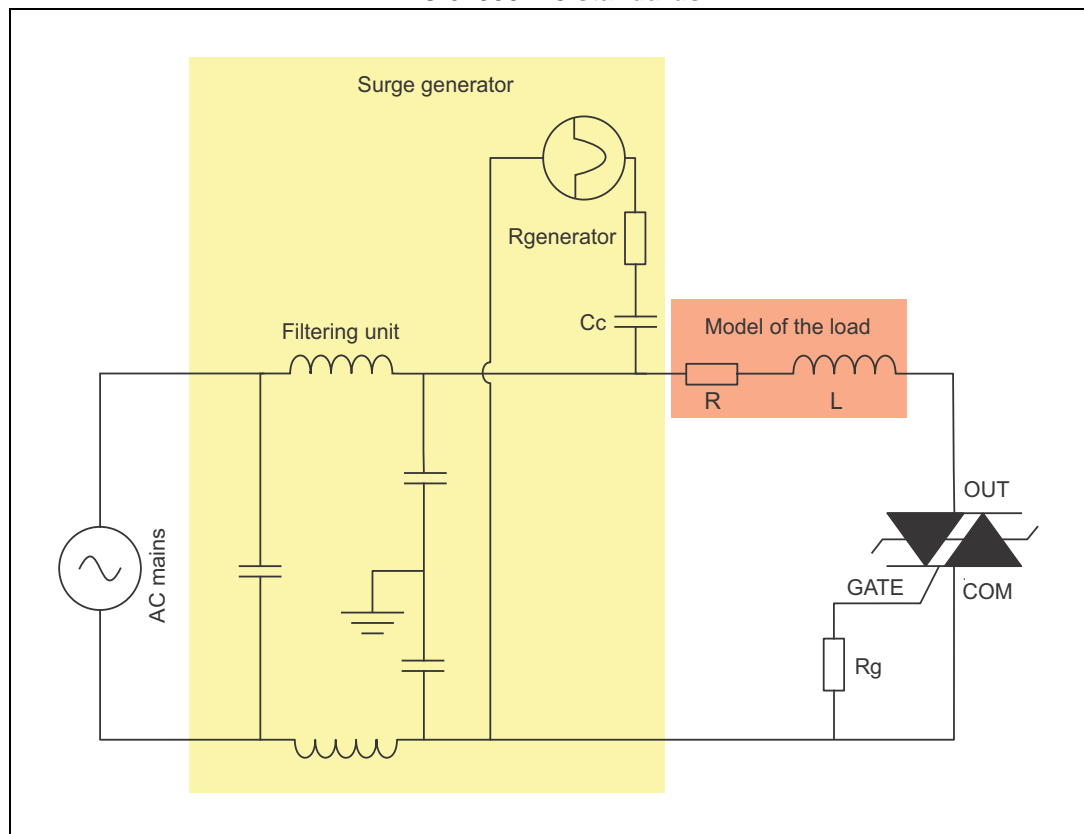


2.2 AC line transient voltage ruggedness

In comparison with standard Triacs, which are not robust against surge voltage, the ACST310-8B is self-protected against over-voltage, specified by the parameter V_{CL} . In addition, the ACST310-8B is a sensitive device (I_{GT} max. 10 mA), but provides a high noise immunity level against fast transients. The ACST310-8B switch can safely withstand AC line transient voltages either by clamping the low energy spikes, such as inductive spikes at switch off, or by switching to the on state (for less than 10 ms) to dissipate higher energy shocks through the load. This safety feature works even with high turn-on current ramp up.

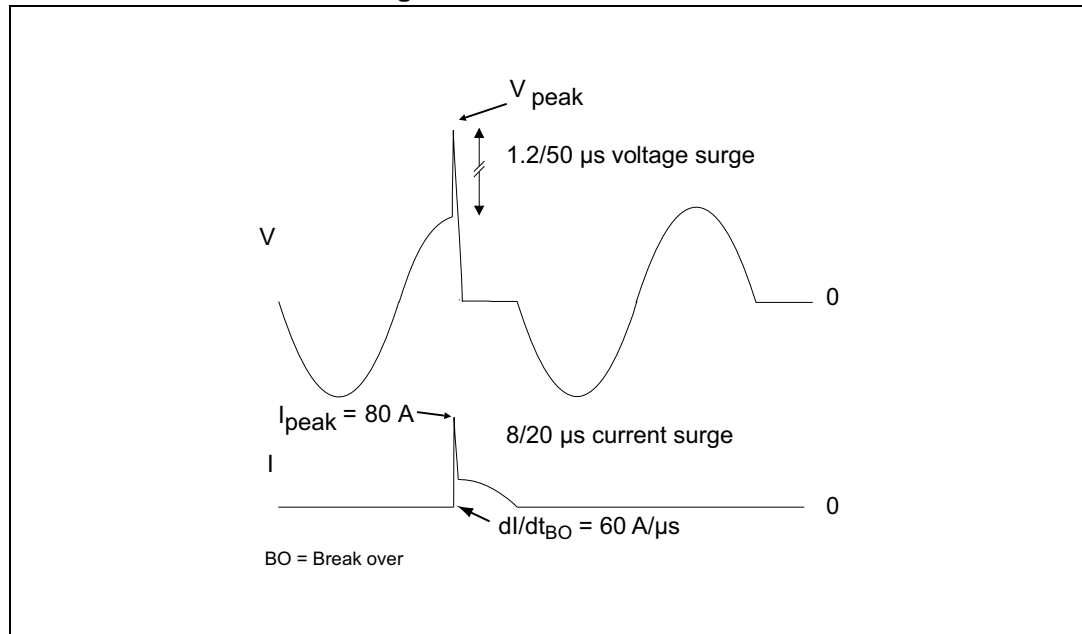
The test circuit of [Figure 18](#) represents the ACST310-8B application, and is used to stress the ACST310-8B switch according to the IEC 61000-4-5 standard conditions. With the additional effect of the load which is limiting the current, the ACST310-8B switch withstands the voltage spikes up to 2 kV on top of the peak line voltage. The protection is based on an overvoltage crowbar technology. The ACST310-8B folds back safely to the on state as shown in [Figure 19](#). The ACST310-8B recovers its blocking voltage capability after the surge and the next zero current crossing. Such a non-repetitive test can be done at least 10 times on each AC line voltage polarity.

Figure 18. Overvoltage ruggedness test circuit for resistive and inductive loads for IEC 61000-4-5 standards



1. $R = 30 \, \Omega$, $L = 10 \, \mu H$, $V_{pp} = 2 \, kV$ (Surge Generator), $R_g = 220 \, \Omega$, AC mains = $230 \, V_{RMS}$ 50 Hz

Figure 19. Typical voltage and current waveforms across the ACST310-8B during IEC 61000-4-5 standard test



2.3 Electrical noise immunity

The ACST310-8B is a sensitive device (I_{GT} max. 10 mA) and can be controlled directly through a simple resistor by a logic level circuit, and still provides a high electrical noise immunity. The intrinsic immunity of the ACST310-8B is shown by the specified dV/dt equal to 1000 V/ μs at 125 °C. This immunity level is 5 to 10 times higher than the immunity provided by an equivalent standard technology Triac with the same sensitivity. In other words, the ACST310-8B with $I_{GT} = 10$ mA has immunity comparable only for higher gate current device (I_{GT} higher than 35 mA).

3 Package information

- Epoxy meets UL94-V0
- Lead-free package
- Halogen free molding compound

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

3.1 DPAK package information

Figure 20. DPAK package outline

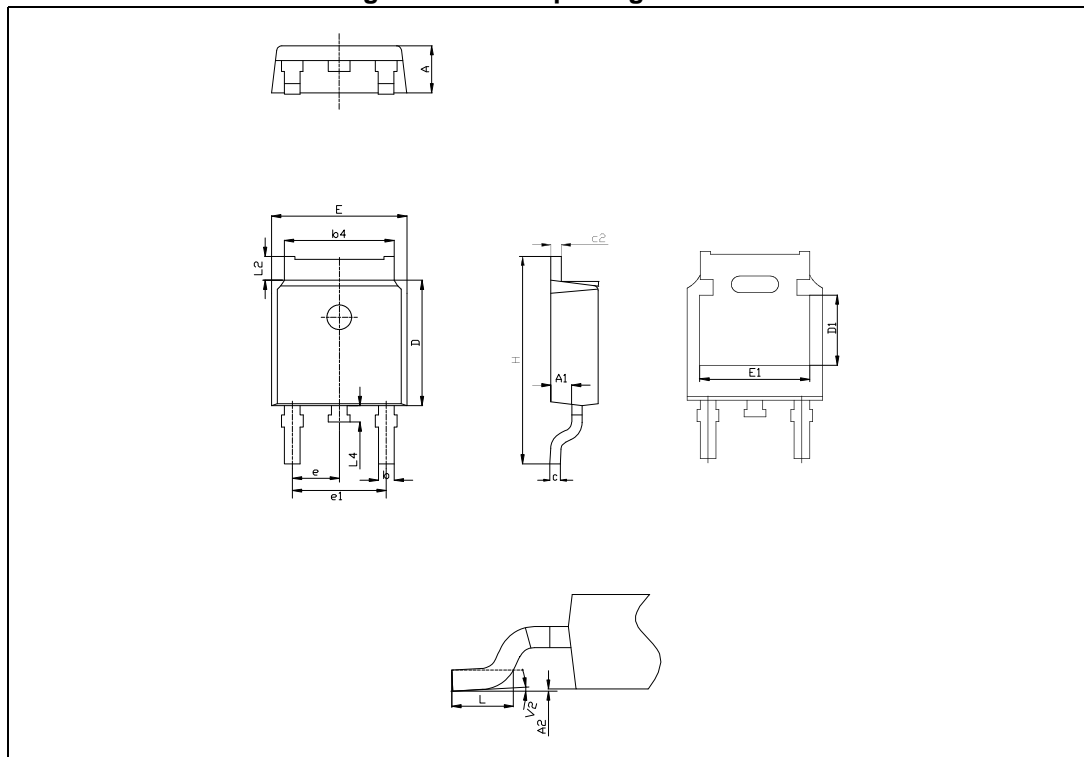
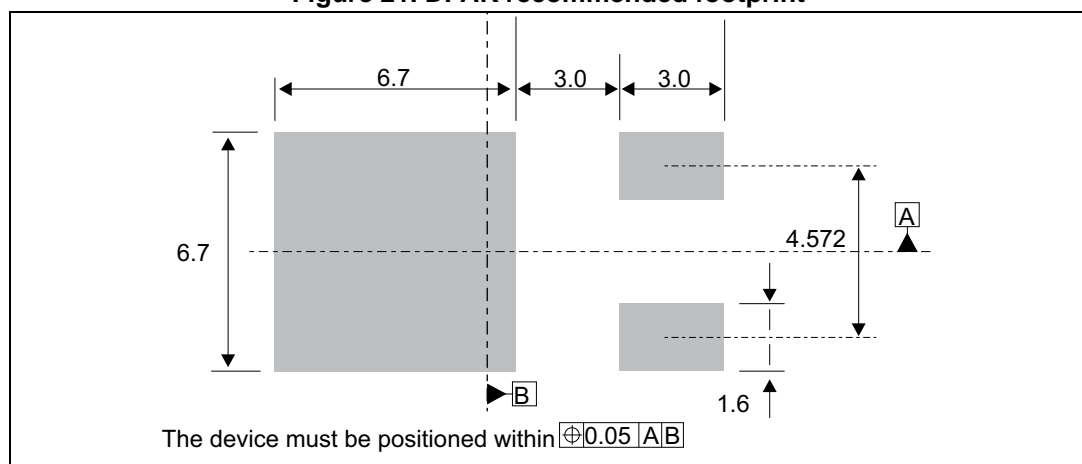


Table 6. DPAK package mechanical data

Ref.	Dimensions					
	Millimeters			Inches ⁽¹⁾		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		2.18	2.40		0.0858	0.0945
A1		0.90	1.10		0.0354	0.0433
A2		0.03	0.23		0.0012	0.0091
b		0.64	0.90		0.0252	0.0354
b4		4.95	5.46		0.1949	0.2150
c		0.46	0.61		0.0181	0.0240
c2		0.46	0.60		0.0181	0.0236
D		5.97	6.22		0.2350	0.2449
D1		4.95	5.60		0.1949	0.2205
E		6.35	6.73		0.2500	0.2650
E1		4.32	5.50		0.1701	0.2165
e	2.286			0.09		
e1		4.40	4.70		0.1732	0.1850
H		9.35	10.40		0.3681	0.4094
L		1.00	1.78		0.0394	0.0701
L2			1.27			0.0500
L4		0.60	1.02		0.0236	0.0402
V2		-8 °	+8 °		-8 °	+8 °

1. Inches only for reference

Figure 21. DPAK recommended footprint



4 Ordering information

Figure 22. Ordering information scheme

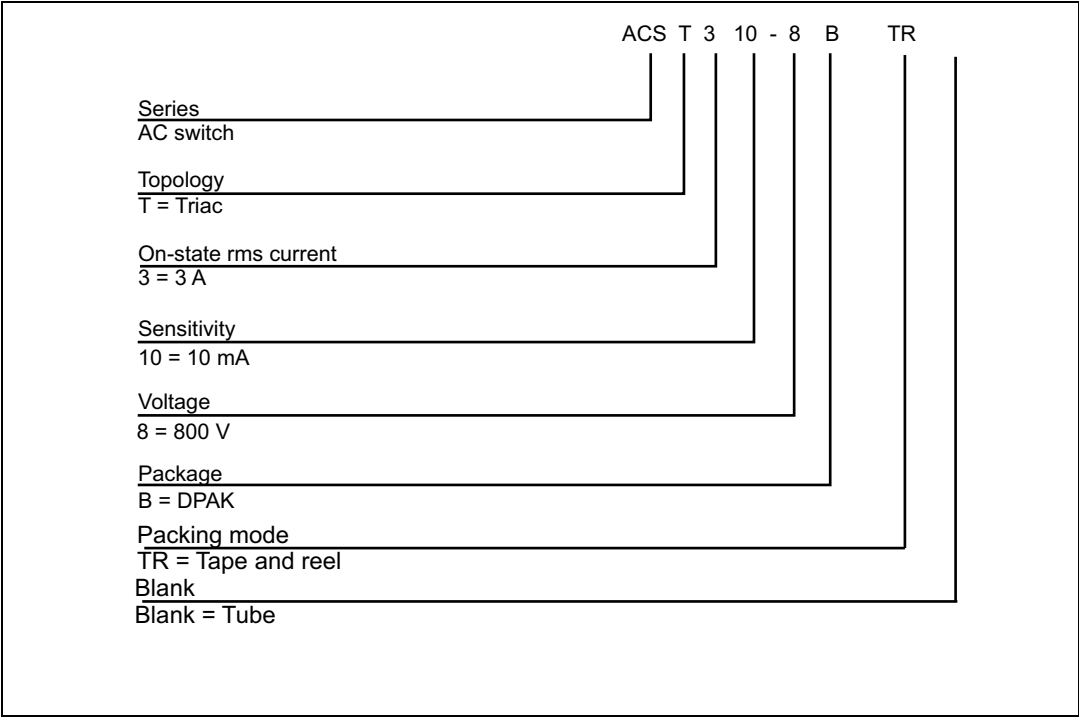


Table 7. Ordering information

Order code	Marking	Package	Weight	Base qty.	Packing mode
ACST310-8B	ACST 3108	DPAK	0.32 g per pc.	75	Tube
ACST310-8BTR				2500	Tape and reel

5 Revision history

Table 8. Document revision history

Date	Revision	Changes
24-Feb-2017	1	Initial release.

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