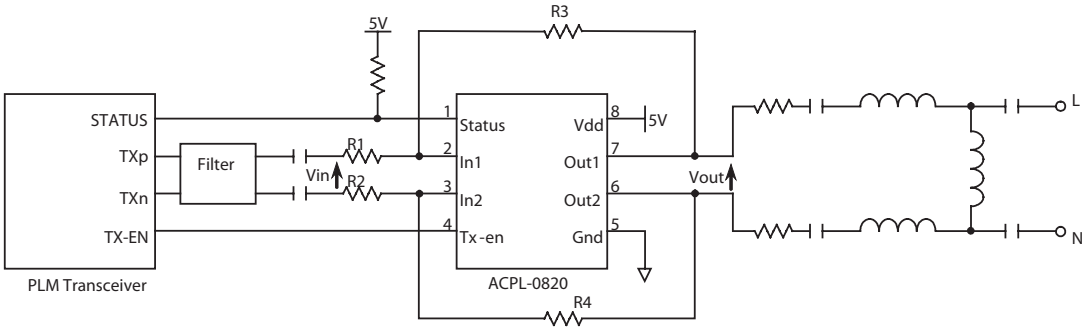
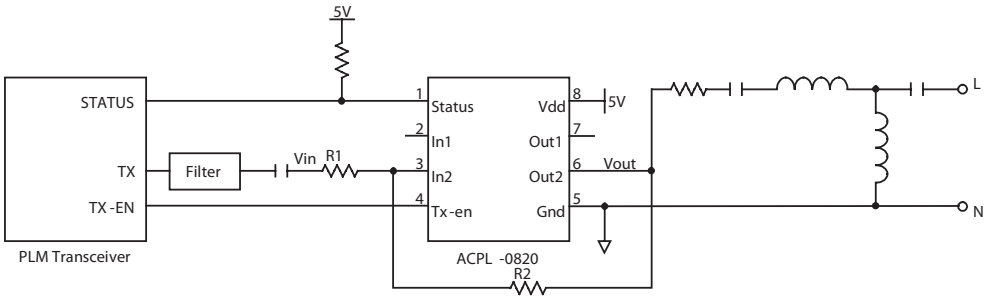
## Connection Diagrams

a) Differential to differential Connections



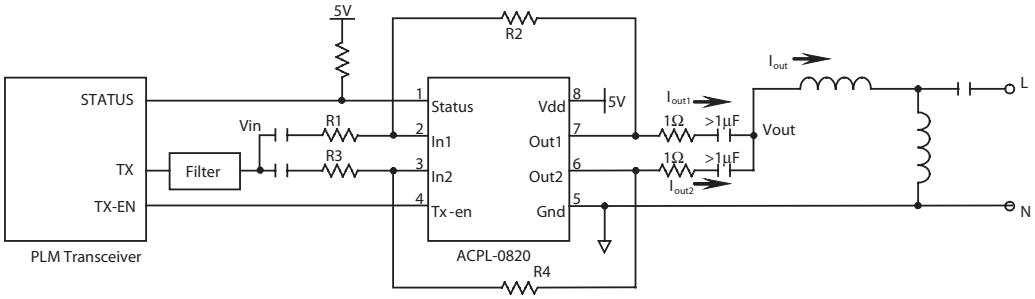

Gain of Amp1 = - R3/R1, Gain of Amp2 = - R4/R2, R1=R2, R3=R4, Overall Differential Output $V_{out} = (R3/R1) \cdot V_{in}$

b) Single-ended to single-ended Connections



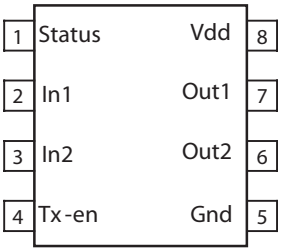

Gain of Amp2 = - R2/R1, Overall Output Voltage $V_{out} = - (R2/R1) \cdot V_{in}$

c) High Driving Capacity Connections of Dual Line Drivers




Gain of Amp1 = - R2/R1, Gain of Amp2 = - R4/R3, R1 = R3, R2 = R4, R5 = R6, Overall Output Voltage Vout ≈ - (R2/R1) . Vin, Iout = Iout1+Iout2

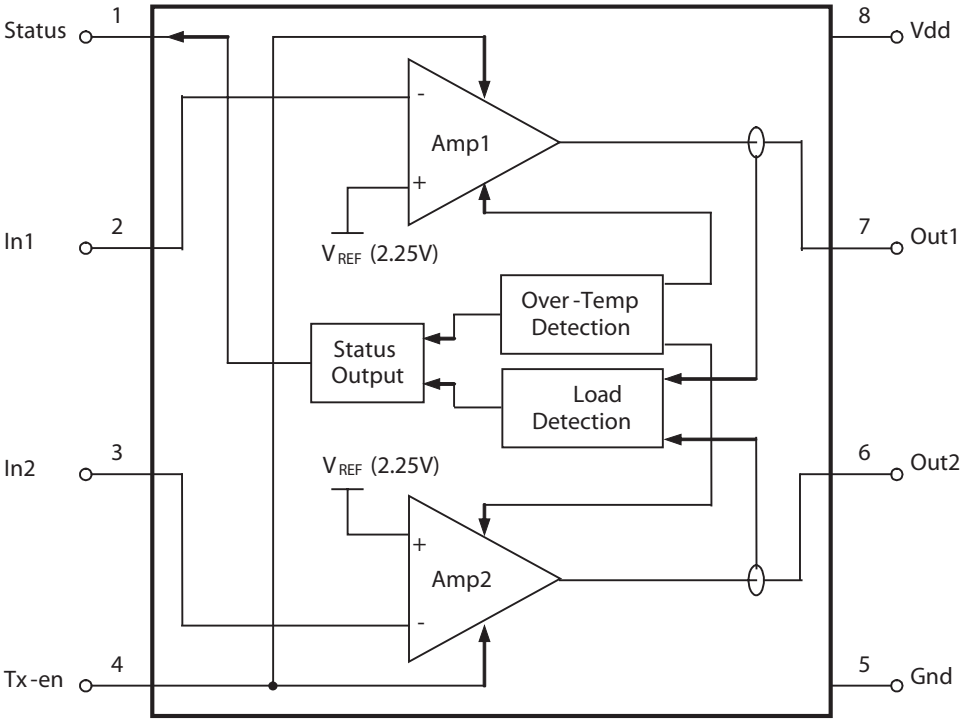
## Package Pin Out




## Pin Descriptions

| Pin No. | Symbol | Function | Description |
|---|---|---|---|
| 1 | Status | Line condition detection | A logic low indicates line conditions such as - load detection for $I_{out}$ < -0.25 A- over-temperature detection for $T_j$ =130°C (typ.) |
| 2 | In1 | Amp1 Input | Transmit signal input for 1st Line Driver |
| 3 | In2 | Amp2 Input | Transmit signal input for 2nd Line Driver |
| 4 | Tx-en | Transmit enable | A logic high enables both outputs (Out1 & Out2) of the dual line drivers;A logic low disables both outputs and setit to high impedance state (tri-state) |
| 5 | GND | Power supply ground | Power supply and signal ground |
| 6 | Out2 | Amp2 output | Transmit signal output for 2nd Line Driver |
| 7 | Out1 | Amp1 output | Transmit signal output for 1st Line Driver |
| 8 | $V_{DD}$ | 5 V power supply | 5 V DC power supply |

## Block Diagram



## Ordering Information

| Part number | Option RoHS Compliant | Packaging | Surface Mount | Tape & Reel | Quantity |
|---|---|---|---|---|---|
| ACPL-0820 | -000E | SO-8 | X | | 100 per tube |
| | -500E | SO-8 | X | X | 1500 per reel |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

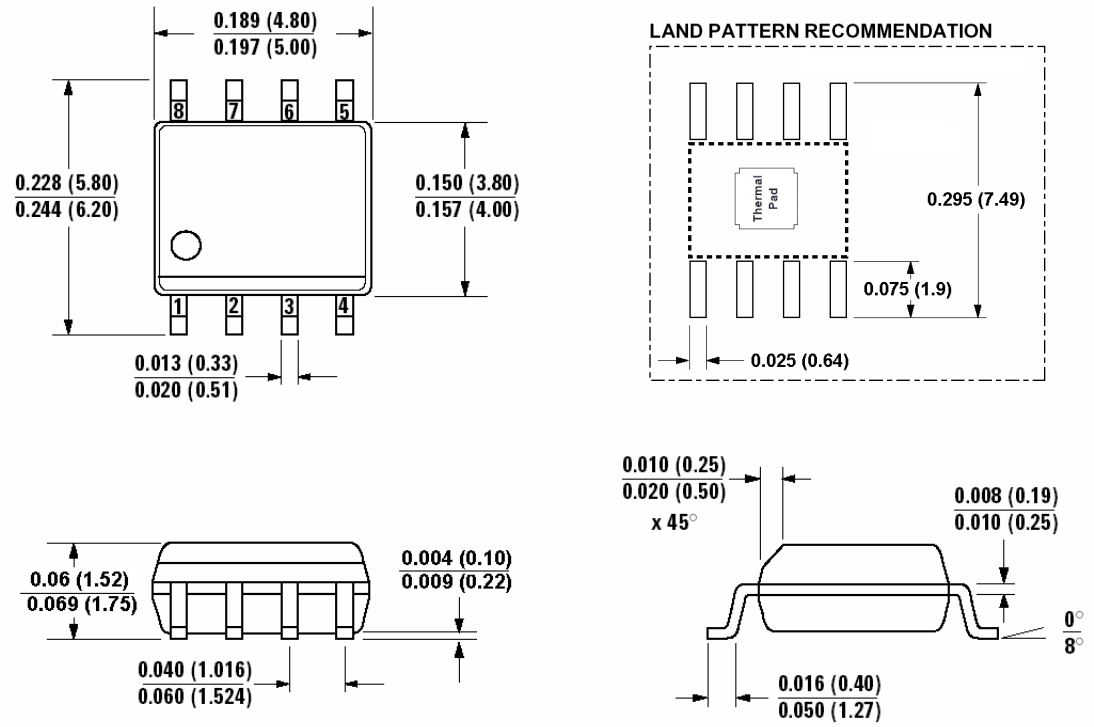
ACPL-0820-500E to order product of SO-8 package in Tape and Reel packaging and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

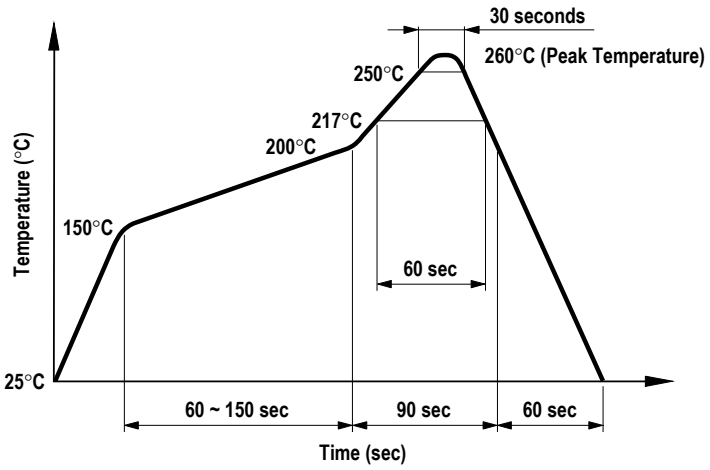
## Package Outline Drawings

### ACPL-0820 Small Outline SO-8 Package




DIMENSIONS IN INCHES AND (MILLIMETERS)

## Recommended Pb-free IR Profile




Note: Non-halide flux should be used.

1) One-time soldering reflow is recommended within the condition of temperature and time profile shown.
2) When using another soldering method such as infrared ray lamp, the temperature may rise partially in the mold of thedevice. Keep the temperature on the package of the device within the condition of (1) above.

## Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Storage Temperature | $T_S$ | -55 | 125 | °C |
| Ambient Operating Temperature | $T_A$ | -40 | 85 | °C |
| Junction Temperature | $T_J$ | | 150 | °C |
| Supply Voltage | $V_{DD}$ | -0.5 | 5.5 | Volts |
| Output Voltage | $V_O$ | -0.5 | $V_{DD}$ | Volts |
| Tx-in Voltage | $V_{IN1}$ or $V_{IN2}$ | -0.5 | $V_{DD}$ | Volts |
| Tx-en Voltage | $V_{Tx\text{-}en}$ | -0.5 | $V_{DD}$ | Volts |
| Solder Reflow Temperature Profile | (See **Solder Reflow Temperature Profile** Section) | | | |

## Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Ambient Operating Temperature | $T_A$ | -40 | 25 | 85 | °C |
| Supply Voltage | $V_{DD}$ | 4.75 | 5 | 5.25 | V |

## Electrical Specifications

Unless otherwise noted, for sinusoidal waveform input, all typical values are at $T_A$ = 25°C and $V_{DD}$ = 5 V; all Minimum/ Maximum specifications are at Recommended Operating Limits. (Note: $V_{In} = V_{In1} - V_{In2}$)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Condition | Fig. | Note |
|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ Supply Current | $I_{dd}$ | | 2.1 | 7.1 | mA | $V_{Tx\text{-}en}$ = 0V, $V_{Inp}$ (& $V_{Inn}$ )= 0$V_{PP}$, $I_{Out}$ ($I_{Out1}$ & $I_{Out2}$) no load | 1 | |
| | | | 30 | 40 | mA | $V_{Tx\text{-}en}$ = 5V, $V_{Inp}$ (& $V_{Inn}$ )= 0$V_{PP}$, $I_{Out}$ ($I_{Out1}$ & $I_{Out2}$) no load | 2,3 | |
| Junction Over-Temperature Detection Threshold | | | 130 | | °C | $V_{Tx\text{-}en}$ = 5V, $V_{Inp}$ (or $V_{Inn}$ )= 0$V_{PP}$,$I_{Out}$ ($I_{Out1}$ & $I_{Out2}$) no load | 12,14 | |
| Junction Over-Temperature Shutdown Threshold | | | 150 | | °C | $V_{Tx\text{-}en}$ = 5V, $V_{Inp}$ (or $V_{Inn}$ )= 1$V_{PP}$, $I_{Out}$ ($I_{Out1}$ & $I_{Out2}$) no load | 11,14 | 1 |
| Load Detection Threshold | | | 0.5 (Diff) | | App | $V_{Tx\text{-}en}$ = 5V, $V_{Inp}$ (& $V_{Inn}$ )= 1.25$V_{PP}$,f=132kHz, Gain = -2, $R_{L1}$ (&$R_{L2}$) = 2.5Ω | 10,13 | 2 |
| Status Logic High Output | $V_{Status\text{-}H}$ | $V_{DD}$-1 | | $V_{DD}$ | V | $V_{DD}$ = 3.5V, $I_{Status}$ = -2mA | | |
| Status Logic Low Output | $V_{Status\text{-}L}$ | 0 | | 0.8 | V | $V_{DD}$ = 5V, $I_{Status}$ = 2mA | | |
| Power SupplyRejection Ratio | PSRR | | 72 | | dB | 50Hz ripple, $V_{rippe}$ 200m$V_{PP}$, $V_{Tx\text{-}en}$ = 5V, $V_{Inp}$ (or $V_{Inn}$ )= 0$V_{PP}$, $I_{Out}$ ($I_{Out1}$ & $I_{Out2}$) no load | | |
| DC Bias Voltage | $V_{Bias}$ | | 2.25 | | V | $V_{Tx\text{-}en}$ = 5V, $I_{Out}$ ($I_{Out1}$ & $I_{Out2}$) no load | | |
| Output Impedance | $Z_O$ | | 12 | | kΩ | $V_{Tx\text{-}en}$ = 0V, $V_{Inp}$ (or $V_{Inn}$ )= 0$V_{PP}$, open loop, f =132kHz | | |
| | | | 0.5 | | Ω | $V_{Tx\text{-}en}$ = 5V, $V_{Inp}$ (or $V_{In2}$ )= 0$V_{PP}$, f =132kHz | | |
| Gain Bandwidth Product | GBW | 2 | 3 | | MHz | $V_{Tx\text{-}en}$ = 5V, $V_{In1}$ (or $V_{Inn}$)= 1$V_{PP}$, $R_{L1}$ (&$R_{L2}$) = 25Ω | 4, 14 | |
| Transmit Enable Threshold Voltage | $V_{th,(Tx\text{-}en)}$ | 0.8 | 1.6 | 2.4 | V | $V_{Inp}$ (or $V_{Inn}$ )= 1$V_{PP}$, f =132kHz, $I_{Out}$ ($I_{Out1}$ & $I_{Out2}$) no load | | |
| Tx Enable Time | τ | | 0.2 | 2 | µs | $V_{Tx\text{-}en}$ = 0->5V, $V_{Inp}$ = 1.25$V_{PP}$, $V_{Inn}$ = 3.25$V_{PP}$, f =132kHz, $R_{L1}$ (&$R_{L2}$) = 470Ω | 9, 15 | |
| Tx Disable Time | | | 0.9 | | µs | $V_{Tx\text{-}en}$ = 5->0V, $V_{Inp}$ = 1.25$V_{PP}$, $V_{Inn}$ = 3.25$V_{PP}$, f =132kHz, $R_{L1}$ (&$R_{L2}$) = 470Ω | 9, 15 | |
| 2nd Harmonic Distortion | HD2 | | -69 | -60 | dB | $V_{Tx\text{-}en}$ = 5V, $V_{Out1}$ (& $V_{Out2}$)= 3.5$V_{PP}$, Gain = -2, $R_L$ = 50Ω$T_A$=25°C | 5-8, 16 | 3 |
| 3rd Harmonic Distortion | HD3 | | -74 | -65 | dB | | | 3 |
| Output Current | $I_O$ | | 1.5 | | App | $V_{Tx\text{-}en}$ = 5V, f= 132kHz | | 4 |
| Thermal Resistance | $\theta_{JA}$ | | 110 | | °C/W | 1oz. copper trace, 2-layer PCB, still air, $T_A$=25°C | | |
| | | | 40 | | °C/W | 1oz. copper trace, 4-layer PCB, still air, $T_A$=25°C | | |
| 2nd Harmonic Distortion (1App Load) | HD2 | | -55 | | dB | $V_{Tx\text{-}en}$ = 5V, $V_{Out1}$ (& $V_{Out2}$)= 3.5$V_{PP}$, f =132kHz, Gain = -2, $R_L$ = 7Ω, $T_A$=25°C | | 3 |
| 3rd Harmonic Distortion (1App Load) | HD3 | | -65 | | dB | | | 3 |

Notes:

1. Threshold of rising junction temperature with hysteresis of 20°C (typ.).
2. See Application Information section for more information on the load detection feature.
3 Values obtained at differential mode connections.
4. Transmit duty ratio to be limited to 0.5 maximum.

## Performance Plots

Unless otherwise noted, all typical plots are at $T_A$ = 25°C, $V_{DD}$ = 5 V, sinusoidal waveform input.
(Note: $A_{OL}$=$A_{OL1}$ or $A_{OL2}$)

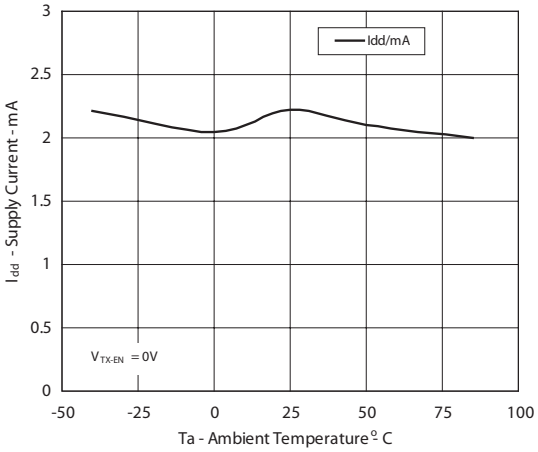



**Figure 1. Supply Current vs Temperature for Tx disabled.**

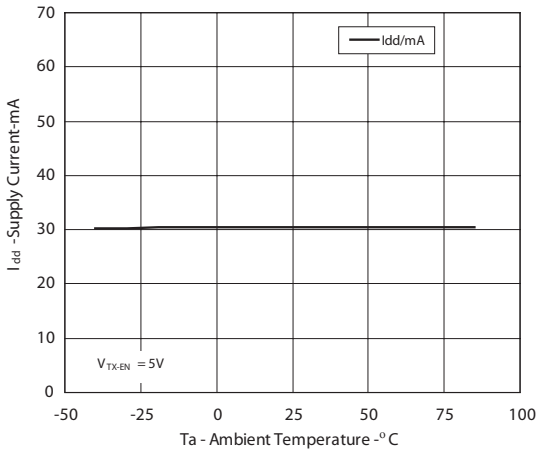



**Figure 2. Supply Current vs Temperature for Tx enabled.**

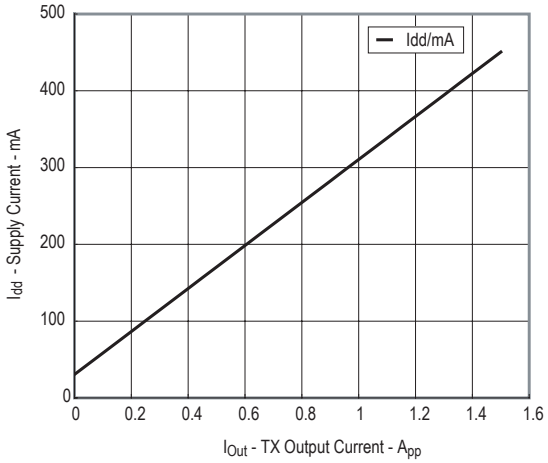



**Figure 3. Supply Current vs Output Current.**

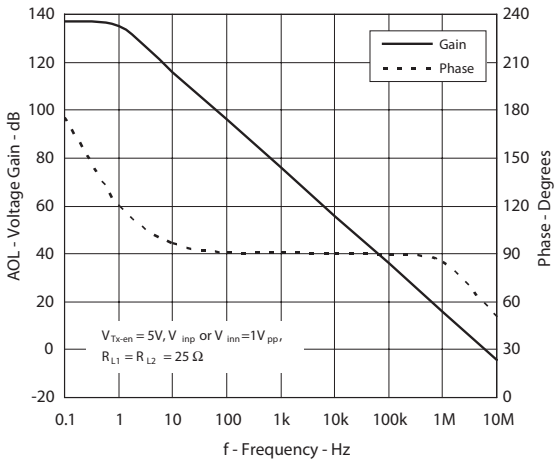



**Figure 4. Gain and phase vs. frequency.**

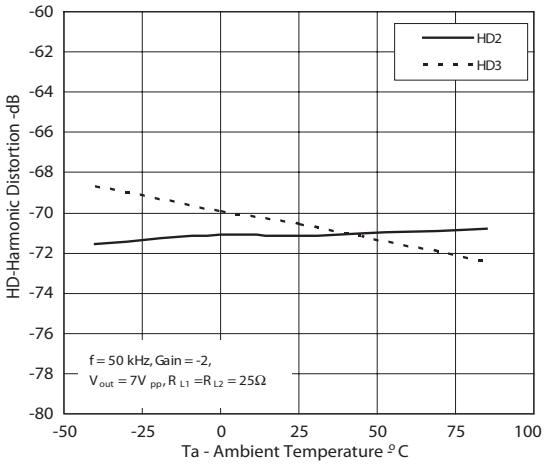



**Figure 5. Output harmonic distortion vs. temperature for f = 50 kHz.**

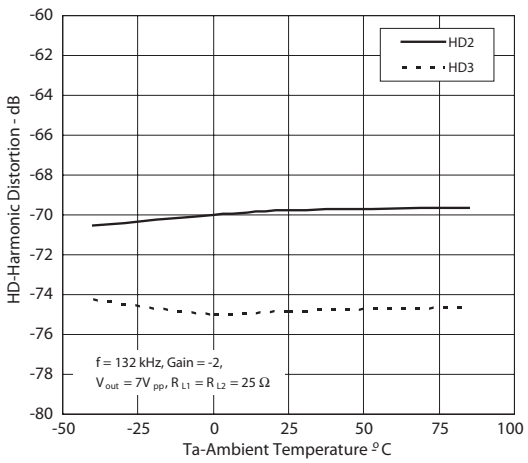



**Figure 6. Output harmonic distortion vs. temperature for f = 132 kHz.**

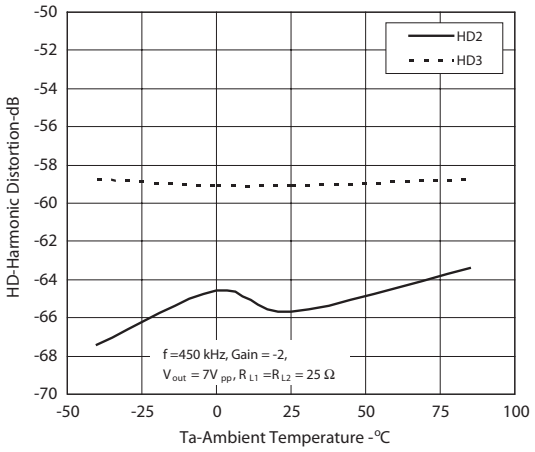



**Figure 7. Output Harmonics Distortion Vs temperature for f=450kHz.**

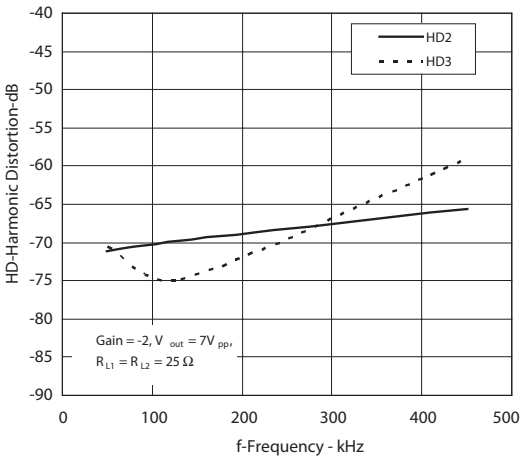



**Figure 8. Output harmonic distortion vs. Frequency.**

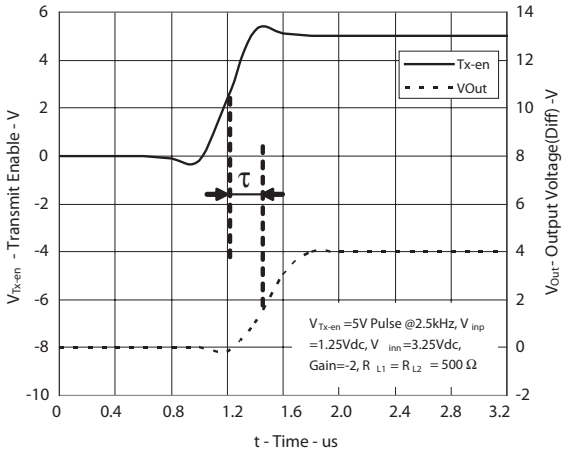



**Figure 9. Tx enable time.**

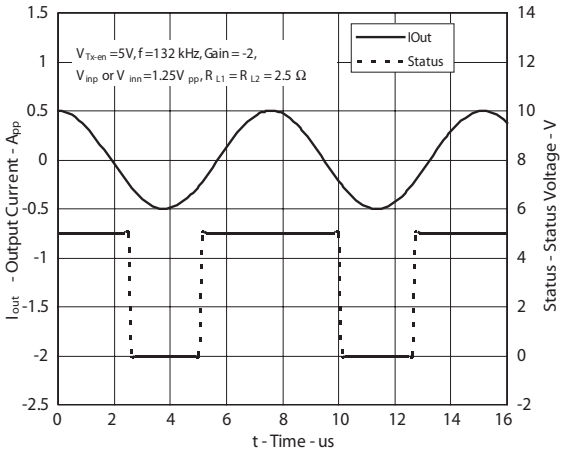



**Figure 10. Output load detection.**

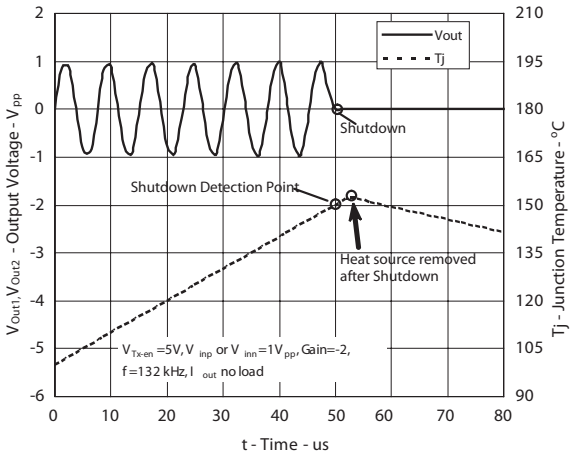



**Figure 11. Out1 or Out2 Thermal Characteristics.**

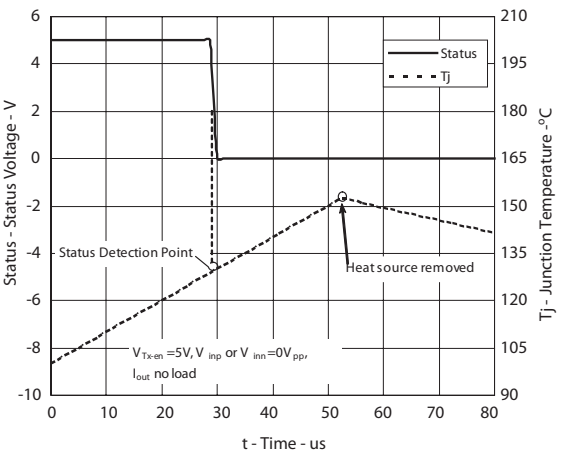



**Figure 12. Status O/P Thermal Characteristics.**

## Test Circuit Diagrams

Unless otherwise noted, all test circuits are at $T_A$ = 25°C, $V_{DD}$ = 5 V, sinusoidal waveform input, and signal frequency f = 132 kHz.

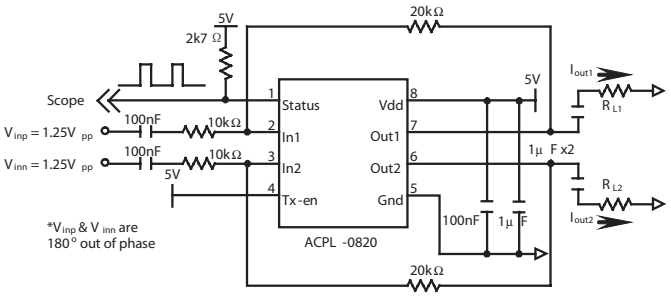



**Figure 13. Load detection test circuit.**

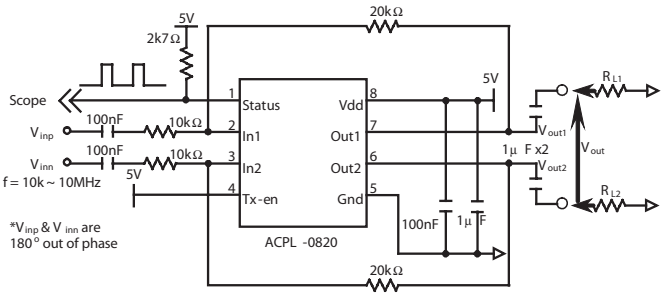



**Figure 14. Gain bandwidth product & Over Temp test circuit.**

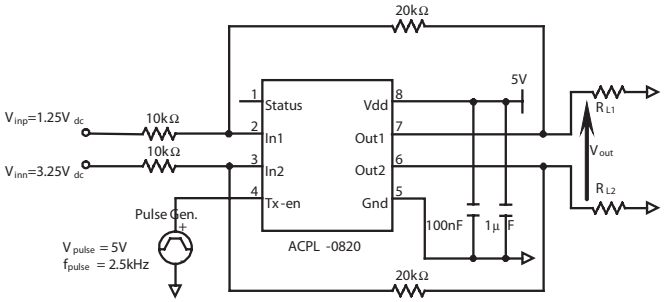



**Figure 15. Tx enable/disable time test circuit.**

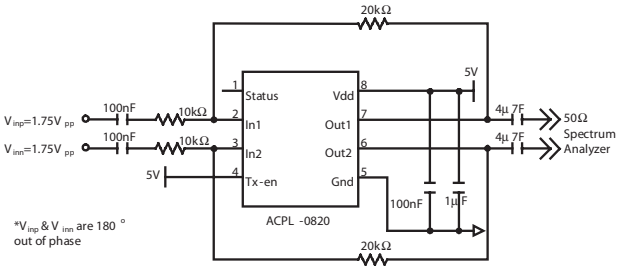



**Figure 16. Tx-out harmonic distortion test circuit.**

## Application Information

ACPL-0820 is designed to work with various transceivers and can be used with a variety of modulation methods including ASK, FSK and BPSK. Figure 17 shows a typical transformer isolated line driving application in a powerline modem using Frequency Shift Keying (FSK) modulation scheme.

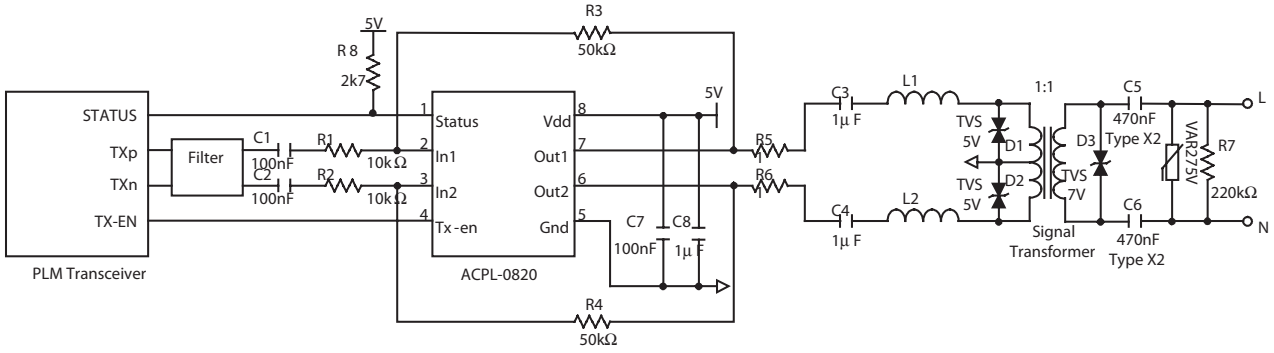



**Figure 17. Schematic of Isolated ACPL-0820 application for FSK modulation scheme.**

## Line Driver

The dual line drivers combined is capable of driving powerline load impedances with output signals up to 7 VPP. The biasing point of the line driver is controlled internally. The biasing point set enables optimum modulation frequencies up to 150 kHz.

The outputs of the line drivers are coupled onto the powerline using a simple differential mode LC coupling circuit as shown in Figure 18. Refer to Table 1 for some typical component values. Capacitors C5 & C6 and inductor L3 attenuate the 50/60 Hz powerline transmission frequency. A suitable value for L3 can range in value from 200 µH to 1 mH. To reduce the series coupling impedance at the modulation frequency, L1 & L2 are included to compensate for the reactive impedance of C3 & C4. These inductors should be of a low resistance type capable of meeting the peak current requirements. To meet safety regulatory requirements, capacitors C5 & C6 need to be of X2 safety rated. Since these types of capacitors typically have a very wide tolerance range of 20%, it is recommended to use as low a Q factor as possible for the L1/C3 & L2/C4 combinations.

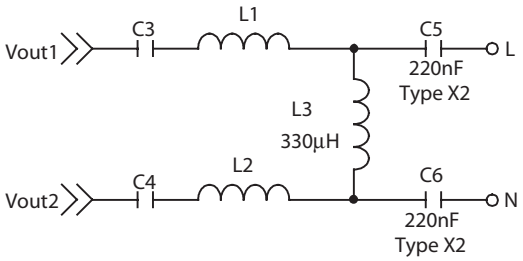



**Figure 18. LC coupling network.**

**Table 1. Typical component values for LC coupling network.**

| | LC Coupling | |
|---|---|---|
| **Carrier Frequency** (kHz) | **L1 (or L2) (µH)** | **C3 (or C4) (nF)** |
| 110 | 15 | 150 |
| 120 | 10 | 220 |
| 132 | 6.8 | 220 |
| 150 | 6.8 | 220 |

Although the series coupling impedance is minimized to reduce insertion loss, it has to be sufficiently large to limit the peak current to the desired level in the worst expected powerline load condition. The peak output current is effectively limited by the total series coupling resistance, which is made up of the series resistance of L1 & L2, the series resistance of the fuse and any other resistive elements connected in the coupling network.

To reduce power dissipation when not operating in transmit mode the line driver stage is shut down to a low power high impedance state (or tri-state) by pulling the Tx-en input (pin 4) to a logic low state.

## External Transient Voltage Protection

To protect ACPL-0820 against high voltage transients caused by voltage surges and disconnecting/connecting the modem, it is necessary to add external bi-directional transient voltage protectors such as D1, D2 (both 5V rated) & D3 (7V rated) as shown in Figure 17 in the circuit. But care must be taken to ensure that the total output capacitance as seen by each output is not more than 1nF to prevent oscillations.

Another mandatory protection against AC power surges from the mains can be achieved by adding an appropriate Metal Oxide Varistor (MOV) across the powerline terminals after the fuse.

## Internal Protection and Sensing

ACPL-0820 includes 2 sensing and protection features to ensure robust operation under wide ranging environmental conditions.

The 1st protection features is the over-temperature shutdown. This particular feature protects the line driver stage from over-temperature stress. Should the IC junction temperature reach a level above 150°C, the line driver circuit will be shut down and the output of Status (pin 1) is pulled to the logic low state simultaneously.

The 2nd feature is load detection sensing feature. The powerline impedance is quite unpredictable and varies not just at different connection points but is also time variant. ACPL-0820 includes this current sensing feature, which may be utilized to feedback information on the instantaneous powerline load conditions. Should the output current reaches a level greater than 0.5 App, the status pin output is pulled to a logic low state for the entire duration when the peak current is exceeding -0.25 A, as shown in Figure 10. Using the period of the pulse together with the known coupling impedance, the actual powerline load can be calculated. Table 2 shows the logic output of the Status pin.

**Table 2. Status pin logic output.**

| | **Normal** | **Over-Temperature** | **I < -0.25 A** |
|---|---|---|---|
| Status output | High | Low | Low (pulsed) |