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1 Block diagram and pin configuration

Figure 1. Block diagram

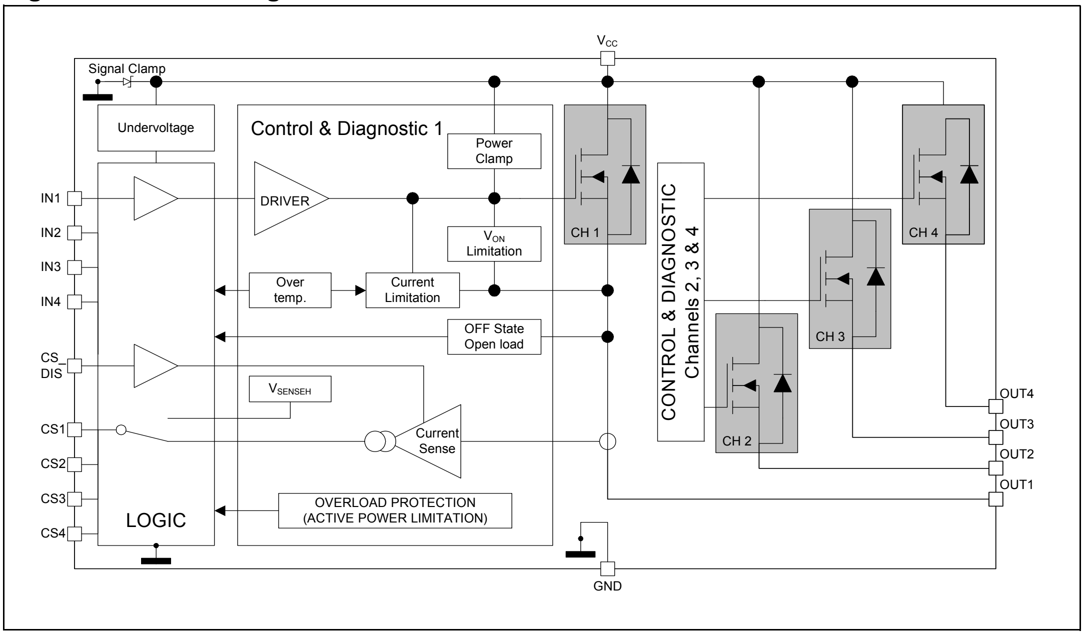


Table 1. Pin functions

Name	Function
V_{CC}	Battery connection.
$OUTPUT_n$	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
$INPUT_n$	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CURRENT $SENSE_n$	Analog current sense pin, delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

Figure 2. Configuration diagram (top view)

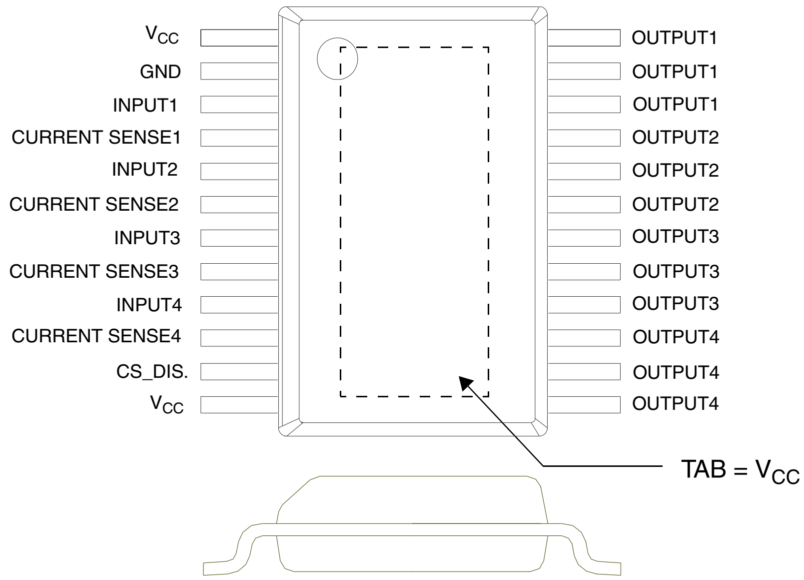
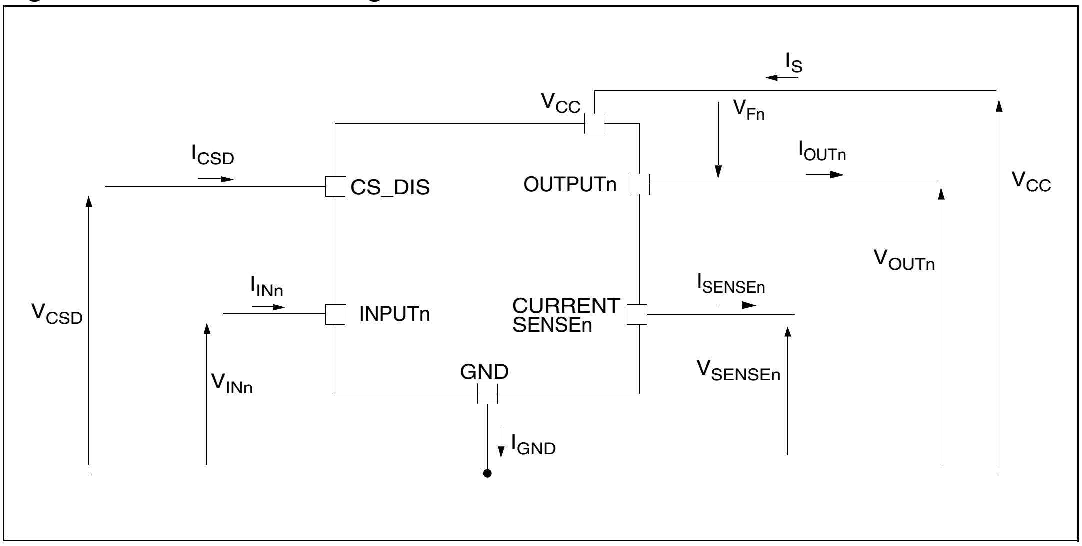


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1 kΩ resistor	X	Through 22 kΩ resistor	Through 10 kΩ resistor	Through 10 kΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: *$V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.*

2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the “Absolute maximum ratings” tables may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	20	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC} - 41 to +V_{CC}	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy (single pulse) (L = 3 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; $I_{OUT} = I_{limL}$(Typ.))	104	mJ
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 KΩ; C = 100 pF) – Input – Current sense – CS_DIS – Output – V_{CC}	 4000 2000 4000 5000 5000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj-case}$	Thermal resistance junction-case (with one channel ON)	2.8	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	See *Figure 36*	°C/W

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 28 V, -40 °C < T_j < 150 °C, unless otherwise stated.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown		2.5	3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance(1)	I_{OUT} = 2 A; T_j = 25 °C			50	mΩ
		I_{OUT} = 2 A; T_j = 150 °C			100	
		I_{OUT} = 2 A; V_{CC} = 5 V; T_j = 25 °C			65	
V_{clamp}	Clamp voltage	I_S = 20 mA	41	46	52	V

Table 5. Power section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Supply current	Off-state; V_{CC} = 13 V; T_j = 25 °C; V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0 V		2[(2)]	5[(2)]	µA
		On-state; V_{CC} = 13 V; V_{IN} = 5 V; I_{OUT} = 0 A		8	14	mA
$I_{L(off)}$	Off-state output current [(1)]	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25 °C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125 °C	0		5	
V_F	Output - V_{CC} diode voltage[(1)]	$-I_{OUT}$ = 2 A; T_j = 150 °C			0.7	V

1. For each channel
2. PowerMOS leakage included.

Table 6. Switching (V_{CC} = 13 V; T_j = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 6.5 Ω (see *Figure 6.*)		20		µs
$t_{d(off)}$	Turn-off delay time	R_L = 6.5 Ω (see *Figure 6.*)		35		µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L = 6.5 Ω		See *Figure 26*		V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L = 6.5 Ω		See *Figure 28*		V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 6.5 Ω (see *Figure 6.*)		0.15		mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 6.5 Ω (see *Figure 6.*)		0.25		mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	V_{CSD} = 0.9 V	1			µA
V_{CSDH}	CS_DIS high level voltage		2.1			V

Table 7. Logic inputs (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CSDH}	High level CS_DIS current	V_{CSD} = 2.1 V			10	µA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	I_{CSD} = 1 mA	5.5		7	V
		I_{CSD} = -1 mA		-0.7		

Table 8. Protections and diagnostics [(1)]

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC} = 13 V	19	27	38	A
		5 V < V_{CC} < 28 V			38	A
I_{limL}	Short circuit current during thermal cycling	V_{CC} = 13 V; $T_R < T_j < T_{TSD}$		7		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; V_{IN} = 0; L = 6 mH	V_{CC}-41	V_{CC}-46	V_{CC}-52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.1 A; T_j = -40 °C...150 °C (see *Figure 8*)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.05 A; V_{SENSE} = 0.5 V; V_{CSD} = 0 V; T_j = -40 °C...150 °C	1050	2110	3170	
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 1 A; V_{SENSE} = 4V; V_{CSD} = 0 V; T_j = -40 °C...150 °C	1510	1890	2650	
		T_j = 25 °C...150 °C	1510	1890	2270	
dK_1/K_1 [(1)]	Current sense ratio drift	I_{OUT} = 1 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; T_j = -40 °C to 150 °C	-13		13	%

Table 9. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 2 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; T_j = -40 °C...150 °C T_j = 25 °C...150 °C	 1600 1600	 1800 1800	 2230 2000	
dK_2/K_2(1)	Current sense ratio drift	I_{OUT} = 2 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; T_j = -40 °C to 150 °C	-8		8	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 4 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; T_j = -40 °C...150 °C T_j = 25 °C...150 °C	 1620 1620	 1770 1770	 1990 1920	
dK_3/K_3(1)	Current sense ratio drift	I_{OUT} = 4 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; T_j = -40 °C to 150 °C	-6		6	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 0 V; T_j = -40 °C...150 °C	0		1	µA
		I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{CSD} = 0 V; V_{IN} = 5 V; T_j = -40 °C...150 °C	0		2	
		I_{OUT} = 2 A; V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 5 V; T_j = -40 °C...150 °C	0		1	
I_{OL}	Open-load on-state current detection threshold	V_{IN} = 5 V; 8 V < V_{CC} < 18 V; I_{SENSE} = 5 µA	4		20	mA
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 4 A; V_{CSD} = 0 V	5			V
V_{SENSEH}	Analog sense output voltage in fault condition(2)	V_{CC} = 13 V; R_{SENSE} = 10 KΩ		8		V
I_{SENSEH}	Analog sense output current in fault condition(2)	V_{CC} = 13 V; V_{SENSE} = 5 V		9		mA
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	V_{SENSE} < 4 V, 0.5 A < I_{OUT} < 4 A I_{SENSE} = 90 % of $I_{SENSEMAX}$ (see *Figure 4*)		40	100	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS_DIS pin	V_{SENSE} < 4 V; 0.5 A < I_{OUT} < 4 A I_{SENSE} = 10 % of $I_{SENSEMAX}$ (see *Figure 4*)		5	20	µs
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE} < 4 V, 0.5 A < I_{OUT} < 4 A I_{SENSE} = 90 % of $I_{SENSEMAX}$ (see *Figure 4*)		80	250	µs

Table 9. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4 V, I_{SENSE} = 90 % of $I_{SENSEMAX}$, I_{OUT} = 90 % of I_{OUTMAX} I_{OUTMAX} = 2 A (see *Figure 7*)			60	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE} < 4 V, 0.5 A < I_{OUT} < 4 A I_{SENSE} = 10 % of $I_{SENSEMAX}$ (see *Figure 4*)		80	250	µs

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation, overtemperature and open-load off-state detection.

Table 10. Open-load detection (8V<V_{CC}<18V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load off-state voltage detection threshold	V_{IN} = 0 V	2	See *Figure 5*	4	V
t_{DSTKON}	Output short circuit to V_{cc} detection delay at turn-off	See *Figure 5*	180		1200	µs
$I_{L(off2)r}$	Off-state output current at V_{OUT} = 4 V	V_{IN} = 0 V; V_{SENSE} = 0 V; V_{OUT} rising from 0 V to 4 V	-120		0	µA
$I_{L(off2)f}$	Off-state output current at V_{OUT} = 2 V	V_{IN} = 0 V; V_{SENSE} = V_{SENSEH} V_{OUT} falling from V_{CC} to 2 V	-50		90	µA
td_vol	Delay response from output rising edge to V_{SENSE} rising edge in open-load	V_{OUT} = 4 V; V_{IN} = 0 V V_{SENSE} = 90 % of V_{SENSEH}			20	µs

Figure 4. Current sense delay characteristics

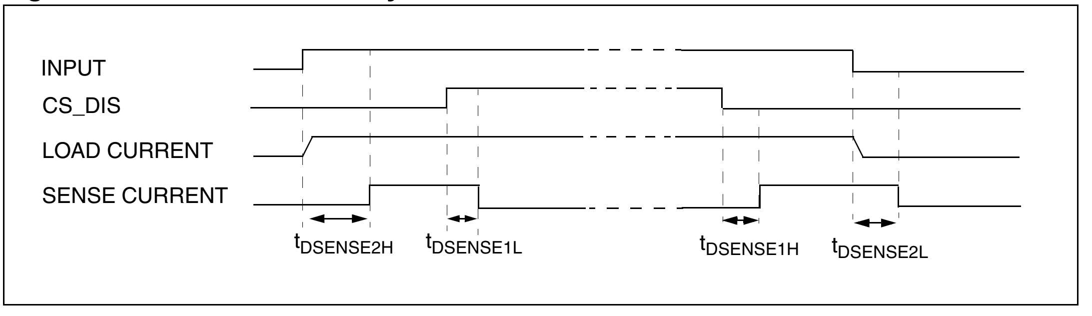


Figure 5. Open-load off-state delay timing

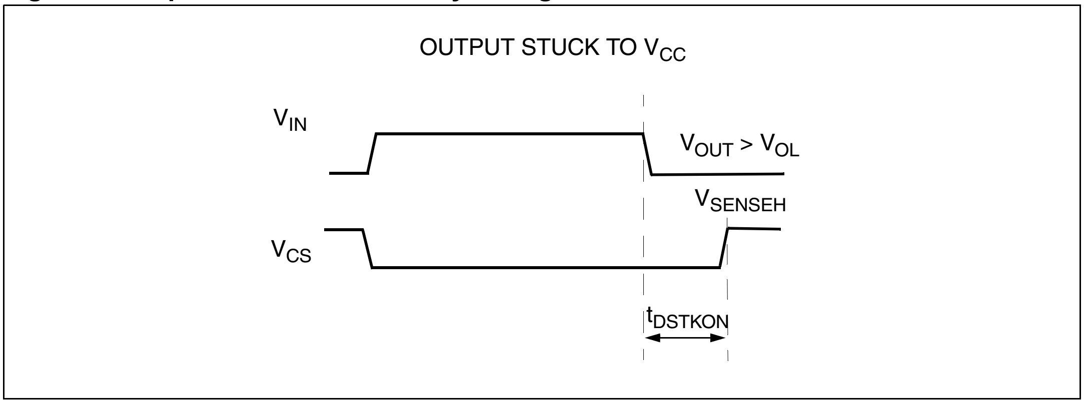


Figure 6. Switching characteristics

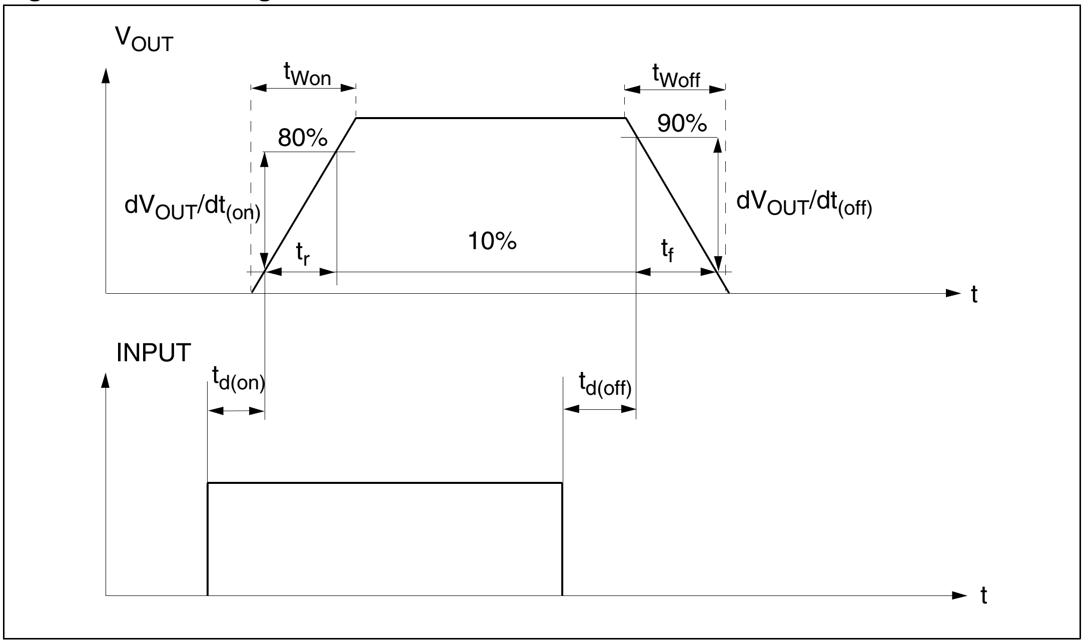


Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

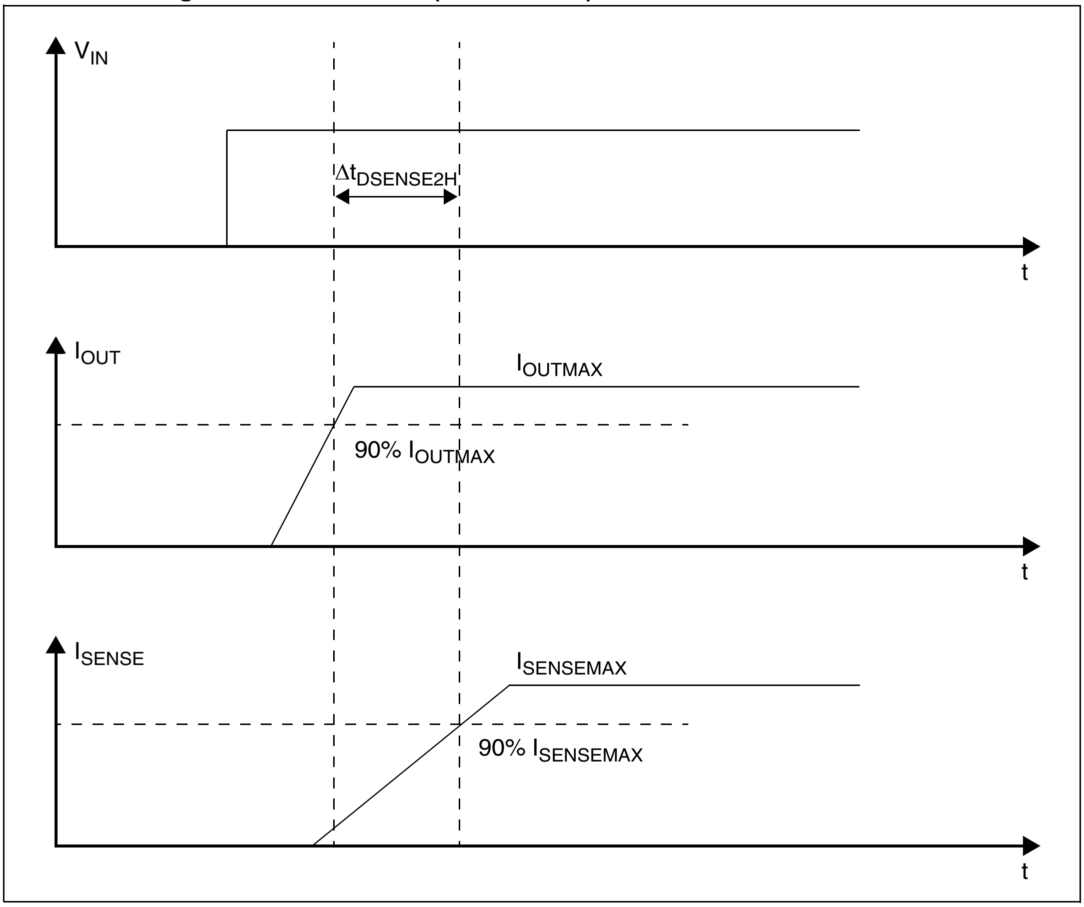


Figure 8. Output voltage drop limitation

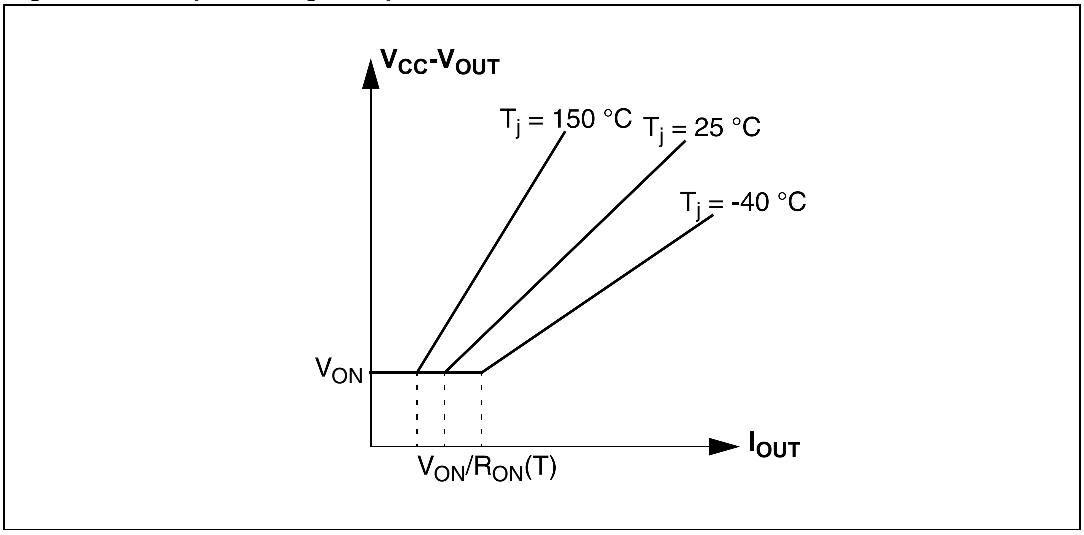


Figure 9. I_{OUT}/I_{SENSE} vs I_{OUT}

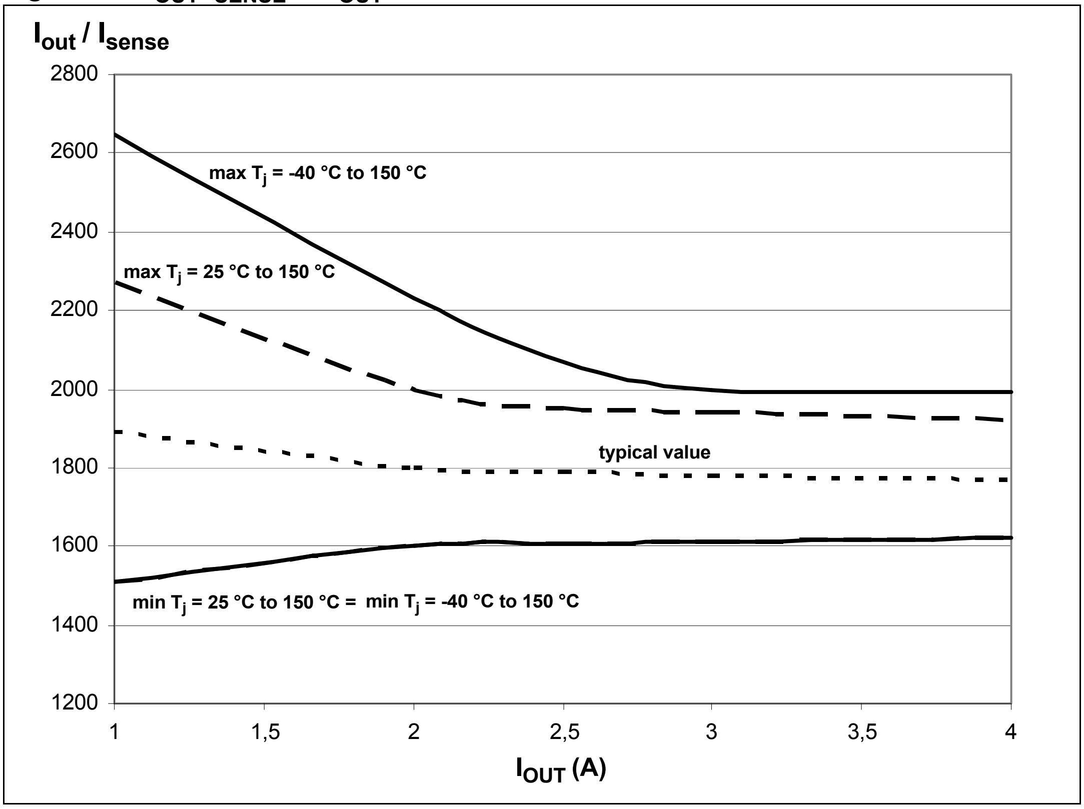
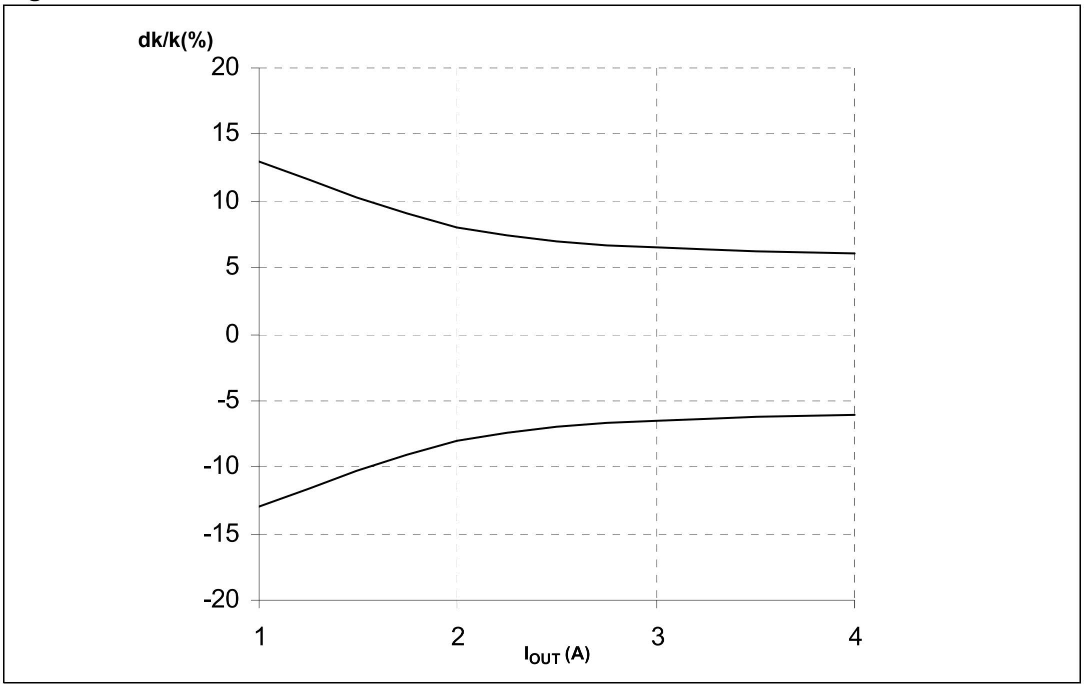


Figure 10. Maximum current sense ratio drift vs load current



Note: Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Input	Output	Sense (V_{CSD} = 0 V)(1)
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overload	H H	X (no power limitation) Cycling (power limitation)	Nominal V_{SENSEH}
Short circuit to GND (power limitation)	L H	L L	0 V_{SENSEH}
Open-load off-state (with external pull-up)	L	H	V_{SENSEH}
Short circuit to V_{CC} (external pull-up disconnected)	L H	H H	V_{SENSEH} < Nominal
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels[1]		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV		Min.	Max.	
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50µs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1µs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1µs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b[2]	+65V	+87V	1 pulse			400ms, 2Ω

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004E Test pulse	Test level results	
	III	VI
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b[1]	C	C

1. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device performed as designed after exposure to disturbance.
E	One or more functions of the device did not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 11. Normal operation

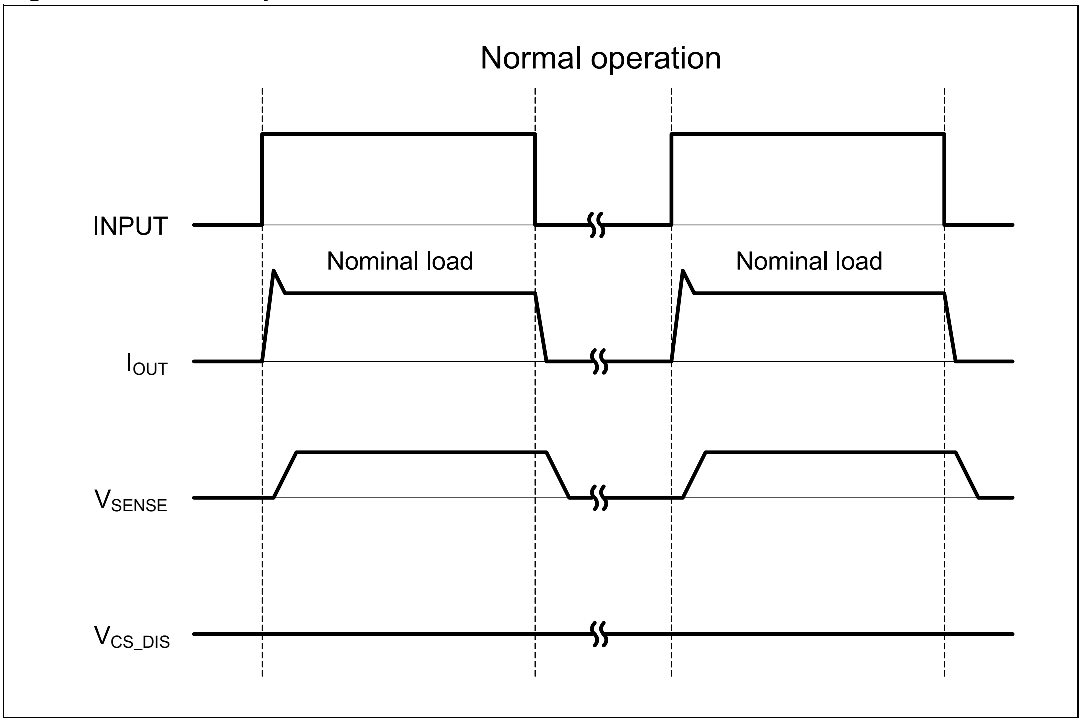


Figure 12. Overload or short to GND

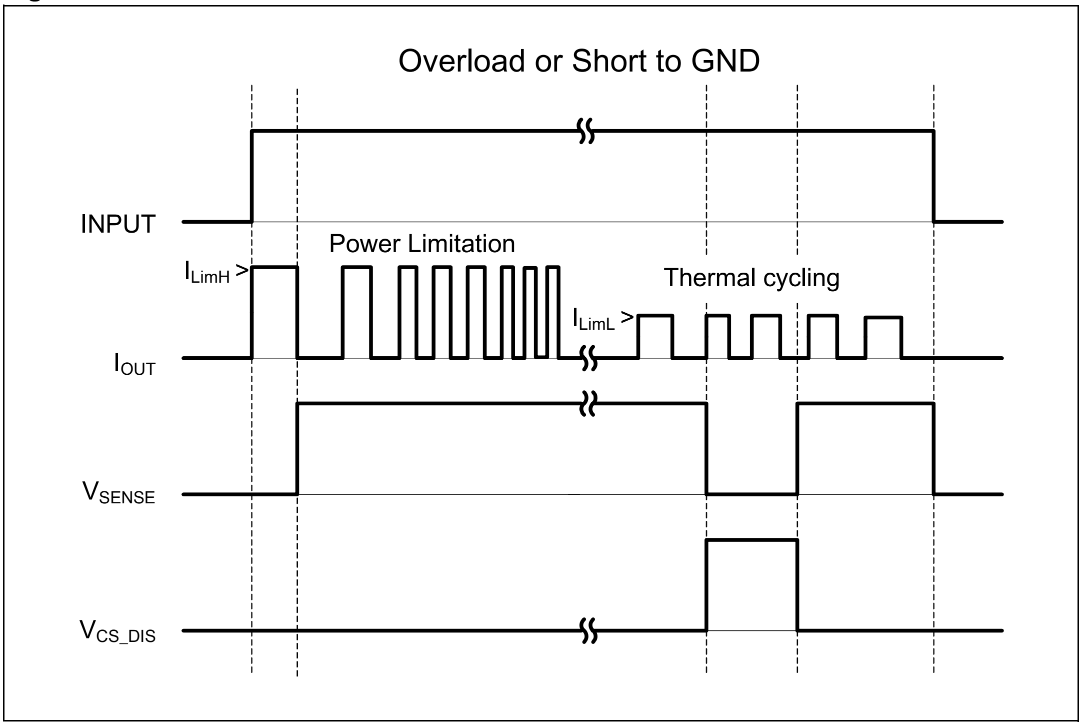


Figure 13. Intermittent overload

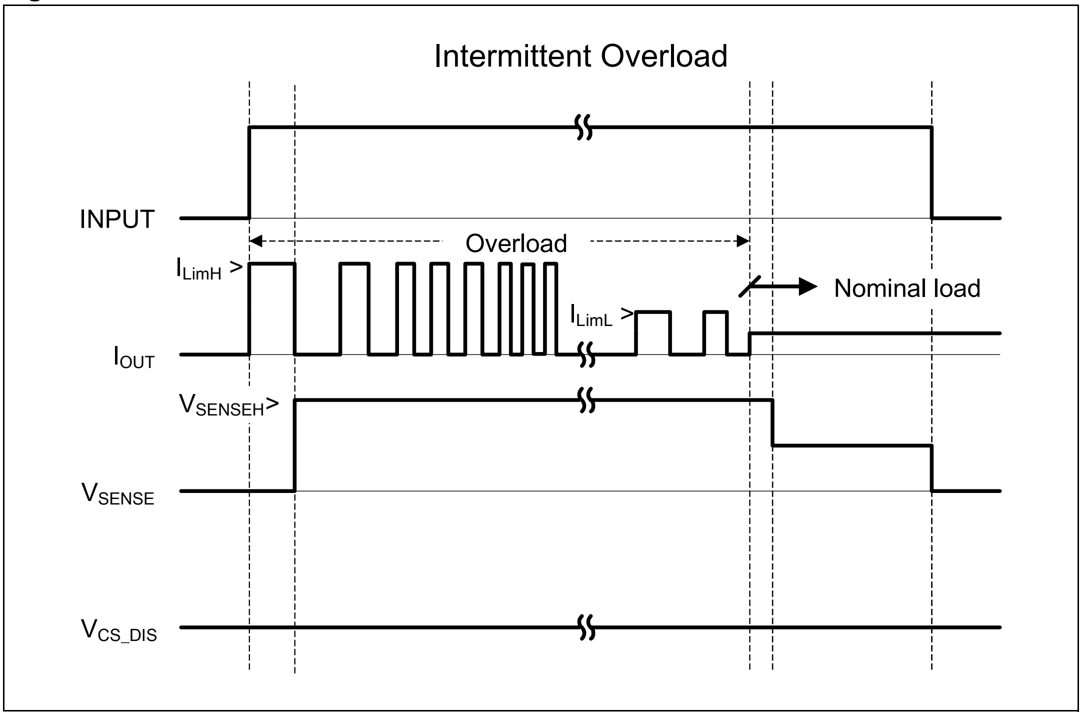


Figure 14. Off-state open-load with external circuitry

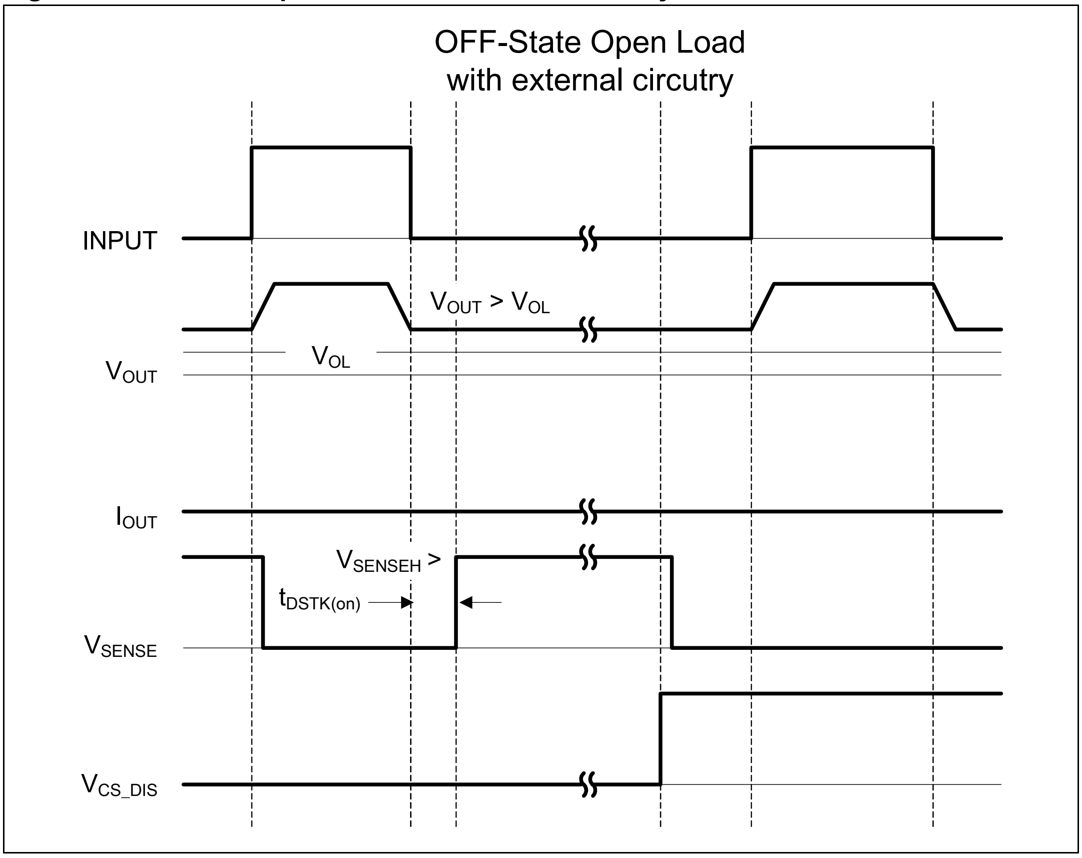


Figure 15. Short to V_{CC}

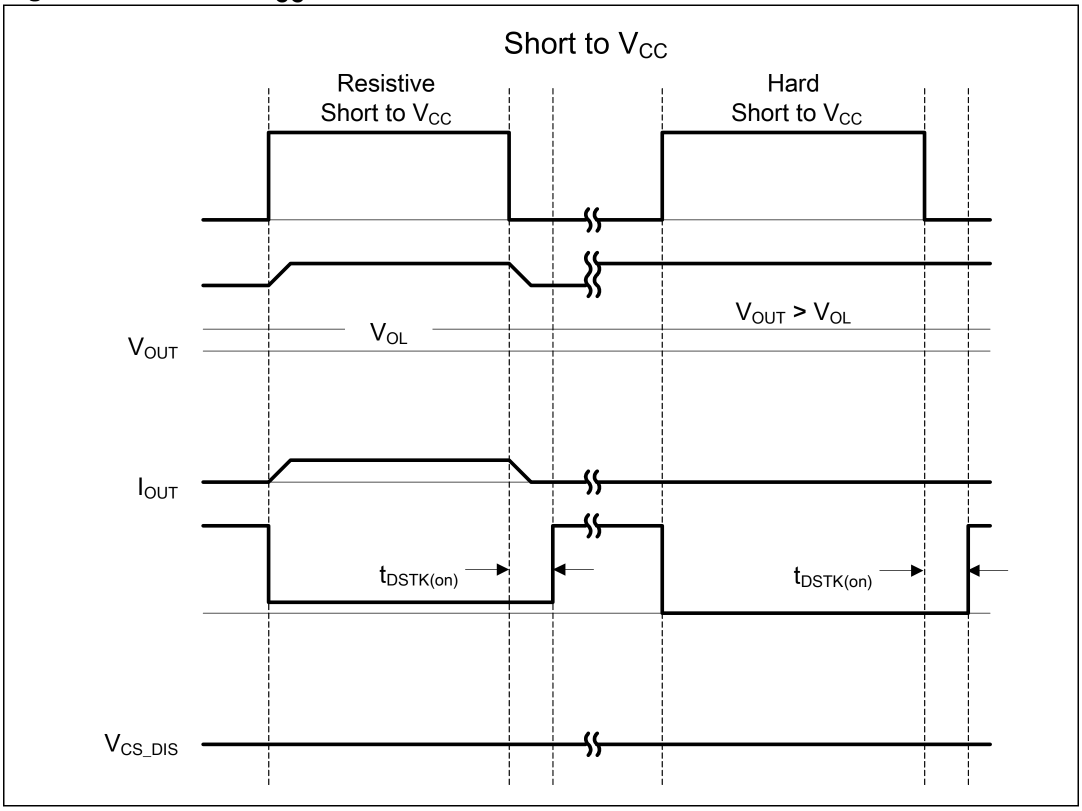
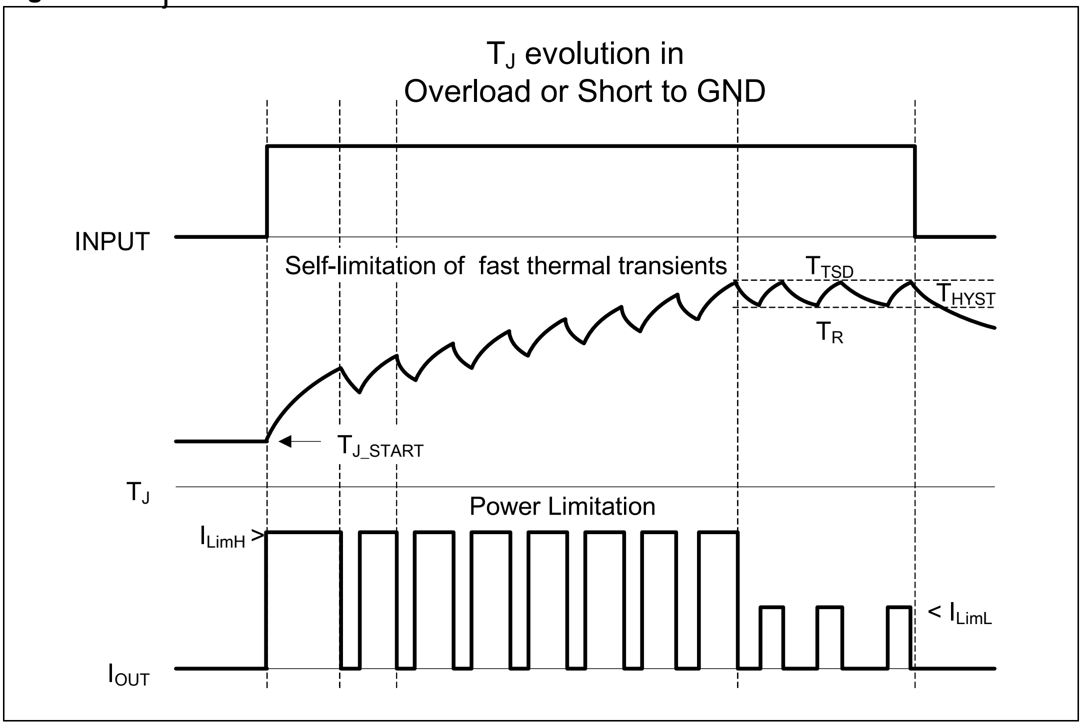


Figure 16. T_j evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 17. Off-state output current

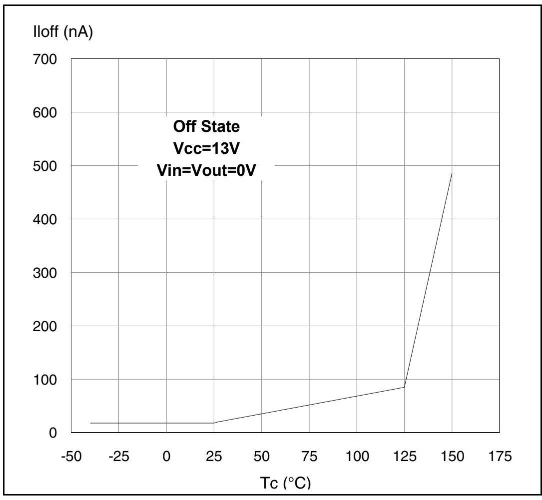


Figure 18. High level input current

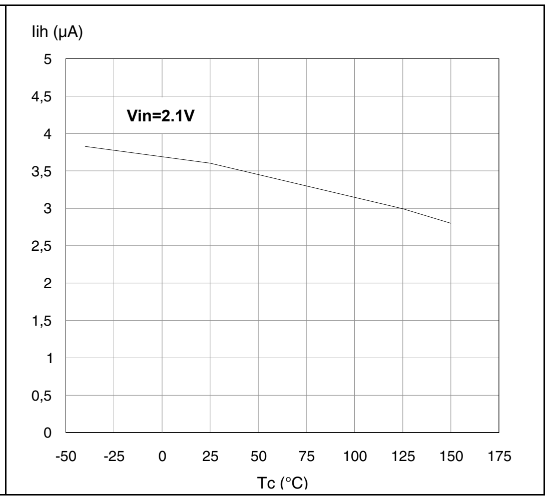


Figure 19. Input clamp voltage

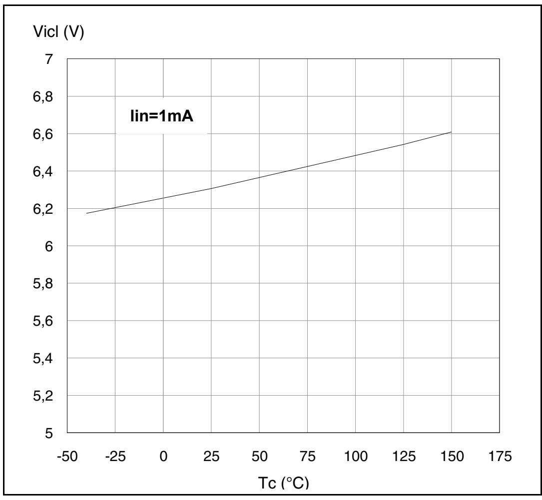


Figure 20. Input low level

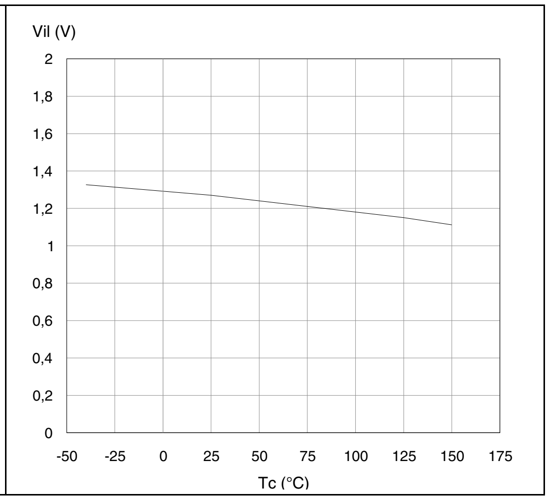


Figure 21. Input high level

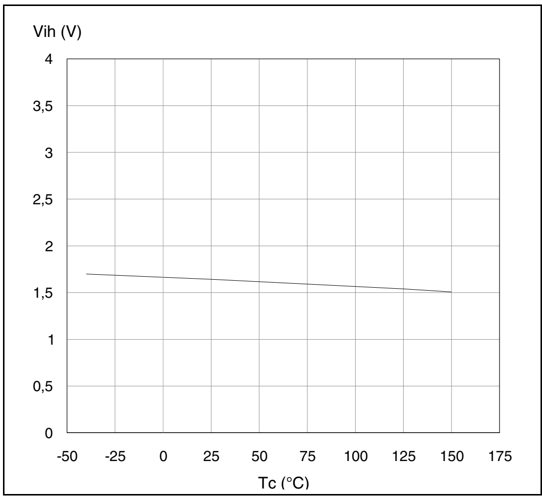


Figure 22. Input hysteresis voltage

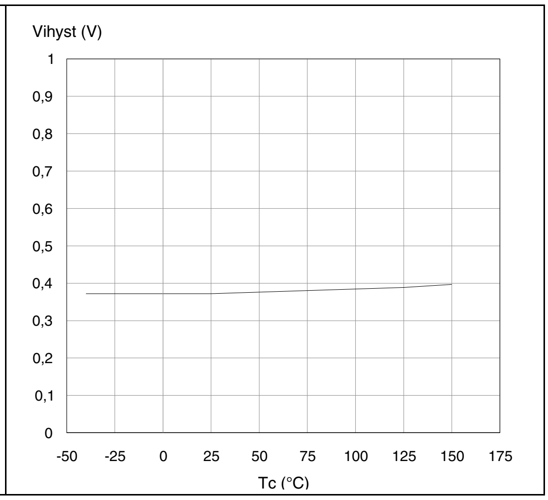


Figure 23. On-state resistance vs T_{case}

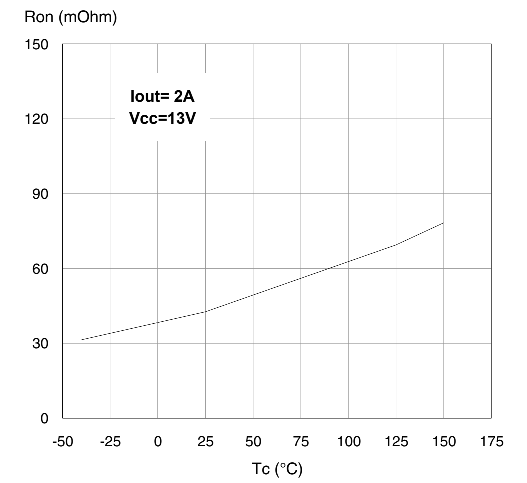


Figure 24. On-state resistance vs V_{CC}

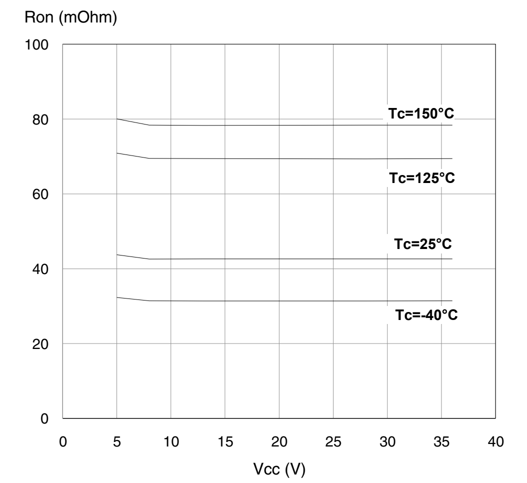


Figure 25. Undervoltage shutdown

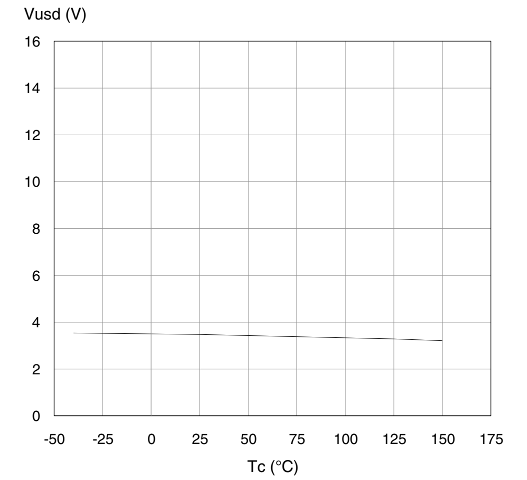


Figure 26. Turn-on voltage slope

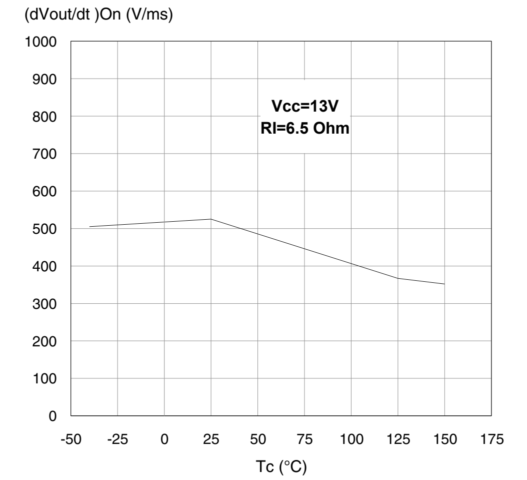


Figure 27. I_{LIMH} vs T_{case}

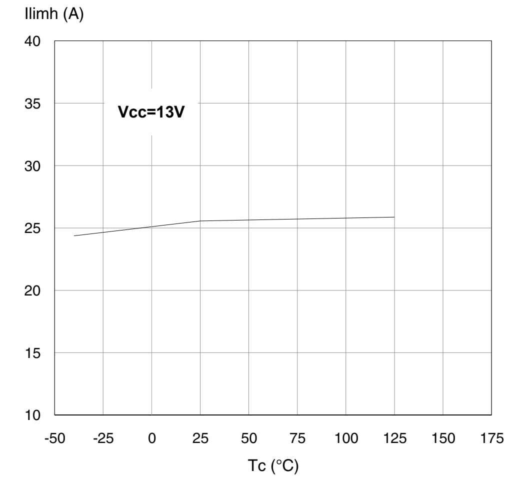


Figure 28. Turn-off voltage slope

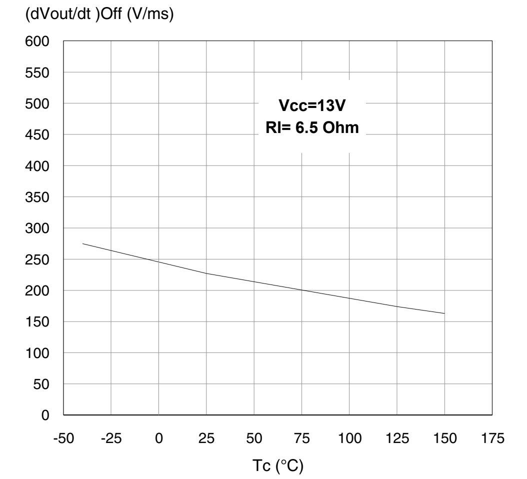


Figure 29. CS_DIS high level voltage

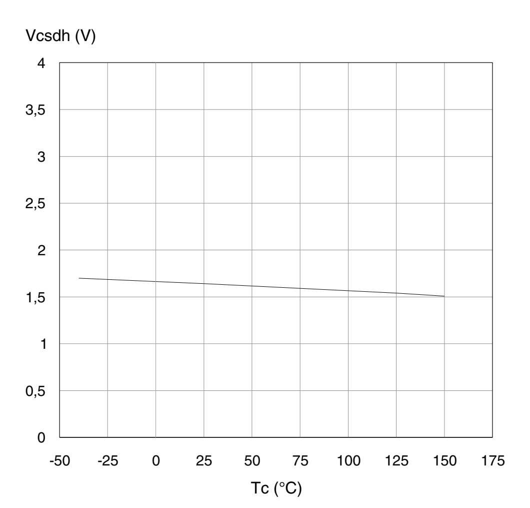


Figure 30. CS_DIS clamp voltage

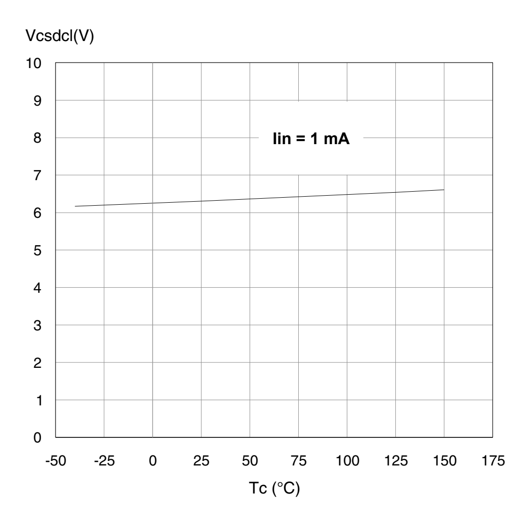
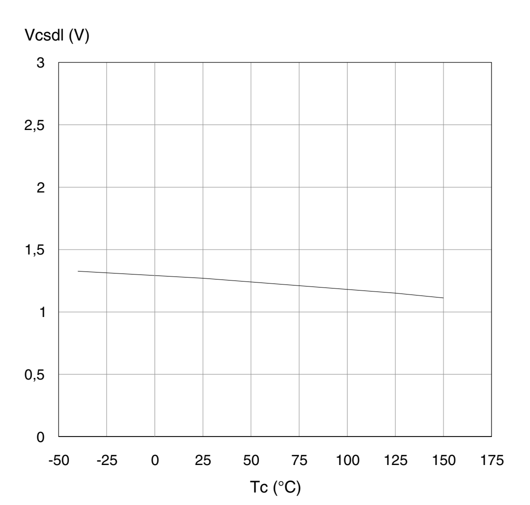
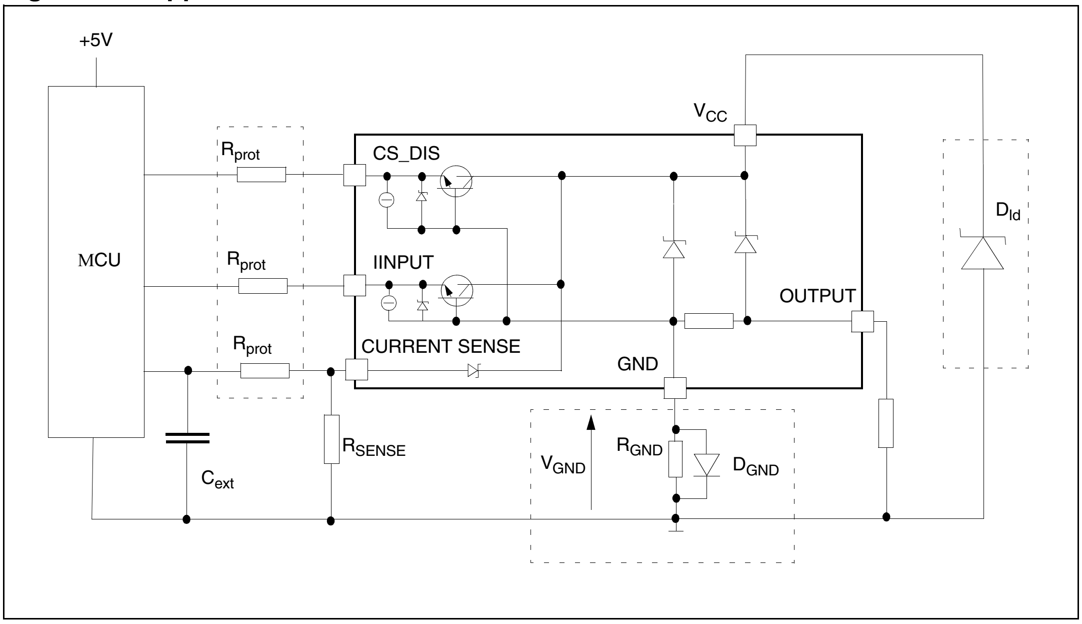


Figure 31. CS_DIS low level voltage



3 Application information

Figure 32. Application schematic



Note: Channel 2, 3, 4 have the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600$ mV / ($I_{S(on)max}$).
2. $R_{GND} \geq (-V_{CC})$ / ($-I_{GND}$)

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

Equation 1

$$P_D = (-V_{CC})^2/R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are on in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize *Section 3.1.2: Solution 2: diode (DGND) in the ground line*.

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (≈600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins to latch-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 2

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak} = -100 V and $I_{latchup} \geq 20$ mA; $V_{OH\mu C} \geq 4.5$ V

$5\ k\Omega \leq R_{prot} \leq 180\ k\Omega$.

Recommended values: R_{prot} = 10 kΩ, C_{EXT} = 10 nF.

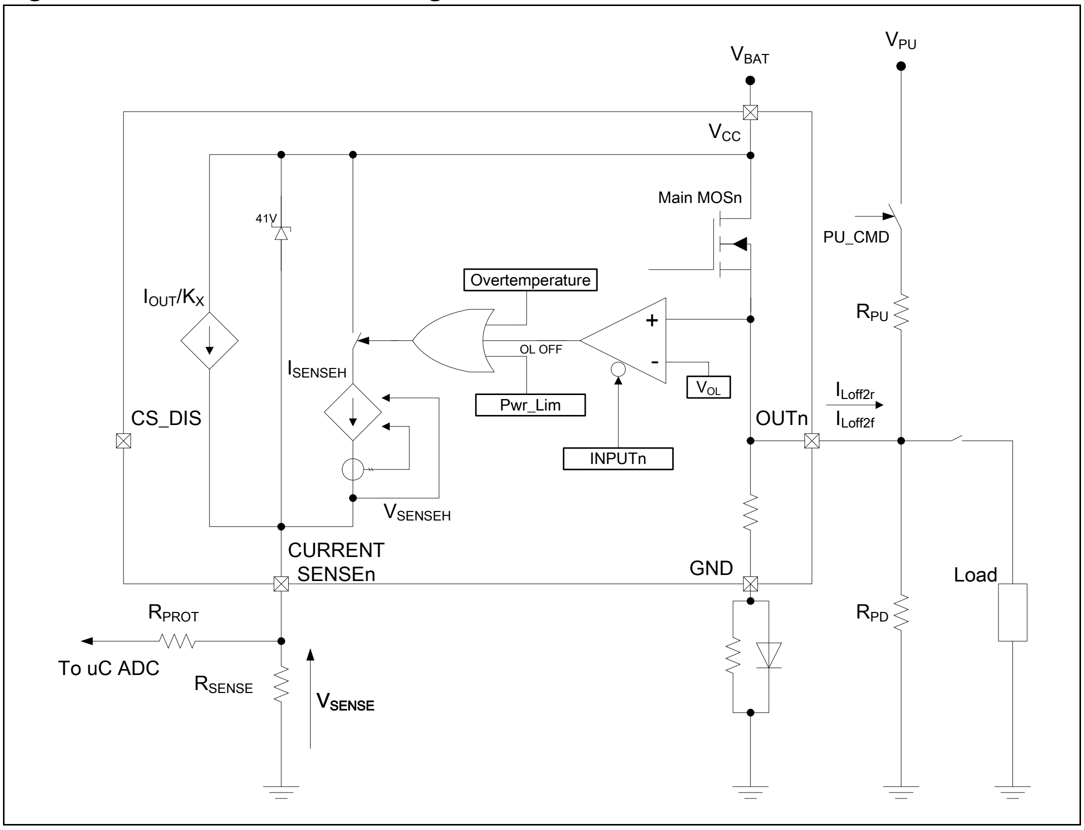
3.4 Current sense and diagnostic

The current sense pin performs a double function (see *Figure 33: Current sense and diagnostic*):

- **Current mirror of the load current in normal operation,** delivering a current proportional to the load one according to a known ratio $\mathbf{K_X}$.
  The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE}. Linearity between I_{OUT} and V_{SENSE} is ensured up to 5V minimum (see parameter V_{SENSE} in *Table 9: Current sense (8 V < V_{CC} < 18 V)*). The current sense accuracy depends on the output current (refer to current sense electrical characteristics *Table 9: Current sense (8 V < V_{CC} < 18 V)*).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to *Truth table*):
  - Power limitation activation
  - Overtemperature
  - Short to V_{CC} in off-state
  - Open-load in off-state with additional external components.

A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 33. Current sense and diagnostic



3.4.1 Short to V_{CC} and off-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

Off-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

An external pull down resistor R_{PD} connected between output and GND is mandatory to avoid misdetection in case of floating outputs in off-state (see *Figure 33: Current sense and diagnostic*).

R_{PD} must be selected in order to ensure $V_{OUT} < V_{OLmin}$ unless pulled up by the external circuitry:

Equation 3

$$V_{OUT}\big|_{Pull-up\_OFF} = R_{PD} \cdot I_{L(off2)f} < V_{OL\min} = 2V$$

$R_{PD} \leq 22\ K\Omega$ is recommended.

For proper open-load detection in off-state, the external pull-up resistor must be selected according to the following formula:

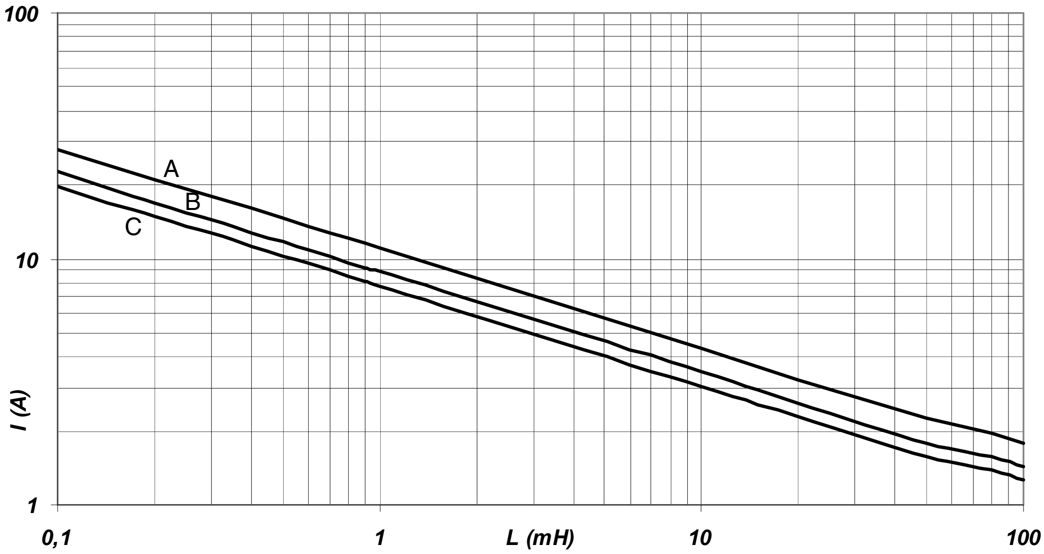
Equation 4

$$V_{OUT}\big|_{Pull-up\_ON} = \frac{R_{PD} \cdot V_{PU} - R_{PU} \cdot R_{PD} \cdot I_{L(off2)r}}{R_{PU} + R_{PD}} > V_{OL\max} = 4V$$

For the values of V_{OLmin},V_{OLmax}, $I_{L(off2)r}$ and $I_{L(off2)f}$ see *Table 10: Open-load detection (8V<V_{CC}<18V)*.

3.5 Maximum demagnetization energy (V_{CC} = 13.5 V)

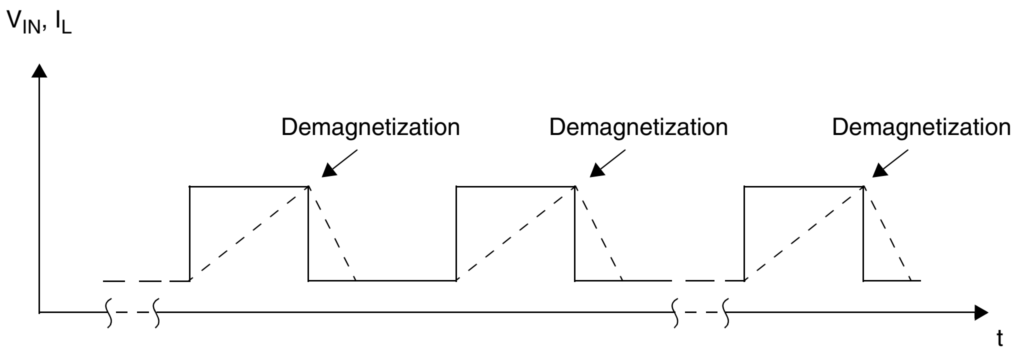
Figure 34. Maximum turn-off current versus inductance (for each channel)



A: T_{jstart} = 150°C single pulse

B: T_{jstart} = 100°C repetitive pulse

C: T_{jstart} = 125°C repetitive pulse



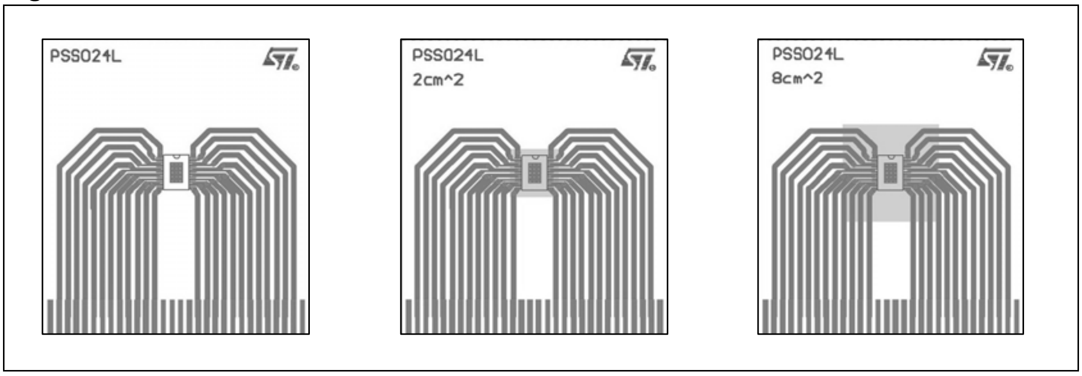
Note: *Values are generated with R_L = 0Ω*

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 PowerSSO-24 thermal data

Figure 35. PowerSSO-24 PC board



Note: *Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70 µm (front and back side), Copper areas: from minimum pad lay-out to 8 cm^2).*

Figure 36. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

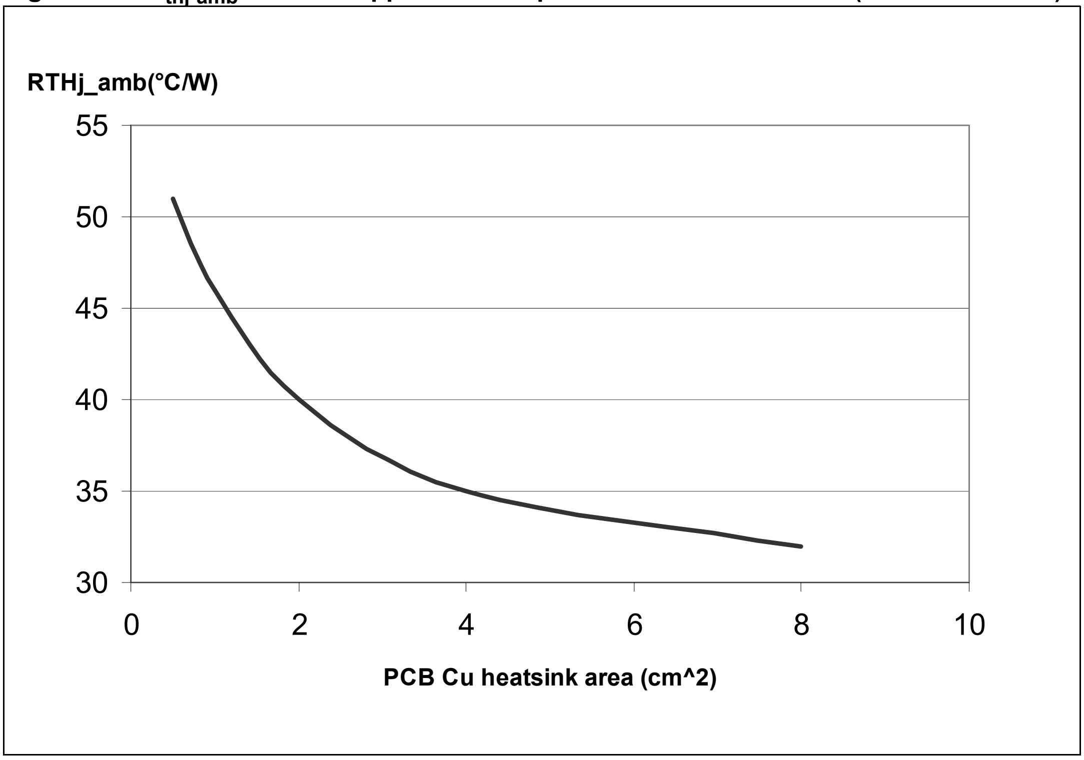


Figure 37. PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)

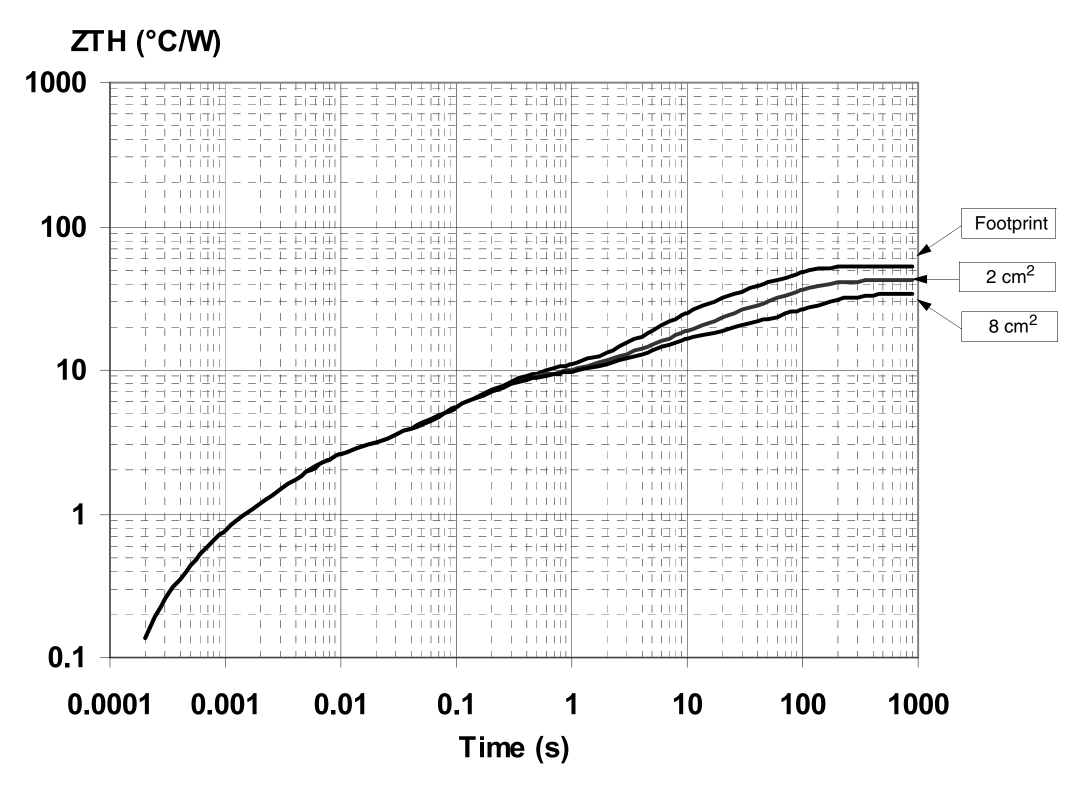
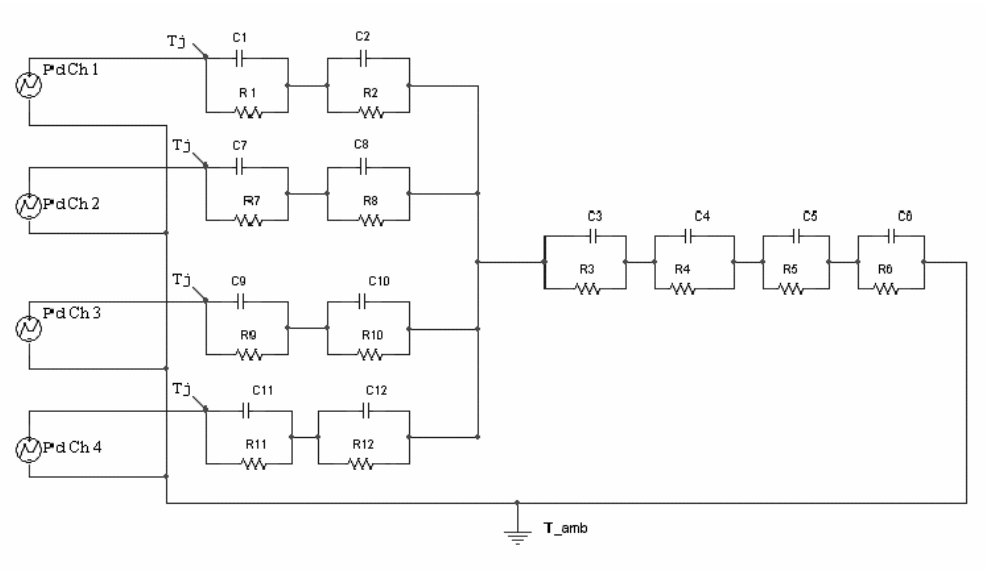


Figure 38. Thermal fitting model of a double channel HSD in PowerSSO-24



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 5: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Table 15. Thermal parameters

Area/island (cm^2)	Footprint	2	8
R1 = R7 = R9 = R11 (°C/W)	0.4		
R2 = R8 = R10 = R12 (°C/W)	2		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1 = C7 = C9 = C11 (W.s/°C)	0.001		
C2 = C8 = C10 = C12 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 PowerSSO-24 mechanical data

Figure 39. PowerSSO-24 package dimensions

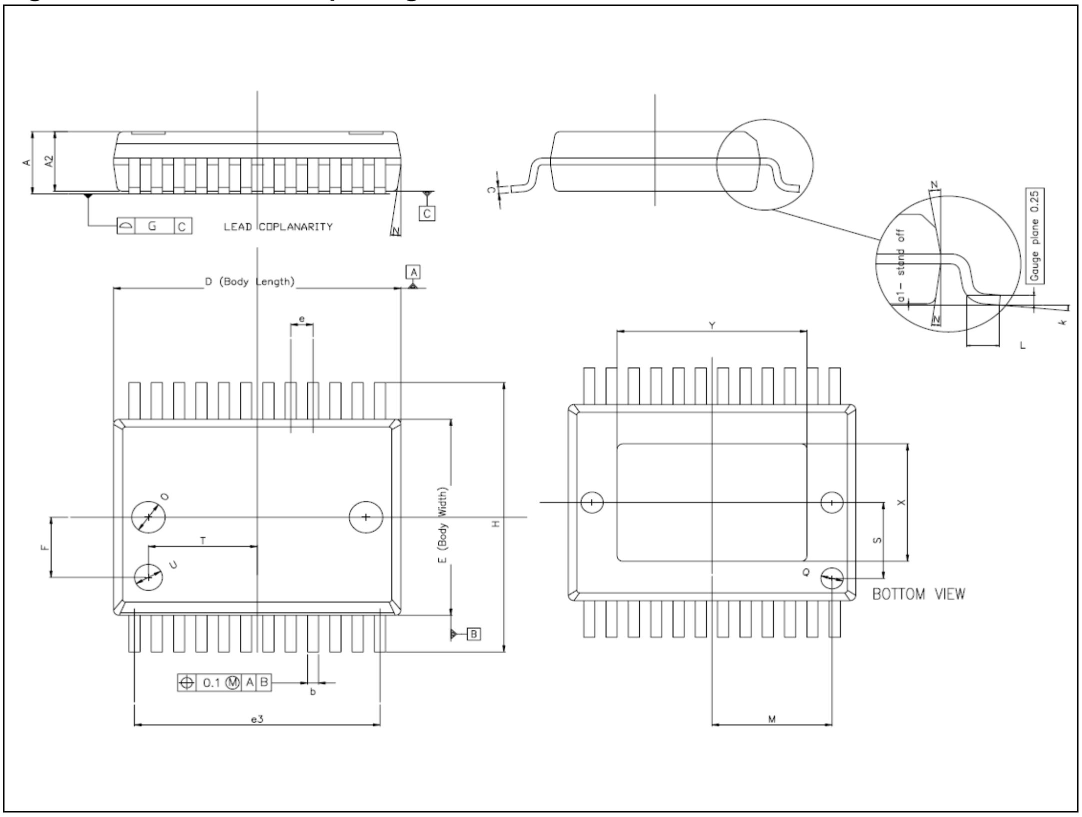
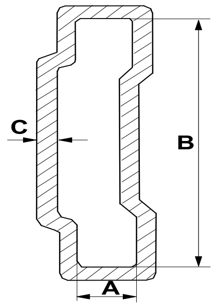


Table 16. PowerSSO-24 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.45
A2	2.15		2.35
a1	0		0.1
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.40		7.60
e		0.8	
e3		8.8	
F		2.3	
G			0.1
H	10.1		10.5
h			0.4
k	0°		8°
L	0.55		0.85
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1.0	
N			10°
X	4.1		4.7
Y	6.5		7.1

5.3 Packing information

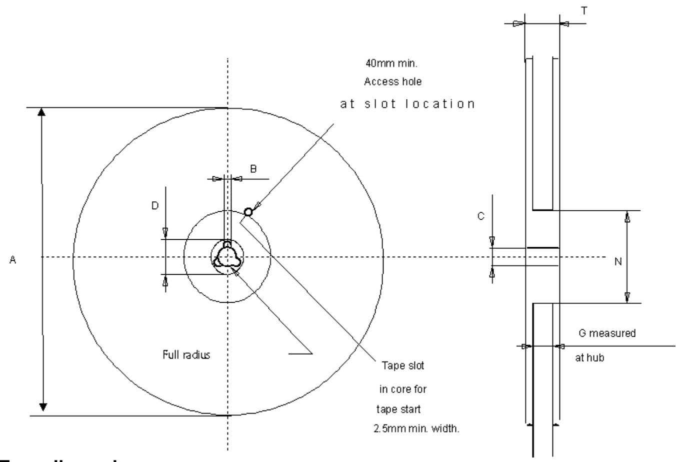
Figure 40. PowerSSO-24 tube shipment (no suffix)



Base q.ty	49
Bulk q.ty	1225
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 41. PowerSSO-24 tape and reel shipment (suffix "TR")



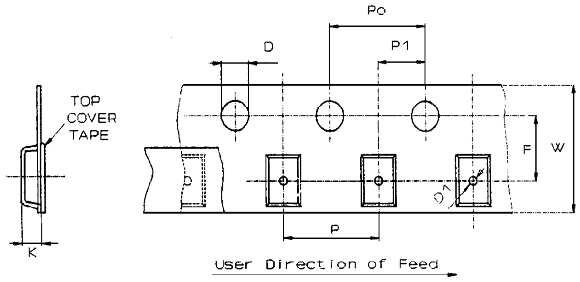
Reel dimensions

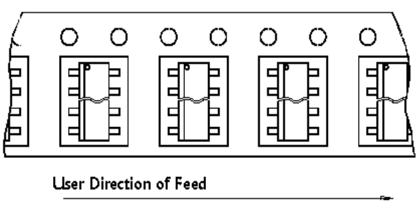
Base q.ty	1000
Bulk q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	100
T (max)	30.4

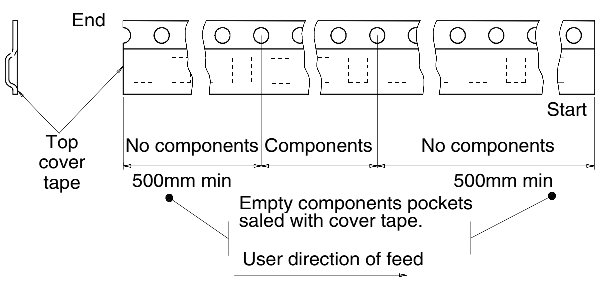
Tape dimensions
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape hole spacing	**P0 (± 0.1)**	4
Component spacing	**P**	12
Hole diameter	**D (± 0.05)**	1.55
Hole diameter	**D1 (min)**	1.5
Hole position	**F (± 0.1)**	11.5
Compartment depth	**K (max)**	2.85
Hole spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







6 Order codes

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-24	VNQ5E050AK-E	VNQ5E050AKTR-E

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
06-Jun-2007	1	Initial release.
27-Mar-2008	2	Updated *Table 9: Current sense (8 V < V_{CC} < 18 V)*: – added dk1/k1, dk2/k2, dk3/k3 parameters – changed $t_{DSENSE2H}$ max value from 300 µs to 250 µs Updated *Table 10: Open-load detection (8V<V_{CC}<18V)*: – added $I_{L(off2)r}$, $I_{L(off2)f}$ and td_vol parameters Added *Figure 9.: I_{OUT}/I_{SENSE} vs I_{OUT}*. Added *Figure 10.: Maximum current sense ratio drift vs load current* Added *Section 2.4: Waveforms*. Added *Section 2.5: Electrical characteristics curves*. Updated *Section 3: Application information*: – added *Section 3.4: Current sense and diagnostic* Updated *Section 4: Package and PC board thermal data*: – added *Figure 37.: PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)* – added *Table 15: Thermal parameters*.
17-Mar-2009	3	Changed *Table 16: PowerSSO-24 mechanical data*
22-Jun-2009	4	*Table 16: PowerSSO-24 mechanical data*: – Changed L (min) value from 6 to 0.55 – Changed L (max) value from 1 to 0.85
22-Jul-2009	5	Updated *Figure 39: PowerSSO-24 package dimensions*.
26-Oct-2010	6	*Table 5: Power section*: – V_{USD}: updated minimum value
20-Sep-2013	7	Updated Disclaimer