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1 Block diagram and pin description

Figure 1. Block diagram

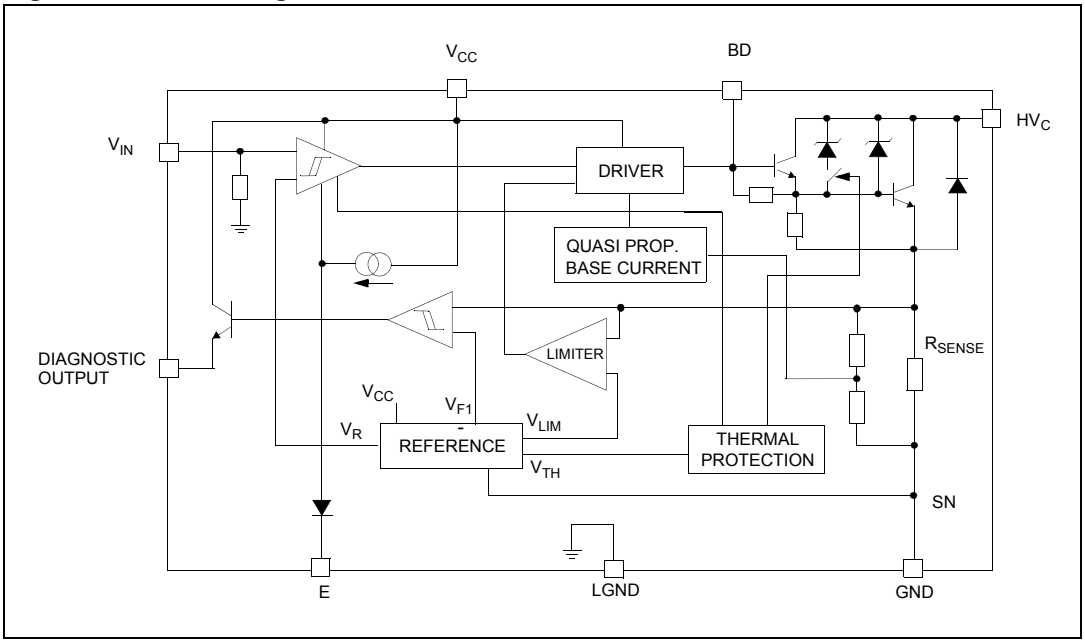

Table 2. Pin function

Pin number	Name	Function
1, 5	LGND	Signal ground
2, 3, 4	GND	Emitter power ground
6	E	Enable(1)
7	V_{CC}	Logic supply voltage
8	BD	Base darlington
9	INPUT	Logic input channel (internal pull down)
10	FLAG	Diagnostic output signal (open emitter)
Tab	HV_C	Primary coil output driver (open collector)

1. When grounded the input is enabled

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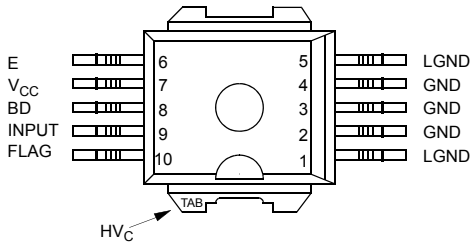
Figure 2. Connection diagram (top view)



Note:
Pin 1 and pin 5 must be connected to pin2, pin 3 and pin 4

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2 Electrical specifications

2.1 Absolute maximum rating

Stressing the device above the ratings listed in the “Absolute maximum ratings” tables may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
HV_c	Collector voltage (internally limited)	-0.3 to V_{clamp}	V
I_C	Collector current (internally limited)	10	A
$I_{C(gnd)}$	DC current on emitter power	±10.5	A
V_{CC}	Driving stage supply voltage	-0.3 to 7	V
I_s	Driving circuitry supply current	±200	mA
$I_{s(gnd)}$	DC current on ground pin	±1	A
V_{IN}	Input voltage	-0.3 to V_{CC} + 0.3	V
I_{IN}	Maximum input current	100	mA
f_{IN}	Logic input frequency in operative mode	DC to 150	Hz
$V_{OUT(flag)}$	Output voltage primary threshold current level	-0.3 to V_{CC} + 0.3	V
$I_{OUT(flag)}$	Flag output current	100	mA
P_{max}	Power Dissipation (T_c = 25 °C)	125	W
$E_{s/b}$	Self clamped energy during output power clamping (see *Figure 5*)	275	mJ
V_{ESD}	ESD voltage (HV_c pin)	±4	KV
V_{ESD}	ESD voltage (enable pin)	+1.5; -2	KV
V_{ESD}	ESD voltage (other pins)	±2	KV
I_{BD}	Input darlington base current	150	mA
V_{BD}	Input darlington base voltage	Internally limited	V
T_j	Operating junction temperature	-40 to 150	°C
T_{stg}	Storage temperature range	-55 to 150	°C
V_E	Maximum enable voltage	-0.3 to 5.5	V
I_E	Maximum enable current	±150	µA

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2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (max)	1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (max)	51	°C/W

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3 Electrical characteristics

5.3 V < V_{bat} < 24 V; V_{CC} = 5 V ±10 %; -40 °C < T_j < 125 °C; R_{coil} = 580 mΩ; L_{coil} = 3.75 mH unless otherwise specified[a].

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{cl}	High voltage clamp	I_{coil} = 6.5 A	320	380	420	V
V_{lcl}	Low voltage clamp	I_{coil} = 6.5 A; T_j = T_{sd}	30	40	50	V
$V_{ce(sat)}$	Power stage saturation voltage	I_C = 6 A; V_{IN} = 4 V		1.5	2	V
$I_{CC(stdby)}$	Standby supply current	IN = Off			11	mA
I_{CC}	DC logic current	V_b = 16 V; I_C = 6.5 A; f = 100 Hz; Load = Coil; V_{CC} = 5.5 V			40	mA
$I_{CC(peak)}$	Peak DC logic current during on phase	I_C = 6.5 A		100	150	mA
V_{CC}	DC logic voltage		4.5		5.5	V
I_{cl}	Coil current limit	-40 °C < T_j < 125 °C[1]	9		11	A
$I_{c(off)}$	Output off-state current	IN = Off; V_{HVC} = 24 V; V_{CC} = 5 V; T_j = 25 °C			5	mA
V_{INH}	High level input voltage	V_{CC} = 4.5 V	4		V_{CC}	V
V_{INL}	Low level input voltage	V_{CC} = 5.5 V	-0.3		0.8	V
$V_{IN(hyst)}$	Input threshold hysteresis		0.4			V
I_{INH}	High level input current	V_{IN} = 4 V			100	µA
I_{INL}	Low level input current	V_{IN} = 0.8 V	0		30	µA
I_{INpd}	Input active pull down	V_{IN} = 4 V	10		100	µA
V_{diagH}	High level flag output voltage	R_{EXT} = 22 KΩ; C_{EXT} = 1 nF[2]	V_{CC} - 1		V_{CC}	V
V_{diagL}	Low level flag output voltage	R_{EXT} = 22 KΩ; C_{EXT} = 1 nF[2]			0.5	V
I_{diagTH}	Coil current level threshold	T_j = 25 °C	4.25	4.5	4.75	A
I_{diagTD}	Coil current level threshold drift	(See *Figure 4*)				

a. Parametric degradation are allowed with 5.3 V< V_b < 10 V and V_b > 24 V.

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Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{diag}	High level flag output current	$I_C > I_{diagTH}$; V_{diag} = 3 V	0.5			mA
$I_{diag(leak)}$	Leakage current on flag output	V_{IN} = Low; V_{CC} = 5.5 V			10	µA
V_F	Anti parallel diode forward voltage	I_C = -1 A			2	V
$E_{s/b}$	Single pulse avalanche energy	L = 6 mH; I_C = 8 A		180		mJ
t_{ON}	Turn-on time	R_c = 0.5 Ω; L_c = 3.75 mH; T_j = 25 °C; V_{bat} = 13 V (see *Figure 3*)		1	5	µs
t_{OFF}	Turn-off time	R_c = 0.5 Ω; L_c = 3.75 mH; I_C = 6.5 A; T_j = 25 °C; V_{bat} = 13 V (see *Figure 3*)		15	25	µs
T_{sd}	Thermal shutdown intervention		150			°C
V_{EH}	High level enable voltage	V_{IN} = V_{INH}; OUT = Off(3)	2			V
V_{EL}	Low level enable voltage	V_{OUT} free to follow V_{IN}			0.40	V
I_{EH}	High level enable current	V_E = 5 V			500	µA
I_{EL}	Low level enable current	V_E < 0.4 V	-200			µA
$V_{BD(off)}$	Base darlington voltage off	V_E = V_{EH}			1	V
$V_{BD(on)}$	Base darlington voltage on	V_{IN} = V_{INH}; V_E = V_{EL}; I_C = 6.5 A	1.8			V

1. The primary coil current value I_{cl} must be measured ms after desaturation of the power stage.
2. No internal pull-down.
3. If ENABLE pin is floating OUT = Off for every input status.

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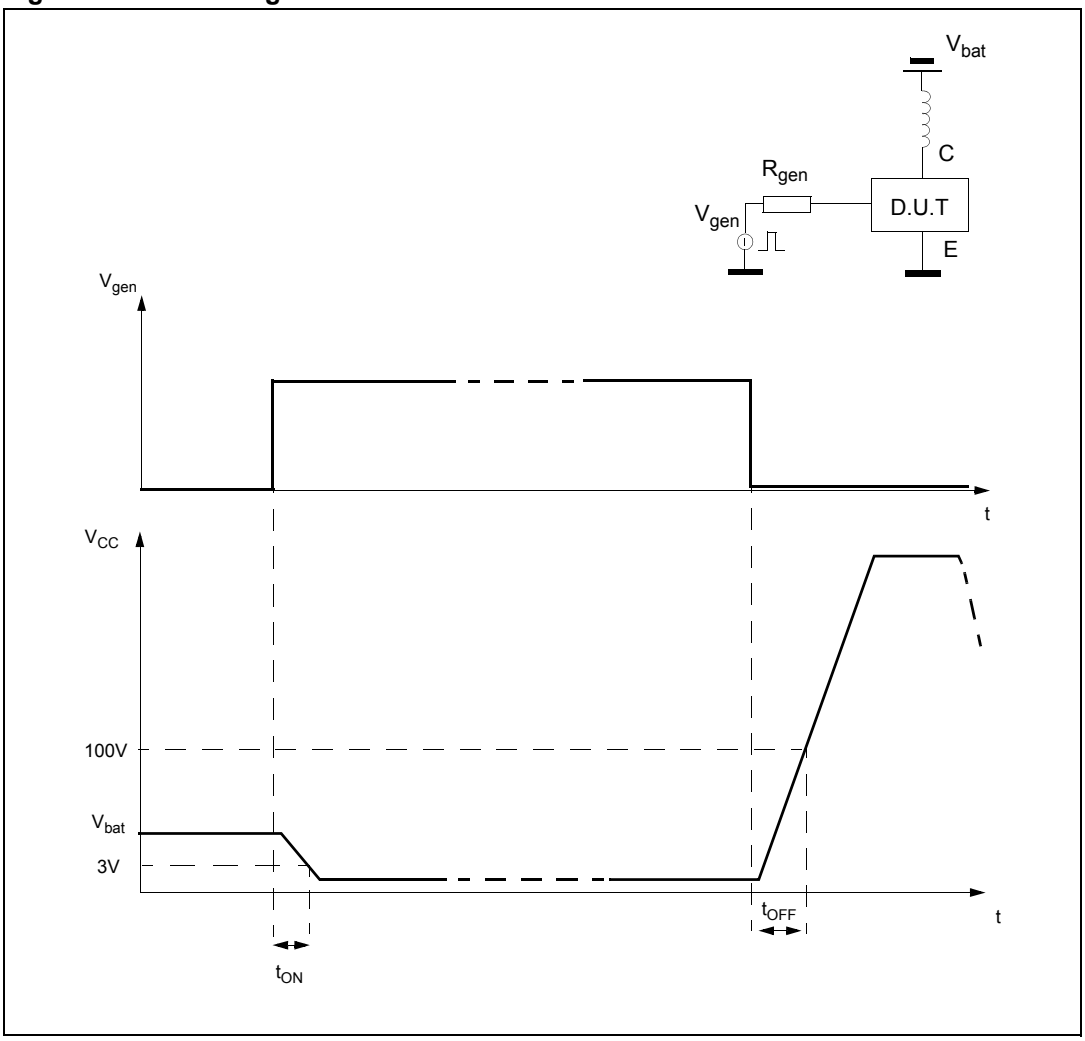
Figure 3. Switching time for inductive load



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3.1 Electrical characteristics curves

Figure 4. Flag current vs temperature

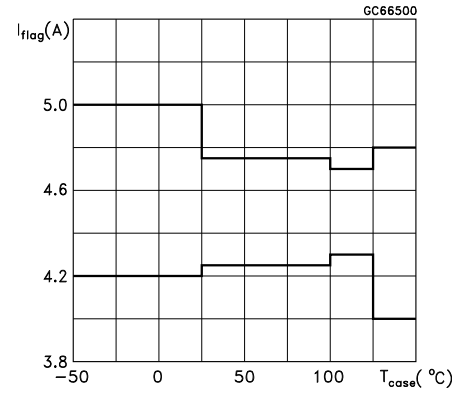


Figure 5. Single pulse avalanche energy capability

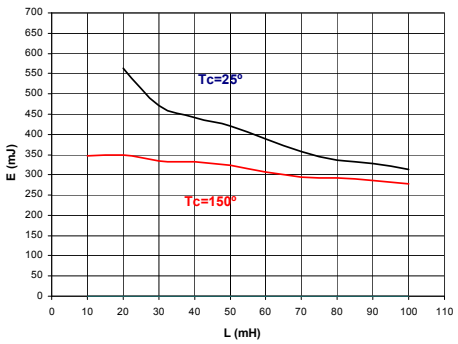


Figure 6. Self clamped inductive switching current vs time

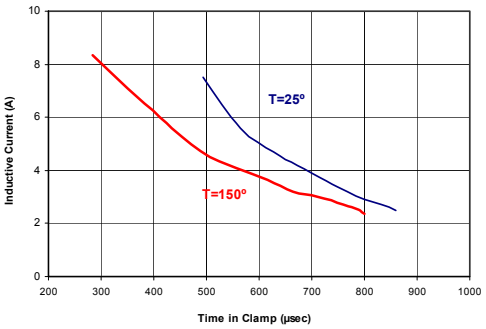
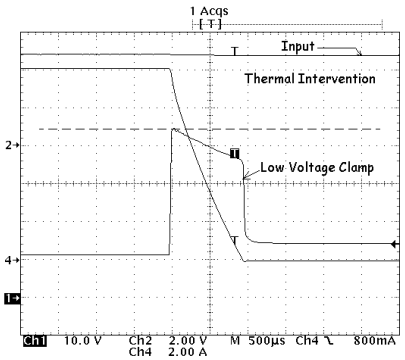


Figure 7. Low voltage clamp feature



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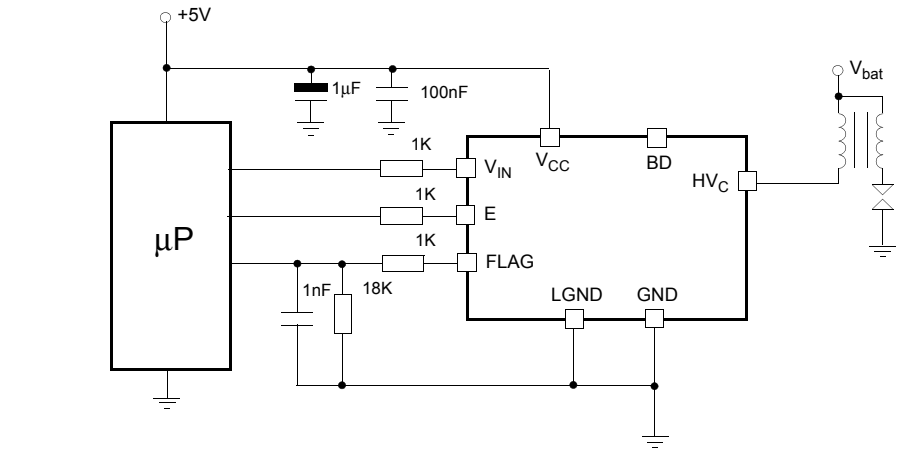
4 Application schematic

Figure 8. Application diagram



Note:
ENABLE pin can be alternatively connected to LGND.

4.1 Principle of operation

The VB525SP-E is mainly intended as a high voltage power switch device driven by a logic level input and interfaces directly to a high energy electronic ignition coil.

The input V_{IN} of the VB525SP-E is fed from a low power signal generated by an external controller that determines both dwell time and ignition point. During V_{IN} high (≥ 4 V) the VB525SP-E increases current in the coil to the desired, internally set current level.

After reaching this level, the coil current remains constant until the ignition point, that corresponds to the transition of V_{IN} from high to low (typ. 1.9 V threshold).

During the coil current switch-off, the primary voltage HV_C is clamped at an internally set value V_{cl}, typically 380 V. The transition from saturation to desaturation, coil current limiting phase, must have the ability to accommodate an overvoltage.

A maximum overshoot of 20 V is allowed.

4.2 Feedback

When the collector current exceeds 4.5 A, the feedback signal is turned high and it remains so, until the input voltage is turned-off.

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4.3 Overvoltage

The VB525SP-E can withstand the following transients of the battery line:

- -100 V / 2 msec (R_i = 10 Ω)
- +100 V / 0.2 msec (R_i = 10 Ω)
- +50 V / 400 msec (R_i = 4.2 Ω, with V_{IN} = 3 V)

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5 Package information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 PowerSO-10 mechanical data

Figure 9. PowerSO-10 package dimensions

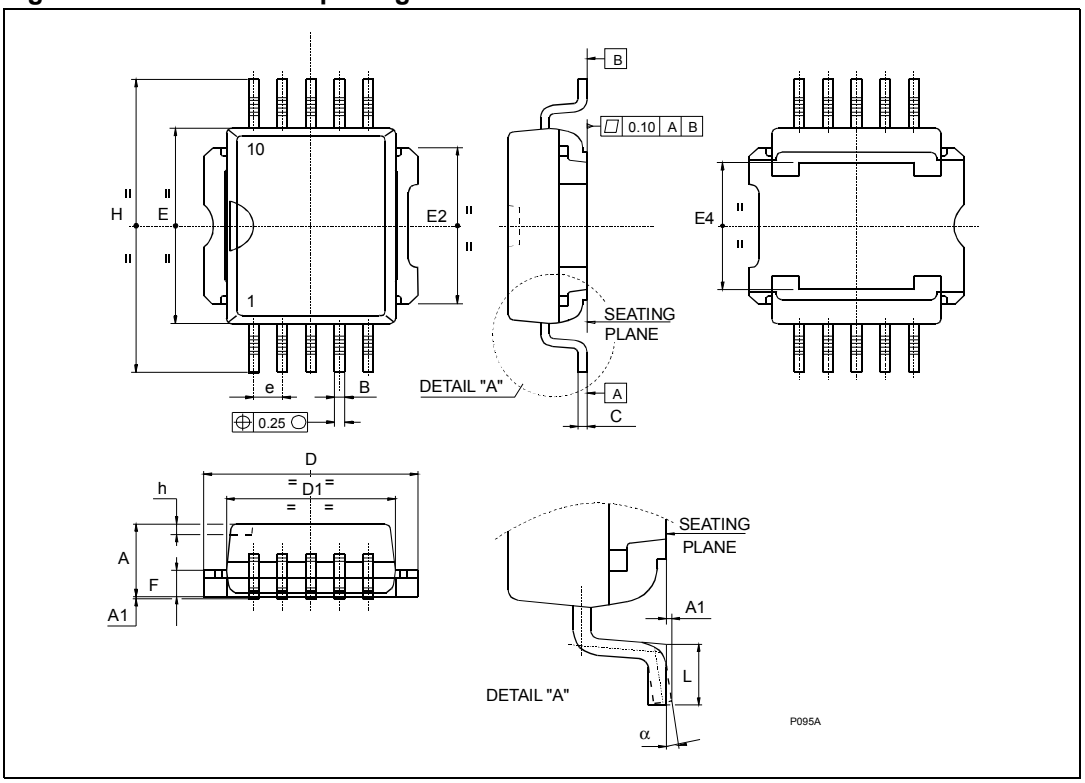

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Table 6. PowerSO-10 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	3.35		3.65
A(1)	3.4		3.6
A1	0.00		0.10
B	0.40		0.60
B(1)	0.37		0.53
C	0.35		0.55
C(1)	0.23		0.32
D	9.40		9.60
D1(2)	7.40		7.60
E(2)	9.30		9.50
E2	7.20		7.60
E2(1)	7.30		7.50
E4	5.90		6.10
E4(1)	5.90		6.30
e		1.27	
F	1.25		1.35
F(1)	1.20		1.40
H	13.80		14.40
H(1)	13.85		14.35
h		0.50	
L	1.20		1.80
L(1)	0.80		1.10
α	0º		8º
α(1)	2º		8º

1. Muar only POA P013P.
2. Resin protrusion not included (max value: 0.20 mm per side).

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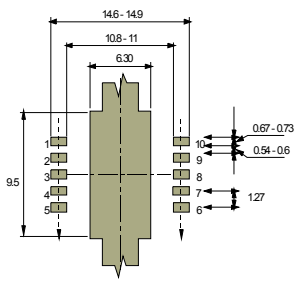
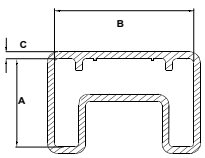
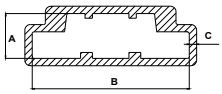
5.3 Packing information

Figure 10. PowerSO-10 suggested pad layout and tube shipment (no suffix)





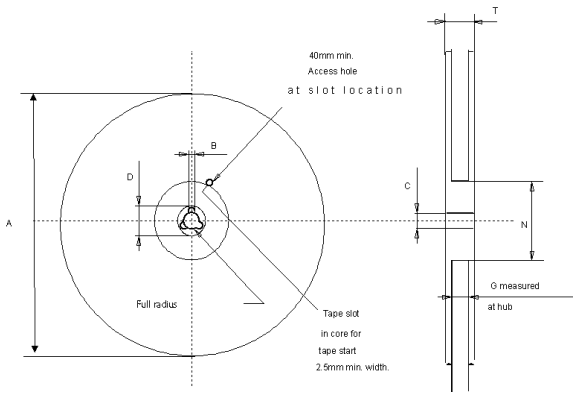
CASABLANCA MUAR



All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

Figure 11. PowerSO-10 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

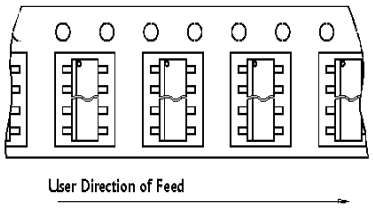
All dimensions are in mm.

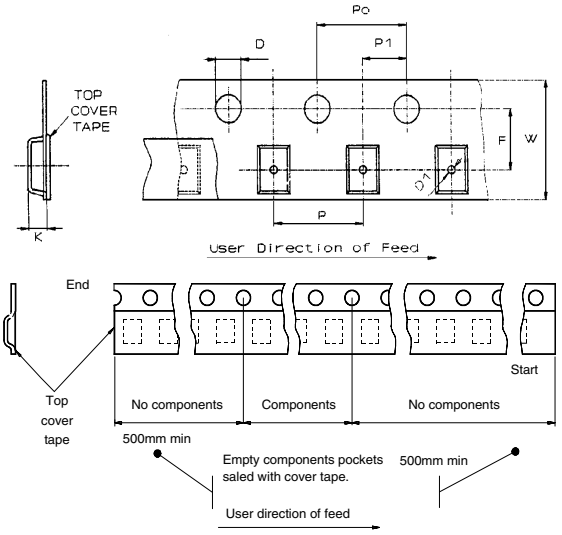
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	24
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.





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6 Revision history

Table 7. Document revision history

Date	Revision	Changes
27-Sep-2010	1	Initial release.
18-Sep-2013	2	Updated Disclaimer

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