1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage 6.5V
Output Voltage.................. (V_{SS} – 0.3V) to (V_{IN} + 0.3V)
Power Dissipation................Internally Limited **(Note 7)**
Maximum Voltage on Any Pin ....V_{IN} +0.3V to -0.3V
Operating Temperature Range...... -40°C < T_J < 125°C
Storage Temperature..........................-65°C to +150°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{IN} = V_R + 1.5V$, **(Note 1)**, I_L = 100 µA, C_L = 3.3 µF, $\overline{SHDN} > V_{IH}$, T_A = +25°C. **Boldface** type specifications apply for junction temperatures of -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Operating Voltage	V_{IN}	**2.7**	—	**6.0**	V	**Note 2**
Maximum Output Current	I_{OUTMAX}	**800**	—	—	mA	
Output Voltage	V_{OUT}	**V_R – 2.5%**	V_R ± 0.5%	**V_R + 2.5%**	V	$V_R \geq 2.5V$
		V_R – 2%	V_R ± 0.5%	**V_R + 3%**		$V_R = 1.8V$
V_{OUT} Temperature Coefficient	$\Delta V_{OUT}/\Delta T$	—	40	—	ppm/°C	**Note 3**
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	—	0.007	**0.35**	%	$(V_R + 1V) \leq V_{IN} \leq 6V$
Load Regulation **(Note 4)**	$\Delta V_{OUT}/V_{OUT}$	**-0.01**	0.002	**+0.01**	%/mA	I_L = 0.1 mA to I_{OUTMAX}
Dropout Voltage **(Note 5)**	$V_{IN}–V_{OUT}$	—	20	**30**	mV	$V_R \geq 2.5V$, I_L = 100 µA
		—	50	**160**		I_L = 100 mA
		—	150	**480**		I_L = 300 mA
		—	260	**800**		I_L = 500 mA
		—	450	**1300**		I_L = 800 mA
		—	1000	**1200**		V_R = 1.8V, I_L = 500 mA
		—	1200	**1400**		I_L = 800 mA
Supply Current	I_{DD}	—	80	**130**	µA	$\overline{SHDN} = V_{IH}$, I_L = 0
Shutdown Supply Current	I_{SHDN}	—	0.05	**1**	µA	$\overline{SHDN}$ = 0V
Power Supply Rejection Ratio	PSRR	—	64	—	db	F ≤ 1 kHz
Output Short Circuit Current	I_{OUTSC}	—	1200	1400	mA	V_{OUT} = 0V
Thermal Regulation	$\Delta V_{OUT}/\Delta P_D$	—	0.04	—	V/W	**Note 6**
Output Noise	eN	—	260	—	nV/√Hz	$I_L = I_{OUTMAX}$, F = 10 kHz

Note 1: V_R is the regulator output voltage setting.

2: The minimum V_{IN} has to justify the conditions: $V_{IN} \geq V_R + V_{DROPOUT}$ and $V_{IN} \geq 2.7V$ for I_L = 0.1 mA to I_{OUTMAX}.

3:

$$TCV_{OUT} = \frac{(V_{OUTMAX} - V_{OUTMIN}) - 10^6}{V_{OUT} \times \Delta T}$$

4: Regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

5: Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value measured at a 1.5V differential.

6: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to I_{LMAX} at V_{IN} = 6V for T = 10 ms.

7: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction-to-air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown. Please see **Section 5.0 "Thermal Considerations"** for more details.

8: Hysteresis voltage is referenced to V_R.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, $V_{IN} = V_R + 1.5V$, **(Note 1)**, $I_L = 100\ \mu A$, $C_L = 3.3\ \mu F$, $\overline{\text{SHDN}} > V_{IH}$, $T_A = +25°C$. **Boldface** type specifications apply for junction temperatures of -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{\text{SHDN}}$ Input						
$\overline{\text{SHDN}}$ Input High Threshold	V_{IH}	**45**	—	—	$\%V_{IN}$	
$\overline{\text{SHDN}}$ Input Low Threshold	V_{IL}	—	—	**15**	$\%V_{IN}$	
$\overline{\text{ERROR}}$ Output (SOIC Only)						
Minimum Operating Voltage	V_{MIN}	1.0	—	—	V	
Output Logic Low Voltage	V_{OL}	—	—	**400**	mV	1 mA Flows to $\overline{\text{ERROR}}$
$\overline{\text{ERROR}}$ Threshold Voltage	V_{TH}	—	$0.95 \times V_R$	—	V	
$\overline{\text{ERROR}}$ Positive Hysteresis	V_{HYS}	—	50	—	mV	**Note 8**

Note 1: V_R is the regulator output voltage setting.

2: The minimum V_{IN} has to justify the conditions: $V_{IN} \geq V_R + V_{DROPOUT}$ and $V_{IN} \geq 2.7V$ for $I_L = 0.1$ mA to I_{OUTMAX}.

3:

$$TCV_{OUT} = \frac{(V_{OUTMAX} - V_{OUTMIN}) - 10^6}{V_{OUT} \times \Delta T}$$

4: Regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

5: Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value measured at a 1.5V differential.

6: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to I_{LMAX} at $V_{IN} = 6V$ for T = 10 ms.

7: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction-to-air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown. Please see **Section 5.0 "Thermal Considerations"** for more details.

8: Hysteresis voltage is referenced to V_R.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{IN} = V_R + 1.5V$, $I_L = 100\ \mu A$, $C_L = 3.3\ \mu F$, $\overline{\text{SHDN}} > V_{IH}$, $T_A = +25°C$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Operating Temperature Range	T_J	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-DDPAK	θ_{JA}	—	57	—	°C/W	
Thermal Resistance, 5L-TO-220	θ_{JA}	—	71	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	

Note 1: Operation in this range must not cause T_J to exceed Maximum Junction Temperature (+125°C).

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

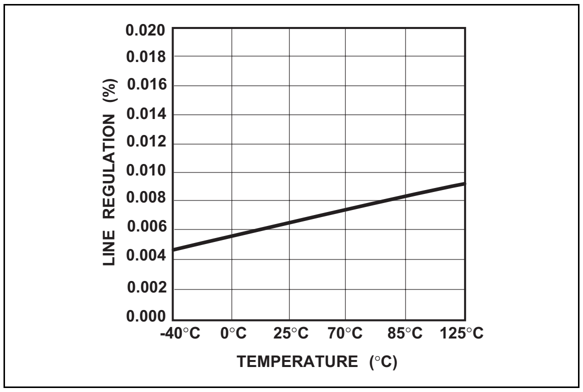


FIGURE 2-1: Line Regulation vs. Temperature.

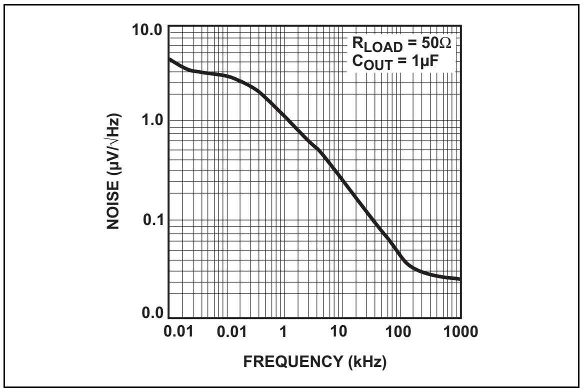


FIGURE 2-2: Output Noise vs. Frequency.

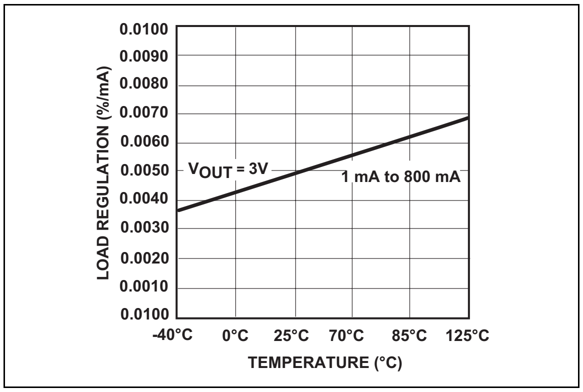


FIGURE 2-3: Load Regulation vs. Temperature.

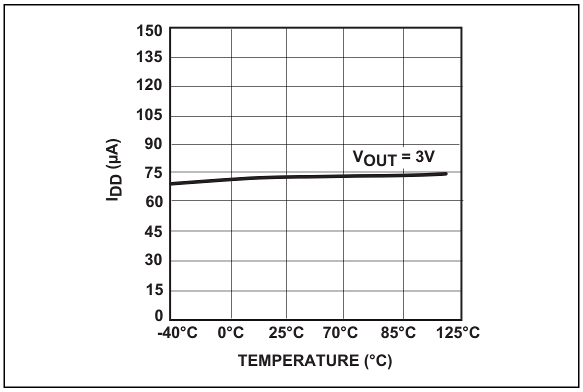


FIGURE 2-4: I_{DD} vs. Temperature.

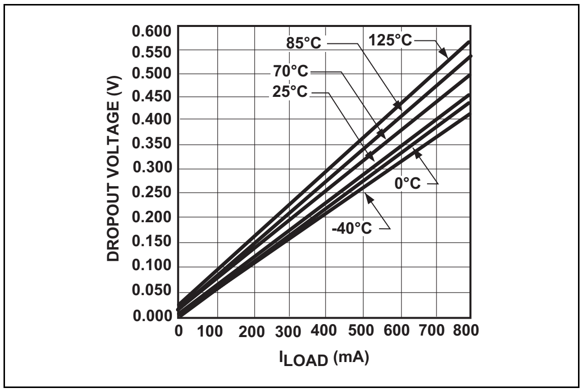


FIGURE 2-5: 3.0V Dropout Voltage vs. I_{LOAD}.

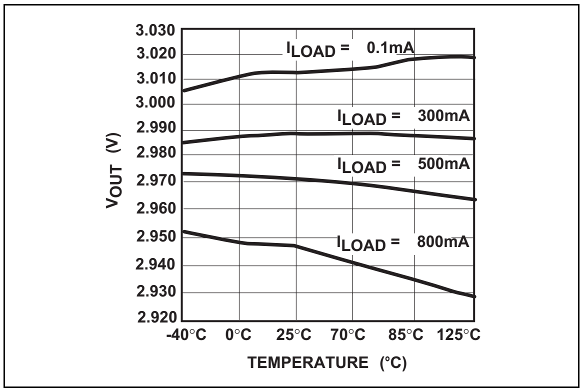


FIGURE 2-6: 3.0V V_{OUT} vs.Temperature.

2.0 TYPICAL PERFORMANCE CURVES (CONT)

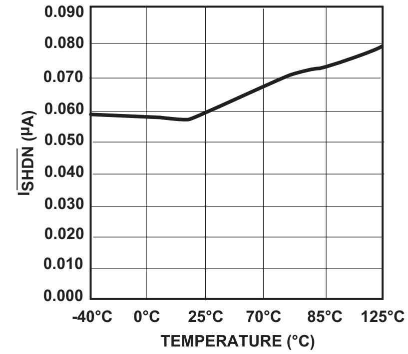


FIGURE 2-1: *$I_{\overline{SHDN}}$ vs. Temperature.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. (8-Pin SOIC)	Pin No. (5-Pin DDPAK) (5-Pin TO-220)	Symbol	Description
1	5	V_{OUT}	Regulated voltage output
2	3	GND	Ground terminal
3	—	NC	No connect
4	1	BYPASS	Reference bypass input
5	—	$\overline{\text{ERROR}}$	Out-of-Regulation Flag (open-drain output)
6	2	$\overline{\text{SHDN}}$	Shutdown control input
7	—	NC	No connect
8	4	V_{IN}	Unregulated supply input

3.1 Regulated Output Voltage (V_{OUT})

Regulated voltage output.

3.2 Ground (GND)

Ground terminal.

3.3 Reference Bypass (BYPASS)

Reference bypass input. Connecting a 470 pF to this input further reduces output noise.

3.4 Out-of-Regulation Flag ($\overline{\text{ERROR}}$)

Out-of-regulation flag (open-drain output). This output goes low when V_{OUT} is out-of-tolerance by approximately -5%.

3.5 Shutdown Control ($\overline{\text{SHDN}}$)

Shutdown control input. The regulator is fully enabled when a logic-high is applied to this input. The regulator enters shutdown when a logic-low is applied to this input. During shutdown, the output voltage falls to zero and the supply current is reduced to 0.05 µA (typical).

3.6 Unregulated Supply (V_{IN})

Unregulated supply input.

4.0 DETAILED DESCRIPTION

The TC1265 is a precision, fixed-output LDO. Unlike bipolar regulators, the TC1265's supply current does not increase with load current. In addition, V_{OUT} remains stable and within regulation over the entire 0 mA to $I_{LOADMAX}$ load current range (an important consideration in RTC and CMOS RAM battery back-up applications).

Figure 4-1 shows a typical application circuit.

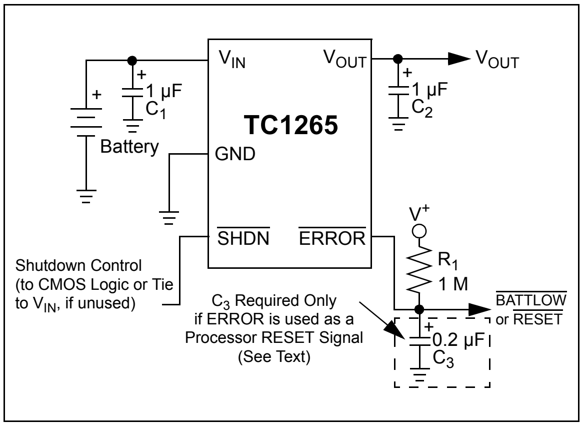


FIGURE 4-1: *Typical Application Circuit.*

4.1 Output Capacitor

A 1 µF (min.) capacitor from V_{OUT} to ground is required. The output capacitor should have an Effective Series Resistance (ESR) greater than 0.1Ω and less than 5Ω. A 1 µF capacitor should be connected from V_{IN} to GND if there is more than 10 inches of wire between the regulator and the AC filter capacitor, or if a battery is used as the power source. Aluminum electrolytic or tantalum capacitor types can be used. Since many aluminum electrolytic capacitors freeze at approximately -30°C, solid tantalums are recommended for applications operating below -25°C. When operating from sources other than batteries, supply-noise rejection and transient response can be improved by increasing the value of the input and output capacitors, and by employing passive filtering techniques.

4.2 $\overline{\text{ERROR}}$ Output

$\overline{\text{ERROR}}$ is driven low whenever V_{OUT} falls out of regulation by more than – 5% (typ.). This condition may be caused by low input voltage, output current limiting, or thermal limiting. The $\overline{\text{ERROR}}$ threshold is 5% below rated V_{OUT} regardless of the programmed output voltage value (e.g., $\overline{\text{ERROR}} = V_{OL}$ at 4.75V (typ.) for a 5.0V regulator and 2.85V (typ.) for a 3.0V regulator). $\overline{\text{ERROR}}$ output operation is shown in Figure 4-2.

Note that $\overline{\text{ERROR}}$ is active when V_{OUT} is at or below V_{TH} and inactive when V_{OUT} is above $V_{TH} + V_H$.

As shown in Figure 4-1, $\overline{\text{ERROR}}$ can be used as a battery low flag or as a processor $\overline{\text{RESET}}$ signal (with the addition of timing capacitor C_3). $R_1 \times C_3$ should be chosen to maintain $\overline{\text{ERROR}}$ below V_{IH} of the processor $\overline{\text{RESET}}$ input for at least 200 ms to allow time for the system to stabilize. Pull-up resistor R_1 can be tied to V_{OUT}, V_{IN} or any other voltage less than (V_{IN} + 0.3V).

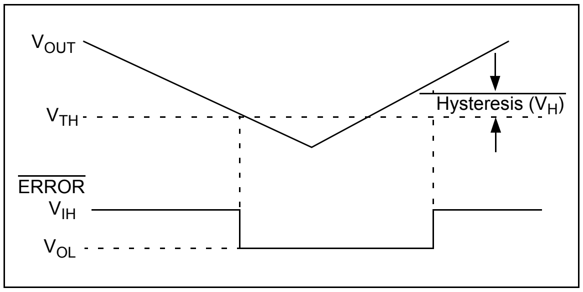


FIGURE 4-2: *$\overline{\text{ERROR}}$ Output Operation.*

5.0 THERMAL CONSIDERATIONS

5.1 Thermal Shutdown

Integrated thermal protection circuitry shuts the regulator off when die temperature exceeds 160°C. The regulator remains off until the die temperature drops to approximately 150°C.

5.2 Power Dissipation

The amount of power the regulator dissipates is primarily a function of input voltage, output voltage and output current. The following equation is used to calculate worst-case actual power dissipation:

EQUATION 5-1:

$$P_D = (V_{INMAX} - V_{OUTMIN})I_{LOADMAX}$$

Where:

P_D = Worst-case actual power dissipation
V_{INMAX} = Maximum voltage on V_{IN}
V_{OUTMIN} = Minimum regulator output voltage
$I_{LOADMAX}$ = Maximum output (load) current

The maximum allowable power dissipation (Equation 5-2) is a function of the maximum ambient temperature (T_{AMAX}), the maximum allowable die temperature (T_{JMAX}) and the thermal resistance from junction-to-air (θ_{JA}).

EQUATION 5-2:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

Where:

P_D = Worst-case actual power dissipation
V_{INMAX} = Maximum voltage on V_{IN}
V_{OUTMIN} = Minimum regulator output voltage
$I_{LOADMAX}$ = Maximum output (load) current

Table 5-1 and Table 5-2 show various values of θ_{JA} for the TC1265 package types.

TABLE 5-1: THERMAL RESISTANCE GUIDELINES FOR TC1265 IN 8-PIN SOIC PACKAGE

Copper Area (Topside)*	Copper Area (Backside)	Board Area	Thermal Resistance (θ_{JA})
2500 sq mm	2500 sq mm	2500 sq mm	60°C/W
1000 sq mm	2500 sq mm	2500 sq mm	60°C/W
225 sq mm	2500 sq mm	2500 sq mm	68°C/W
100 sq mm	2500 sq mm	2500 sq mm	74°C/W

* Pin 2 is ground. Device is mounted on the top-side.

TABLE 5-2: THERMAL RESISTANCE GUIDELINES FOR TC1265 IN 5-PIN DDPAK/TO-220 PACKAGE

Copper Area (Topside)*	Copper Area (Backside)	Board Area	Thermal Resistance (θ_{JA})
2500 sq mm	2500 sq mm	2500 sq mm	25°C/W
1000 sq mm	2500 sq mm	2500 sq mm	27°C/W
125 sq mm	2500 sq mm	2500 sq mm	35°C/W

* Tab of device attached to top-side copper

Equation 5-1 can be used in conjunction with Equation 5-2 to ensure regulator thermal operation is within limits. For example:

Given:

V_{INMAX} = 3.3V ± 10%
V_{OUTMIN} = 2.7V ± 0.5%
$I_{LOADMAX}$ = 275 mA
T_{JMAX} = 125°C
T_{AMAX} = 95°C
θ_{JA} = 60°C/W (SOIC)

Find:

1. Actual power dissipation
2. Maximum allowable dissipation

Actual power dissipation:

$$P_D \approx (V_{INMAX} - V_{OUTMIN})I_{LOADMAX}$$
$$P_D = (3.3 \times 1.1) - (2.7 \times .995)275 \times 10^{-3}$$
$$P_D = 260 \text{ mW}$$

Maximum allowable power dissipation:

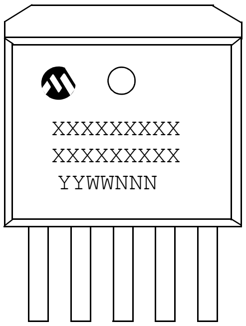
$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$
$$P_{DMAX} = \frac{(125 - 95)}{60}$$
$$P_{DMAX} = 500 \text{ mW}$$

In this example, the TC1265 dissipates a maximum of 260 mW, below the allowable limit of 500 mW. In a similar manner, Equation 5-1 and Equation 5-2 can be used to calculate maximum current and/or input voltage limits. For example, the maximum allowable V_{IN} is found by substituting the maximum allowable power dissipation of 500 mW into Equation 5-1, from which V_{INMAX} = 4.6V.

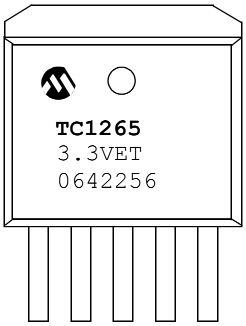
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

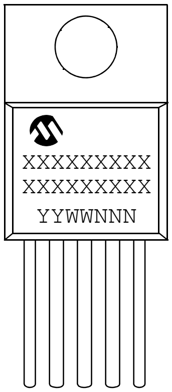
5-Lead DDPAK



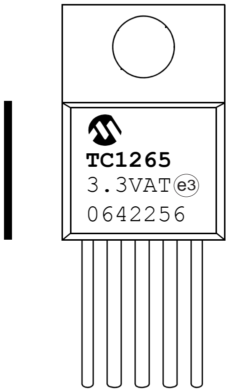
Example



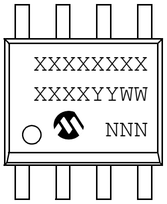
5-Lead TO-220



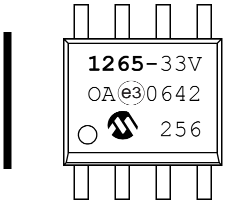
Example:



8-Lead SOIC (150 mil)



Example:

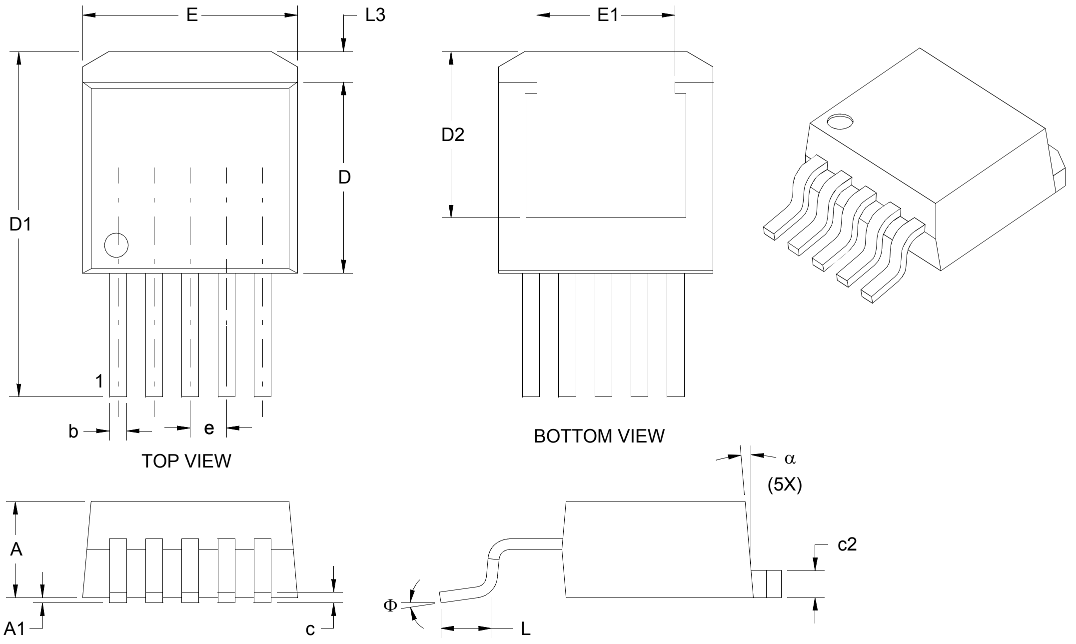


Legend:		
	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic (ET) (DDPAK))

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins			5			5	
Pitch	e	.067 BSC			1.70 BSC		
Overall Height	A	.170	.177	.183	4.32	4.50	4.65
Standoff §	A1	.000	.005	.010	0.00	0.13	0.25
Overall Width	E	.385	.398	.410	9.78	10.11	10.41
Exposed Pad Width	E1	.256 REF			6.50 REF		
Molded Package Length	D	.330	.350	.370	8.38	8.89	9.40
Overall Length	D1	.549	.577	.605	13.94	14.66	15.37
Exposed Pad Length	D2	.303 REF			7.75 REF		
Lead Thickness	c	.014	.020	.026	0.36	0.51	0.66
Pad Thickness	c2	.045	--	.055	1.14	--	1.40
Lead Width	b	.026	.032	.037	0.66	0.81	0.94
Foot Length	L	.068	.089	.110	1.73	2.26	2.79
Pad Length	L3	.045	--	.067	1.14	--	1.70
Foot Angle	Φ	--	--	8°	--	--	8°
Mold Draft Angle	α	3°	--	7°	3°	--	7°

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.
See ASME Y14.5M

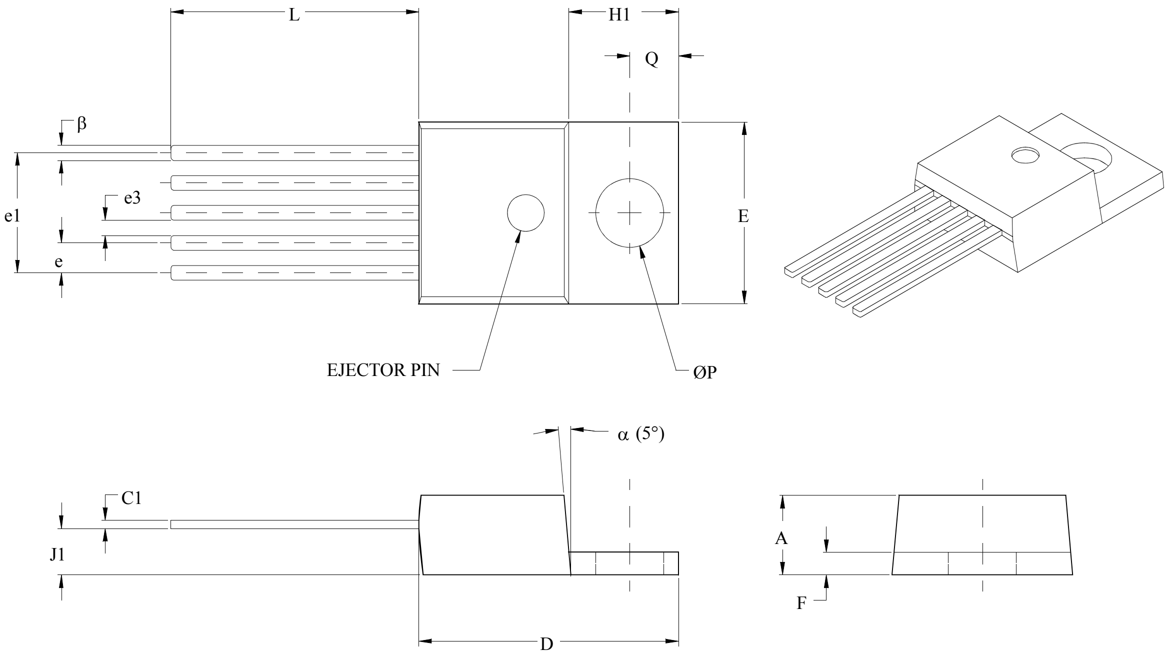
JEDEC equivalent: TO-252

Drawing No. C04-012

Revised 07-19-05

5-Lead Plastic Transistor Outline (AT) (TO-220)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*		MILLIMETERS	
Dimension Limits		MIN	MAX	MIN	MAX
Lead Pitch	e	.060	.072	1.52	1.83
Overall Lead Centers	e1	.263	.273	6.68	6.93
Space Between Leads	e3	.030	.040	0.76	1.02
Overall Height	A	.160	.190	4.06	4.83
Overall Width	E	.385	.415	9.78	10.54
Overall Length	D	.560	.590	14.22	14.99
Flag Length	H1	.234	.258	5.94	6.55
Flag Thickness	F	.045	.055	1.14	1.40
Through Hole Center	Q	.103	.113	2.62	2.87
Through Hole Diameter	P	.146	.156	3.71	3.96
Lead Length	L	.540	.560	13.72	14.22
Base to Bottom of Lead	J1	.090	.115	2.29	2.92
Lead Thickness	C1	.014	.022	0.36	0.56
Lead Width	β	.025	.040	0.64	1.02
Mold Draft Angle	α	3°	7°	3°	7°

* Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254 mm) per side.

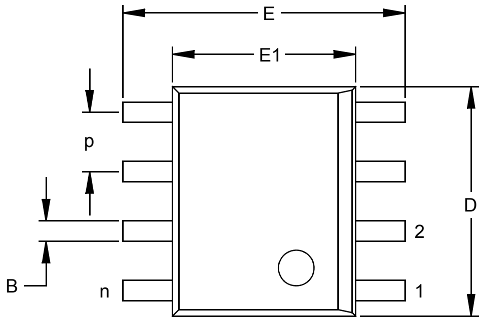
JEDEC equivalent: TO-220

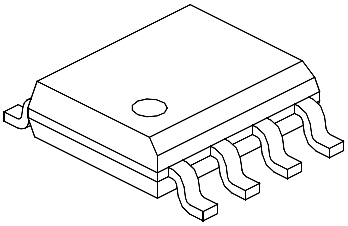
Drawing No. C04-036

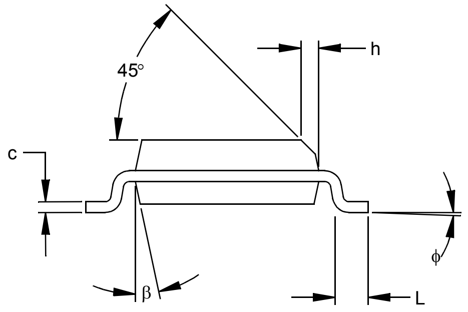
Revised 08-01-05

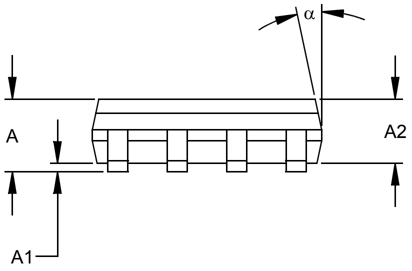
8-Lead Plastic Small Outline (SN) – Narrow, 150 mil Body (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

APPENDIX A: REVISION HISTORY

Revision D (October 2006)

- **Section 1.0 “Electrical Characteristics”**: Changed dropout voltage voltage typical value for I_L = 500 mA from 700 to 1000 and maximum value from 1000 to 1200 for. Changed typical value for I_L = 800 mA from 890 to 1200
- **Section 6.0 “Packaging Information”**: Added pb-free symbol to package marking information
- Added disclaimer to package outline drawings
- Updated package outline drawings as needed
- Added Appendix A - Revision History

Revision C (October 2004)

- Not Documented

Revision B (May 2002)

- Not Documented

Revision A (March 2002)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X.XX	XX	XX
Device	**Voltage Option**	**Package**	**Tape and Reel**

Device	TC1265 Fixed Output CMOS LDO with Shutdown
Voltage Option:*	1.8V = 1.8V 2.5V = 2.5V 3.0V = 3.0V 3.3V = 3.3V * Other output voltages are available. Please contact your local Microchip sales office for details.
Package	AT = Plastic (TO-220), 5-Lead ET = Plastic Transistor Outline (DDPAK), 5-Lead ETTR = Plastic Transistor Outline (DDPAK), 5-Lead, Tape and Reel OA = Plastic SOIC, (150 mil Body), 8-lead OATR = Plastic SOIC, (150 mil Body), 8-lead, Tape and Reel

Examples:

a)	TC1265-1.8VAT	1.8V LDO, TO-220-5 pkg.
b)	TC1265-2.5VAT	2.5V LDO, TO-220-5 pkg.
c)	TC1265-3.0VAT	3.0V LDO, TO-220-5 pkg.
d)	TC1265-3.3VAT	3.3V LDO, TO-220-5 pkg.
a)	TC1265-1.8VETTR	1.8V LDO, DDPAK-5 pkg., Tape and Reel
b)	TC1265-2.5VETTR	2.5V LDO, DDPAK-5 pkg., Tape and Reel
c)	TC1265-3.0VETTR	3.0V LDO, DDPAK-5 pkg., Tape and Reel
d)	TC1265-3.3VETTR	3.3V LDO, DDPAK-5 pkg., Tape and Reel
a)	TC1265-1.8VOA	1.8V LDO, SOIC-8 pkg.
b)	TC1265-1.8VOATR	1.8V LDO, SOIC-8 pkg., Tape and Reel
c)	TC1265-2.5VOA	2.5V LDO, SOIC-8 pkg.
d)	TC1265-2.5VOATR	2.5V LDO, SOIC-8 pkg., Tape and Reel
e)	TC1265-3.0VOA	3.0V LDO, SOIC-8 pkg.
f)	TC1265-3.0VOATR	3.0V LDO, SOIC-8 pkg., Tape and Reel
g)	TC1265-3.3VOA	3.3V LDO, SOIC-8 pkg.
h)	TC1265-3.3VOATR	3.3V LDO, SOIC-8 pkg., Tape and Reel

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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