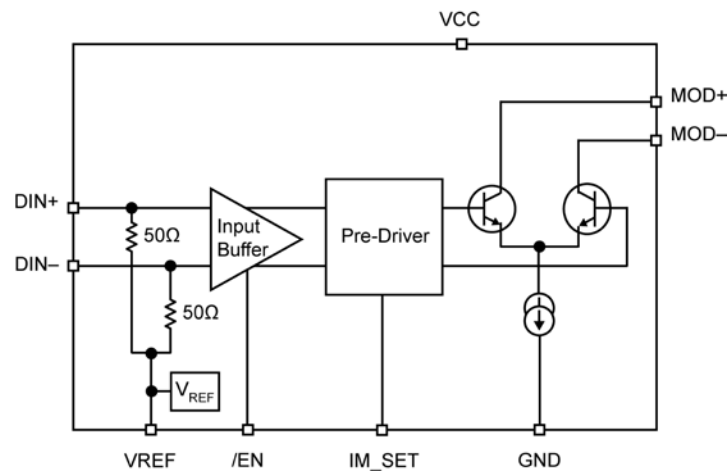


Functional Block Diagram

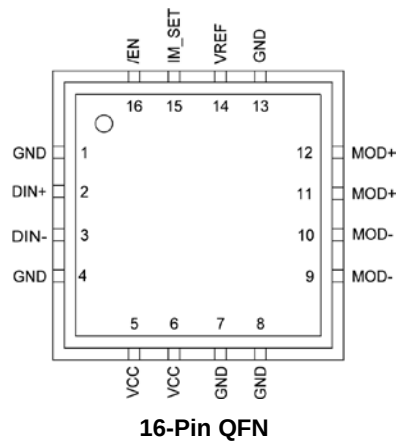


Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88982LMG	QFN-16	Industrial	982L with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY88982LMGTR ⁽²⁾	QFN-16	Industrial	982L with Pb-Free bar-line indicator	NiPdAu Pb-Free

- Notes:
- 1. Contact factory for die availability. Dice are guaranteed at T_A = +25°C, DC Electricals only.
 - 2. Tape and Reel.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Function
1, 4, 7, 8, 13	GND	Ground. Ground and exposed pad must be connected to the plane of the most negative potential.
2	DIN+	Non-Inverting Input Data. Internally terminated with 50Ω to a reference voltage.
3	DIN-	Inverting Input Data. Internally terminated with 50Ω to a reference voltage.
5, 6	VCC	Supply Voltage. Bypass with a 0.1μF//0.01μF low ESR capacitor as close to VCC pin as possible.
9, 10	MOD-	Inverted Modulation Current Output. Provides modulation current when input data is negative.
11, 12	MOD+	Non-Inverted Modulation Current Output. Provides modulation current when input data is positive.
14	VREF	Reference Voltage. Install a 0.1μF capacitor between VREF and VCC.
15	IM_SET	Modulation current setting and control. The voltage applied to this pin will set the modulation current. To be connected to the MIC3003 pin 24 (VMOD+). Input impedance 25kΩ.
16	/EN	A high level signal applied to this pin will disable the output stage of the driver. Internally pulled down with 25kΩ resistor.

Truth Table

DIN+	DIN-	/EN	MOD+ ⁽¹⁾	MOD-	Laser Output ⁽²⁾
L	H	L	H	L	L
H	L	L	L	H	H
X	X	H	H	H	L

Notes:

1. $I_{MOD} = 0$ when MOD+ = H.
2. Assuming that the laser is tied to MOD+.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{IN}) -0.5V to +4.0V
 CML Input Voltage (V_{IN}) $V_{CC}-1.2V$ to $V_{CC}+0.5V$
 TTL Control Input Voltage (V_{IN}) 0V to V_{CC}
 Lead Temperature (soldering, 20sec.) +260°C
 Storage Temperature (T_s) -65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{CC}) +3.0V to +3.6V
 Ambient Temperature (T_A) -40°C to +85°C
 Package Thermal Resistance⁽³⁾
 QFN
 (θ_{JA}) Still-air 60°C/W
 (ψ_{JB}) 33°C/W

DC Electrical Characteristics

$T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = +3.0V$ to $+3.6V$, unless otherwise noted. Typical values are $V_{CC} = +3.3V$, $T_A = 25^\circ\text{C}$, $I_{MOD} = 60\text{mA}$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	Modulation current excluded		48	65 ⁽⁴⁾	mA
V_{MOD_MIN}	Minimum Voltage Required at the Driver Output (headroom) for Proper Operation		0.6			V
$R_{IN(DATA)}$	Input Resistance (DIN+, DIN-)		45	50	55	Ω
V_{ID}	Differential Input Voltage Swing		200		2400	mV _{PP}
/EN Low					0.8	V
/EN High			2			V
$R_{IN(I_{MOD_SET})}$	I_{M_SET} Input Resistance			25		k Ω
V_{IM_SET}	Voltage Range on I_{M_SET} Pin	I_{MOD} range 10mA – 90mA			1.2	V

AC Electrical Characteristics

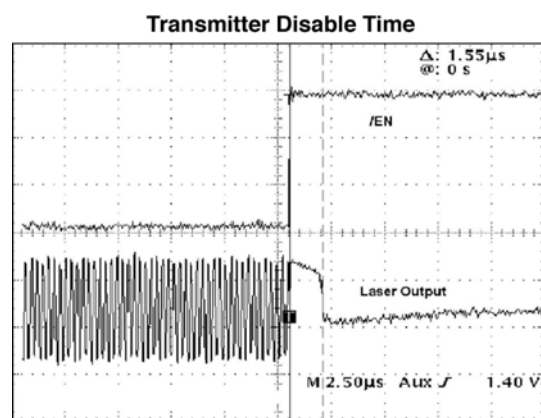
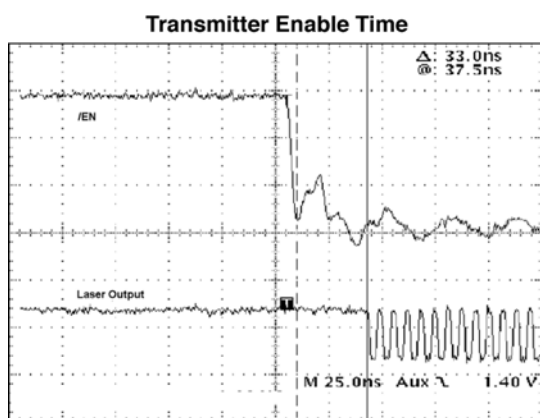
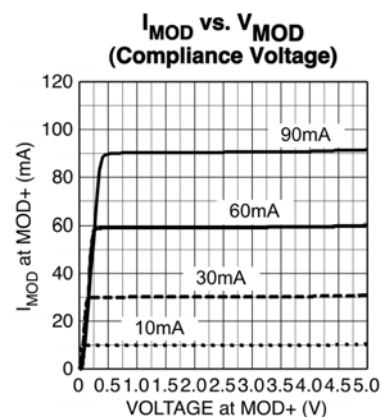
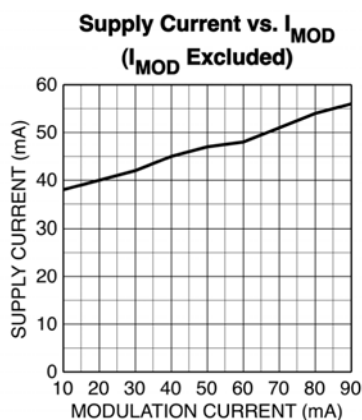
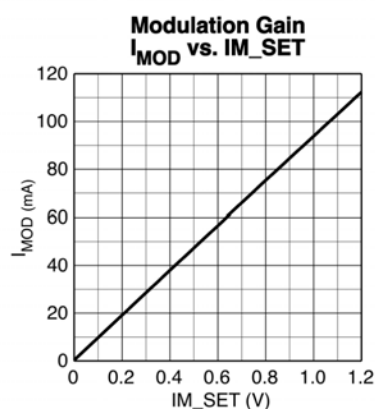
$T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = +3.0V$ to $+3.6V$, unless otherwise noted. Typical values are $V_{CC} = +3.3V$, $T_A = 25^\circ\text{C}$, $I_{MOD} = 60\text{mA}$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Data Rate	NRZ	0.155		2.7	Gbps
I_{MOD}	Modulation Current ⁽⁵⁾	AC-coupled	10		90	mA
		DC-coupled	10		70 ⁽⁶⁾	mA
I_{MOD_OFF}	Modulation OFF Current	Current at MOD+ when the device is disabled.			750	μA
t_r	Output Current Rise Time	20% to 80%, $I_{MOD} = 60\text{mA}$, 15 Ω load		55	80	ps
t_f	Output Current Fall Time	20% to 80%, $I_{MOD} = 60\text{mA}$, 15 Ω load		55	80	ps
	Total Jitter	@2.5Gbps data rate			20	ps _{PP}
	Pulse-Width Distortion	I_{MOD} range 10mA – 90mA			20	ps

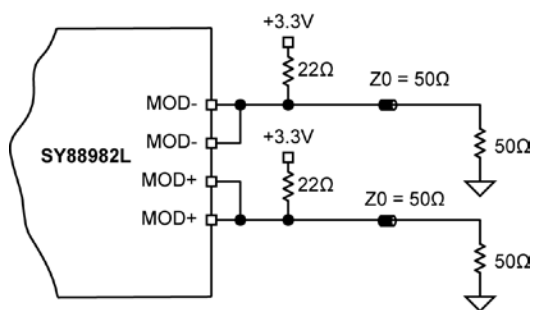
Notes:

- Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
- The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
- Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. ψ_{JB} uses a 4-layer and θ_{JA} in still air unless otherwise stated.
- $I_{CC} = 48\text{mA}$ for worst-case conditions with $I_{MOD} = 90\text{mA}$, $T_A = +85^\circ\text{C}$, $V_{CC} = 3.6$.
- Load = 15 Ω .
- Assuming $V_{CC} = 3.0V$, Laser bandgap voltage = 1V, laser package inductance = 1nH, laser equivalent series resistor = 5 Ω , and damping resistor = 10 Ω .

Typical Operating Characteristics

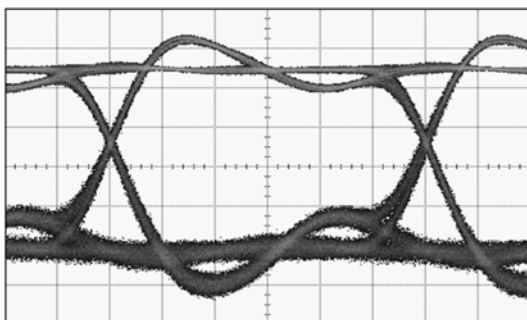


Test Circuit



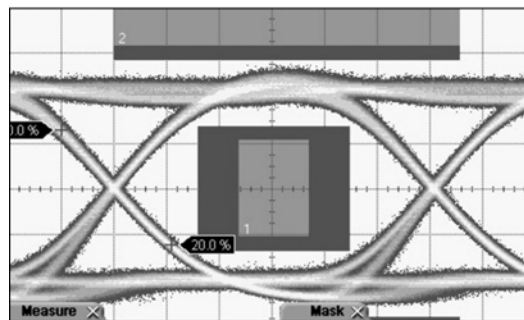
Functional Characteristics

Electrical Eye Diagram
2.5Gbps, PRBS 2²³-1, 15Ω Load, 60mA Modulation



TIME (66ps/div.)

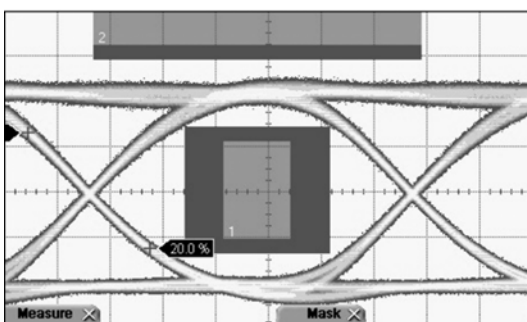
Optical Eye Diagram
2.7Gbps, PRBS 2²³-1, Laser AC-Coupled



TIME (66ps/div.)

ER = 10dB, 30% Mask Margin

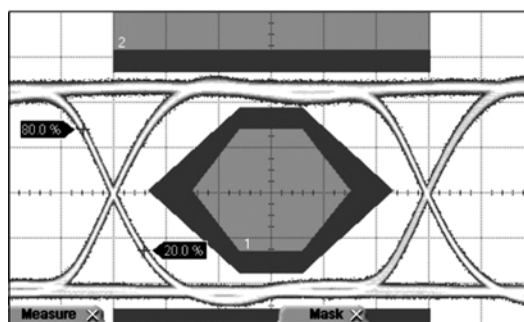
Optical Eye Diagram
2.5Gbps, PRBS 2²³-1, Laser DC-Coupled



TIME (65ps/div.)

ER = 11dB, 30% Mask Margin

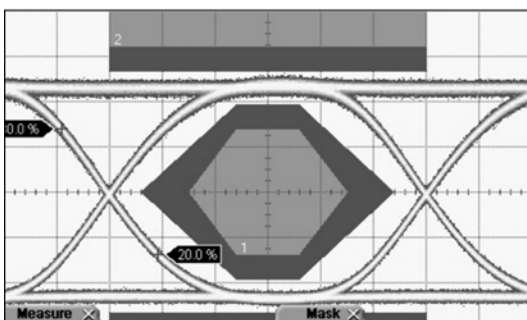
Optical Eye Diagram with OC-48 Filter
1.25Gbps, PRBS 2²³-1, Laser DC-Coupled



TIME (133ps/div.)

ER = 11dB, 55% Mask Margin

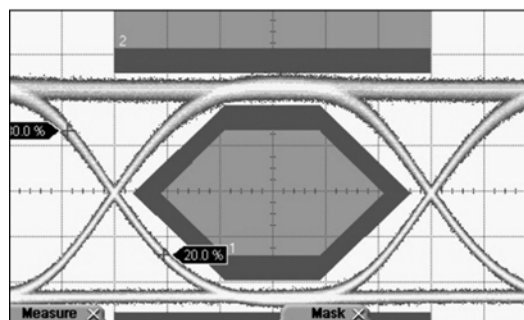
Optical Eye Diagram
622Mbps, PRBS 2²³-1, Laser DC-Coupled



TIME (267ps/div.)

ER = 11.3dB, 60% Mask Margin

Optical Eye Diagram
155Mbps, PRBS 2²³-1, Laser DC-Coupled



TIME (1075ps/div.)

ER = 11.3dB, 60% Mask Margin

Input and Output Stages

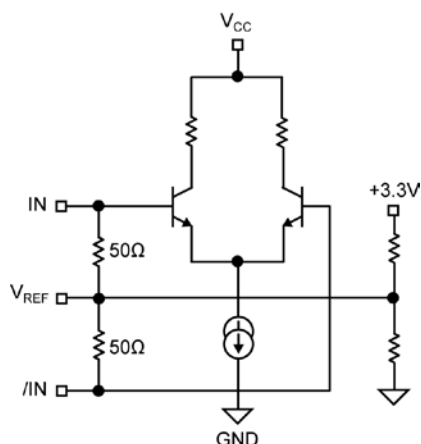


Figure 1a. Simplified Input Stage

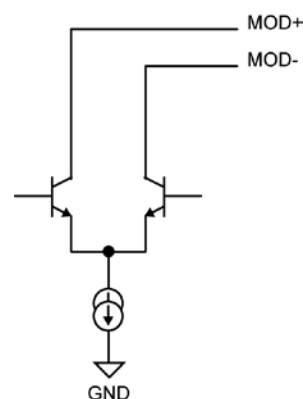


Figure 1b. Simplified Output Stage

Interfacing the Input to Different Logic Drivers

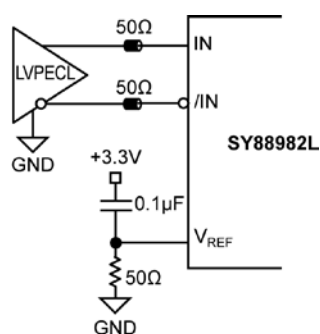


Figure 2a. DC-Coupling to LVPECL Driver

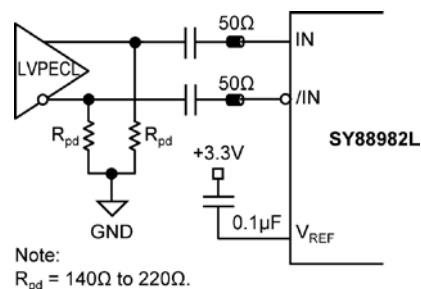


Figure 2b. AC-Coupling to LVPECL Driver

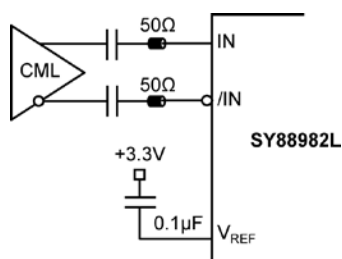


Figure 2c. AC-Coupling to CML Driver

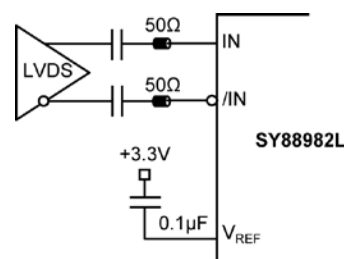


Figure 2d. AC-Coupling to LVDS Driver

Application Information

The typical applications diagram on the first page shows how to connect the driver to the laser, single ended. To improve transition time and laser response, the laser can be driven differentially as shown in Figures 3 and 4. Driving the laser differentially will also minimize the crosstalk with the rest of the circuitry on the board, especially the receiver.

DC-Coupling

In addition to the low power consumption and high modulation current, the SY88982L offers a high compliance voltage. As can be seen in the "Typical Operating Characteristics" section (I_{MOD} vs. V_{MOD} curves), the minimum voltage needed at the output of the driver for proper operation is less than 600mV, leaving a large headroom, V_{CC} -600mV, to the laser with the damping resistor. To show the importance of this high compliance voltage, consider the voltage drops along the path from V_{CC} to ground through the laser, damping resistor, and driver:

$$V_{CC} = \text{Driver Headroom} + V_{Rd} + V_{laser}$$

$$V_{Rd} = R_d \times I_{MOD}$$

$$V_{laser} = V_{band-gap} + R_{laser} \times I_{MOD} + L di/dt$$

$$V_{band-gap} + R_{laser} \times I_{MOD} = 1.6V \text{ at maximum for a Fabry Perrot or a DFB laser.}$$

$L di/dt$ is the voltage drop due to the laser parasitic inductance during I_{MOD} transitions. Assuming $L = 1nH$, $t_f = t_r = 80ps$ (measured between 20% and 80% of I_{MOD}), and $I_{MOD} = 70mA$ (42mA from 20% to 80%), then $L di/dt$ will be equal to 525mV. This number can be minimized by making the laser leads as short as possible and using an RC compensation network between the cathode of the laser and ground or across the laser driver outputs as shown in Figure 3.

To be able to drive the laser DC-coupled with a high current, it is necessary to keep the damping resistor as small as possible. For example, if the drop due to parasitic inductance of the laser is neglected (compensated for) and the maximum drop across the laser (1.6V) considered while keeping a minimum of 600mV headroom for the driver, then the maximum damping resistor that allows a 70mA modulation current into the laser is:

$$R_{dmax} = (V_{CC} - 0.6V - 1.6V) / 0.07A$$

The worst case will be with $V_{CC} = 3.0V$, leading to $R_{dmax} = 11.4\Omega$

On the other hand, the smaller is the value of R_d , the higher is the overshoot/undershoot on the optical signal from the laser. In the circuit shown in Figure 3, the RC compensation network across the driver

outputs (MOD+ and MOD-) allows the user $R_d = 10\Omega$. The optical eye diagrams at data rates of 155Mbps/622Mbps/1.25Gbps/2.5Gbps, shown in "Functional Characteristics" section, are all obtained with the same circuit using $R_d = 10\Omega$, $R_{Comp} = 100\Omega$, and $C_{Comp} = 3pF$. The compensation network may change from one board to another and from one type of laser to another. An additional compensation network (RC) can be added at the laser cathode for further compensation and eye smoothing.

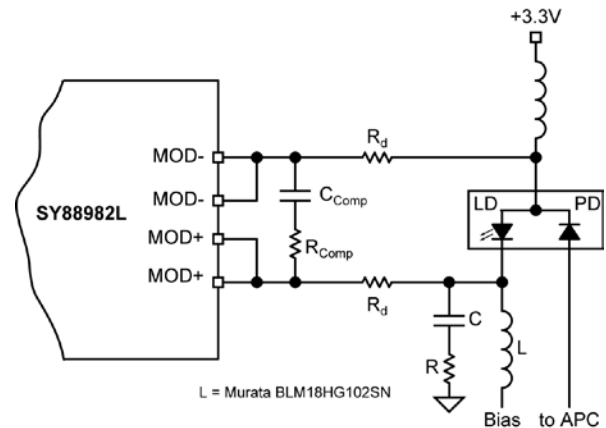


Figure 3. Laser DC-Coupled

AC-Coupling

When trying to AC couple the laser to the driver, the headroom of the driver is no longer a problem since it is DC isolated from the laser with the coupling capacitor. At the output, the headroom of the driver is determined by the pull-up network. In Figure 4, the modulation current out of the driver is split between the pull-up network and the laser. If, for example, the total pull-up resistor is twice the sum of the damping resistor and laser equivalent series resistance, only two thirds (2/3) of the modulation current will be used by the laser. So, to keep most of the modulation current going through the laser, the total pull-up resistor must be kept as high as possible. One solution consists in using an inductor alone as pull-up, presenting a high impedance path for the modulation current and zero ohm (Ω) path for the DC current offering a headroom of the driver equal to V_{CC} and almost all the modulation current goes into the laser. The inductor alone will cause signal distortion, and, to improve that, a combination of resistors and inductors can be used (as shown on Figure 4). In this case, the headroom of the driver is $V_{CC} - R_1 \times \alpha I_{MOD}$, where αI_{MOD} is the portion of the modulation current that goes through the pull-up network.

When the laser is AC-coupled to the driver, the coupling capacitor creates a low-frequency cutoff in the circuit, and its value must be chosen as large as

possible. If the value of the cap is too high, it will slow down the fast signals edges, and, if its value is too small, it won't be able to hold a constant change between the first bit and the last bit of a long string of identical bits in a low data rate application. This leads to higher pattern-dependent jitter in the transmitter signal. 0.1 μ F is found to be good for all applications from 155Mbps to 2.7Gbps.

AC-coupling the laser to the driver brings a solution to the driver headroom problem at the expense of extra components, loss of part of the modulation current wasted in the pull-up network, and additional power consumption.

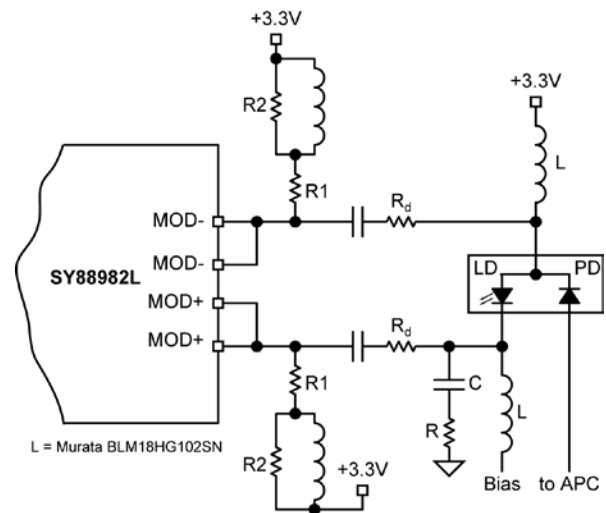
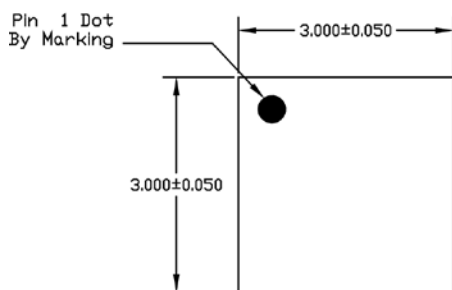
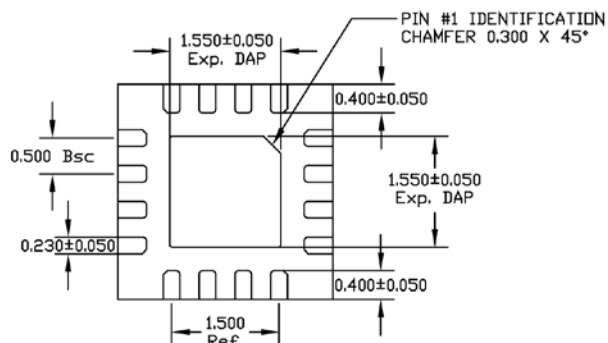


Figure 4. Laser AC-Coupled

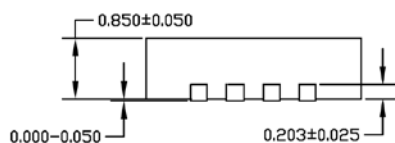
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

16-Pin (3mm x 3mm) QFN

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