

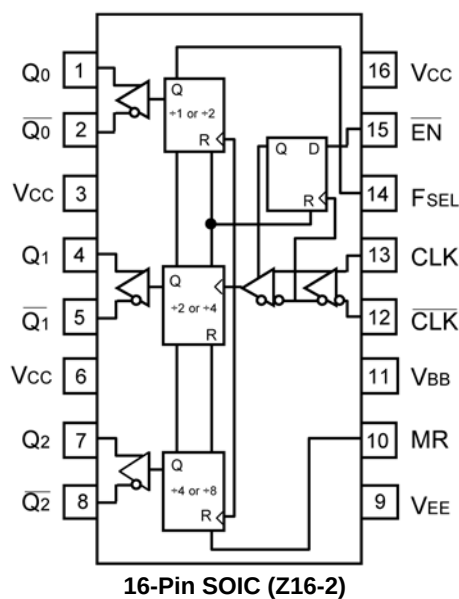
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S834ZC	Z16-2	Commercial	SY100S834ZC	Sn-Pb
SY100S834ZCTR ⁽¹⁾	Z16-2	Commercial	SY100S834ZC	Sn-Pb
SY100S834LZC	Z16-2	Commercial	SY100S834LZC	Sn-Pb
SY100S834LZCTR ⁽¹⁾	Z16-2	Commercial	SY100S834LZC	Sn-Pb
SY100S834ZI	Z16-2	Industrial	SY100S834ZI	Sn-Pb
SY100S834ZITR ⁽¹⁾	Z16-2	Industrial	SY100S834ZI	Sn-Pb
SY100S834LZI	Z16-2	Industrial	SY100S834LZI	Sn-Pb
SY100S834LZITR ⁽¹⁾	Z16-2	Industrial	SY100S834LZI	Sn-Pb
SY100S834ZG ⁽²⁾	Z16-2	Industrial	SY100S834ZG with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100S834ZGTR ^(1, 2)	Z16-2	Industrial	SY100S834ZG with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100S834LZG ⁽²⁾	Z16-2	Industrial	SY100S834LZG with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100S834LZGTR ^(1, 2)	Z16-2	Industrial	SY100S834LZG with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Tape and reel.
2. Pb-Free package is recommended for new designs.

Pin Configuration



Pin Description

Pin Name	Pin Function
CLK	Differential clock inputs.
F _{SEL}	Function select, single-sided ECL logic.
$\overline{\text{EN}}$	Synchronous enable, single-sided ECL logic.
MR	Master reset, single-sided ECL logic.
V _{BB}	Reference output.
Q0	Differential $\div 1$ or $\div 2$ outputs.
Q1	Differential $\div 2$ or $\div 4$ outputs.
Q2	Differential $\div 4$ or $\div 8$ outputs.

3.3V PECL Output DC Electrical Characteristics⁽¹⁾

V_{CC} = 3.3V $\pm 10\%$; R_L = 50 Ω to V_{CC} -2V; V_{EE} = GND.

Symbol	Parameter	T _A = -40°C			T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I _{EE}	Power Supply Current	–	–	49	–	–	49	–	–	49	–	–	54	mA
V _{CH}	Output HIGH Voltage	2.215	2.295	2.42	2.275	2.235	2.42	2.275	2.345	2.42	2.275	2.345	2.42	V
V _{OL}	Output LOW Voltage	1.47	1.605	1.745	1.49	1.595	1.68	1.49	1.595	1.68	1.49	1.595	1.68	V
V _{IH}	Input HIGH Voltage	2.135	–	2.42	2.135	–	2.42	2.135	–	2.42	2.135	–	2.42	V
V _{IL}	Input LOW Voltage	1.49	–	1.825	1.49	–	1.825	1.49	–	1.825	1.49	–	1.825	V
V _{BB}	Output Reference Voltage	1.92	–	2.04	1.92	–	2.04	1.92	–	2.04	1.92	–	2.04	V
V _{CMR}	Common Mode Range ⁽²⁾	2	–	2.9	1.9	–	2.9	1.9	–	2.9	1.9	–	2.9	V
I _{IH}	Input HIGH Current	–	–	150	–	–	150	–	–	150	–	–	150	μ A
I _{IL}	Input LOW Current	0.5	–	–	0.5	–	–	0.5	–	–	0.5	–	–	μ A

Notes:

- These values are for V_{CC} = 3.3V. Level specifications will vary 1:1 with V_{CC}.
- The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} (min.) and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. Note for PECL operation that the V_{CMR} (min.) will be fixed at 3.3V – IV_{CMR} (min.)].

5V PECL Output DC Electrical Characteristics⁽²⁾

$V_{CC} = 3.3V \pm 10\%$; $R_L = 50\Omega$ to $V_{CC} - 2V$; $V_{EE} = GND$.

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = 0^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	–	–	49	–	–	49	–	–	49	–	–	54	mA
V_{CH}	Output HIGH Voltage	3.915	3.995	4.12	3.975	4.045	4.12	3.975	4.045	4.12	3.975	4.045	4.12	V
V_{OL}	Output LOW Voltage	3.17	3.305	3.445	3.19	3.295	3.38	3.19	3.295	3.38	3.19	3.295	3.38	V
V_{IH}	Input HIGH Voltage	3.835	–	4.12	3.835	–	4.12	3.835	–	4.12	3.835	–	4.12	V
V_{IL}	Input LOW Voltage	3.19	–	3.525	3.19	–	3.525	3.19	–	3.525	3.19	–	3.525	V
V_{BB}	Output Reference Voltage	3.62	–	3.74	3.62	–	3.74	3.62	–	3.74	3.62	–	3.74	V
V_{CMR}	Common Mode Range ⁽²⁾	2	–	4.6	1.9	–	4.6	1.9	–	4.6	1.9	–	4.6	V
I_{IH}	Input HIGH Current	–	–	150	–	–	150	–	–	150	–	–	150	μA
I_{IL}	Input LOW Current	0.5	–	–	0.5	–	–	0.5	–	–	0.5	–	–	μA

Notes:

1. These values are for $V_{CC} = 5V$. Level specifications will vary 1:1 with V_{CC} .
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} (min.) and 1V. The lower end of the CMR range varies 1:1 with V_{EE} . Note for PECL operation that the V_{CMR} (min.) will be fixed at $3.3V - IV_{CMR}$ (min.)].

NECL Output DC Electrical Characteristics

$V_{CC} = \text{GND}$; $R_L = 50\Omega$ to $V_{CC} - 2V$; $V_{EE} = -3.0V$ to $-5.5V$.

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	–	–	49	–	–	49	–	–	49	–	–	54	mA
V_{CH}	Output HIGH Voltage	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	–1025	–955	–880	V
V_{OL}	Output LOW Voltage	–1830	–1695	–1555	–1830	–1705	–1620	–1810	–1705	–1620	–1810	–1705	–1620	V
V_{IH}	Input HIGH Voltage	–1165	–	–880	–1165	–	–880	–1165	–	–880	–1165	–	–880	V
V_{IL}	Input LOW Voltage	–1810	–	–1475	–1810	–	–1475	–1810	–	–1475	–1810	–	–1475	V
V_{BB}	Output Reference Voltage	–1.38	–	–1.26	–1.38	–	–1.26	–1.38	–	–1.26	–1.38	–	–1.26	V
V_{CMR}	Common Mode Range ⁽¹⁾	–1.3	–	–0.4	–1.4	–	–0.4	–1.4	–	–0.4	–1.4	–	–0.4	V
I_{IH}	Input HIGH Current	–	–	150	–	–	150	–	–	150	–	–	150	μA
I_{IL}	Input LOW Current	0.5	–	–	0.5	–	–	0.5	–	–	0.5	–	–	μA

Note:

1. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} (min.) and 1V. The lower end of the CMR range varies 1:1 with V_{EE} . The numbers in the spec table assume a nominal $V_{EE} = -3.3V$. Note for PECL operation, the V_{CMR} (min.) will be fixed at $3.3V - IV_{CMR}$ (min.) I_L .

AC Electrical Characteristics⁽¹⁾

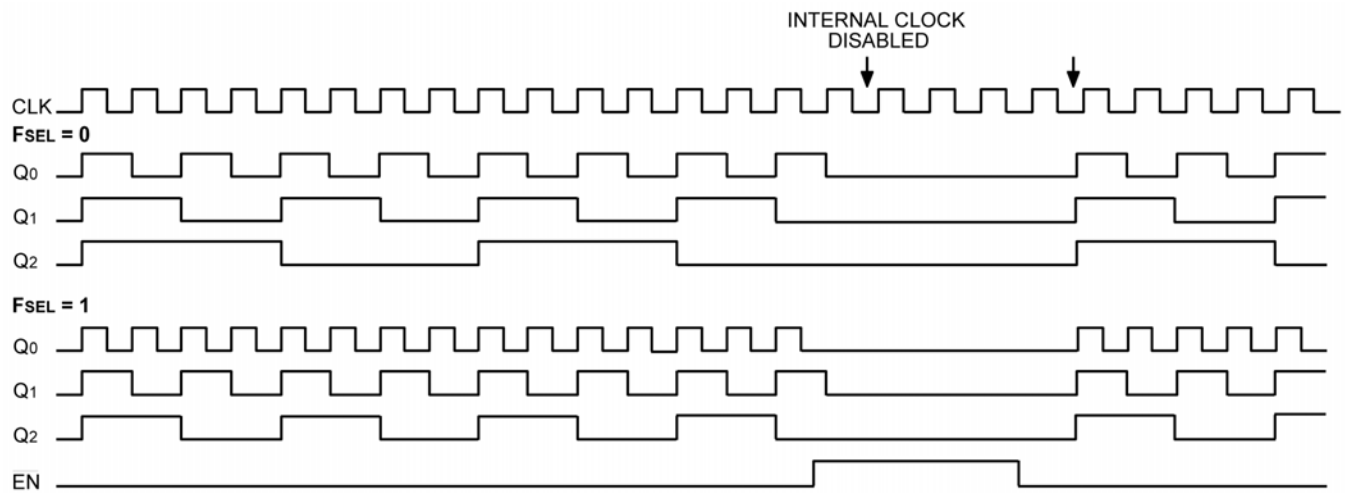
$V_{EE} = V_{EE} \text{ (min.) to } V_{EE} \text{ (max.)}; V_{CC} = \text{GND.}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation Delay to Output CLK	960	1100	1200	960	1100	1200	960	1100	1200	960	1100	1200	ps
t_{PHL}	MR	650	800	1010	650	800	1010	650	800	1010	650	800	1010	ps
t_{SKEW}	Within-Device Skew ⁽²⁾	–	–	50	–	–	50	–	–	50	–	–	50	ps
t_S	Set-Up Time $\overline{\text{EN}}$	400	–	–	400	–	–	400	–	–	400	–	–	ps
t_H	Hold Time $\overline{\text{EN}}$	200	–	–	200	–	–	200	–	–	200	–	–	ps
V_{PP}	Minimum Input Swing	250	–	–	250	–	–	250	–	–	250	–	–	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	275	400	525	275	400	525	275	400	525	275	400	525	ps

Notes:

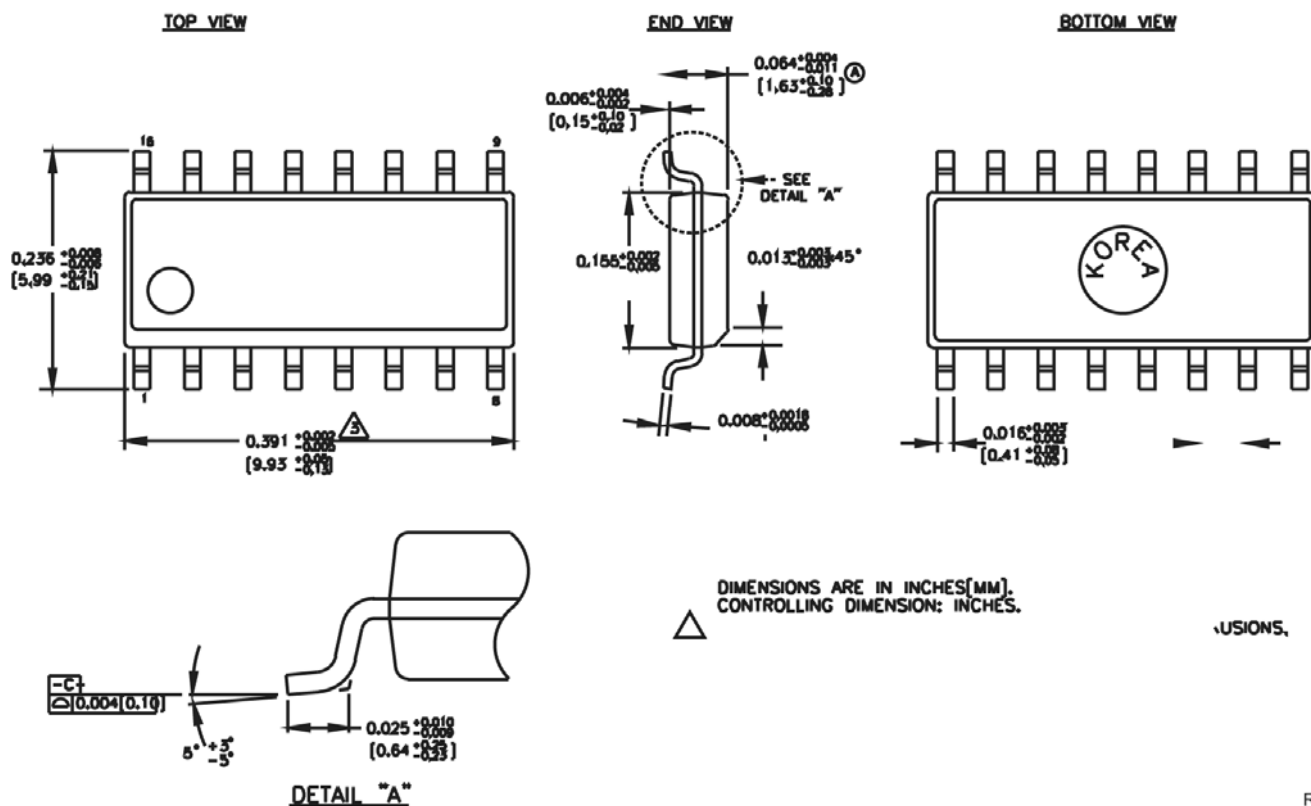
- Parametric values specified at:
 - 5V power supply range, 100S834 series: –4.2V to –5.5V
 - 3V power supply range, 100S834L series: –3.0V to –3.8V
- Within-Device Skew is specified for identical transition.

Timing Diagram



The $\overline{\text{EN}}$ signal will freeze the internal clocks to the flip-flops on the first falling edge of CLK after its assertion. The internal dividers will maintain their state during the internal clock freeze and will return to clocking once the internal clocks are unfrozen. The outputs will transition to their next states in the same manner, time, and relationship as they would have had the $\overline{\text{EN}}$ signal not been asserted.

Package Information



Rev. 02

xx-Pin Package Type (code)

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