1 Electrical ratings

Symbol	Parameter	Value		Unit
		TO-220/D ² PAK/I ² PAK	TO-220FP	
V _{GS}	Gate-Source Voltage	± 30		V
I _D	Drain Current (continuous) at T _C = 25°C	20	20 (<i>Note</i> 3)	Α
I _D	Drain Current (continuous) at T _C = 100°C	12.6	12.6 (<i>Note</i> 3)	А
I _{DM} Note 2	Drain Current (pulsed)	80	80 (<i>Note</i> 3)	Α
P _{TOT}	Total Dissipation at $T_{C} = 25^{\circ}C$	192	45	W
	Derating Factor	1.2	0.36	W/°C
dv/dt Note 1	Peak Diode Recovery voltage slope	15		V/ns
V _{ISO}	Insulation Withstand Volatge (DC)		2000	V
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-65 to 1	50	°C

Table 1. Absolute maximum ratings

Table 2.Thermal data

		TO-220/D ² PAK/I ² PAK	TO-220FP	Unit
Rthj-case	Thermal Resistance Junction-case Max	0.65	2.8	°C/W
Rthj-amb	Thermal Resistance Junction-amb Max	62.5		°C/W
Т	Maximum Lead Temperature For Soldering Purpose	300		°C

Table 3. Avalanche characteristics

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, repetitive or Not-Repetitive (pulse width limited by Tj max)	10	А
E _{AS}	Single Pulse Avalanche Energy (starting Tj=25°C, I _D =5A, V _{DD} = 50V)	650	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = 250μA, V _{GS} = 0	500			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating, V _{DS} = Max Rating,Tc = 125°C			1 10	μΑ μΑ
I _{GSS}	Gate Body Leakage Current (V _{DS} = 0)	V _{GS} = ±30V			±100	μΑ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	4	5	V
R _{DS(on)}	Static Drain-Source On Resistance	V _{GS} = 10 V, I _D = 10 A		0.20	0.25	Ω

Table 5. Dynamic

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} Note 4	Forward Transconductance	$V_{DS} > I_{D(ON)} \times R_{DS(ON)max,}$ $I_{D} = 10A$		10		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} =25V, f=1 MHz, V _{GS} =0		1480 285 34		pF pF pF
C _{oss eq.} Note 5	Equivalent Ouput Capacitance	V_{GS} =0, V_{DS} =0V to 400V		130		pF
Rg	Gate Input Resistance	f=1MHz Gate DC Bias=0 Test Signal Level=20mV Open Drain		1.6		Ω
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} =400V, I _D = 20A V _{GS} =10V (see Figure 15)		40 13 19	56	nC nC nC



Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	V_{DD} =250 V, I _D =10A, R _G =4.7 Ω , V _{GS} =10V (see Figure 16)		24 16		ns ns
t _{r(Voff)} t _f t _c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} =400 V, I _D =20A, R _G =4.7 Ω , V _{GS} =10V (see Figure 16)		9 8.5 23		ns ns ns

Table 6. Switching times

Table 7.Source drain diode

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} Note 2	Source-drain Current Source-drain Current (pulsed)				20 80	A A
V _{SD} Note 4	Forward on Voltage	I _{SD} =20A, V _{GS} =0			1.5	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} =20A, di/dt = 100A/µs, V _{DD} =100 V, Tj=25°C		350 4.6 26		ns µC A
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} =20A, di/dt = 100A/µs, V _{DD} =100 V, Tj=150°C		435 5.9 27		ns µC A

(1) I_{SD} \leq\!\!20A, di/dt \leq\!\!400A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_j \leq T_{JMAX}

(2) Pulse width limited by safe operating area

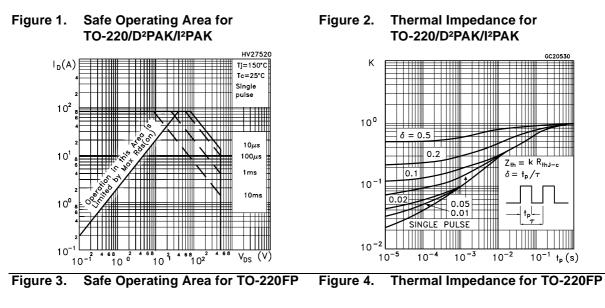
(3) Limited only by maximum temperature allowed

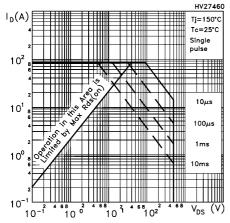
(4) Pulsed: pulse duration = 300μ s, duty cycle 1.5%

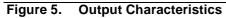
(5) $C_{oss eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

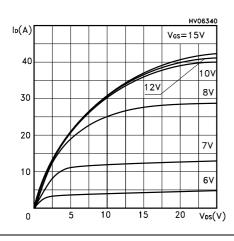


2.1 Electrical Characteristics (curves)









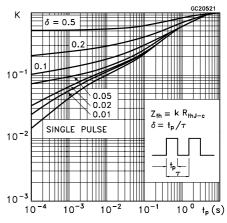
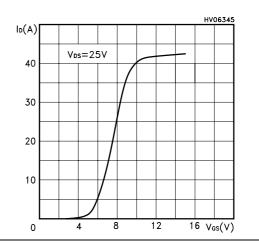


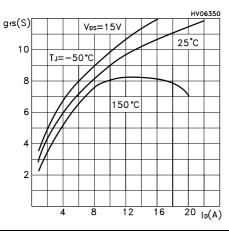
Figure 6. Transfer Characteristics

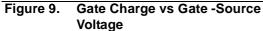


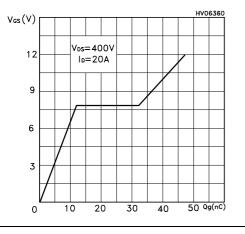
57

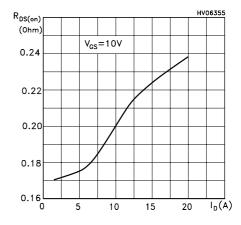
Figure 8.

Figure 7. Transconductance









Static Drain-Source on Resistance

Figure 11. Capacitance Variations

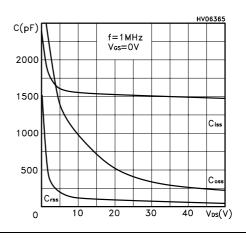
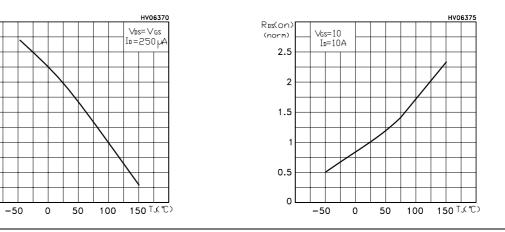


Figure 10. Normalized Gate Threshold Voltage Figure 12. Normalized on Resistance vs vs Temperatute Temperature



VGS(th) (norm)

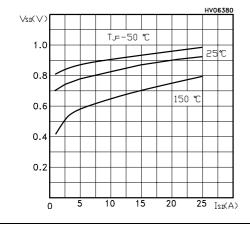
1.1

0.9

0.8

0.7

Figure 13. Source-drain Diode Forward Characteristics





3 Test circuits

Figure 14. Switching Times Test Circuit For Resistive Load

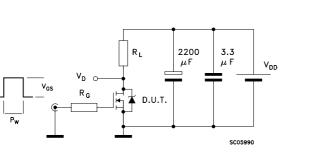


Figure 16. Test Circuit For Indictive Load Switching and Diode Recovery Times

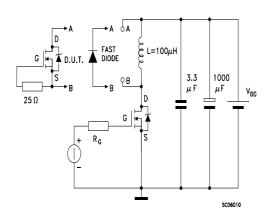


Figure 17. Unclamped Inductive Waveform

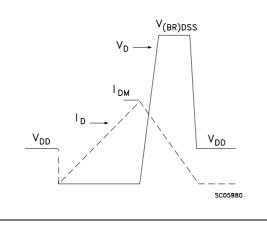
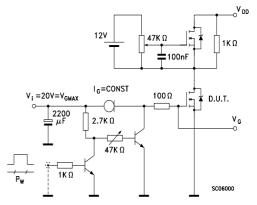
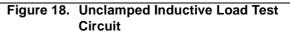
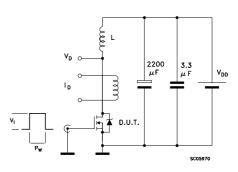




Figure 15. Gate Charge Test Circuit







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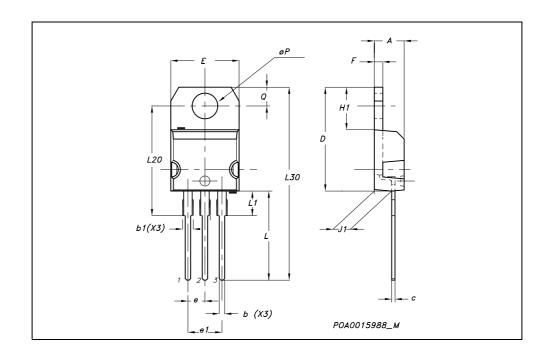
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com



DIM.		mm.		inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX
А	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
С	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
е	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	1
øP	3.75		3.85	0.147	İ	0.151
Q	2.65		2.95	0.104		0.116

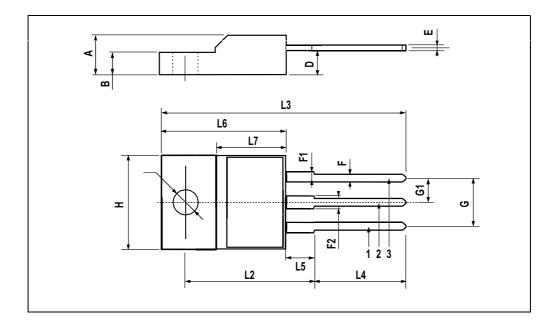




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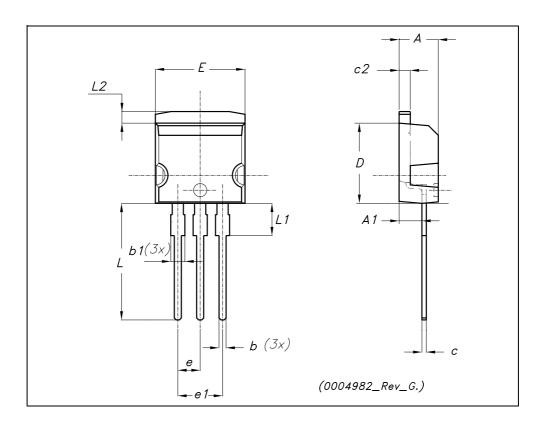
DIM.		mm.			inch	
	MIN.	TYP	MAX.	MIN.	TYP.	MAX
А	4.4		4.6	0.173		0.181
В	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
Е	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
Н	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126

TO-220FP MECHANICAL DATA



DIM.		mm.		inch		
DINI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
С	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
е	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055

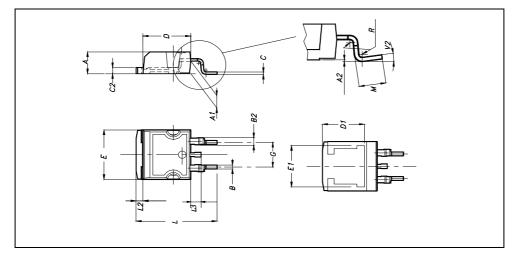




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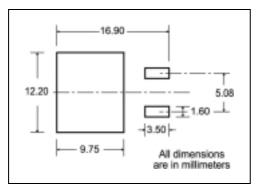
DIM		mm.		inch			
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.	
А	4.4		4.6	0.173		0.181	
A1	2.49		2.69	0.098		0.106	
A2	0.03		0.23	0.001		0.009	
В	0.7		0.93	0.027		0.036	
B2	1.14		1.7	0.044		0.067	
С	0.45		0.6	0.017		0.023	
C2	1.23		1.36	0.048		0.053	
D	8.95		9.35	0.352		0.368	
D1		8			0.315		
E	10		10.4	0.393			
E1		8.5			0.334		
G	4.88		5.28	0.192		0.208	
L	15		15.85	0.590		0.625	
L2	1.27		1.4	0.050		0.055	
L3	1.4		1.75	0.055		0.068	
М	2.4		3.2	0.094		0.126	
R		0.4			0.015		
V2	0°		4°				

D²PAK MECHANICAL DATA



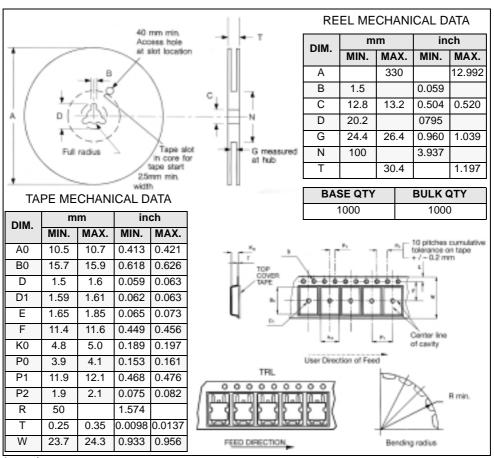


5 Packing mechanical data



D²PAK FOOTPRINT

TAPE AND REEL SHIPMENT



* on sales type

6 Revision History

Date	Revision	Changes
05-Sep-2005	2	Inserted Ecopack indication



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