Figure 2. Block diagram

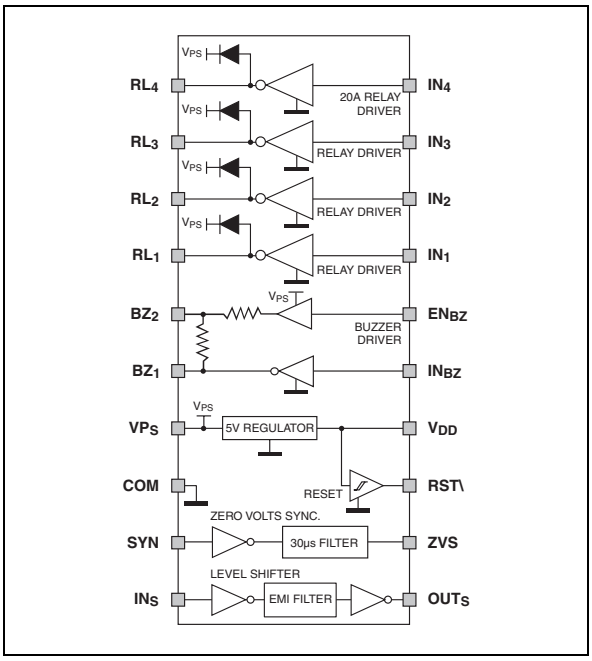
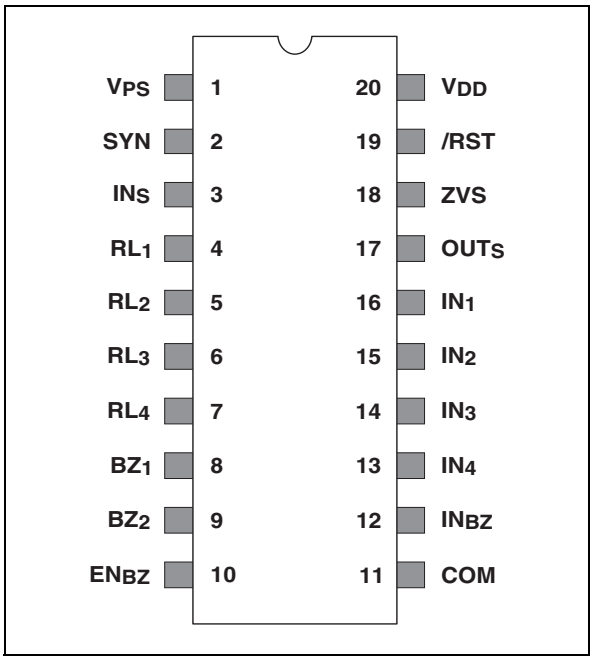


Figure 3. Pin-out connections



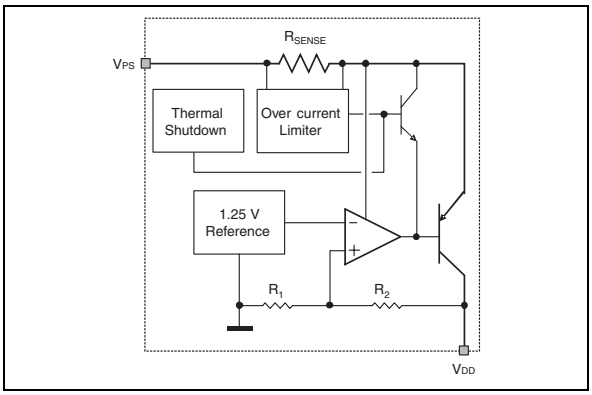
FUNCTIONAL DESCRIPTION

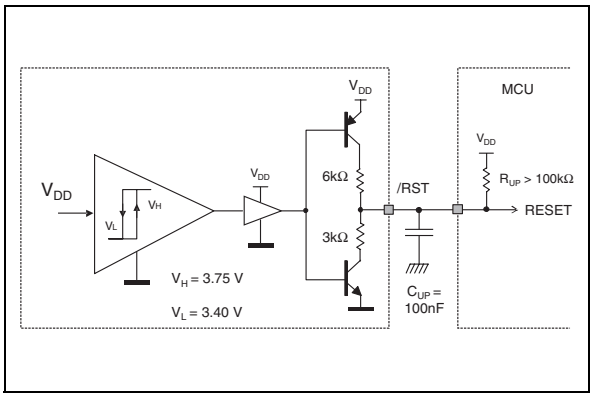
The STCC05 is a control circuit embedding most of the analog & power circuitry of an air conditioner or refrigirator control module. It interfaces the micro-controller MCU with the AC power and cooling process sections.

■ The voltage supply

The 5V voltage regulator supplies the micro-controller MCU. Its input voltage ranges from 7V to 18V; and its average DC output current up to 50mA. With an output filtering capacitor of 100µF, its output voltage accuracy is better than +/- 5% in the whole operating range of the ambient temperature T_{AMB}, the load current I_{DD} and the input voltage V_{PS} , contributing directly to the ADC accuracy.

The regulator includes also an over current limiter and a thermal shutdown. The over current limiter protects the regulator against output short circuits and inrush currents during the power up. The current limiter is made of a serial shunt resistance as current sensor and a circuit that regulates the input current. Moreover, the thermal shutdown protects the whole circuit against overload operations. It is made of a thermal sensing junction and a hysteresis comparator that is able to switch off the passing element.



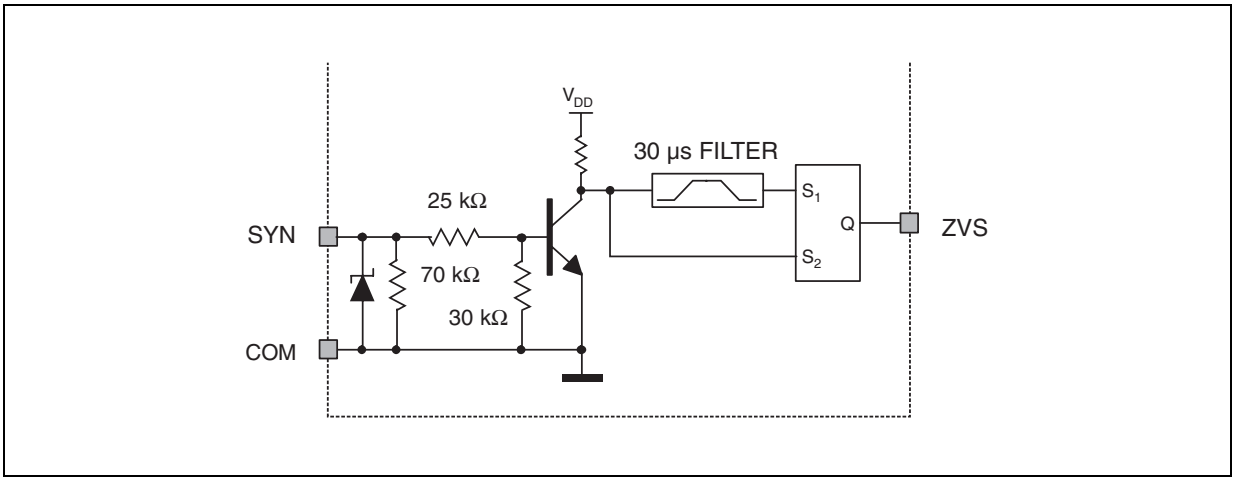


■ The reset circuit

This circuit ensures a Low Voltage Detection (LVD) of the output of the regulator. Most micro-controllers have an active RESET pin in the low state: so, the /RST pin will be active at low state.
The reset comparator senses the regulator voltage V_{DD}. The /RST pin goes high when V_{DD} is higher than the high threshold V_H = 3.75V and after a delay time T_{UP}; and is low when the V_{DD} decreases below the low threshold V_L = 3.4V after the delay time T_{DW}.
These delays are set by an external capacitor C_{UP} connected to the /RST pin and depend on the trigger thresholds of /RST: For C_{UP} = 100nF, T_{UP}= 400µs with V_{TH}= V_H/2; T_{DW}= 200µs with V_{TH}= V_L/2.

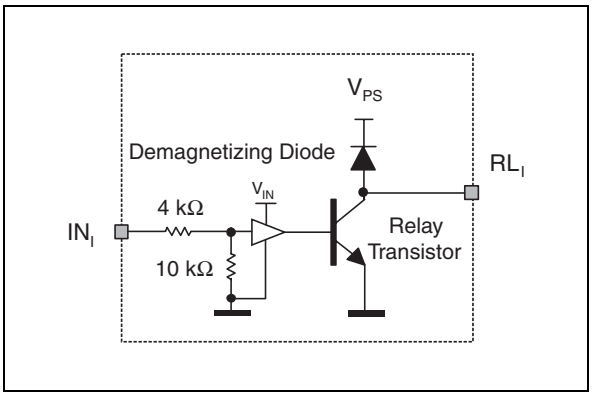
■ The Zero Voltage Synchronization ZVS circuit

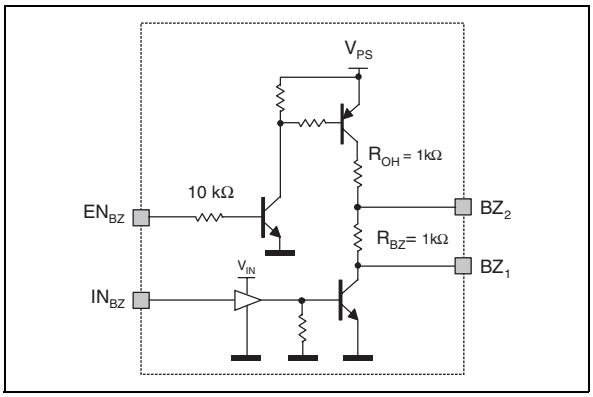
The Zero Voltage Synchronization ZVS circuit generates the signal ZVS that synchronizes the whole operation with the AC line cycle (20 ms on 50 Hz or 16.7 ms on 60 Hz). This signal allows the MCU to control the AC loads and achieve the timing functions.
The input pin SYN is an image of the mains voltage. It is connected to either the power supply transformer through a resistor R_{ZV} or an opto-coupler that is controlled directly by the AC line voltage. The circuit is protected against fast line transient voltages: a robust ESD protection and a 30µs digital filter are implemented to provide a higher immunity to the MCU operation. Its output signal ZVS is inverted respect to the input signal V_{SYN}.



■ The relay coil drivers

These robust circuits allow a DC relay coil to be driven by an MCU output. The relay coil has a minimum resistance of 580Ω and has a power up to 0.25W for V_{PS} = 12 V. These characteristics are representative of 3A relays such as FTR-F3AA-12V or JQ1A-12V series.
The output stage is made of a transistor and a demagnetization diode. The transistor is referred to the ground COM, has a DC current rating of 50mA; and its collector is connected to the output RL_I (I=1, 2, 3). The diode is connected between the output pin RL_I and the supply pin V_{PS}.
Moreover, a fourth coil driver has an extended 150mA current capability to be able to drive the coil of a relay having a 130Ω minimum resistance and a 1.1W maximum power. These characteristics are representative of 20A relays such as G4A-E-DC12, OMIF-S-112 or UKH12S series.





■ The buzzer driver with enable control

The MCU can excite a warning buzzer with a 50% PWM signal. The buzzer driver amplifies this signal in current and translates it from the 5V MCU output to the V_{PS} supply to produce the right sound level from the buzzer.

The output stage is made of a NPN transistor, a PNP transistor and two 1kΩ resistors.

The NPN transistor, referred to the power ground COM, is controlled by the input IN_{BZ}; its collector is connected to the output BZ_1. The input IN_{BZ} is driven by a simple push-pull MCU buffer.

The PNP transistor, referred to the V_{PS} polarity, is controlled by the input EN_{BZ}; and its collector is connected to the output BZ_2 through a 1kΩ resistor. The input EN_{BZ} is driven by a simple push-pull MCU buffer.

The pin BZ_2 is the supply terminal of the buzzer; and the circuit has a DC current rating of 9mA and the PWM section runs from 10Hz up to 5kHz.

A 1kΩ resistor R_{BZ} is connected between the BZ_1 and BZ_2 pins to discharge the buzzer periodically. Moreover, the addition of an external capacitor-resistor network on BZ_2 pin will allow the buzzer to turn on and off smoothly when the pin EN_{BZ} is toggling.

■ The speed sensor level shifter

The OUT_S signal is generated by an electronic signal such as the indoor fan speed clock issued of a Hall Effect sensor or a door switch signal and is transmitted to the MCU. As the IN_S input may be disturbed; a spike suppressor and a simple EMI filter are added to increase the input robustness. The output signal OUT_S is not inverted with respect to the input signal IN_S.

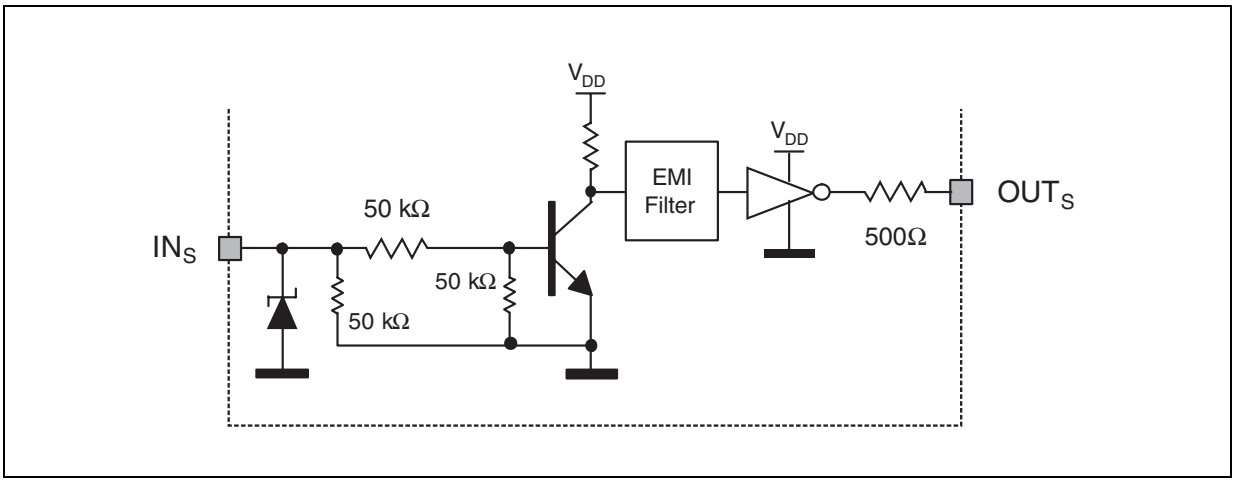


Table 2: Absolute Ratings (limiting values)

Symbol	Pin	Parameter name & conditions	Value	Unit
V_{DD}	V_{DD}	Output supply voltage	- 0.3 to 6	V
V_{PS}	V_{PS}, IN_S	Power supply voltage, level shifter input	- 0.3 to 20	V
V_{SYN}	SYN	ZVS input voltage, R_{ZV} = 15kΩ	- 1 to 20	V
V_{MO}	BZ_1, BZ_2, RL_x, x = 1 to 4	Output voltage	- 0.3 to V_{PS} + 0.3	V
V_I	IN_1, IN_2, IN_3	Input logic voltage	- 0.3 to V_{DD} + 0.3	V
V_O	ZVS, OUT_S, /RST	Output logic voltage	- 0.3 to V_{DD} + 0.3	V
I_M	V_{PS}	Maximum sourced current pulse, tp = 10ms	500	mA
	RL_x, x = 1 to 3	Maximum sunk driver current pulse, tp = 10ms	60	mA
		Maximum DC sunk current	50	mA
	RL_4	Maximum sunk driver current pulse, tp = 10ms	160	mA
		Maximum DC sunk current	150	mA
	RL_x, x = 1 to 4	Maximum diver diode reverse current	1	mA
$I_{BZ\ AV}$	BZ_1, BZ_2	Average output current	± 2	mA
$I_{BZ\ PK}$	BZ_1, BZ_2	Peak output current, tp = 50µs	± 50	mA
ΣI_M	RL_x, I = 1 to 4	Maximum DC sunk current in all relay drivers V_{PS} = 16V, T_{AMB}= 70°C, I_{DD}= 50mA, DIP-20	220	mA
		Maximum DC sunk current in all relay drivers V_{PS} = 16V, T_{AMB}= 85°C, I_{DD}= 25mA, DIP-20	300	
P_{DIS}	All	Maximum dissipation, DIP-20, T_{AMB}= 70°C	0.90	W
T_{AMB}	All	Operating ambient temperature	- 20 to 85	°C
T_J	All	Operating junction temperature	- 10 to 150	°C
		Storage junction temperature	- 25 to 150	°C

Table 3: Electromagnetic Compatibility Ratings
(T_J = 25°C, according to typical application diagram of page 1, unless otherwise specified)

Symbol	Node	Parameter name & conditions	Value	Unit
V_{ESD}	All pins	ESD protection, MIL-STD 883 method 3015, HBM model	± 2	kV
V_{ESD}	IN_S, SYN, V_{PS}, V_{DD}	ESD protection, IEC 61000-4-2, per intput, in air (1)	± 2	
		ESD protection, IEC 61000-4-2, per intput, in contact (1)	± 2	
V_{PPB}	All pins	Total peak pulse voltage Burst, IEC 61000-4-4, (2)	± 4	

Note 1: System oriented test circuit with R_{ZV} = 15kΩ, R_{INS} = 2.2kΩ and C_{DD} = C_{PS} = 100nF
Note 2: System oriented test circuit; refer to application section

Table 4: Thermal Resistance

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	DIP-20 thermal resistance junction to ambient Single PCB with a copper thickness = 35µm and surface S_{CU} = 0.5cm²	90	°C/W

Table 5: Electrical Characteristics (T_J = 25°C, V_{CC} = 12V, unless otherwise specified)

Symbol	Pin	Name	Conditions	Min.	Typ	Max.	Unit
Voltage supply							
V_{DD}	V_{DD}	Output voltage supply	I_{DD} = 5 to 40mA T_{amb} = 0 to 70°C V_{PS} = 9 to 16V C_{DD} = 100µF $V_{IN1\ to\ 4}$ = 0V	4.75	5	5.25	V
V_{PS}	V_{PS}	Input supply voltage		7		18	V
I_{SQ}	V_{PS}	Quiescent supply current	V_{DD} = 5V, I_{DD} = 0 (open)		1.3	2	mA
I_{IN_SC}	V_{PS}	Limiting input current	V_{DD} = 0V Output in short circuit	50	80	120	mA
T_{OFF}	V_{DD}	Shutdown temperature			170		°C
ΔT	V	Releasing thermal hysteresis			15		°C
Reset circuit							
V_H	V_{DD}	Disabling reset threshold		3.4	3.75	4	V
V_L		Enabling reset threshold		3.1	3.4	3.6	
V_{HYS}		Threshold hysteresis			0.35		
T_{UP}	/RST	Disabling reset delay time	C_{UP} = 100nF, $V_{TH} = V_H/2$, R_{UP} = 100kΩ	200	400	800	µs
T_{DW}		Enabling reset delay time	C_{UP} = 100nF, $V_{TH} = V_L/2$, R_{UP} = 100kΩ	100	200	400	
Zero Voltage synchronization circuit							
T_D	ZVS	Transition filtering time	Rising and falling step	10	30	70	µs
V_{TH}	SYN	Transition threshold		0.6	1.1	1.4	V
I_{SYN}	SYN	Input nominal current	V_{SYN} = 5V		0.3		mA
			V_{SYN} = 18V		0.9	1.5	
Level shifter, zero voltage synchronization, reset circuits							
V_{OH}	LVOUT /RST ZVS	High level output voltage		0.8 V_{DD}			V
V_{OL}		Low level output voltage				0.2 V_{DD}	V
Relay coil drivers							
I_{IN4}	IN_4	Input activating current	V_{IN4} = 5V		0.85	1.4	mA
V_{ON}	RL_4	On state output voltage	I_{ON} = 150mA, V_{IN4} > 3.1V		1	1.2	V
I_{INx}	$IN_{1\ to\ 3}$	Input activating current	V_{INx} = 5V		0.85	1.4	mA
V_{ON}	$RL_{1\ to\ 3}$	On state output voltage	I_{ON} = 50mA, V_{INx} > 3.1V		1	1.2	V
$V_{RL\ H}$	$RL_{1\ to\ 4}$	Off state output voltage	V_{INx} < 50.8V, R_L = 580Ω	0.9 V_{PS}		V_{PS}	V
V_{INx}	$IN_{1\ to\ 4}$	Transition threshold		0.8	1.9	3.1	V
Buzzer driver with enable control							
V_{INBZ}	IN_{BZ}	Input muting voltage		0.8	1.5	3.1	V
F_{BUZ}		Buzzer PWM frequency	Duty cycle = 50%	0.01		5	kHz
R_{OH}	BZ_2	On state output resistance	V_{INBZ} = 0V, V_{ENBZ} > 3.1V, I_{BZ2} = 5mA		1		kΩ
V_{ON}	BZ_1	On state output voltage	I_{ON} = 25mA, V_{INBZ} > 3.1V, V_{ENBZ} = 0V, t_p = 50µs		1	1.4	V
V_{ENBZ}	EN_{BZ}	Enable threshold voltage		0.8	2	3.1	V
R_{BZ}		BZ_1 - BZ_2 Buzzer resistance			1		kΩ
Speed sensor level shifter							
$V_{INS\ H}$	IN_S	High level detection		7		18	V
$V_{INS\ L}$		Low level detection				0.8	V
I_{INS}		Internal input current	V_{INS} = 12V		500	800	µA

DC CHARACTERISTICS

Figure 4: Typical regulator voltage V_{DD} variation versus its output current I_{DD} at T_J = 25°C

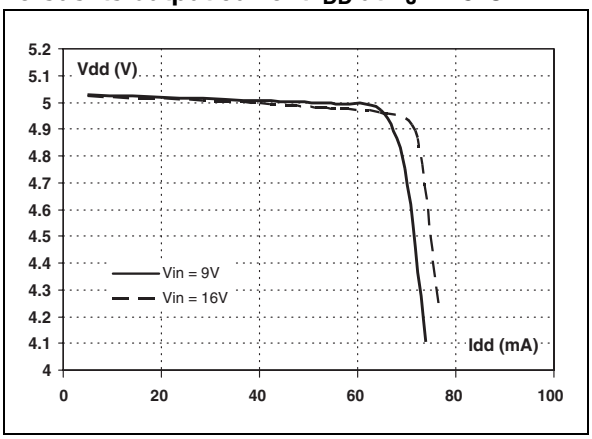


Figure 5: Typical regulator voltage V_{DD} variation versus its junction temperature at V_{IN} = 12V

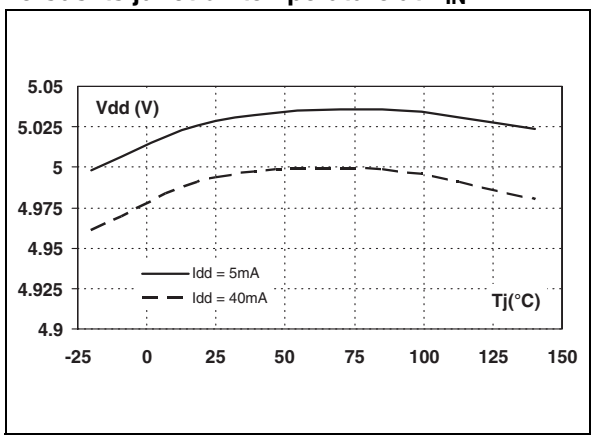


Figure 6: Typical relay driver $R_{L\ (1\ to\ 3)}$ on-state voltage variation versus its current

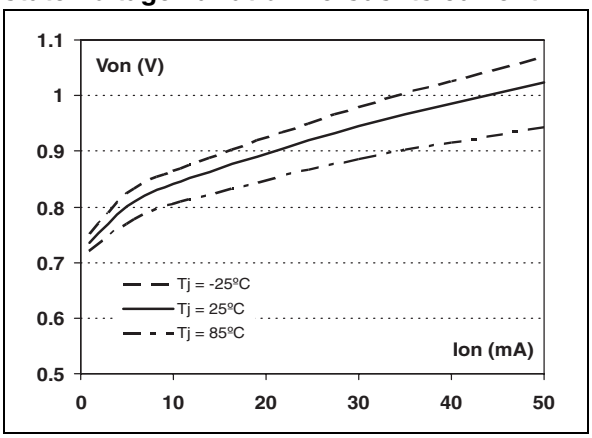
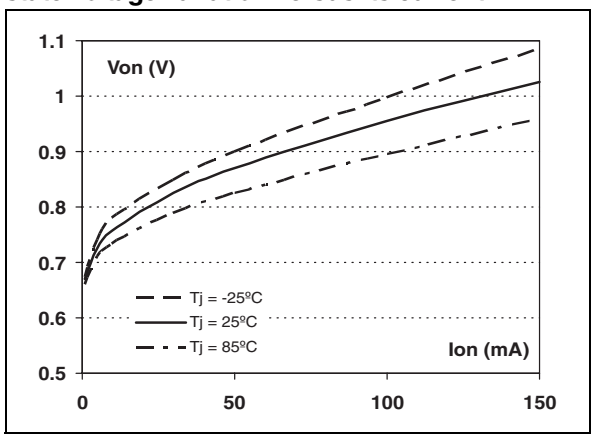


Figure 7: Typical compressor relay driver RL_4 on-state voltage variation versus its current



AIR CONDITIONER APPLICATION CONSIDERATIONS

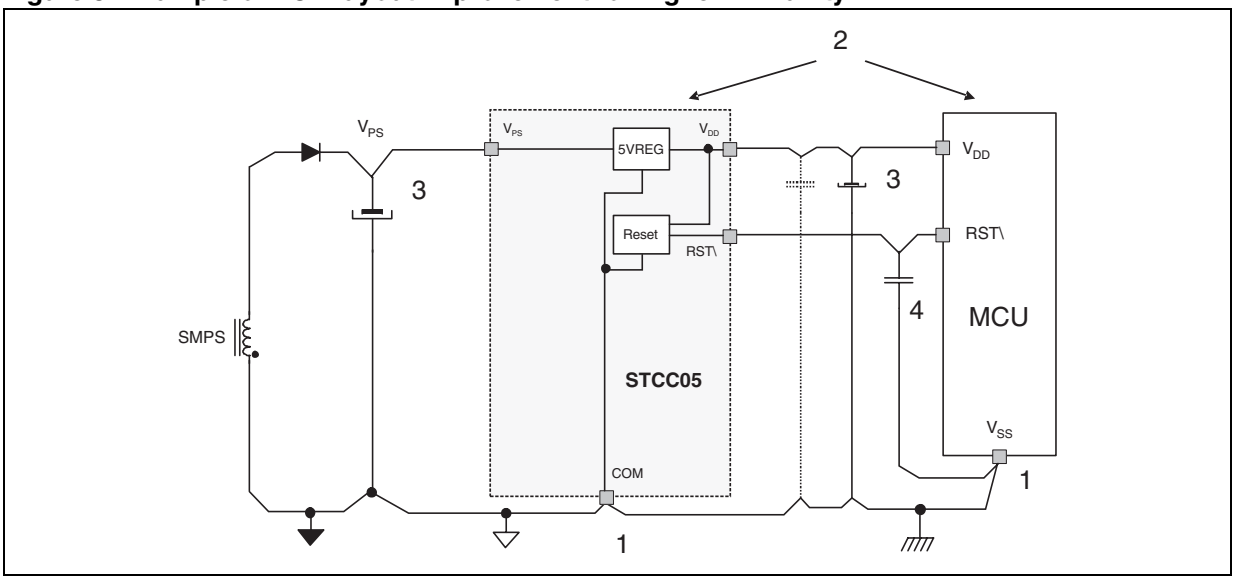
■ IMMUNITY IMPROVEMENT OF STCC05 AND THE MICROCONTROLLER

Some basic rules can be applied to improve the STCC05 immunity in its application:

- The power ground of V_{PS} should be split from the signal ground of V_{DD}, **(1)**
- The STCC05 is placed as close as possible of the MCU, **(2)**
- The supply capacitors would increase the system immunity by being placed closed to the blocks they feed, or putting decoupling capacitors (f.i. $C_{DD} = C_{PS} = 100nF$) **(3)**
- Large supply wire on the PCB should be avoided to reduce sensitivity to radiated interferences.
- A decoupling capacitor can be put on the pin IN_S of the speed sensor interface and the MCU reset pin (f.i. $C_{INS} = 10nF$; $C_{UP} = 100nF$). **(4)**

Depending of the PCB layout quality, others capacitors may be put on sensitive pins such as the output regulator pin V_{DD} and the zero crossing synchronization input pin SYN.

Figure 8: Example of PCB layout improvement for higher immunity



■ STCC05 ELECTROMAGNETIC COMPATIBILITY

Standards such as IEC61000-4-x evaluate the electromagnetic compatibility of appliance systems. To test the immunity level of the STCC05 to the IEC61000-4-4 (Electrical Fast Transient Bursts), a board representative of usual application control unit should be considered by applying the immunity design rules defined in the previous paragraph.

IEC61000-4-4 test does not allow any measurement equipment to be connected to the tested system, as it would corrupt the test results. That is why this board should include a remote monitoring circuit based on optic fibers. Thus, without any electrical link with an oscilloscope, it is possible to monitor the V_{DD} voltage as well as the /RST or the ZVS outputs of the STCC05, during the IEC61000-4-4 test. This optical link detects parasitic commutations of outputs as short as 60ns.

With this board, and the burst generator coupled to the mains as specified in the IEC61000-4-4 standard (see the following principle diagram), the STCC05 has been tested successfully at 4kV.

Figure 9: IEC61000-4-4 Electrical Fast Transient Burst general STCC05 test circuit

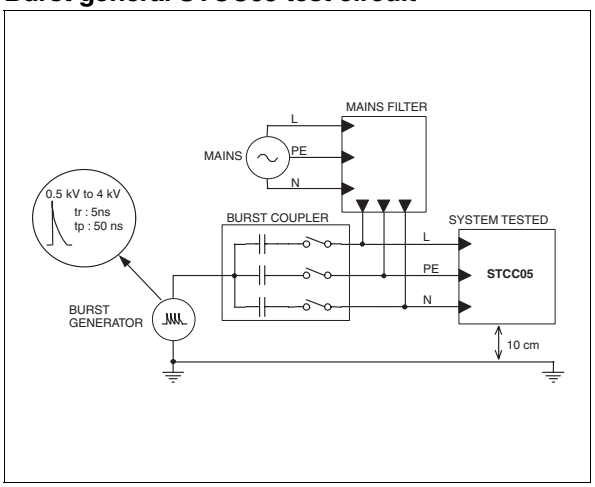
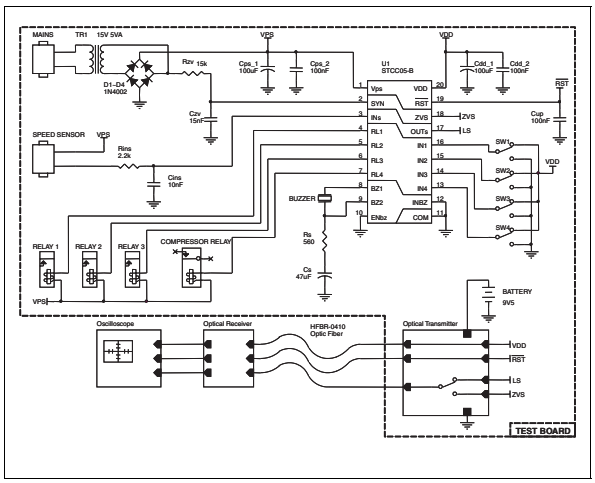


Figure 10: Test circuit schematic



■ STCC05 POWER PERFORMANCE VERSUS ITS THERMAL CAPABILITY

Figure 11: Driver current sum versus regulator current at T_{AMB} = 85°C for V_{PS} = 12, 14, 16, 18V

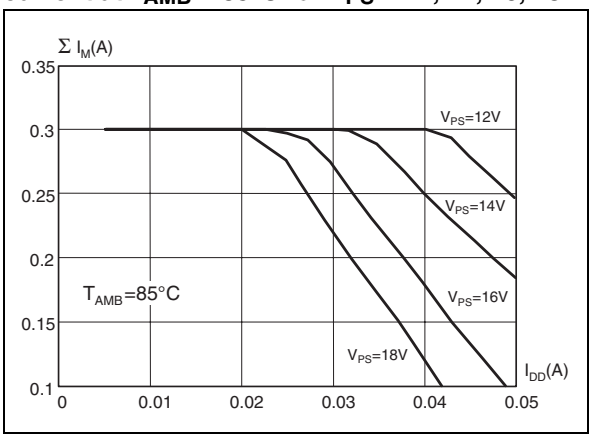
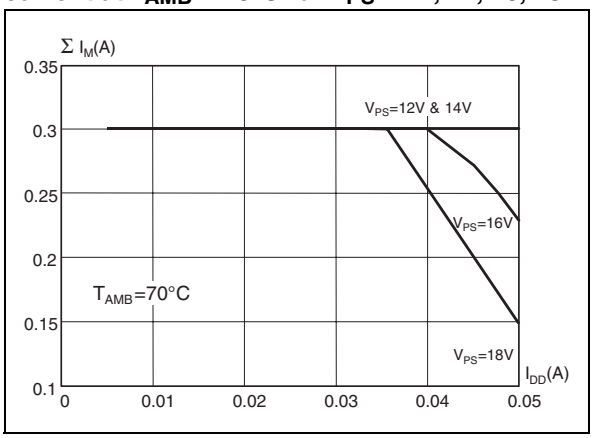


Figure 12: Driver current sum versus regulator current at T_{AMB} = 70°C for V_{PS} = 12, 14, 16, 18V



The main heat sources of the circuit during operation are the voltage regulator and the relay coil drivers. Depending of the power supply voltage V_{PS}, the ambient temperature T_{AMB}, and the thermal of resistance of the package $R_{th(j-a)}$, the sum of all the coil driver currents ΣI_M is linked to the output regulator current I_{DD}. In order to avoid spurious thermal shutdown of the system, it is advised to respect this relationship as shown on figures 7 and 8.

■ EXTENSION OF THE REGULATOR CURRENT CAPABILITY

The output current capability of the STCC05 voltage regulator can be increased in a cost effective manner by adding an external ballast transistor and two biasing resistors. With such a circuit, the output voltage regulation remains at 5V 5%, and the current limitation is still active.
Such a topology generates also power losses in the external power transistor especially when the supply voltage V_{PS} is high or the regulator is in current limiting mode. Therefore it is advised to use a package with a suitable thermal resistance ($R_{th\ j\text{-}a}$).
An example is proposed in the following figure doubling the regulator current capability of the solution to 100mA while producing a current limitation typically at 110mA.

Figure 13: Circuit diagram to extend the STCC05 regulator current to 100mA

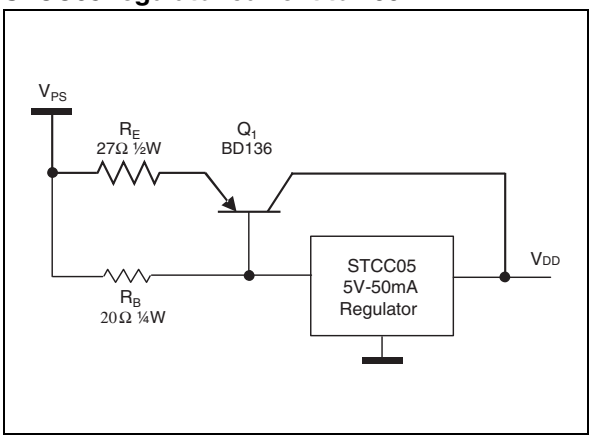
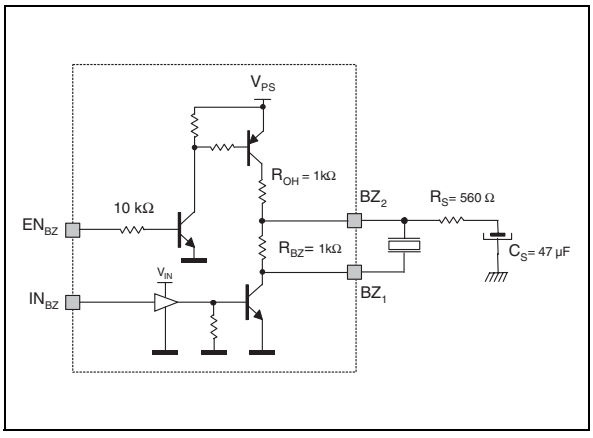


Figure 14: Application diagram of the buzzer drive

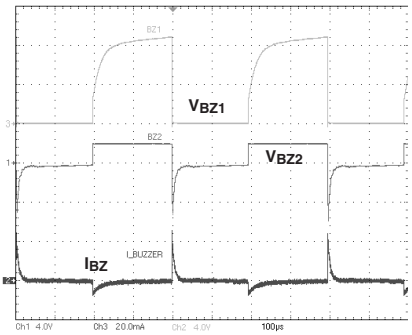


■ FLOATING BUZZER OPERATION

The sound produced by the buzzer is controlled by the frequency of the square signal applied to the IN_{BZ} input pin.
The external R_S C_S network connected to the BZ_2 output pin produces a soft sound by smoothing the buzzer supplying envelope at power up and power down. Contrary to basic drivers, which directly apply

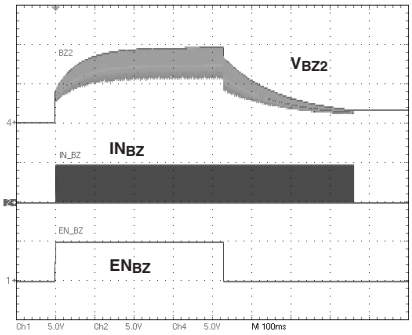
the voltage to the buzzer, this circuit feeds the buzzer with the exponential voltage induced by the charge and the discharge of the R_S C_S network.
The R_{OH} and R_S resistors contribute to reduce high harmonic sound distortions. Indeed, they limit the peak current through the buzzer, feed the buzzer with the C_S capacitor voltage, and limit the current through the low side NPN transistor of the driver.
Therefore to set rising/falling durations of the sound shape, it is advised to adjust only the value of the C_S capacitor.
The integrated R_{BZ} resistor is selected to discharge the buzzer when the low side transistor is off, especially at the maximum operating frequency. The buzzer is completely discharged within five times the time constant of the resistor-buzzer with $\tau = R_{BZ} \times C_{BUZZER}$.
Therefore, $R_{BZ} < 1 / (10 \times F_{MAX} \times C_{BUZZER})$. Since the buzzer capacitance C_{BUZZER} is about 20nF at the maximum operating frequency of driver is 5kHz, this R_{BZ} resistance is set at 1kΩ.

Figure 15: Buzzer terminal voltages V_{BZ1} & V_{BZ2} and buzzer current I_{BZ}



Time : 100µs/div , V_{BZ1} & V_{BZ2} : 4V/div , I_{BZ} : 20mA/div

Figure 16: Buzzer terminal voltage V_{BZ2} with buzzer enable and input circuit signals

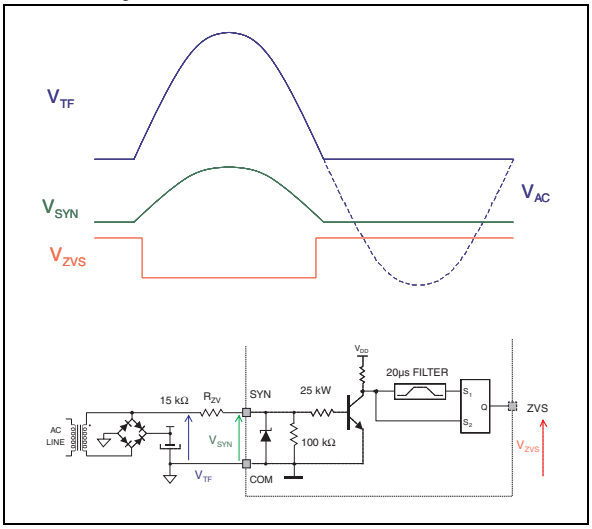


Time : 100ms/div , V_{BZ2} , EN_{BZ} & IN_{BZ} : 5V/div

■ ZERO CROSSING DETECTION CIRCUITS

The detection of the zero crossing of the AC line voltage can be achieved at least on two ways with the STCC05, depending of the power supply unit.
When the power supply uses a magnetic 50/60Hz transformer, the input pin SYN is connected to a transformer output through a resistor R_{ZV}, the electrical path being closed by the low side bridge diodes.

Figure 17: ZVS circuit operation using the AC secondary of a transformer



The delay between the real Zero Crossing event and the falling edge of ZVS depends on the internal filtering time, the resistance R_{ZV}, the rectifier drop voltage V_F, the V_{PS} supply load and the temperature. The STCC05 contribution to this delay can be evaluated by measuring the delay between its input voltage V_{TF} and its output voltage V_{ZVS}. When using V_F = 0.8V, R_{ZV} = 15kΩ, V_{PS} = 15V, I_{CC} = 20mA, it is about 50 µs on rising voltage V_{TF} and 115 µs on falling voltage V_{TF}.
When the power supply uses a switch mode power supply, the input pin SYN is synchronized by an opto-coupler, which is connected to the mains terminals through high resistances. The isolator output is on all the time except during the zero crossing where no more current feeds the input and the output transistor switches off.

Finally, the opto-coupler could be connected directly in high side mode between the SYN and the V_{DD} pins: the ZVS signal is then made of high level pulses synchronized with the zero crossing. However, the coupler could be connected in low side mode with an external 10k pull-up resistor to V_{DD}: the ZVS is now inverted with low level pulses.

Figure 18: ZVS circuit operation with an opto-coupler

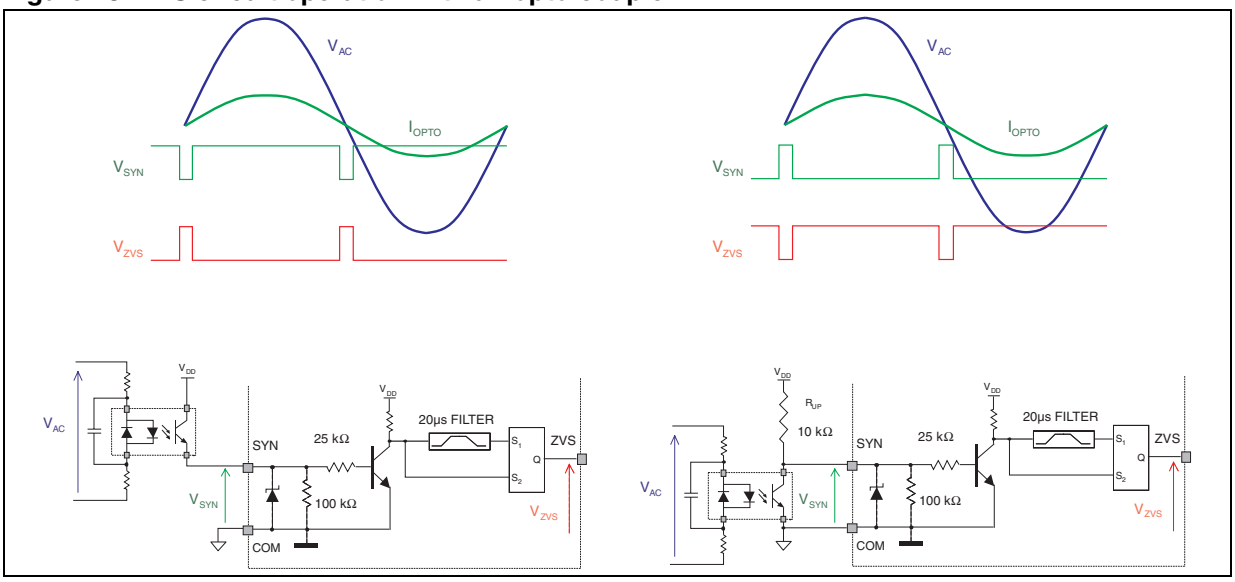


Figure 19: Ordering Information Scheme

STCC X - B Z

Circuit configuration and related application

05 = Air conditioner control

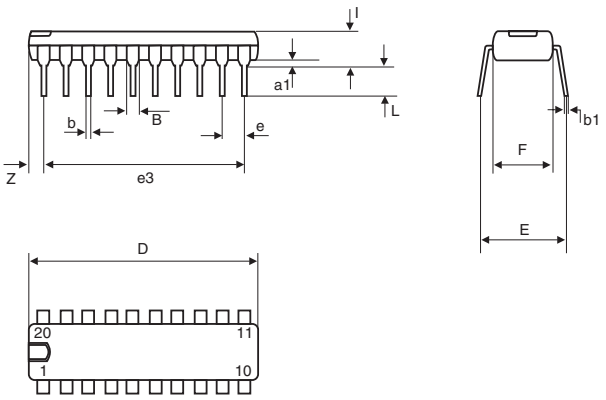
Typical power supply voltage

B = 12V

Package

D4 = DIP-20

Figure 20: DIP-20 Package Mechanical Data



REF.	DIMENSIONS					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.508			0.020		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.279
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

Table 6: Ordering Information

Part Number	Marking	Package	Weight	Base qty	Delivery mode
STCC05-BD4	STCC05-B	DIP-20	1.4 g	20	Tube

Table 7: Revision History

Date	Revision	Description of Changes
05-Oct-2004	1	First issue