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1 Introduction

The MPC5746R family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed for flexibility to support a variety of applications. The advanced and cost-efficient host processor core of the MPC5746R automotive controller family complies with the Power Architecture embedded category. It operates at speeds as high as 200 MHz and offers high-performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems, and configuration code to assist with users' implementations. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

Note

Within this document, $V_{DD\_HV\_IO}$ refers to supply pins $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FEC}$, and $V_{DD\_HV\_IO\_MSC}$

1.1 Block diagram

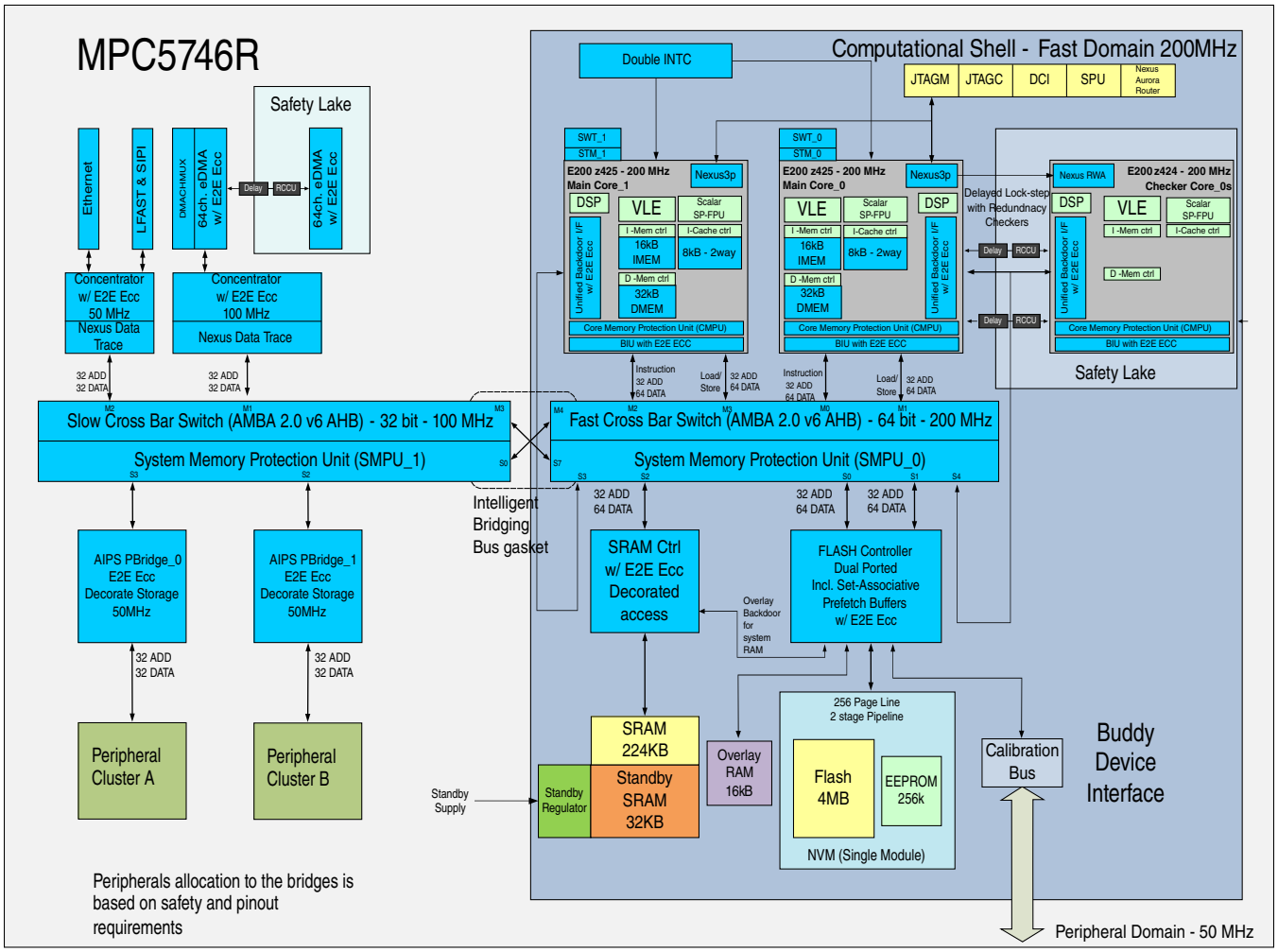


Figure 1. Core block diagram

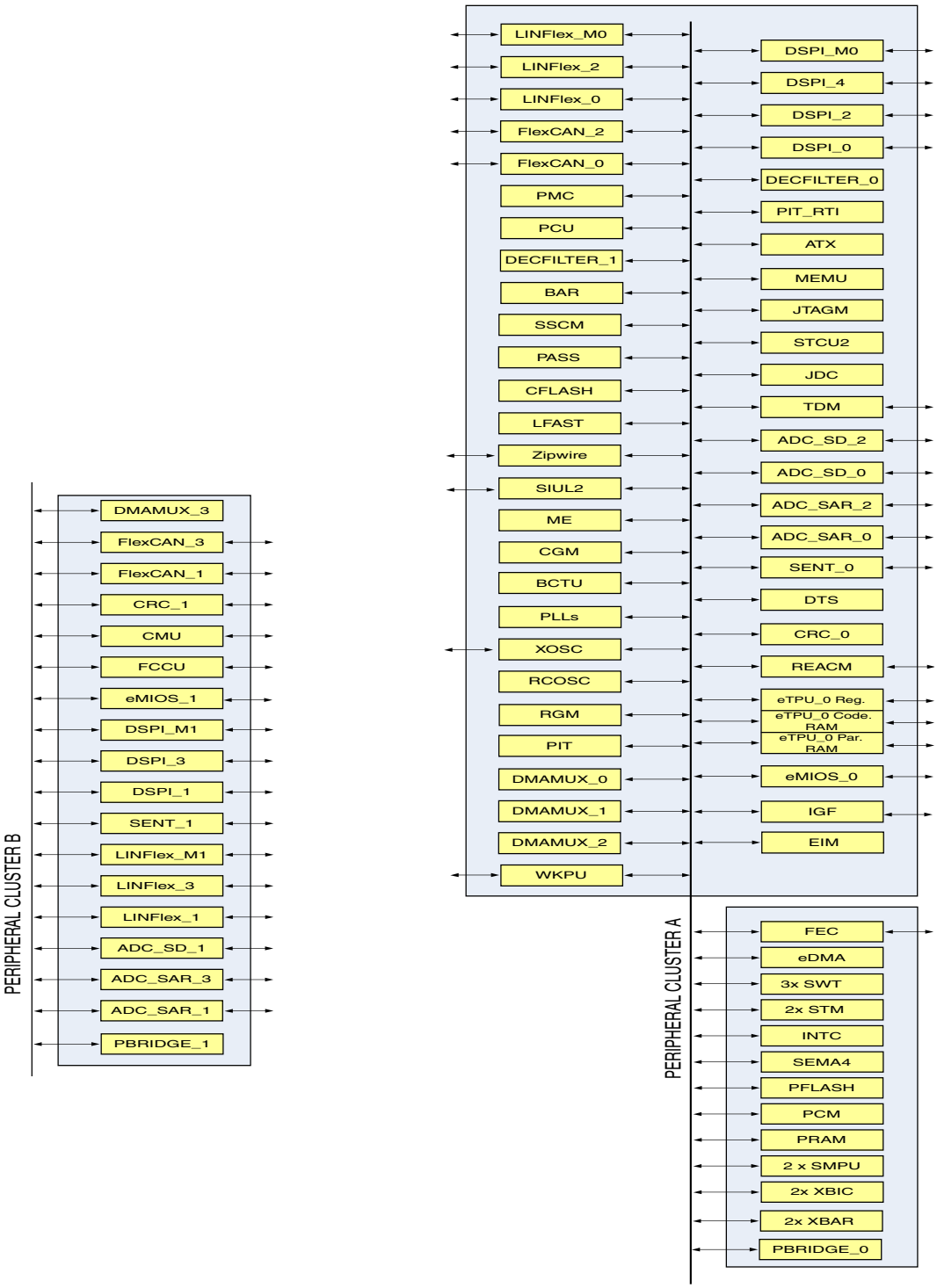


Figure 2. Peripherals allocation

2 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

3 Absolute maximum ratings

Functional operating conditions are given in the DC electrical specifications. Absolute maximum voltages are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond listed maxima may affect device reliability or cause permanent damage to the device.

Table 1. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Value		Unit
			Min	Max	
Cycle	Lifetime power cycles	—		1000k	—
V_{DD_LV}	1.2 V core supply voltage [2, 3, 4]	—	–0.3	1.5	V
$V_{DD\_LV\_BD}$	Emulation module voltage[2, 3, 4]	—	–0.3	1.5	V
$V_{DD\_HV\_IO\_MAIN}$	I/O supply voltage[5]	—	–0.3	6.0	V
$V_{DD\_HV\_IO\_JTAG}$	Crystal oscillator and JTAG supply	Reference to V_{SS}	–0.3	6.0	V
$V_{DD\_HV\_IO\_FEC}$	FEC supply voltage	Not using Ethernet Reference to V_{SS}	–0.3	6.0	V
$V_{DD\_HV\_IO\_MSC}$	MSC supply voltage	Reference to V_{SS}	–0.3	6.0	V
$V_{DD\_HV\_PMC}$	Power Management Controller supply voltage [6]	—	–0.3	6.0	V
$V_{DD\_HV\_FLA}$	Decoupling pin for flash regulator[6]	—	–0.3	—	V
V_{DDSTBY}	RAM standby supply voltage[6]	—	–0.3	6.0	V
$V_{SS\_HV\_ADV\_SD}$	S/D ADC ground voltage	Reference to V_{SS}	–0.3	0.3	V
$V_{SS\_HV\_ADV\_SAR}$	SAR ADC ground voltage	Reference to V_{SS}	–0.3	0.3	V
$V_{DD\_HV\_ADV\_SAR}$	SAR ADC supply voltage	Reference to $V_{SS\_HV\_ADV\_SAR}$	–0.3	6.0	V
$V_{DD\_HV\_ADV\_SD}$	S/D ADC supply voltage	Reference to $V_{SS\_HV\_ADV\_SD}$	–0.3	6.0	V
$V_{SS\_HV\_ADR\_SD}$	S/D ADC ground reference	Reference to V_{SS}	–0.3	0.3	V
$V_{SS\_HV\_ADR\_SAR}$	SAR ADC ground reference	Reference to V_{SS}	–0.3	0.3	V
$V_{DD\_HV\_ADR\_SAR}$	SAR ADC alternate reference	Reference to $V_{SS\_HV\_ADR\_SAR}$	–0.3	6.0	V
$V_{DD\_HV\_ADR\_SD}$	S/D ADC alternate reference	Reference to $V_{SS\_HV\_ADR\_SD}$	–0.3	6.0	V
$V_{DD\_LV\_BD}$ - V_{DD_LV}	Emulation module supply differential to 1.2 V core supply	—	–0.3	1.5	V
$V_{SS} – V_{SS\_HV\_ADR\_SAR}$	$V_{SS\_HV\_ADR\_SAR}$ differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{SS\_HV\_ADR\_SD}$	$V_{SS\_HV\_ADR\_SD}$ differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{SS\_HV\_ADV\_SAR}$	$V_{SS\_HV\_ADV\_SAR}$ differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{SS\_HV\_ADV\_SD}$	$V_{SS\_HV\_ADV\_SD}$ differential voltage	—	–0.3	0.3	V
V_{IN}	I/O input voltage range[7]	—	–0.3	6.0	V
		Relative to $V_{SS\_HV\_IO}$, [8, 9]	–0.3	—	
		Relative to $V_{DD\_HV\_IO}$[8, 9]	—	0.3	
I_{INJD}	Maximum DC injection current for digital pad	Per pin, applies to all digital pins	–5	5	mA

Table continues on the next page...

Table 1. Absolute maximum ratings (continued)

Symbol	Parameter	Conditions[1]	Value		Unit
			Min	Max	
I_{INJA}	Maximum DC injection current for analog pad	Per pin, applies to all analog pins	–5	5	mA
I_{MAXSEG}[10, 11]	Maximum current per I/O segment	—	–120	120	mA
T_{STG}	Storage temperature range and non-operating times	—	–55	175	°C
STORAGE	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 60 °C	—	20	yrs
T_{SDR}	Maximum solder temperature[12] Pb-free package	—	—	260	°C
MSL	Moisture sensitivity level[13]	—	—	3	—

1. Voltage is referenced to V_{SS} unless otherwise noted.
2. Allowed 1.45 – 1.5 V for 60 seconds cumulative time at maximum T_J = 150 °C, remaining time as defined in note -1 and note -1.
3. Allowed 1.375 – 1.45 V for 10 hours cumulative time at maximum T_J = 150 °C, remaining time as defined in note -1.
4. 1.32 – 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.275 V at maximum T_J = 150 °C.
5. Allowed 5.5 – 6.0 V for 10 hours cumulative time at maximum T_J = 150 °C, remaining time at or below 5.0 V +10%.
6. Allowed 3.6 – 4.5 V for 10 hours cumulative time at maximum T_J = 150 °C, remaining time at or below 3.3 V +10%. This is an internally regulated supply. Values given are for reference only.
7. The maximum input voltage on an I/O pin tracks with the associated I/P supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3V can be used for nominal calculations.
8. Relative value can be exceeded, if design measures are taken to ensure injection current limitation (parameters I_{INJD} and I_{INJA}).
9. $V_{DD\_HV\_IO}/V_{SS\_HV\_IO}$ refers to supply pins and corresponding grounds: $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FEC}$, $V_{DD\_HV\_IO\_MSC}$.
10. Sum of all controller pins (including both digital and analog) must not exceed 200 mA. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.
11. The average current values given in the "I/O pad current specifications" section should be used to calculate total I/O segment current.
12. Solder profile per IPC/JEDEC J-STD-020D.
13. Moisture sensitivity per JEDEC test method A112.

4 Electromagnetic Compatibility (EMC)

EMC measurements to IC-level IEC standards are available from NXP on request.

5 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device.

All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

Device failure is defined as: "If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature. Maximum DC parametrics variation within 10% of maximum specification."

Table 2. ESD ratings

Parameter	Conditions	Value	Unit
ESD for Human Body Model (HBM)[1]	All pins	2000	V
ESD for field induced Charged Device Model (CDM)[2]	All pins	500	V

1. This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing
2. This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level

6 Operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted.

The device operating conditions must not be exceeded in order to guarantee proper operation and reliability.

NOTE

All power supplies need to be powered up to ensure normal operation of the device.

Table 3. Device operating conditions

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
Frequency						
f_{SYS}	Device operating frequency[1]	T_J -40 °C to 150 °C	—	—	200	MHz
Temperature						
T_J	Operating temperature range - junction		–40.0	—	150.0	°C
T_A (T_L to T_H)	Operating temperature range - ambient		–40.0	—	125.0	°C
Voltage						
V_{DD_LV}	External core supply voltage[2, 3]	LVD/HVD enabled	1.2	—	1.32	V
		LVD/HVD disabled[4, 5, 6]	1.18	—	1.38	
$V_{DD\_HV\_IO\_MAIN}$	I/O supply voltage [7]		3.5	—	5.5	V

Table continues on the next page...

Table 3. Device operating conditions (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$V_{DD\_HV\_IO\_FEC}$	FEC I/O supply voltage[8]	5 V range	3.5	—	5.5	V
		3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_IO\_MSC}$	MSC I/O supply voltage[9]	5 V range	3.5	—	5.5	V
		3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_IO\_JTAG}$[10]	JTAG I/O supply voltage[11]	5 V range	3.5	—	5.5	V
		3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_PMC}$[12]	Power Management Controller (PMC) supply voltage	Full functionality	3.5	—	5.5	V
V_{DDSTBY}[13]	RAM standby supply voltage[14]	—	1.3	—	5.9	V
V_{STBY_BO}	Standby RAM brownout voltage	—	—	—	0.9	V
$V_{DD\_LV\_STBY\_SW}$	Standby RAM switch V_{DD_LV} voltage threshold	—	0.95	—	—	V
$V_{DD\_HV\_ADV\_SD}$	S/D ADC supply voltage[15, 16]	—	4.5	—	5.5	V
$V_{DD\_HV\_ADV\_SAR}$	SAR ADC supply voltage [17]	—	3.0	—	5.5	V
$V_{DD\_HV\_ADR\_SD}$	S/D ADC reference	—	3.0	—	5.5	V
$V_{DD\_HV\_ADR\_SD} - V_{DD\_HV\_ADV\_SD}$	S/D ADC reference differential voltage	—	—	—	25	mV
$V_{SS\_HV\_ADR\_SD} - V_{SS\_HV\_ADV\_SD}$	$V_{SS\_HV\_ADR\_SD}$ differential voltage	—	–25	—	25	mV
$V_{DD\_HV\_ADR\_SAR}$	SAR ADC reference	—	3.0	—	5.5	V
$V_{DD\_HV\_ADR\_SAR} - V_{DD\_HV\_ADV\_SAR}$	SAR ADC reference differential voltage	—	—	—	25	mV
$V_{SS\_HV\_ADR\_SAR} - V_{SS\_HV\_ADV\_SAR}$	$V_{SS\_HV\_ADR\_SAR}$ differential voltage	—	–25	—	25	mV
$V_{SS\_HV\_ADV\_SD} - V_{SS}$	$V_{SS\_HV\_ADV\_SD}$ differential voltage	—	–25	—	25	mV
$V_{SS\_HV\_ADV\_SAR} - V_{SS}$	$V_{SS\_HV\_ADV\_SAR}$ differential voltage	—	–25	—	25	mV
$V_{RAMP\_VDD\_LV}$	Slew rate on power supply pins (VDD_LV)	Ramp up	0.069	—	100	V/ms
		Ramp down	0.0345	—	100	
$V_{RAMP\_VDD\_HV\_IO\_MAIN}$, $V_{RAMP\_VDD\_HV\_PMC}$	Slew rate on power supply pins (VDD_HV_IO_MAIN, VDD_HV_PMC)	Ramp up	0.148	—	100	V/ms
		Ramp down	0.125	—	100	
Injection current						
I_{IC}	DC injection current (per pin)[18, 19, 20]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	Maximum current per power segment[21, 22]	—	–80	—	80	mA

1. Maximum operating frequency is applicable to the computational cores and platform for the device.
2. Core voltage as measured on device pin to guarantee published silicon performance.
3. During power ramp, voltage measured on silicon might be lower. maximum performance is not guaranteed, but correct silicon operation is guaranteed. See power management and reset management for description.
4. Maximum core voltage is not permitted for entire product life. See absolute maximum rating.
5. When internal LVD/HVDs are disabled, external monitoring is required to guarantee device operation. Failure to monitor externally supply voltage may result in erroneous operation of the device.

6. This LVD/HVD disabled supply voltage condition only applies after LVD/HVD are disabled by the application during the reset sequence, and the LVD/HVD are active until that point.
7. The pad are operative till 3.0V full performance. The IRC oscillator is supplied by this pin and it is setting the min voltage limit.
8. FEC will be used only in 3.3V mode. In 5V mode the segment is a general IO segment with the same characteristics of IO_MAIN.
9. MSC will be used only in 3.3V mode. In 5V mode the segment is a general IO segment with the same characteristics of IO_MAIN.
10. If XOSC is enabled via DCF_UTEST_Miscellaneous[XOSC_EN], $V_{DD\_HV\_IO\_JTAG}$ must be within the operating range before RESET pin is released.
11. JTAG will be used only in 3.3V mode. In 5V mode the segment is a general IO segment with the same characteristics of IO_MAIN.
12. The startup of flash regulator and memory initialization immediately after Phase0 of reset sequence could cause a drop of the PMC supply. No LVD event will be generated as during this time the LVD monitors are not enabled.
13. V_{DDSTBY} supply must be present before and after power up/down of the device supplies and the ramp rate should be less than 33.3 kV/s.
14. RAM retention is not guaranteed below 1.3 V, but no effect on RAM operation for voltages below 1.3 V when V_{DD_LV} is above the minimum value.
15. For supply voltages between 3.6V and 4.5V there will be no guaranteed precision of ADC (accuracy/linearity). ADC will recover to a fully functional state when the voltage rises above 4.5V.
16. $V_{DD\_HV\_ADV\_SD}$ must be higher or equal than the $V_{DD\_HV\_ADV\_SAR}$ supply to guarantee full performance. It is recommended to connect the $V_{DD\_HV\_ADV\_SD}$ to $V_{DD\_HV\_ADV\_SAR}$ at board level.
17. Temperature Sensor and its associated Band-Gap reference are supplied by this pin. The temperature sensor performance is guaranteed only between 4.5 V and 5.5 V.
18. Full device lifetime without performance degradation.
19. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See the absolute maximum ratings table for maximum input current for reliability requirements.
20. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current will be injected through the clamp diode to the supply rail. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature. For more information, see the device characterization report.
21. Sum of all controller pins (including both digital and analog) must not exceed 200 mA. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.
22. The average current values given in the "I/O pad current specifications" section should be used to calculate total I/O segment current.

Table 4. Emulation (buddy) device operating conditions

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
Frequency						
—	Standard JTAG 1149.1/1149.7 frequency	—	—	—	50	MHz
—	High-speed debug frequency	—	—	—	320	MHz
—	Data trace frequency	—	—	—	1250	MHz
Temperature						
T_{J_BD}	Device junction operating temperature range	Packaged devices	–40.0	—	150.0	°C
T_{A_BD}	Ambient operating temperature range	Packaged devices	–40.0	—	125.0	°C
Voltage						
$V_{DD\_LV\_BD}$	Buddy core supply voltage	—	1.18	—	1.32	V
$V_{DD\_HV\_IO\_BD}$	Buddy I/O supply voltage	—	3.0	—	5.5	V
V_{RAMP_BD}	Buddy slew rate on power supply pins	—	—	—	500	V/ms

7 DC electrical specifications

The following table describes the DC electrical specifications.

Table 5. DC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{DD_LV}	Maximum operating current on the V_{DD_LV} supply [1]	MPC5746R/ MPC5745R	—	—	700	mA
		MPC5743R/ MPC5742R	—	—	610	
$I_{DD\_LV\_PE}$	Operating current on the V_{DD_LV} supply for flash program/erase	—	—	—	40	mA
$I_{DD\_HV\_PMC}$	Operating current on the $V_{DD\_HV\_PMC}$ supply[2]	Flash read	—	—	40	mA
		Flash P/E	—	—	70	
		PMC only	—	—	35	
	Operating current on the $V_{DD\_HV\_PMC}$ supply (internal core reg bypassed)	Flash read	—	—	10	mA
		Flash P/E	—	—	40	
$I_{VRCCTRL}$	Core regulator DC current output on VRC_CTRL pin	—	—	—	25	mA
I_{DDSTBY_ON}	32 KB RAM Standby Leakage Current (standby regulator on, RAM not operational)[3, 4, 5]	V_{DDSTBY} @1.3 V to 5.9 V, T_J = 150 °C	—	—	575	µA
		V_{DDSTBY} @1.3 V to 5.9 V, T_A = 40 °C	—	—	55	
		V_{DDSTBY} @1.3 V to 5.9 V, T_A = 85 °C	—	—	65	
I_{DDSTBY_REG}	32 KB RAM Standby Regulator Current [6]	V_{DDSTBY} @1.2 V to 5.9 V, Tj = 150 °C	—	—	50	µA
$I_{DD\_LV\_BD}$	BD Debug/Emulation low voltage supply operating current[7]	T_J = 150 °C $V_{DD\_LV\_BD}$ = 1.32 V	—	—	250	mA
$I_{DD\_HV\_IO\_BD}$	Debug/Emulation high voltage supply operating current (Aurora + JTAG/ LFAST)	T_J = 150 °C	—	—	130	mA
I_{BG}	Bandgap reference current consumption		—	—	600	µA
$I_{DD\_BD\_STBY}$	BD Debug/Emulation low voltage supply standby current	T_J = 150 °C $V_{DD\_LV\_BD}$ = 1.32 V	—	—	120	mA
I_{VDDA}	VDDA supply current		—	16	25	mA

1. Value is derived from a typical application at 200MHz, Core 0 Data and Instruction Cache On, Core 1 in Lockstep mode, typical usage for SARADC, SDADC, DMA, eTPU, eMIOS, CAN, MSC, SPI, SENT, PIT, and Flash reads.

2. This value is considering the use of the internal core regulator with an external ballast with the minimum value of h_{FE} of 60.
3. Data is retained for full TB range of -40 °C to 125 °C. RAM supply switch to the standby regulator occurs when the V_{DD_LV} supply falls below 0.95V.
4. V_{DDSTBY} may be supplied with a non-regulated power supply, but the absolute maximum voltage on V_{DDSTBY} given in the absolute maximum ratings table must be observed.
5. The maximum value for I_{DDSTBY_ON} is also valid when switching from the core supply to the standby supply, and when powering up the device and switching the RAM supply back to V_{DD_LV}
6. When the V_{DDSTBY} pin is powered, the standby RAM regulator current is present on the pin, regardless if the device is in standby mode or not. No current is present on the pin when V_{DDSTBY} pin is set to 0V, disabling the standby regulator.
7. Worst case usage (data trace, data overlay, full Aurora utilization).

8 I/O pad specification

The following table describes the different pad type configurations.

Table 6. I/O pad specification descriptions

Pad type	Description
General-purpose I/O pad	General-purpose I/O pads with four selectable output slew rate settings. The GPIO pads have CMOS input threshold levels.
LVDS pads	Low Voltage Differential Signal interface pads
Input only pads	These pads, which ensure low input leakage, are associated with the ADC channels. The digital inputs of these pads have CMOS, and TTL input threshold levels.

Note

Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin.

8.1 Input pad specifications

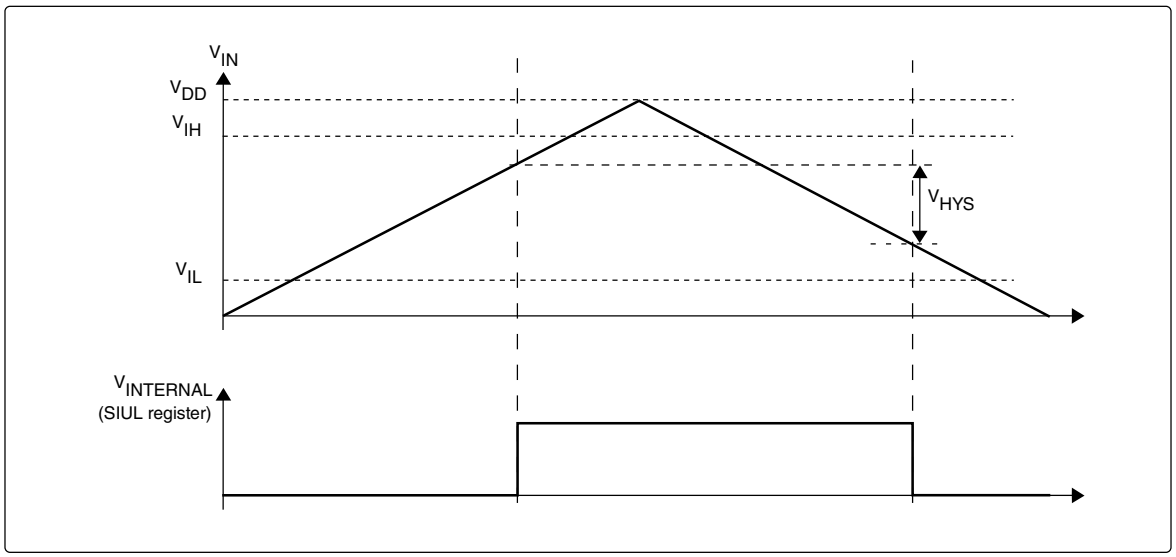


Figure 3. I/O input DC electrical characteristics definition

Table 7. I/O input DC electrical characteristics

Symbol	Parameter[1]	Conditions	Value[2]			Unit
			Min	Typ	Max	
VIHTTL	TTL input high level	3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V	2.0	—	$V_{DD\_HV\_IO}$ + 0.3	V
VILTTL	TTL input low level	3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V	V_{SS} -0.3	—	0.6	V
VHYSTTL	TTL level input hysteresis	3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.3	—	—	V
VDRFTTTL	TTL Input VIL/VIH temperature drift	—	—	—	100[3]	mV
VIHCMOS_H	CMOS input high level (with hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.65 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
VIHCMOS	CMOS input high level (without hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.55 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
VILCMOS_H	CMOS input low level (with hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V	V_{SS} -0.3	—	0.35 * $V_{DD\_HV\_IO}$	V
VILCMOS	CMOS input low level (without hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V	V_{SS} -0.3	—	0.4 * $V_{DD\_HV\_IO}$	V
VHYSCMOS	CMOS input hysteresis	3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.1 * $V_{DD\_HV\_IO}$	—	—	V
VDRFTCMOS	CMOS Input VIL/VIH temperature drift	—	—	—	100[3]	mV
INPUT CHARACTERISTICS[4]						
I_{LKG}	Digital input leakage	GPIO pins V_{SS} < V_{IN} < $V_{DD\_HV\_IO}$	-1.0	—	1.0	µA
C_{IN}	Input capacitance	GPIO and Input pins	—	—	8	pF

1. Supported input levels vary according to pad types. Pad type "pad_sr_hv" supports only the CMOS input level, while pad type "pad_isatww_st_hv" supports TTL and CMOS levels. Refer to the IO spreadsheet attached to the Reference Manual for the pad type of each pin.

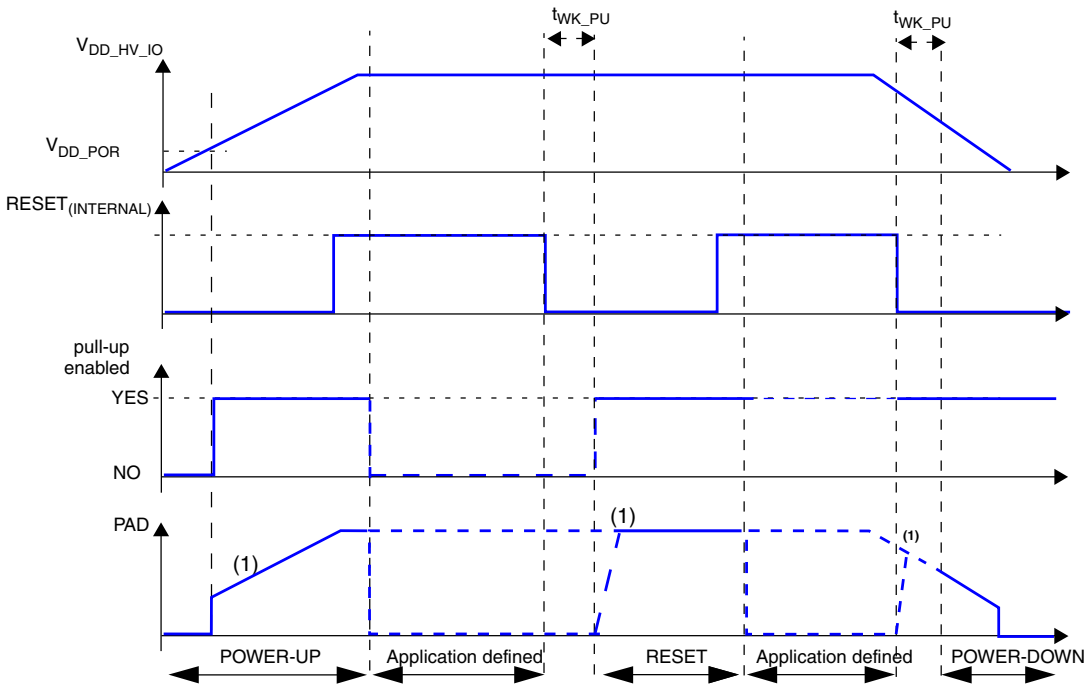
2. TTL level input specifications apply to the digital inputs on the analog input pins, and not the GPIO pins on the device.
3. In a 1 ms period, assuming stable voltage and a temperature variation of ±30 Â°C, VIL/VIH shift is within ±50 mV. For SENT requirement, refer to Note in the "I/O pad current specifications" section.
4. For LFAST, microsecond bus, and LVDS input characteristics, refer to dedicated communication module chapters.

The following table provides the current specifications for the GPIO pad weak pull-up and pull-down.

Table 8. GPIO Pull-Up/Down DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
|IWPU|	Weak pull-up current absolute value[1]	Vin = VIH = 0.65 * $V_{DD\_HV\_IO}$				µA
		4.5V < $V_{DD\_HV\_IO}$ < 5.5V	30	—	—	
		3.0V < $V_{DD\_HV\_IO}$ < 3.6V	18	—	—	
		Vin = VIL = 0.35 * $V_{DD\_HV\_IO}$				
		4.5V < $V_{DD\_HV\_IO}$ < 5.5V	—	—	120	
		3.0V < $V_{DD\_HV\_IO}$ < 3.6V	—	—	80	
		Vin = VIL = 1.1V (TTL)				
		4.5V < $V_{DD\_HV\_IO}$ < 5.5V	—	—	130	
|IWPD|	Weak pull-down current absolute value	Vin = VIH = 0.65 * $V_{DD\_HV\_IO}$				µA
		4.5V < $V_{DD\_HV\_IO}$ < 5.5V	—	—	120	
		3.0V < $V_{DD\_HV\_IO}$ < 3.6V	—	—	80	
		Vin = VIL = 0.35 * $V_{DD\_HV\_IO}$				
		4.5V < $V_{DD\_HV\_IO}$ < 5.5V	30	—	—	
		3.0V < $V_{DD\_HV\_IO}$ < 3.6V	18	—	—	
		Vin = VIL = 0.9V (TTL)				
		4.5V < $V_{DD\_HV\_IO}$ < 5.5V	16	—	—	

1. Weak pull-up/down is enabled within tWK_PU = 1 µs after internal/external reset has been asserted. Output voltage will depend on the amount of capacitance connected to the pin.



1 Actual PAD slopes will depend on external capacitances and VDD_HV_IO supply.

Figure 4. Weak pull-up electrical characteristics definition

Analog input leakage and pull up/down information is located in the ADC input description section.

8.2 Output pad specifications

The following figure provides the description of output DC electrical characteristics.

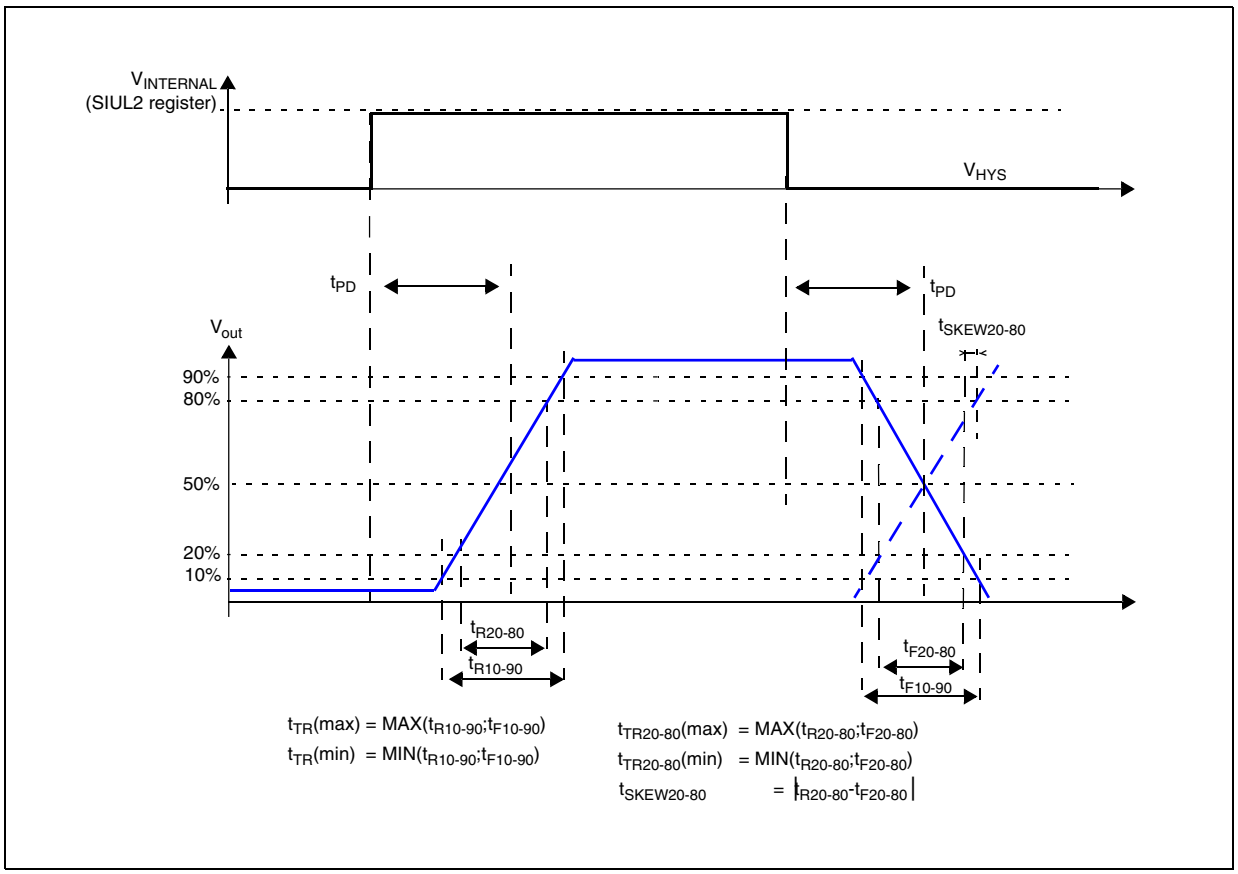


Figure 5. I/O output DC electrical characteristics definition

Table 9. GPIO pad output buffer electrical characteristics

Symbol	Parameter	Conditions	Value [1], [2]			Unit
			Min	Typ	Max	
VOH	GPIO pad output high voltage	4.5V < VDD_HV_IO < 5.0V MSCR[OERC] = 11, IOH = 38mA MSCR[OERC] = 10, IOH = 19mA MSCR[OERC] = 01, IOH = 10mA MSCR[OERC] = 00, IOH = 5mA	0.8 * VDD_HV_IO	—	—	V
		3.0V < VDD_HV_IO < 3.6V MSCR[OERC] = 11, IOH = 19mA MSCR[OERC] = 10, IOH = 10mA MSCR[OERC] = 01, IOH = 7mA MSCR[OERC] = 00, IOH = 5mA	0.8 * VDD_HV_IO	—	—	
VOL	GPIO pad output low voltage	4.5V < VDD_HV_IO < 5.0V MSCR[OERC] = 11, IOL = 48mA MSCR[OERC] = 10, IOL = 24mA MSCR[OERC] = 01, IOL = 12mA	—	—	0.2 * VDD_HV_IO	V

Table continues on the next page...

Table 9. GPIO pad output buffer electrical characteristics (continued)

Symbol	Parameter	Conditions		Value [1], [2]			Unit
				Min	Typ	Max	
		MSCR[OERC] = 00, IOL = 6mA					
		3.0V < VDD_HV_IO < 3.6V MSCR[OERC] = 11, IOL = 24mA MSCR[OERC] = 10, IOL = 12mA MSCR[OERC] = 01, IOL = 9mA MSCR[OERC] = 00, IOL = 6mA		—	—	0.2 * VDD_HV_IO	
tR_F	GPIO pad output transition time (rise/fall)	MSCR[OERC] = 11	CL = 25pF	—	—	1.5	ns
			CL = 50pF	—	—	3	
		MSCR[OERC] = 10	CL = 50pF	—	—	6.5	
		MSCR[OERC] = 01	CL = 50pF	—	—	25	
		MSCR[OERC] = 00	CL = 50pF	—	—	40	
tPD	GPIO pad output propagation delay time	MSCR[OERC] = 11	CL = 25pF	—	—	6	ns
			CL = 50pF	—	—	7.5	
		MSCR[OERC] = 10	CL = 50pF	—	—	11.5	
		MSCR[OERC] = 01	CL = 50pF	—	—	45	
		MSCR[OERC] = 00	CL = 50pF	—	—	75	
$\lvert t_{SKEW\_W} \rvert$	Difference between rise and fall time	-		—	—	10	%

1. All GPIO pad output specifications are valid for 3.0V < VDD_HV_IO < 5.5V, except where explicitly stated.
2. All values need to be confirmed during device validation.

8.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a VDD_HV_IO/VSS_HV_IO supply pair.

The following tables provides I/O consumption figures.

Table 10. I/O current consumption at VDD_HV_IO = 3.6 V

Cell	VDD_HV_IO (V)	Load (pF)	Period1 (ns)	MSCR[OERC]	Idde AVG (mA)	Idde RMS (mA)
pad_sr_hv	3.63	25	12	11	13	37
		50	15		16	36
		200	39		20	44
		25	16	10	8	20
		50	23		9	21
		200	66		12	37
		50	90	01	1.4	4

Table continues on the next page...

Table 10. I/O current consumption at VDD_HV_IO = 3.6 V (continued)

Cell	VDD_HV_IO (V)	Load (pF)	Period1 (ns)	MSCR[OERC]	Idde AVG (mA)	Idde RMS (mA)
		200	130		3	9
		50	150	00	1.6	4
		200	200		4	11

Table 11. I/O current consumption at VDD_HV_IO = 5.5 V

Cell	VDD_HV_IO (V)	Load (pF)	Period1 (ns)	MSCR[OERC]	Idde AVG (mA)	Idde RMS (mA)
pad_sr_hv	5.5	25	9	11	37	83
		50	10.2		42	89
		200	26		46	92
		25	10.5	10	25	53
		50	16		21	44
		200	44		26	49
		50	54	01	6	14
		200	80		15	35
		50	80	00	4	9
		200	130		9	22

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in the table "Absolute maximum ratings".

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{MAXSEG} value given in the table "Device operating conditions".

Note

The MPC5746R I/O Signal Description and Input Multiplexing Tables are contained in a Microsoft Excel workbook file attached to the Reference Manual.

9 Reset pad (PORST, RESET) electrical characteristics

The device implements a dedicated bidirectional reset pin (PORST).

NOTE

PORST pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 kohm.

PORST can optionally be connected to an external power-on supply circuitry.

No restrictions exist on reset signal slew rate apart from absolute maximum rating compliance.

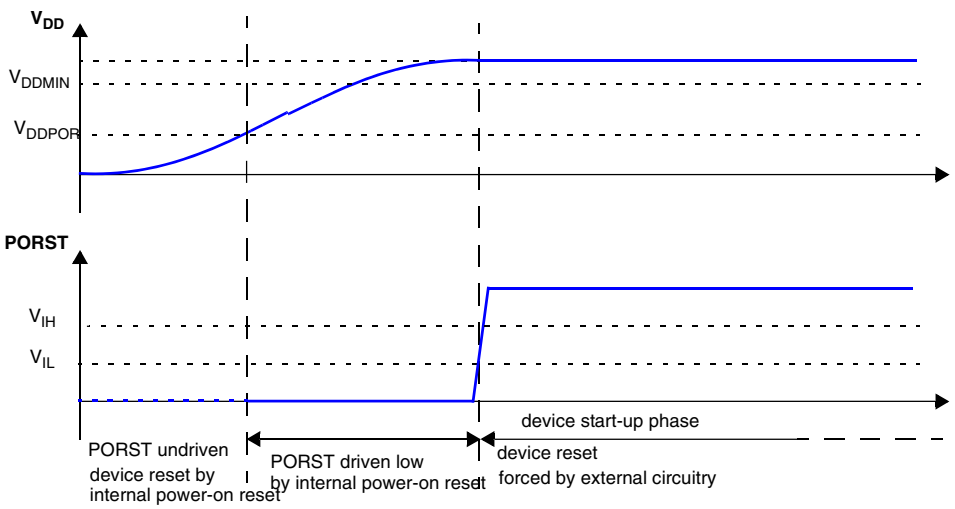


Figure 6. Start-up reset requirements

The following figure describes device behavior depending on supply signal on PORST:

1. PORST low pulse amplitude is too low—it is filtered by input buffer hysteresis. Device remains in current state.
2. PORST low pulse duration is too short—it is filtered by a low pass filter. Device remains in current state.
3. PORST low pulse is generating a reset:
   - a) PORST low but initially filtered during at least W_{FRST}. Device remains initially in current state.
   - b) PORST potentially filtered until W_{NFRST}. Device state is unknown. It may either be reset or remains in current state depending on extra condition (temperature, voltage, device).
   - c) PORST asserted for longer than W_{NFRST}. Device is under reset.

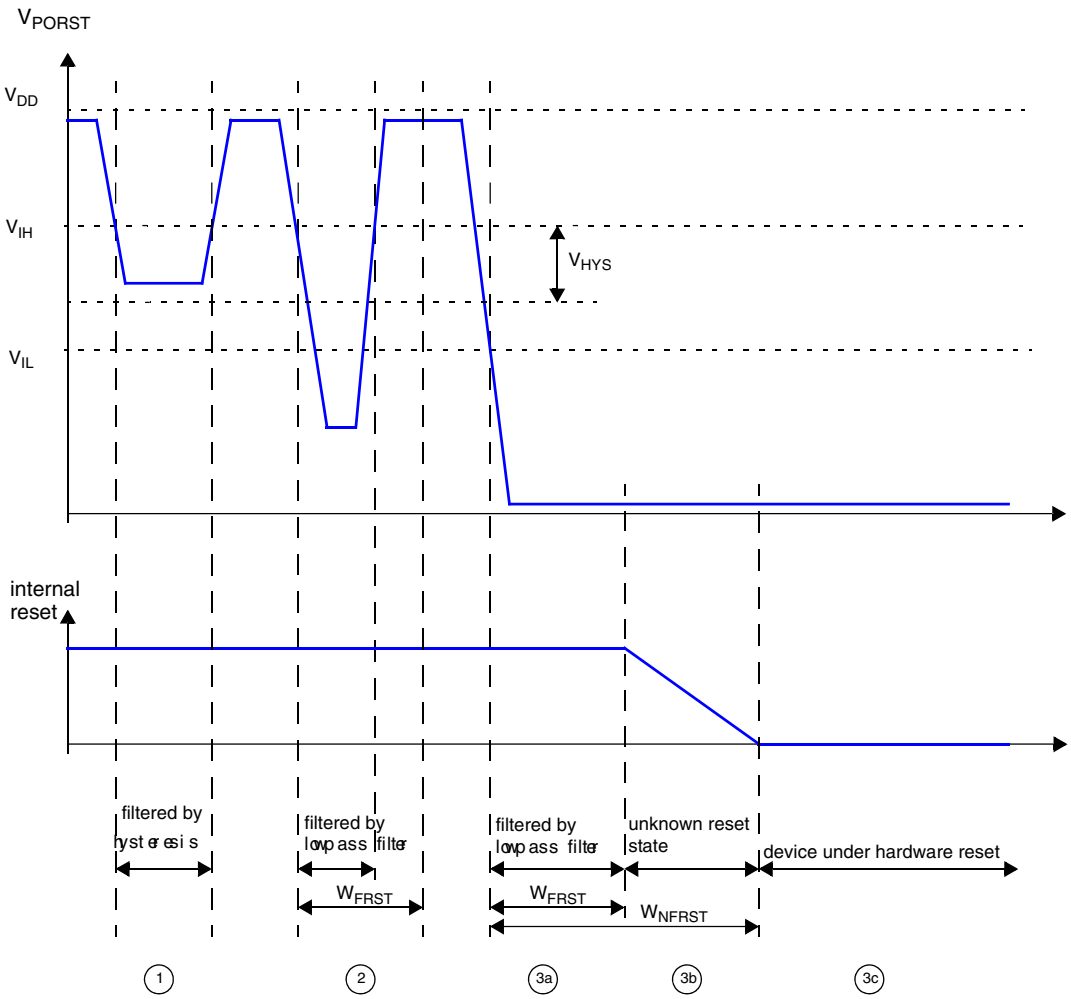


Figure 7. Noise filtering on reset signal

Table 12. Reset electrical characteristics

Symbol	Parameter	Conditions	Value[1]			Unit
			Min	Typ	Max	
V_{IH} Reset	Input high level TTL	3.5 V < VDD_HV_IO < 5.5 V	2.0	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{IL} Reset	Input low level TTL	3.5 V < VDD_HV_IO < 3.6 V	V_{SS} - 0.3	—	0.6	V
		4.5 V < VDD_HV_IO < 5.5 V	V_{SS} - 0.3	—	0.8	
V_{HYS} Reset	Input hysteresis TTL	3.5 V < VDD_HV_IO < 5.5 V	300	—	—	mV
V_{IH} PORST	Input high level CMOS	3.5 V < VDD_HV_IO < 5.5 V	0.65 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{IL} PORST	Input low level CMOS	3.5 V < VDD_HV_IO < 5.5 V	V_{SS} - 0.3	—	0.35 * $V_{DD\_HV\_IO}$	V
V_{HYS} PORST	Input hysteresis CMOS	3.5 V < VDD_HV_IO < 5.5 V	0.1 * $V_{DD\_HV\_IO}$	—	—	mV
V_{DD_POR}	Minimum supply for strong pulldown activation	—	—	—	1.2	V

Table continues on the next page...

Table 12. Reset electrical characteristics (continued)

Symbol	Parameter	Conditions	Value[1]			Unit
			Min	Typ	Max	
I_{OL_R}	Strong pull-down current[2]	Device under power-on reset V_{OL} = 0.35 * $V_{DD\_HV\_IO}$ 3.5 V < VDD_HV_IO < 3.6 V	14	—	—	mA
		Device under power-on reset V_{OL} = 0.35 * $V_{DD\_HV\_IO}$ 4.5 V < VDD_HV_IO < 5.5 V	35	—	—	
$\|I_{WPU}\|$ Reset	Weak pull-up current absolute value	RESET pin V_{IN} = VIH = 0.65 * $V_{DD\_HV\_IO}$ 4.5 V < VDD_HV_IO < 5.5 V	30	—	—	µA
		RESET pin V_{IN} = VIH = 0.65 * $V_{DD\_HV\_IO}$ 3.5 V < VDD_HV_IO < 3.6 V	18	—	—	
		RESET pin V_{IN} = VIL = 0.35 * $V_{DD\_HV\_IO}$ 4.5 V < VDD_HV_IO < 5.5 V	—	—	120	
		RESET pin V_{IN} = VIL = 0.35 * $V_{DD\_HV\_IO}$ 3.5 V < VDD_HV_IO < 3.6 V	—	—	80	
$\|I_{WPD}\|$ PORST	Weak pull-down current absolute value	PORST pin V_{IN} = VIH = 0.65 * $V_{DD\_HV\_IO}$ 4.5 V < VDD_HV_IO < 5.5 V	—	—	120	µA
		PORST pin V_{IN} = VIH = 0.65 * $V_{DD\_HV\_IO}$ 3.5 V < VDD_HV_IO < 3.6 V	—	—	80	
		PORST pin V_{IN} = VIL = 0.35 * $V_{DD\_HV\_IO}$ 4.5 V < VDD_HV_IO < 5.5 V	30	—	—	
		PORST pin V_{IN} = VIL = 0.35 * $V_{DD\_HV\_IO}$ 3.5 V < VDD_HV_IO < 3.6 V	18	—	—	
W_{FRST}	PORST and RESET input filtered pulse	—	—	—	500	ns
W_{NFRST}	PORST and RESET input not filtered pulse	—	2000	—	—	ns
W_{FNMI}	ESR1 input filtered pulse	—	—	—	20	ns
W_{NFNMI}	ESR1 input not filtered pulse	—	400	—	—	ns

1. An external 4.7 KOhm pull-up resistor is recommended to be used with the PORST and RESET pins for fast negation of the signals.

2. Strong pull-down is enabled during power up / phase0 on both pads but after that a weak pull-down is enabled on PORST and a weak pull-up is enabled on RESET.

10 Oscillator and FMPLL

Two on-chip PLLs, the peripheral clock and reference PLL (PLL0), and the frequency modulated system PLL (PLL1) generate the system and auxiliary clocks from the external oscillator.

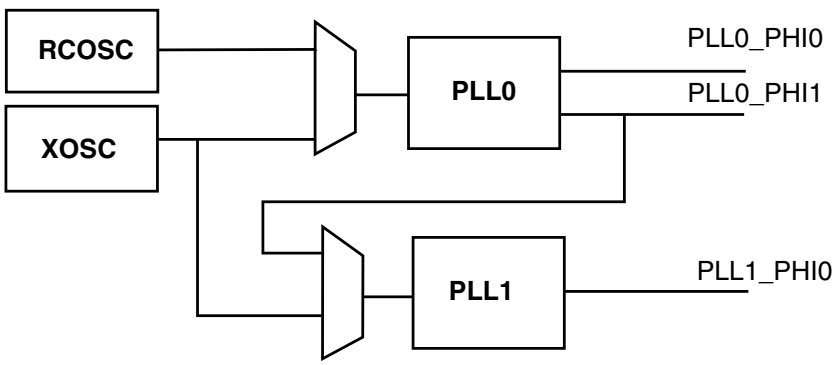


Figure 8. PLL integration

Table 13. PLL0 electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL0IN}	PLL0 input clock[1]	—	8	—	40	MHz
Δ_{PLL0IN}	PLL0 input clock duty cycle[1]	—	40	—	60	%
$f_{PLL0VCO}$	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI0}$	PLL0 output clock PHI0	—	4.762	—	400	MHz
$t_{PLL0LOCK}$	PLL0 lock time	—	—	—	110	µs
$\lvert\Delta_{PLL0PHI1SPJ}\rvert$	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma	—	—	300[2]	ps
$\Delta_{PLL0LTJ}$	PLL0 output long term jitter[2] f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz frequency), 6-sigma pk-pk	–250	—	250	ps
		16 periods accumulated jitter (50 MHz frequency), 6-sigma pk-pk	–300	—	300	ps
		long term jitter (< 1MHz frequency), 6-sigma pk-pk	–650	—	650	ps
I_{PLL0}	PLL0 consumption	FINE LOCK state	—	—	5	mA

1. PLL0IN clock retrieved directly from either internal RCOSC or external FXOSC clock. Input characteristics are granted when using internal RCOSC or external oscillator is used in functional mode.

2. V_{DD_LV} noise due to application in the range V_{DD_LV} = 1.25V (+/-5%) with frequency below PLL bandwidth (40 KHz) will be filtered.

Table 14. FMPLL1 electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL1IN}	PLL1 input clock[1]	—	38	—	78	MHz
Δ_{PLL1IN}	PLL1 input clock duty cycle[1]	—	35	—	65	%
$f_{PLL1VCO}$	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI0}$	PLL1 output clock PHI0	—	4.762	—	200	MHz
$t_{PLL1LOCK}$	PLL1 lock time	—	—	—	100	µs
$f_{PLL1MOD}$	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
		Down spread	0.5	—	4	%
$\lvert\Delta_{PLL1PHI0SPJ}\rvert$	PLL1_PHI0 single period peak to peak jitter	$f_{PLL1PHI0}$ = 200 MHz, 6-sigma pk-pk	—	—	500[2]	ps
I_{PLL1}	PLL1 consumption	FINE LOCK state	—	—	6	mA

1. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock. Input characteristics are granted when using internal PLL0 or external oscillator is used in functional mode.
2. 1.25V +/-5%, application noise below 40kHz at V_{DD_LV} pin - no frequency modulation

All oscillator specifications are valid for $V_{DD\_HV\_IO\_JTAG}$ = 3.0 V to 5.5 V.

Table 15. XOSC External Oscillator electrical specifications

Symbol	Parameter	Conditions		Value		Unit
				Min	Max	
f_{XTAL}	Crystal Frequency Range[1]	—		4	8	MHz
		—		>8	20	
		16MHz < freq < 40MHz (at present, freq = 20M and 40M have been validated, but still needs to be carried out for freq = 16MHz)		>20	40	
t_{cst}	Crystal start-up time[2, 3]	T_J = 150 °C, 20 MHz ≤ f ≤ 40 MHz		—	5	ms
t_{rec}	Crystal recovery time[4]	—		—	0.5	ms
V_{IHEXT}	EXTAL input high voltage[5] (External Reference)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$		V_{REF} + 0.6	—	V
V_{ILEXT}	EXTAL input low voltage (External Reference)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$		—	V_{REF} - 0.6	V
C_{S_EXTAL}	Total on-chip stray capacitance on EXTAL pin[6]	BGA		4.75	5.25	pF
		QFP		5.25	5.75	
C_{S_XTAL}	Total on-chip stray capacitance on XTAL pin[6]	BGA		4.75	5.25	pF
		QFP		5.25	5.75	
g_m	Oscillator Transconductance	T_J = -40 °C to 150 °C	f_{XTAL} ≤ 8 MHz	3	13	mA/V
			f_{XTAL} ≤ 20 MHz	9	35	

Table continues on the next page...

Table 15. XOSC External Oscillator electrical specifications (continued)

Symbol	Parameter	Conditions		Value		Unit
				Min	Max	
			f_{XTAL} ≤ 40 MHz	12	43	
V_{EXTAL}	Oscillation Amplitude on the EXTAL pin after startup[7]	T_J = –40 °C to 150 °C		0.5	1.6	V
I_{XTAL}	XTAL current[7,8]	T_J = –40 °C to 150 °C		—	14	mA

1. The range is selectable by UTEST miscellaneous DCF clients XOSC_LF_EN and XOSC_EN_40MHZ.
2. This value is determined by the crystal manufacturer and board design.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
5. This parameter is guaranteed by design rather than 100% tested.
6. See crystal manufacturer's specification for recommended load capacitor (C_L) values.The external oscillator requires external load capacitors when operating from 8 MHz to 16 MHz. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating at 20 MHz/40 MHz, the integrated load capacitor value is selected via S/W to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance. The capacitance on “EXTAL” and “XTAL” by internal capacitance array is controlled by the XOSC LOAD CAP SEL field of the UTEST Miscellaneous DCF client. See the DCF Records chapter of the Reference Manual.
7. Amplitude on the EXTAL pin after startup is determined by the ALC block, i.e., the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid overdriving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.
8. IXTAL is the oscillator bias current out on the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2-3 mA range and is dependant on the load and series resistance of the crystal. Test circuit is shown in the figure below.

Table 16. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Capacitance on EXTAL (C_{EXTAL})/XTAL (C_{XTAL}) [1,2] (pF)
00000	1.0
00001	2.0
00010	2.9
00011	3.8
00100	4.8
00101	5.7
00110	6.6
00111	7.5
01000	8.5
01001	9.4
01010	10.3
01011	11.2
01100	12.2
01101	13.1
01110	14.0

Table continues on the next page...

Table 16. Selectable load capacitance (continued)

load_cap_sel[4:0] from DCF record	Capacitance on EXTAL (C_{EXTAL})/XTAL (C_{XTAL}) [1, 2] (pF)
01111	15.0
10000-11111	N/A

1. Values are determined from simulation across process corners and voltage and temperature variation. Capacitance values vary ±12% across process, 0.25% across voltage, and no variation across temperature.
2. Values in this table do not include the internal stray capacitances C_{xtal}/C_{extal}.

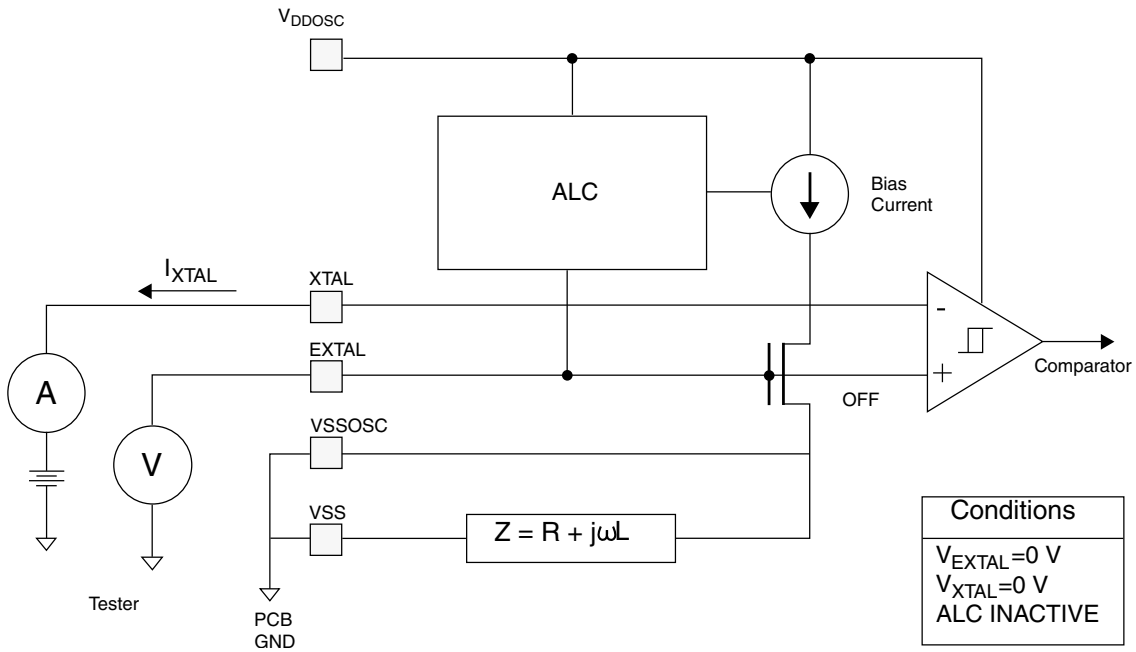


Figure 9. Test circuit

Table 17. Internal RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{Target}	IRCOSC target frequency	—	—	16	—	MHz
δf_{var_noT}	IRC frequency variation without temperature compensation	T < 150 °C	–8	—	8	%
δf_{var_T}	IRC frequency variation with temperature compensation	T < 150 °C	–3	—	3	%
δf_{var_SW}	IRC software trimming accuracy	Trimming temperature	–1	—	1	%
δf_{TRIM}	IRC software trimming step	—	—	+40/-48	—	kHz
T_{start_noT}	Startup time to reach within fvar_noT	Factory trimming already applied	—	—	5	µs
T_{start_T}	Startup time to reach within f_{var_T}	Factory trimming already applied	—	—	120	µs

Table continues on the next page...

Table 17. Internal RC Oscillator electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{AVDD5}	Current consumption on 5 V power supply	After T_{start_T}	—	—	400	µA
I_{DVDD12}	Current consumption on 1.2 V power supply	After T_{start_T}	—	—	175	µA

11 ADC modules

This device's analog sub-system contains a total of four independent 12-bit Successive Approximation (SAR) ADCs and three independent 16-bit Sigma-Delta (S/D) ADCs.

11.1 ADC input description

The following table provides the current specifications for the analog input pad weak pull-up and pull-down, and the resistance for the analog input bias/diagnostic pull up/down.

Table 18. Analog Input Leakage and Pull-Up/Down DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
ILK_AD	Analog input leakage current	Input channel off $4.5V < V_{DD\_HV\_IO} < 5.5V$ $V_{SS\_HV\_ADV\_SAR} < V_{IN} < V_{DD\_HV\_ADV\_SAR}$ $V_{SS\_HV\_ADV\_SD} < V_{IN} < V_{DD\_HV\_ADV\_SD}$	-200	—	200	nA
RPUPD	Analog input bias/ diagnostic pull up/down resistance	200KΩ $3.0V < V_{DD\_HV\_IO} < 5.5V$	130	200	280	KΩ
		100KΩ $3.0V < V_{DD\_HV\_IO} < 5.5V$	65	100	140	
		5KΩ $3.0V < V_{DD\_HV\_IO} < 5.5V$	1.4	5	8.8	
ΔPUPD	RPUPD pull up/down resistance mismatch	$3.0V < V_{DD\_HV\_IO} < 5.5V$	—	—	5	%

11.2 SAR ADC

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

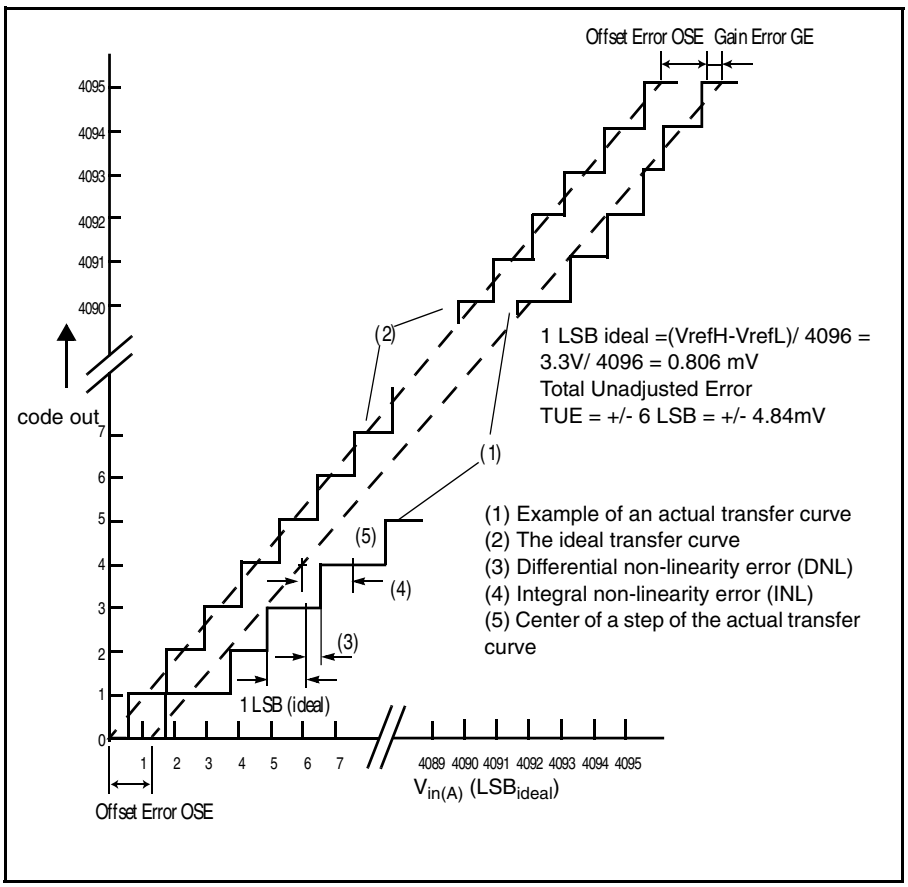


Figure 10. ADC characteristics and error definitions

11.2.1 Input equivalent circuit and ADC conversion characteristics

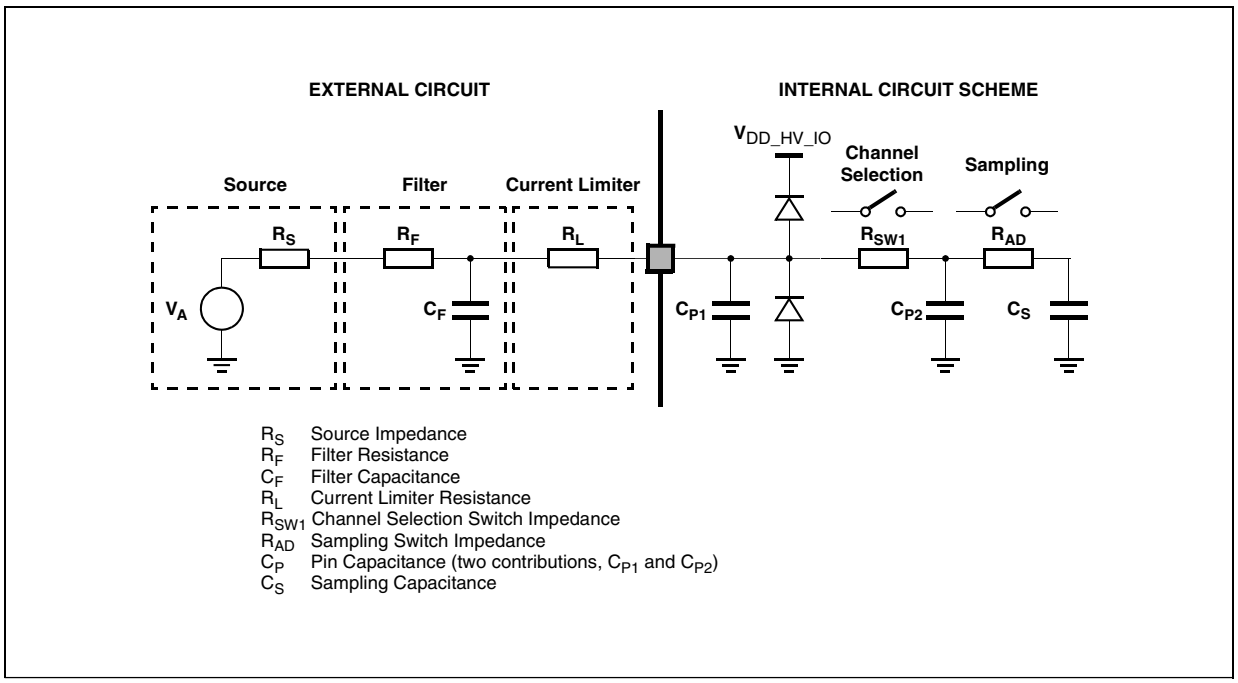


Figure 11. Input equivalent circuit

Table 19. ADC conversion characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CK} [2]	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[3] frequency.)	—	20	—	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time[4]	—	250	—	—	ns
t_{conv}	Conversion time[5]	80 MHz	700	—	—	ns
C_S [6]	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[6]	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}[6]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[6]	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
		V_{REF} range = 3.0 to 3.6 V	—	—	875	Ω
R_{AD}[6]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity	—	–2	—	2	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS[7]	Offset error	—	–6	—	6	LSB
GNE[7]	Gain error	—	–6	—	6	LSB
Input (double ADC channel)	Max leakage	150 °C	—	—	300	nA

Table continues on the next page...

Table 19. ADC conversion characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
SNR	Signal-to-noise ratio	V_{REF} = 3.3 V, Fin ≤ 125 kHz	66	—	—	dB
SNR	Signal-to-noise ratio	V_{REF} = 5.0 V, Fin ≤ 125 kHz	68	—	—	dB
THD	Total harmonic distortion	@ 125 kHz	65	70	—	dB
ENOB[8]	Effective number of bits	Fin < 125 kHz	10.5	—	—	bits
SINAD	Signal-to-noise and distortion	Fin < 125 kHz	(6.02*ENOB)+1.76			dB
$TUE_{IS1WINJ}$	Total unadjusted error for IS1WINJ	Without current injection	–6	—	6	LSB
$TUE_{IS1WWINJ}$	Total unadjusted error for IS1WWINJ	Without current injection	–6	—	6	LSB
I_{DD_VDDA}	Maximum operating current on VDDA	Tj = 150C VDD_LV_COR = 1.32 V	—	3.7	5	mA
I_{DD_VDDR}	Maximum operating current on VREF	Tj = 150C VDD_LV_COR = 1.32 V	—	150	600	µA
V_{BG_REF}, [9]	Band gap reference for self test	Trimmed, INPSAMP=0xFF	1.164	—[10]	1.236	V

1. $V_{DD\_HV\_IO}$ = 3.3 V -5%,+10%, T_J = –40 to +150 °C, unless otherwise specified, and analog input voltage from V_{AGND} to V_{AREF}
2. SAR ADC performance is not guaranteed when IRC is used as clock source for PLL0 to generate SAR ADC clock.
3. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
4. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
5. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
6. See the above figure.
7. Subject to change with additional -40°C characterization on final silicon version.
8. Below 4.5V, ENOB - 9.5b, THD- 60dB at Fin= 125KHz
9. Band gap reference only applies to Cut 2 silicon.
10. Minimum and maximum values are typical +/-3%

NOTE

- For spec complaint operation, do not expose clock sources, including crystal oscillator, IRC, PLL0, and PLL1 on the CLKOUT pads while the SAR ADC is converting.
- The ADC performance specifications are not guaranteed if two or more ADCs simultaneously sample the same shared channel.

11.3 S/D ADC

The SD ADCs are Sigma Delta 16-bit analog-to-digital converters with 333 Ksps maximum output rate.

Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

Table 20. SDn ADC electrical specification

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IN}	ADC input signal	—	0	—	$V_{DD\_HV\_ADV\_SD}$	V
V_{IN_PK2PK}[1]	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$[2] – V_{INM},[3]	Single ended. $V_{INM} = V_{SS\_HV\_ADR\_SD}$	$V_{DD\_HV\_ADR\_SD}$/GAIN			V
		Single ended. $V_{INM} = 0.5*V_{DD\_HV\_ADR\_SD}$ GAIN = 1	$\pm 0.5*V_{DD\_HV\_ADR\_SD}$			
		Single ended. $V_{INM} = 0.5*V_{DD\_HV\_ADR\_SD}$ GAIN = 2,4,8,16	$\pm V_{DD\_HV\_ADR\_SD}$/GAIN			
		Differential $0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	$\pm V_{DD\_HV\_ADR\_SD}$/GAIN			
f_{ADCD_M}	S/D clock frequency	$T_J < 150$ °C	4	14.4	16	MHz
f_{ADCD_S}	Conversion rate	$T_J < 150$ °C	—	—	333	ksps
—	Oversampling ratio	Internal modulator	24	—	256	—
RESOLUTION	S/D register resolution	2's complement notation	16[4]			bit
GAIN	ADC gain	Defined through ADC_SD[PGA] register. Only integer power of 2 are valid gain.	1	—	16	—
$\lvert\delta_{GAIN}\rvert$	Absolute value of the ADC gain error[5]	Before calibration (applies to gain settings =1)	—	—	1	%
		After calibration[6] $\Delta V_{DD\_HV\_ADR\_SD} < 5\%$ $\Delta V_{DD\_HV\_ADV\_SD} < 10\%$ $T_J < 50$ °C	—	—	0.1	%
		After calibration[6] $\Delta V_{DD\_HV\_ADR\_SD} < 5\%$ $\Delta V_{DD\_HV\_ADV\_SD} < 10\%$ $T_J < 150$ °C	—	—	0.2	%
V_{OFFSET}	Conversion offset	Before calibration (applies to all gain settings – 1, 2, 4, 8, 16)	—	10* (1+1/gain)	20	mV
		After calibration[6]	—	—	5	mV
$SNR_{DIFF150}$,[7]	Signal to noise ratio in differential mode 150 ksps output rate	$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$	78	—	—	dB

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Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
		GAIN = 1 T_J < 150 °C				
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 T_J < 150 °C	75	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 4 T_J < 150 °C	72	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 T_J < 150 °C	69	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 16 T_J < 150 °C	65	—	—	
$SNR_{DIFF333}$[7]	Signal to noise ratio in differential mode 333 ksps output rate	4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 1 T_J < 150 °C	72	—	—	dB
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 T_J < 150 °C	69	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 4 T_J < 150 °C	66	—	—	

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Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 T_J < 150 °C	63	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 16 T_J < 150 °C	60	—	—	
SNR_{SE150}[7]	Signal to noise ratio in single ended mode 150 ksps output rate	4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 1 T_J < 150 °C	72	—	—	dB
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 T_J < 150 °C	69	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 4 T_J < 150 °C	66	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 T_J < 150 °C	63	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_DS}$ = $V^{DD\_HV\_ADV\_SD}$ GAIN = 16 T_J < 150 °C	55	—	—	

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Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$THD_{DIFF150}$	Total Harmonic Distortion in differential mode 150 ksps output rate	$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 1 $T_J < 150$ °C	65	—	—	dB
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 $T_J < 150$ °C	68	—	—	
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 4 $T_J < 150$ °C	74	—	—	
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 $T_J < 150$ °C	80	—	—	
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 16 $T_J < 150$ °C	80	—	—	
$THD_{DIFF333}$	Total Harmonic Distortion in differential mode 333 ksps output rate	$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 1 $T_J < 150$ °C	65	—	—	dB
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 $T_J < 150$ °C	68	—	—	
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$	74	—	—	

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Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
		GAIN = 4 T_J < 150 °C				
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 T_J < 150 °C	80	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 16 T_J < 150 °C	77	—	—	
THD_{SE150}	Total Harmonic Distortion in single ended mode 150 ksps output rate	4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 1 T_J < 150 °C	68	—	—	dB
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 T_J < 150 °C	68	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 4 T_J < 150 °C	68	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 T_J < 150 °C	68	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_DS}$ = $V^{DD\_HV\_ADV\_SD}$ G_{AIN} = 16 T_J < 150 °C	68	—	—	

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Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SINAD_{DIFF150}$	Signal to Noise Distortion Ratio in differential mode 150 ksps output rate	$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 1 $T_J < 150$ °C	72	—	—	dB
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 $T_J < 150$ °C	72	—	—	
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 4 $T_J < 150$ °C	69	—	—	
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 $T_J < 150$ °C	68.8	—	—	
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 16 $T_J < 150$ °C	64.8	—	—	
$SINAD_{DIFF333}$	Signal to Noise Distortion Ratio in differential mode 333 ksps output rate	$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 1 $T_J < 150$ °C	66	—	—	dB
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 $T_J < 150$ °C	66	—	—	
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$	63	—	—	

Table continues on the next page...

Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
		GAIN = 4 T_J < 150 °C				
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 T_J < 150 °C	62	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 16 T_J < 150 °C	59	—	—	
$SINAD_{SE150}$	Signal to Noise Distortion Ratio in single ended mode 150 ksps output rate	4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 1 T_J < 150 °C	66	—	—	dB
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 T_J < 150 °C	66	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 4 T_J < 150 °C	63	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 T_J < 150 °C	62	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_DS}$ = $V^{DD\_HV\_ADV\_SD}$ G_{AIN} = 16 T_J < 150 °C	54	—	—	

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Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
SFDR	Spurious free dynamic range	Any GAIN	60	—	—	dB
Z_{DIFF}	Differential input impedance[8, 9]	GAIN = 1	1000	1250	1500	kΩ
		GAIN = 2	600	800	1000	
		GAIN = 4	300	400	500	
		GAIN = 8	200	250	300	
		GAIN = 16	200	250	300	
Z_{CM}	Common Mode input impedance[9, 10]	GAIN = 1	1400	1800	2200	kΩ
		GAIN = 2	1000	1300	1600	
		GAIN = 4	700	950	1150	
		GAIN = 8	500	650	800	
		GAIN = 16	500	650	800	
R_{BIAS}	Bare bias resistance	—	110	144	180	kΩ
ΔV_{INTCM}	Common Mode input reference voltage[11]	—	–12	—	+12	%
V_{BIAS}	Bias voltage	—	—	VDD_HV_ADR_SD/2	—	V
δV_{BIAS}	Bias voltage accuracy	—	–2.5	—	+2.5	%
CMRR	Common mode rejection ratio	—	55	—	—	dB
—	Anti-aliasing filter	External series resistance	—	—	20	kΩ
		Filter capacitances	220	—	—	pF
δ_{RIPPLE}	Pass band ripple [12]	0.333 * f_{ADCD_S}	–1	—	1	%
—	Stop band attenuation	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	40	—	—	dB
		[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	45	—	—	
		[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	50	—	—	
		[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	55	—	—	
		[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	60	—	—	
δ_{GROUP}	Group delay	Within pass band – Tclk is 2/f_{ADCD_M}	—	—	—	—
		OSR = 24	—	—	235.5	Tclk
		OSR = 28	—	—	275	
		OSR = 32	—	—	314.5	
		OSR = 36	—	—	354	

Table continues on the next page...

Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
		OSR = 40	—	—	393.5	
		OSR = 44	—	—	433	
		OSR = 48	—	—	472.5	
		OSR = 56	—	—	551.5	
		OSR = 64	—	—	630.5	
		OSR = 72	—	—	709.5	
		OSR = 75	—	—	696	
		OSR = 80	—	—	788.5	
		OSR = 88	—	—	867.5	
		OSR = 96	—	—	946.5	
		OSR = 112	—	—	1104.5	
		OSR = 128	—	—	1262.5	
		OSR = 144	—	—	1420.5	
		OSR = 160	—	—	1578.5	
		OSR = 176	—	—	1736.5	
		OSR = 192	—	—	1894.5	
		OSR = 224	—	—	2210.5	
		OSR = 256	—	—	2526.5	
		Distortion within pass band	–0.5/ f_{ADCD_S}	—	+0.5/ f_{ADCD_S}	—
f_{HIGH}	High pass filter 3dB frequency	Enabled	—	10e-5* f_{ADCD_S}	—	—
$t_{STARTUP}$	Start-up time from power down state	—	—	—	100	µs
$t_{LATENCY}$	Latency between input data and converted data when input mux does note change[13]	HPF = ON	—	—	δ_{GROUP} + f_{ADCD_S}	—
		HPF = OFF	—	—	δ_{GROUP}	—
$t_{SETTLING}$	Settling time after mux change	Analog inputs are muxed HPF = ON	—	—	2*δ_{GROUP} + 3*f_{ADCD_S}	—
		HPF = OFF	—	—	2*δ_{GROUP} + 2*f_{ADCD_S}	—
$t_{ODRECOVERY}$	Overdrive recovery time	After input comes within range from saturation HPF = ON	—	—	2*δ_{GROUP} + f_{ADCD_S}	—
		HPF = OFF	—	—	2*δ_{GROUP}	—

Table continues on the next page...

Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
C_{S_D}	S/D ADC sampling capacitance after sampling switch[14]	GAIN = 1, 2, 4, 8	—	—	75*GAIN	fF
		GAIN = 16	—	—	600	fF
I_{BIAS}	Bias consumption	At least 1 ADCD enabled	—	—	3.5	mA
I_{ADV_D}	ADCD supply consumption	ADCD enabled	—	2.5	8	mA
ΣI_{ADR_D}	Reference current for one SDADC	ADCD enabled	—	10	50	µA

1. For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal will only be 'clipped'.
2. VINP is the input voltage applied to the positive terminal of the SD ADC.
3. VINM is the input voltage applied to the negative terminal of the SD ADC.
4. For Gain=16, SDADC Resolution is 15 bit.
5. Offset and gain error due to temperature drift can occur in either direction (+/-) for each of the SDADCs on the device.
6. Calibration of gain is possible when gain = 1. Offset Calibration should be done with respect to $0.5*V_{DD\_HV\_ADR\_SD}$ for differential "differential mode" and single ended mode with negative input=$0.5*V_{DD\_HV\_ADR\_SD}$ ". Offset Calibration should be done with respect to 0 for "single ended mode with negative input=0". Both Offset and Gain Calibration is guaranteed for +/-5% variation of $V_{DD\_HV\_ADR\_SD}$, +/-10% variation of $V_{DD\_HV\_ADV\_SD}$, +/-50 C temperature variation.
7. S/D ADC is functional in the range $3.6V < V_{DD\_HV\_ADV\_SD} < 4.5V$ and $3.0V < V_{DD\_HV\_ADR\_SD} < 4.5$ V, SNR paramter degrades by 9 dB.
8. Input impedance in differential mode $Z_{IN} = Z_{DIFF}$
9. Input impedance given at f_{ADCD_M} = 16 MHz. Impedance is inversely proportional to SDADC clock frequency. Z_{DIFF} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{DIFF}, Z_{CM} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{CM}.
10. Input impedance in single-ended mode $Z_{IN} = (2 * Z_{DIFF} * Z_{CM}) / (Z_{DIFF} + Z_{CM})$
11. V_{INTCM} is the Common Mode input reference voltage for the SDADC. It has a nominal value of $(V_{RH\_SD} - V_{RL\_SD}) / 2$.
12. The ±1% passband ripple specification is equivalent to 20 * log10 (0.99) = 0.873 dB.
13. Propagation of the information from the pin to the register CDR[CDATA] and flags SFR[DFEF], SFR[DFFF] is given by the different modules that need to be crossed: delta/sigma filters, high pass filter, fifo module, clock domain synchronizers. The time elapsed between data availability at pin and internal S/D module registers is given by the following formula: REGISTER LATENCY = $t_{LATENCY} + 0.5/f_{ADCD\_S} + 2\ (\sim+1)/f_{ADCD\_M} + 2(\sim+1)/f_{PBRIDGEx\_CLK}$ where f_{ADCD_S} is the after-decimation ADC output data rate, $f_{ADCD\_M}/2$ is the modulator sampling rate and $f_{PBRIDGEx\_CLK}$ is the frequency of the peripheral bridge clock feeds to the ADC S/D module. The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing. Some further latency may be added by the target module (core, DMA, interrupt) controller to process the data received from the ADC S/D module.
14. This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.

12 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

Table 21. Temperature sensor electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
—	Junction temperature monitoring range	—	–40	—	150	°C
T_{SENS}	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	Accuracy	—	–7	—	7	°C

13 LVDS fast asynchronous serial transmission (LFAST) pad electrical characteristics

The LFAST pad electrical characteristics apply to both the LFAST and high-speed debug serial interfaces on the device. The same LVDS pad is used for the Microsecond Channel (MSC) and DSPI LVDS interfaces, with different characteristics given in the following tables.

13.1 LFAST interface timing diagrams

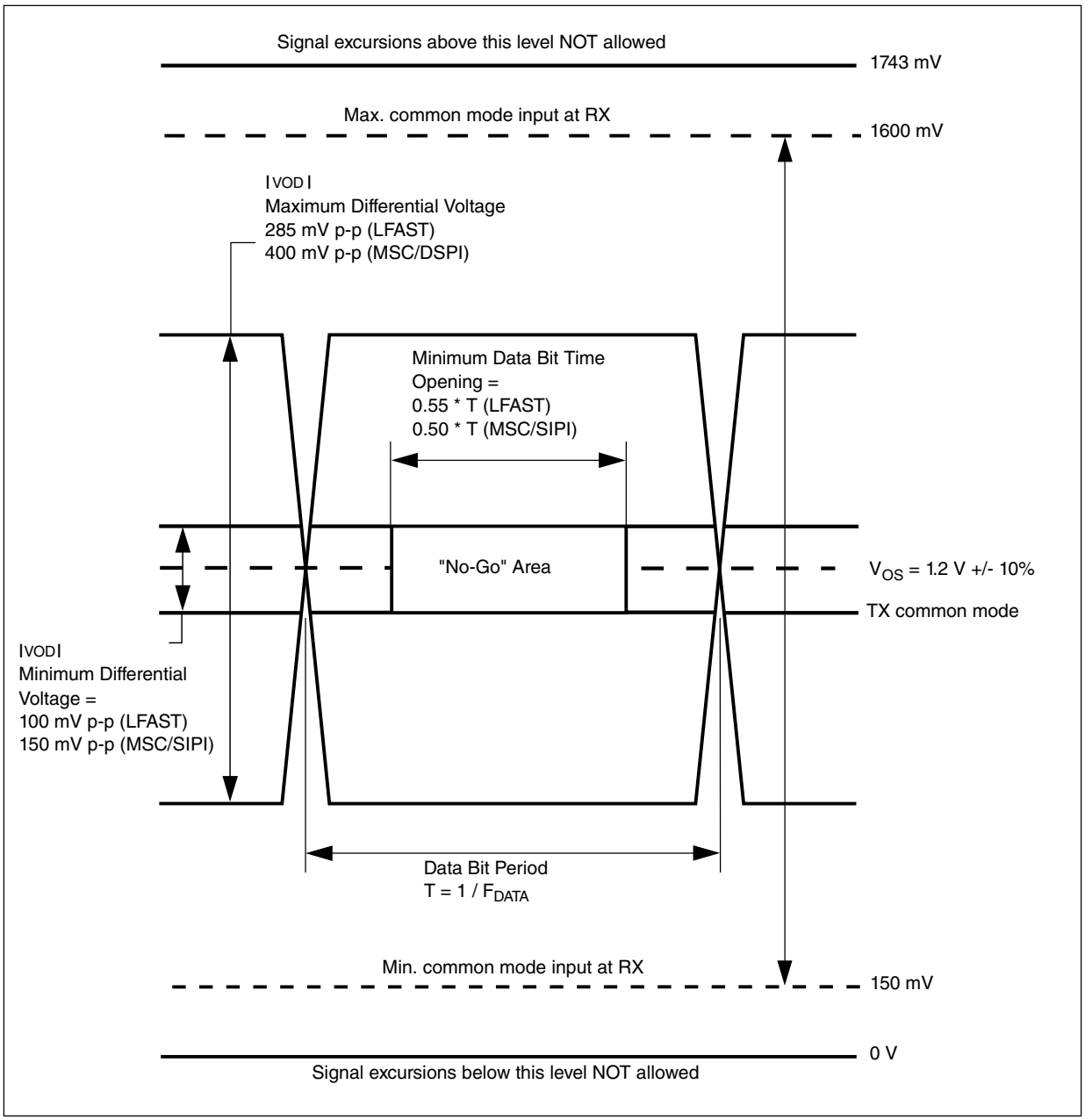


Figure 12. LFAST timing definition

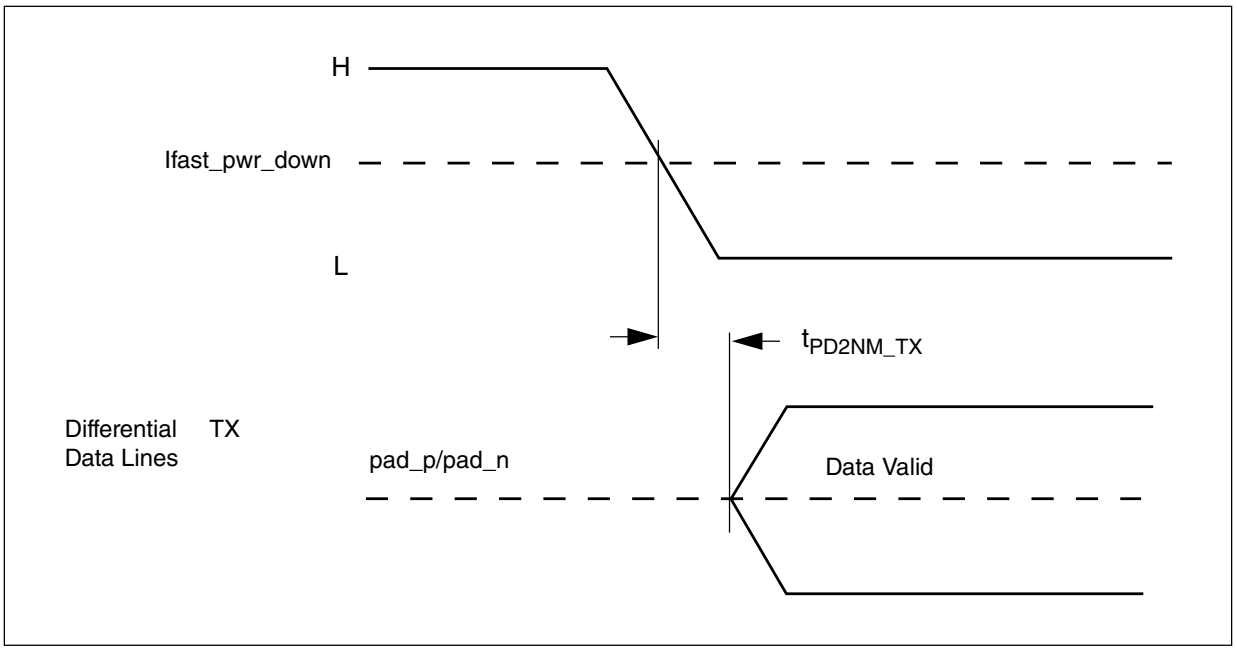


Figure 13. Power-down exit time

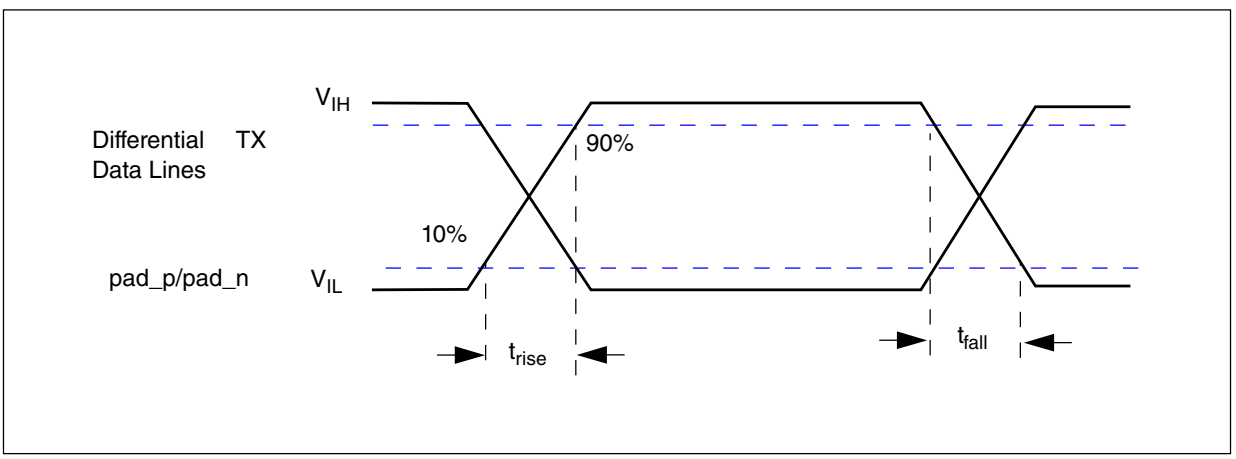


Figure 14. Rise/fall time

13.2 LFAST and MSC /DSPI LVDS interface electrical characteristics

The following table contains the electrical characteristics for the LFAST interface.

The LVDS pad electrical characteristics in this table apply to both the LFAST and High-speed Debug (HSD) LVDS pad, and the MSC/DSPI LVDS pad except where noted in the conditions.

All LVDS pad electrical characteristics are valid from -40 °C to 150 °C.

Table 22. LVDS pad startup and receiver electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
t_{PD2NM_TX}	Transmitter startup time (power down to normal mode)[1]	—	—	0.4	0.55	µs
t_{SM2NM_TX}	Transmitter startup time (sleep mode to normal mode)[2]	Not applicable to the MSC/DSPI LVDS pad	—	0.2	0.5	µs
t_{PD2NM_RX}	Receiver startup time (power down to normal mode)[3]	—	—	20	40	ns
t_{PD2SM_RX}	Receiver startup time (power down to sleep mode)[4]	Not applicable to the MSC/DSPI LVDS pad	—	20	50	ns
I_{LVDS_BIAS}	LVDS bias current consumption	Tx or Rx enabled	—	—	0.95	mA
TRANSMISSION LINE CHARACTERISTICS (PCB Track)						
Z_0	Transmission line characteristic impedance	—	47.5	50	52.5	Ω
Z_{DIFF}	Transmission line differential impedance	—	95	100	105	Ω
RECEIVER						
V_{ICOM}	Common mode voltage	—	0.15[5]	—	1.6[6]	V
$\lvert\Delta_{VI}\rvert$	Differential input voltage	—	100	—	—	mV
V_{HYS}	Input hysteresis	—	25	—	—	mV
R_{IN}	Terminating resistance	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	80	100	120	Ω
		$V_{DD\_HV\_IO}$ = 3.3 V ± 10%	80	115	150	Ω
C_{IN}	Differential input capacitance[7]	—	—	3.5	6.0	pF
I_{LVDS_RX}	Receiver DC current consumption	Enabled	—	—	0.5	mA

1. Total transmitter startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_TX} + 2 peripheral bridge clock periods. The LFAST and High-Speed Debug LFAST pad electrical characteristics are based on worst case internal capacitance values.
2. Total transmitter startup time from sleep mode to normal mode is t_{SM2NM_TX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode. All LFAST and High-Speed Debug LVDS pad electrical characteristics are valid from -40 °C to 150 °C.
3. Total receiver startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_RX} + 2 peripheral bridge clock periods.
4. Total receiver startup time from power down to sleep mode is t_{PD2SM_RX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
5. Absolute min = 0.15 V – (285 mV/2) = 0 V
6. Absolute max = 1.6 V + (285 mV/2) = 1.743 V
7. Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions.

Table 23. LFAST transmitter electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{DATA}	Data rate	—	—	—	320	Mbps
V_{OS}	Common mode voltage	—	1.08	—	1.32	V
$\lvert V_{OD}\rvert$	Differential output voltage swing (terminated)[1, 2]	—	100	200	285	mV
t_{TR}	Rise/Fall time (10%–90% of swing) [3, 4]	—	0.26	—	1.5	ns

Table continues on the next page...

Table 23. LFAST transmitter electrical characteristics (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
C_L	External lumped differential load capacitance[1]	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	10.0	pF
		$V_{DD\_HV\_IO}$ = 3.0 V	—	—	8.5	
I_{LVDS_TX}	Transmitter DC current consumption	Enabled	—	—	3.2	mA

1. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in the figure below.
2. Valid for maximum external load C_L.
3. The LFAST and High-Speed Debug LFAST pad electrical characteristics are based on worst case internal capacitance values.
4. All LFAST and High-Speed Debug LVDS pad electrical characteristics are valid from -40 °C to 150 °C.

The MSC and DSPI LVDS pad electrical characteristics are based on the application circuit and typical worst case internal capacitance values given in Figure 14.

All MSC and DSPI LVDS pad electrical characteristics are valid from -40 °C to 150 °C.

Table 24. MSC/DSPI LVDS transmitter electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
Data Rate						
f_{DATA}	Data rate	—	—	—	80	Mbps
V_{OS}	Common mode voltage	—	1.08	—	1.32	V
$\lvert V_{OD} \rvert$	Differential output voltage swing (terminated)[1, 2]	—	150	200	400	mV
t_{TR}	Rise/Fall time (10%–90% of swing) [3, 4]	—	0.8	—	5.7	ns
C_L	External lumped differential load capacitance[3]	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	40	pF
		$V_{DD\_HV\_IO}$ = 3.0 V	—	—	30	
I_{LVDS_TX}	Transmitter DC current consumption	Enabled	—	—	4.0	mA

1. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in the figure below.
2. Valid for maximum external load C_L.
3. The LFAST and High-Speed Debug LFAST pad electrical characteristics are based on worst case internal capacitance values.
4. All LFAST and High-Speed Debug LVDS pad electrical characteristics are valid from -40 °C to 150 °C.

NOTE

For optimum LVDS performance, it is recommended to set the neighbouring GPIO pads to use Weak Drive.

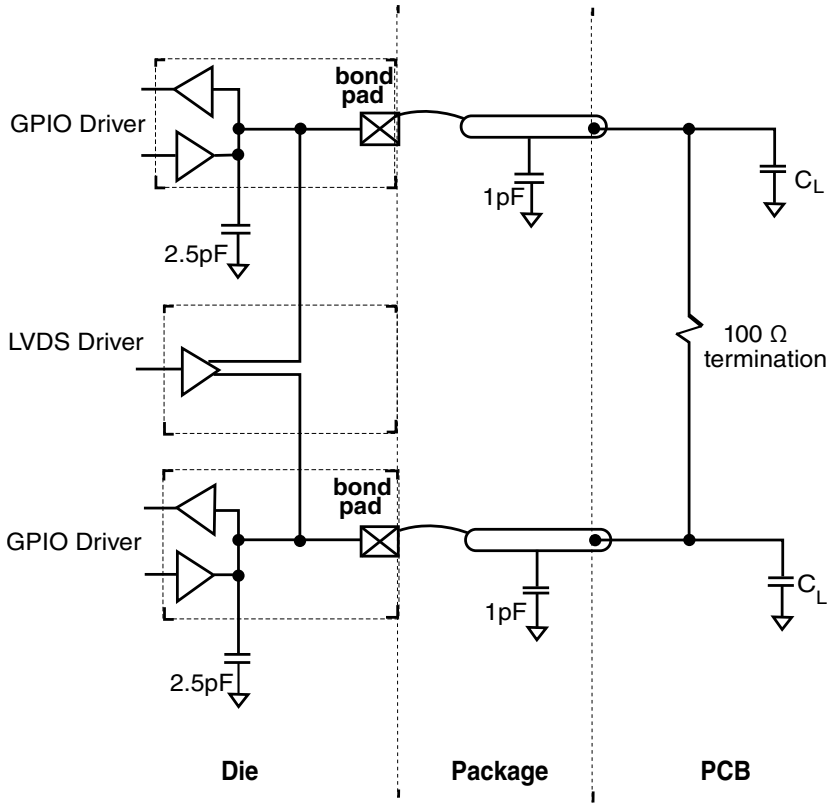


Figure 15. LVDS pad external load diagram

14 LFAST PLL electrical characteristics

The following table contains the electrical characteristics for the LFAST PLL.

The specifications in this table apply to both the interprocessor bus and debug LFAST interfaces.

Table 25. LFAST PLL electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Nominal	Max	
f_{RF_REF}	PLL reference clock frequency	—	10	—	26	MHz
ERR_{REF}	PLL reference clock frequency error	—	–1	—	1	%
D_{CREF}	PLL reference clock duty cycle	—	45	—	55	%
PN	Integrated phase noise (single side band)	f_{RF_REF} = 20 MHz	—	—	–58	dBc
		f_{RF_REF} = 10 MHz	—	—	–64	
f_{VCO}	PLL VCO frequency	—	—	640[1]	—	MHz
t_{LOCK}	PLL phase lock[2]	—	—	—	40	µs
ΔPER_{REF}	Input reference clock single period jitter (peak to peak)	Single period, f_{RF_REF} = 10 MHz	—	—	300	ps

Table continues on the next page...

Table 25. LFAST PLL electrical characteristics (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Nominal	Max	
		Long term, f_{RF_REF} = 10 MHz	–500	—	500	ps
ΔPER_{EYE}	Output Eye Jitter (peak to peak)[3]	—	—	550	—	ps

1. The 640 MHz frequency is achieved with a 10 MHz or 20 MHz reference clock. With a 26 MHz reference, the VCO frequency is 624 MHz.
2. The time from the PLL enable bit register write to the start of phase locks is maximum 2 clock cycles of the peripheral bridge clock that is connected to the PLL on the device.
3. Measured at the transmitter output across a 100 Ohm termination resistor on a device evaluation board. Refer to the figure below.

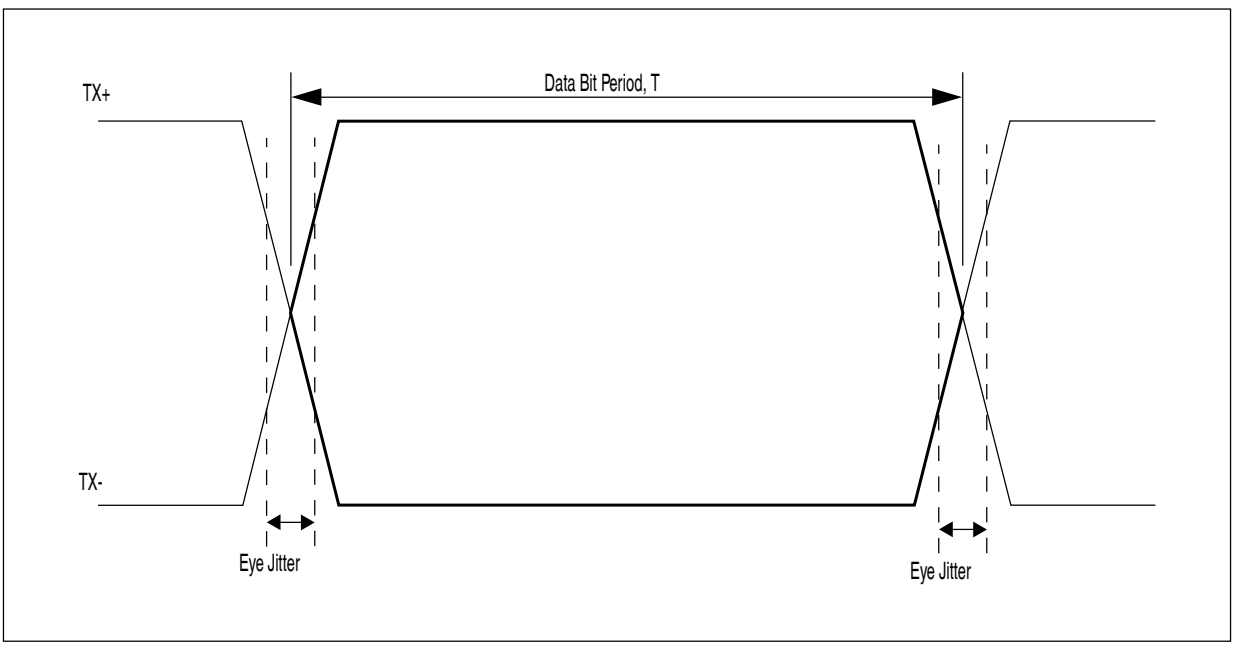


Figure 16. LFAST output 'eye' diagram

15 Aurora LVDS electrical characteristics

The following table describes the Aurora LVDS electrical characteristics.

All Aurora electrical characteristics are valid from -40 °C to 150 °C.

All specifications valid for maximum transmit data rate F_{TX}.

Table 26. Aurora LVDS electrical characteristics

Symbol	Parameter	Conditions	Value[1]			Unit
			Min	Typ	Max	
Transmitter						
F_{TX}	Transmit Data Rate	—	—	—	1.25	Gbps
$\|V_{OD\_LVDS}\|$	Differential output voltage swing (terminated)[2]	—	400	600	800	mV
t_{TR_LVDS}	Rise/Fall time (10%–90% of swing)	—	60	—	—	ps
R_{TV_L}	Differential Terminating resistance	—	81	100	120	Ω
T_{Loss}	Transmission Line Loss due to loading effects	—	—	—	100[3]	dB
Transmission line characteristics (PCB track)						
L_{LINE}	Transmission line length	—	—	—	20	cm
Z_{LINE}	Transmission line characteristic impedance	—	45	50	55	Ω
C_{AC}	External AC Coupling Capacitance	Values are nominal, valid up to ±50%	100	—	270	pF
Receiver						
F_{RX}	Receive Data Rate	—	—	—	1.25	GHz
$\|\Delta_{VI\_L}\|$	Differential input voltage	—	200	—	1000	mV
R_{RV_L}	Terminating resistance	$V_{DD\_HV\_IO\_BD}$ = 5V ±10%	81	100	120	Ω

1. All specifications valid for maximum transmit data rate F_{TX}.
2. The minimum value of 400 mV is only valid for differential resistance (R_{V_L}) = 99 ohm to 101 ohm. The differential output voltage swing tracks with the value of R_{V_L}.
3. Transimission line loss maximum value is specified for the maximum drive level of the Aurora transmit pad.

16 Power management PMC POR LVD sequencing

16.1 Power management electrical characteristics

The power management module monitors the different power supplies. It also generates the internal supplies that are required for correct device functionality. The power management is supplied by the $V_{DD\_HV\_PMC}$ supply.

16.1.1 Recommended power transistors

The following NPN transistors are recommended for use with the on-chip voltage regulator controller: ON Semiconductor™ NJD2873. The collector of the external transistor is preferably connected to the same voltage supply source as the $V_{DD\_HV\_PMC}$ pin.

The following table describes the characteristics of the power transistors.

Table 27. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE}	DC current gain (Beta)	60-550	—
P_D	Absolute minimum power dissipation	1.60	W
I_{CMaxDC}	Maximum DC collector current	2.0	A
VCE_{SAT}	Collector to emitter saturation voltage	300	mV
V_{BE}	Base to emitter voltage	0.95	V
V_C	Minimum voltage at transistor collector	2.5	V

16.1.2 Power management integration

In order to ensure correct functionality of the device, it is recommended to follow the integration scheme shown below.

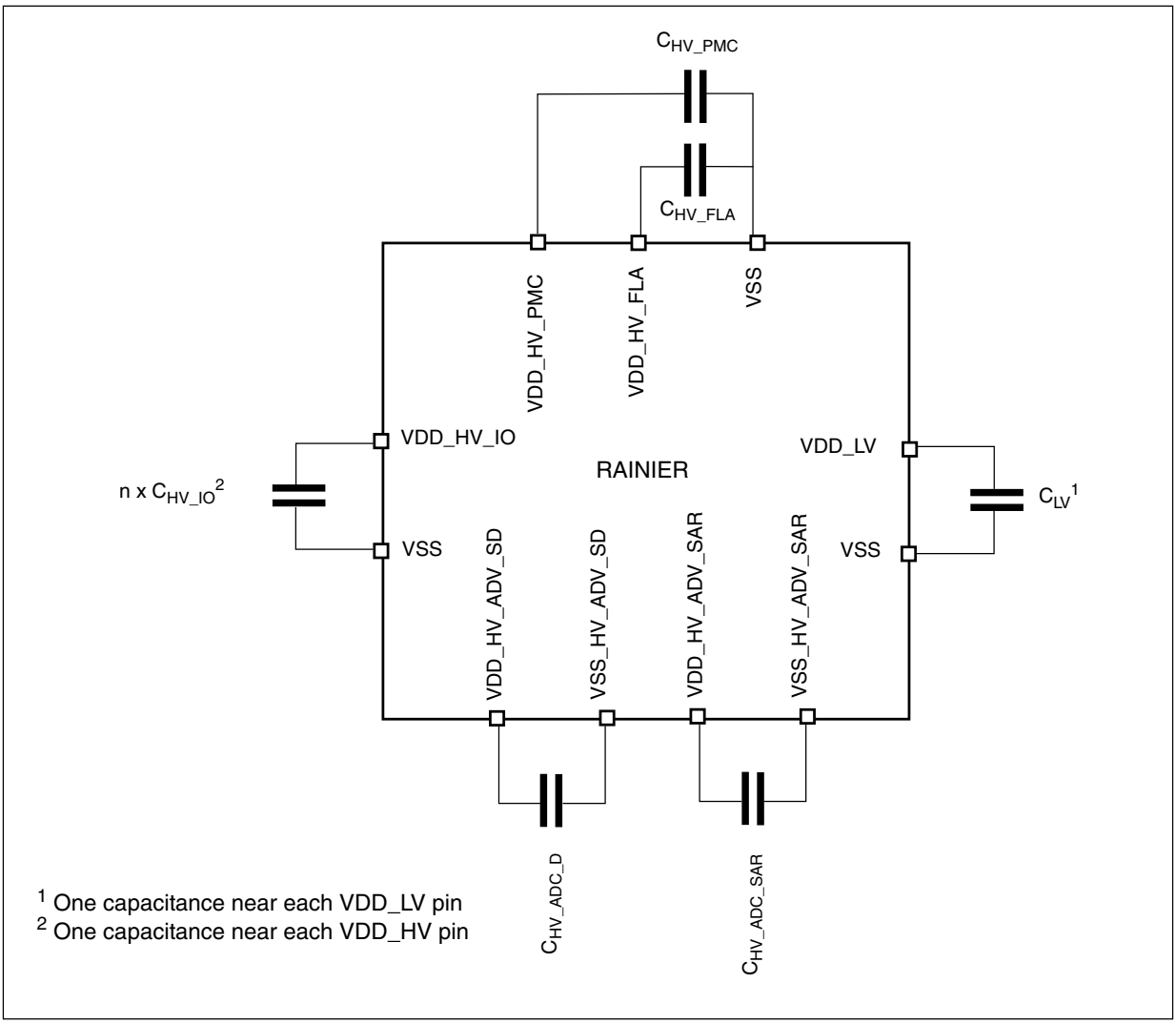


Figure 17. Recommended supply pin circuits

The following table describes the supply stability capacitances required on the device for proper operation.

Table 28. Device power supply integration

Symbol	Parameter	Conditions	Value[1]			Unit
			Min	Typ	Max	
C_{LV}	Minimum V_{DD_LV} external bulk capacitance, [2, 3]	—	4.7	—	—	µF
C_{HV_PMC}	Minimum $V_{DD\_HV\_PMC}$ external bulk capacitance [2, 4]	—	4.7	—	—	µF
C_{HV_IO}	Minimum VDD_HV_IO external capacitance[2]	—	4.7	—	—	µF
C_{HV_FLA}	Minimum $V_{DD\_HV\_FLA}$ external capacitance, [5]	—		2.0		µF
$C_{HV\_ADC\_SAR}$	Minimum $V_{DD\_HV\_ADV\_SAR}$ external capacitance, [6]		10	—	—	µF

Table continues on the next page...

Table 28. Device power supply integration (continued)

Symbol	Parameter	Conditions	Value[1]			Unit
			Min	Typ	Max	
$C_{HV\_ADC\_SD}$	Minimum $V_{DD\_HV\_ADV\_SD}$ external capacitance[7]		1	2.2	—	µF

1. See the above figure for capacitor integration.
2. Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over process, voltage, temperature, and aging.
3. Each V_{DD_LV} pin requires both a 47nF and 0.01µF capacitor for high-frequency bypass and EMC requirements. Remaining capacitance to meet minimum CLV requirement should be placed near the emitter of NPN ballast (if using internal regulation mode), or it should be evenly distributed across VDD_LV pins (if using external regulation mode).
4. Each $V_{DD\_HV\_PMC}$ pin requires both a 47nF and 0.01µF capacitor for high-frequency bypass and EMC requirements.
5. The recommended flash regulator composition capacitor is 1.5µF typical X7R or X5R, with -50% and +35% as min and max. This puts the min cap at 0.75 µF.
6. For noise filtering it is recommended to add high frequency bypass capacitors of three each 0.1 µF and three each 1nF between $V_{DD\_HV\_ADV\_SAR}$ and $V_{SS\_HV\_ADV\_SAR}$. These capacitors need to be placed very close to the MCU pins/balls to have minimum PCB routing between pin/ball and the capacitors.
7. For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $V_{DD\_HV\_ADV\_SD}$ and $V_{SS\_HV\_ADV\_SD}$.

16.1.3 Regulator example for the NJD2873 transistor

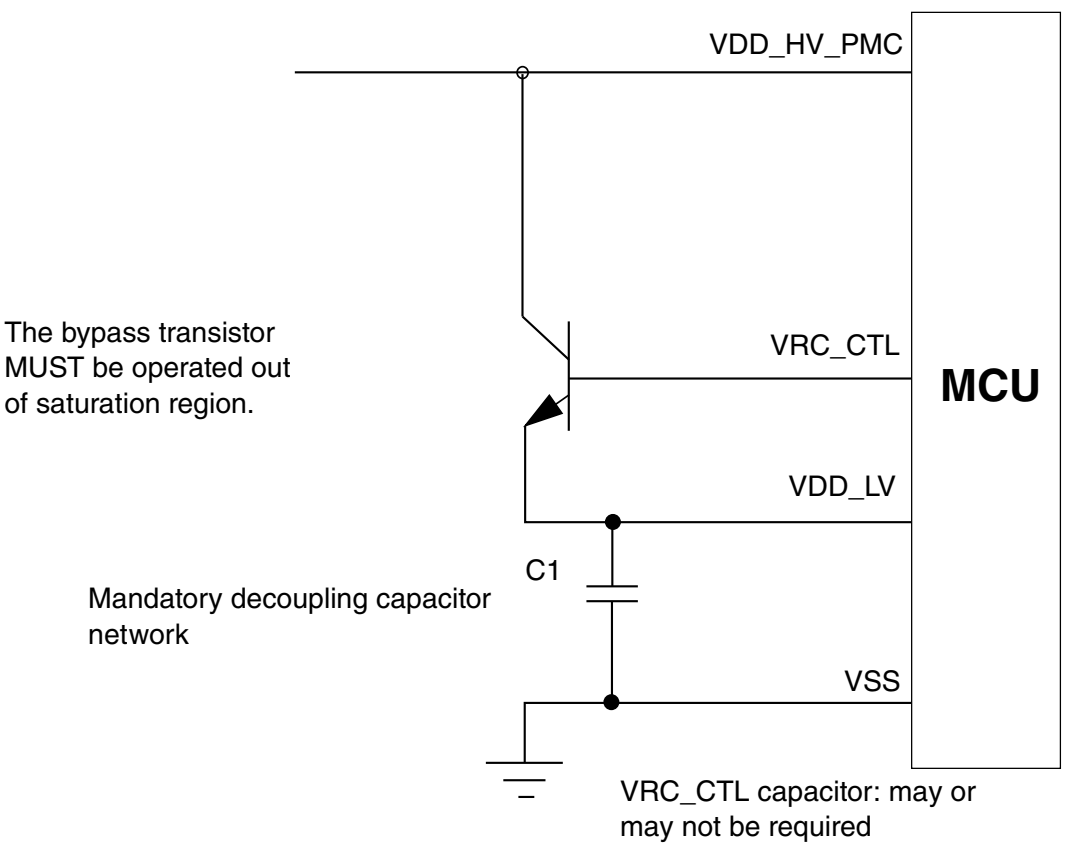


Figure 18. Regulator example

16.1.4 Regulator example for the 2SCR574d transistor

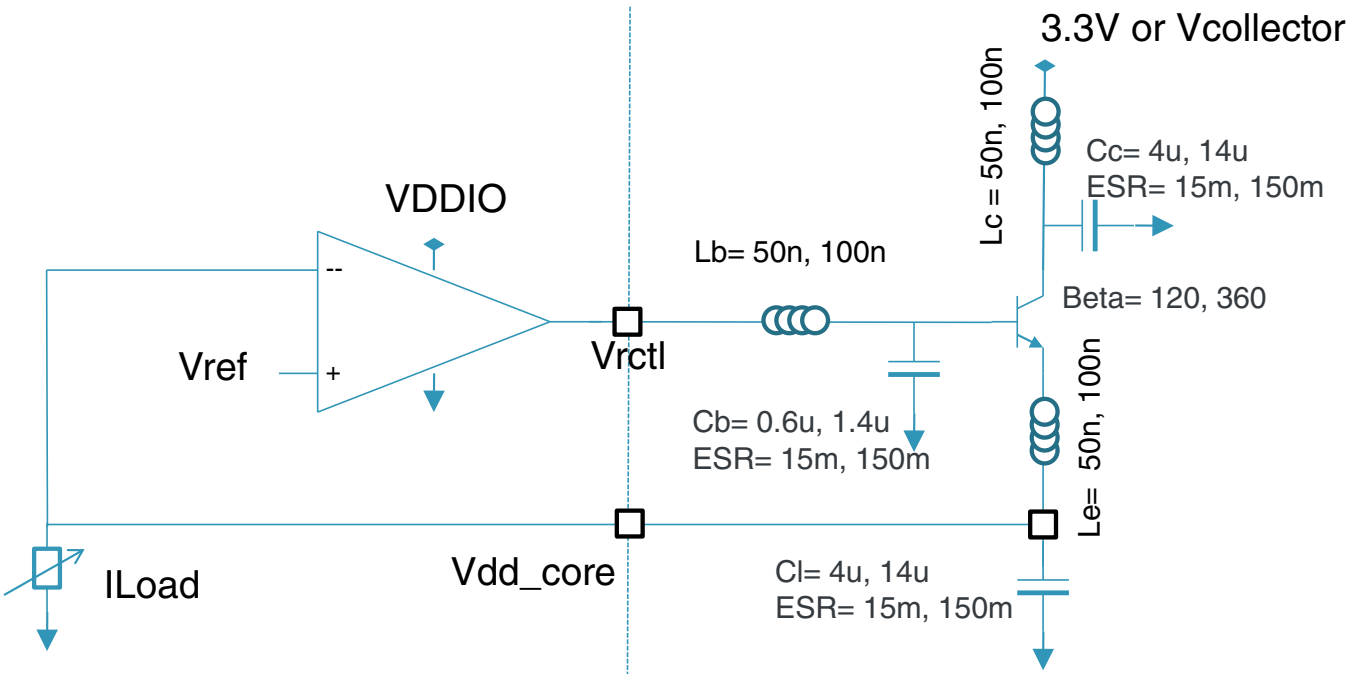


Figure 19. Regulator example

16.1.5 Device voltage monitoring

The LVD/HVDs for the device and their levels are given in the following table. Voltage monitoring threshold definition is provided in the following figure.

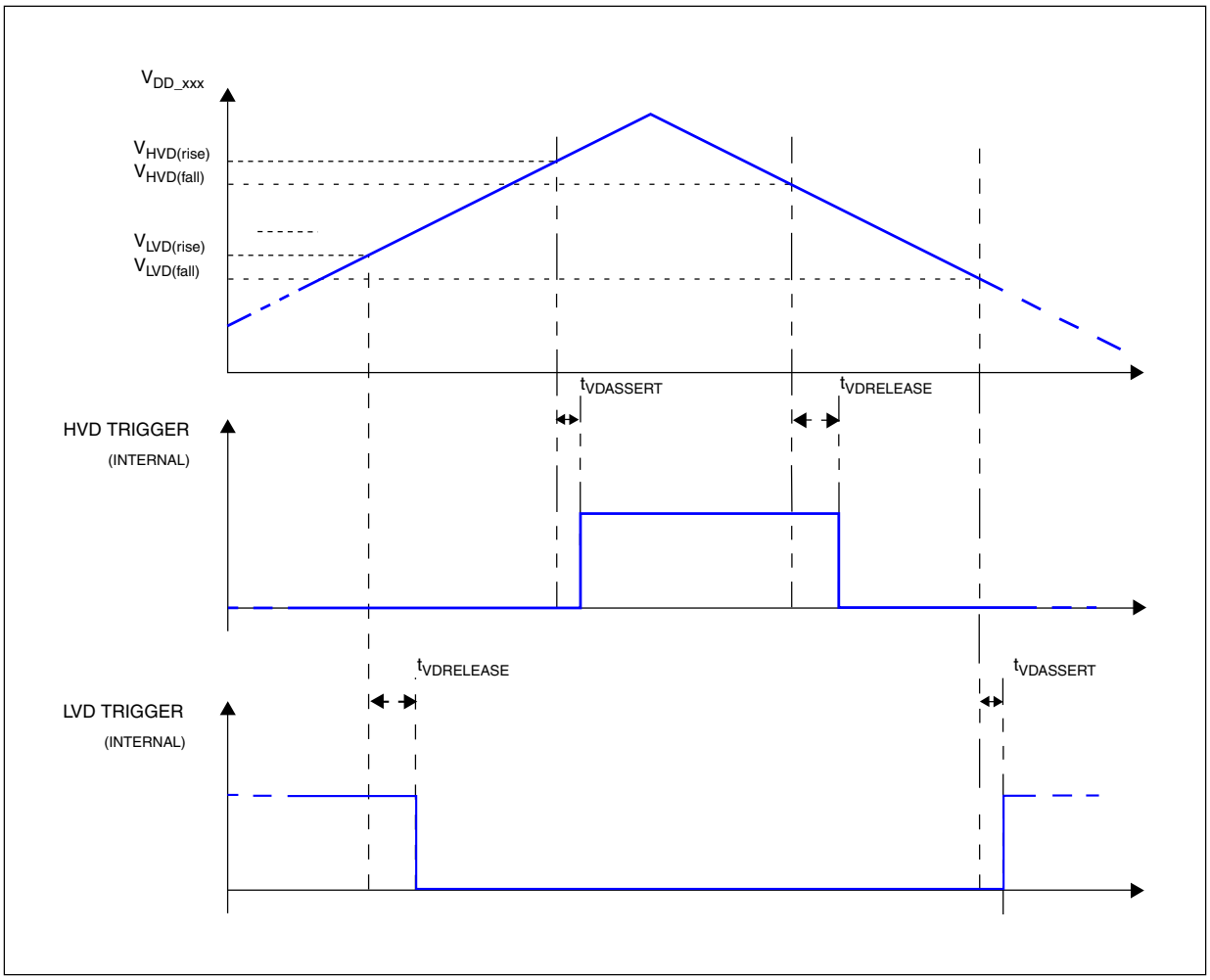


Figure 20. Voltage monitor threshold definition

For V_{DD_LV} levels, a maximum of 30 mV IR drop is incurred from the pin to all sinks on the die. For other LVD, the IR drop is estimated by multiplying the supply current by 0.5 ohm.

LVD is released after $t_{VDRELEASE}$ temporization when upper threshold is crossed, LVD is asserted $t_{VDASSERT}$ after detection when lower threshold is crossed.

HVD is released after $t_{VDRELEASE}$ temporization when lower threshold is crossed, HVD is asserted $t_{VDASSERT}$ after detection when upper threshold is crossed.

Table 29. Voltage monitor electrical characteristics

Symbol	Parameter	Conditions	Configuration			Value			Unit
			Trim bits	Mask Opt.	Pow. Up	Min	Typ	Max	
POR085_c[1]	LV internal supply power on reset	Rising voltage (power up)	N/A	No	Enab.	870	920	970	mV
		Falling voltage (power down)				850	900	950	

Table continues on the next page...

Table 29. Voltage monitor electrical characteristics (continued)

Symbol	Parameter	Conditions	Configuration			Value			Unit
			Trim bits	Mask Opt.	Pow. Up	Min	Typ	Max	
POR098_c	LV internal supply power on reset	Rising voltage (power up)	N/A	No	Enab.	960	1010	1060	mV
		Falling voltage (power down)				940	990	1040	
LVD_core_hot	LV internal[2] supply low voltage monitoring	Rising voltage (trimmed)	6bit	No	Enab.	1146	1169	1193	mV
		Falling voltage (trimmed)				1146	1169	1193	
LVD_core_cold	LV external[3] supply low voltage monitoring	Rising voltage	6bit	Yes	Disab.	1161	1185	1208	mV
		Falling voltage				1161	1185	1208	
HVD_core	LV internal cold supply high voltage monitoring	Rising voltage	6bit	Yes	Disab.	1353	1395	1438	mV
		Falling voltage				1343	1385	1438	
LVD_HV	HV internal supply low voltage monitoring	Rising voltage (trimmed)	6bit	No	Enab.	3300	3400	3500	mV
		Falling voltage (trimmed)				3270	3370	3470	
HVD_HV	HV internal supply high voltage monitoring	Rising voltage	6bit	Yes	Disab.	5530	5700	5870	mV
		Falling voltage				5500	5670	5840	
LVD_IO	Main IO and RC oscillator supply voltage monitoring	Rising voltage (trimmed)	6bit	No	Enab.	3300	3400	3500	mV
		Falling voltage (trimmed)				3270	3370	3470	
LVD_SAR	SAR ADC supply low voltage monitoring	Rising voltage	6bit	Yes	Disab.	2820	2910	3000	mV
		Falling voltage				2790	2880	2970	
$t_{VDASSERT}$	Voltage detector threshold crossing assertion	—	—	—	—	0.1	—	2.0	µs
$t_{VDRELEASE}$	Voltage detector threshold crossing de-assertion	—	—	—	—	5	—	20	µs

1. POR085_c and POR096_c threshold are untrimmed value, before the completion of the power-up sequence. All other LVD/HVD thresholds are provided after trimming.
2. LV internal supply levels are measured on device internal supply grid after internal voltage drop.
3. LV external supply levels are measured on the die size of the package bond wire after package voltage drop.

16.1.6 Power up/down sequencing

The following shows the constraints and relationships for the different power supplies.

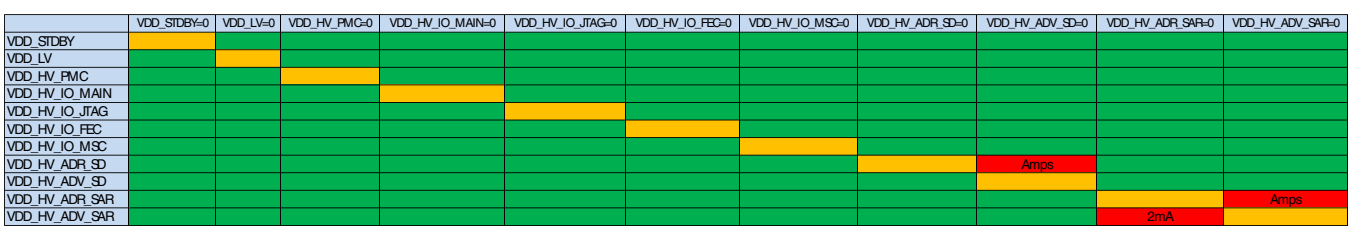


Figure 21. Device supply relation during power-up/power-down sequence

Each column indicates that the corresponding supply is 0 and the other supplies are UP. For example, the "Amps" cell in the "$V_{DD\_HV\_ADV\_SD}$=0" column shows that when $V_{DD\_HV\_ADR\_SD}$ supply is 0 and all other supplies are UP, this supply has a current in Amp flowing into $V_{DD\_HV\_ADR\_SD}$.

17 Flash memory specifications

17.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 30 shows the estimated Program/Erase times.

Table 30. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.

5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

17.2 Flash memory Array Integrity and Margin Read specifications

Table 31. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

17.3 Flash memory module life specifications

Table 32. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years

Table continues on the next page...

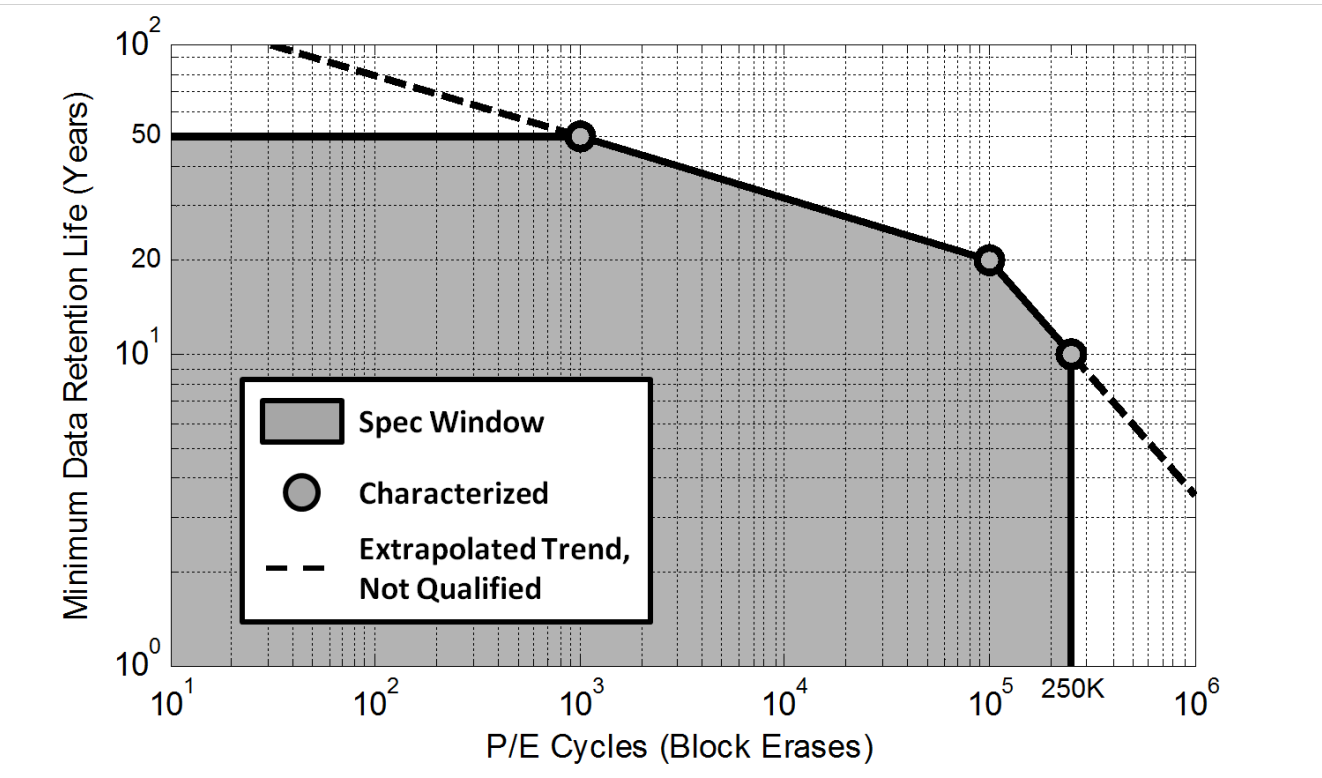
Table 32. Flash memory module life specifications (continued)

Symbol	Characteristic	Conditions	Min	Typical	Units
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

17.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



17.5 Flash memory AC timing specifications

Table 33. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

17.6 Flash read wait state and address pipeline control settings

Table 34 describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the C55FMC array at 150 °C.

Table 34. Flash Read Wait State and Address Pipeline Control Guidelines

Operating Frequency f_{SYS}	RWSC	APC	Flash read latency on mini-cache miss (# of f_{SYS} clock periods)	Flash read latency on mini-cache hit (# of f_{SYS} clock periods)
30 MHz	0	0	3	1
100 MHz	2	1	5	1
133 MHz	3	1	6	1
167 MHz	4	1	7	1
200 MHz	5	2	8	1

18 AC specifications

18.1 Debug and calibration interface timing

18.1.1 JTAG interface timing

These specifications apply to JTAG boundary scan only. See Table 36 for functional specifications.

Table 35. JTAG pin AC electrical characteristics

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{JCYC}	TCK cycle time	100	—	ns
2	t_{JDC}	TCK clock pulse width	40	60	ns
3	$t_{TCKRISE}$	TCK rise and fall times	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	TCK low to TDO data valid	—	16[1]	ns

Table continues on the next page...

Table 35. JTAG pin AC electrical characteristics (continued)

#	Symbol	Characteristic	Value		Unit
			Min	Max	
7	t_{TDOI}	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	TCK falling edge to output valid	—	600[2]	ns
12	t_{BSDVZ}	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	TCK rising edge to boundary scan input invalid	15	—	ns

1. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
2. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

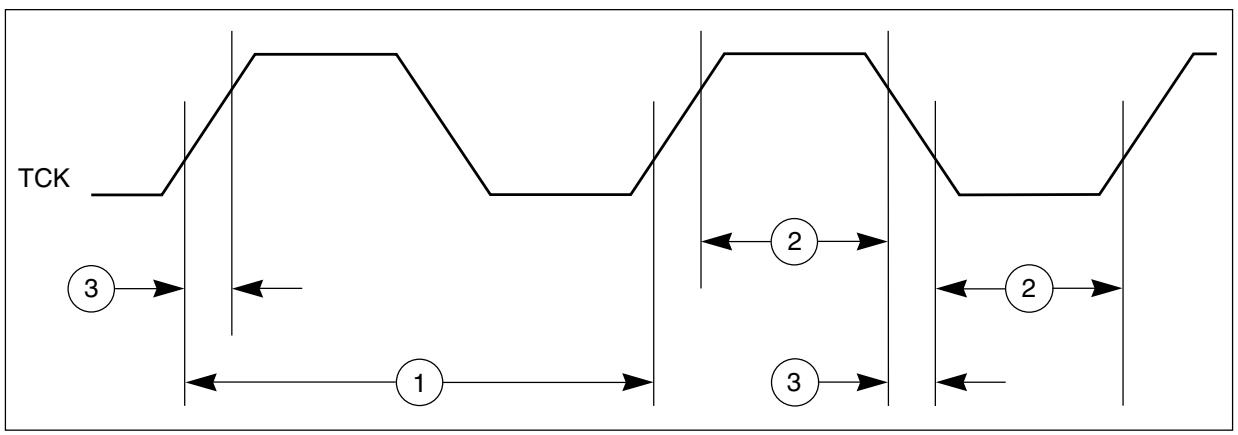


Figure 22. JTAG test clock input timing

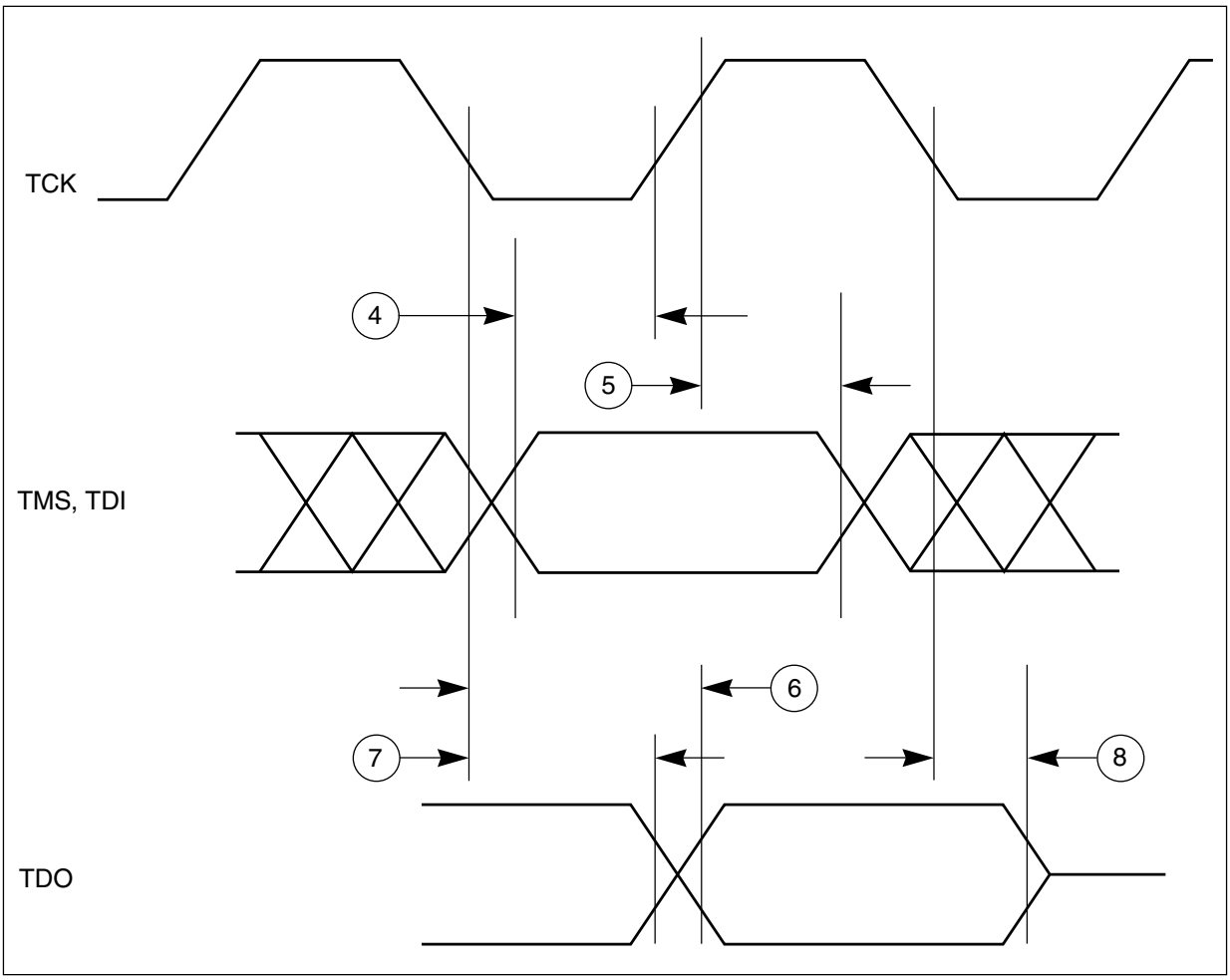


Figure 23. JTAG test access port timing

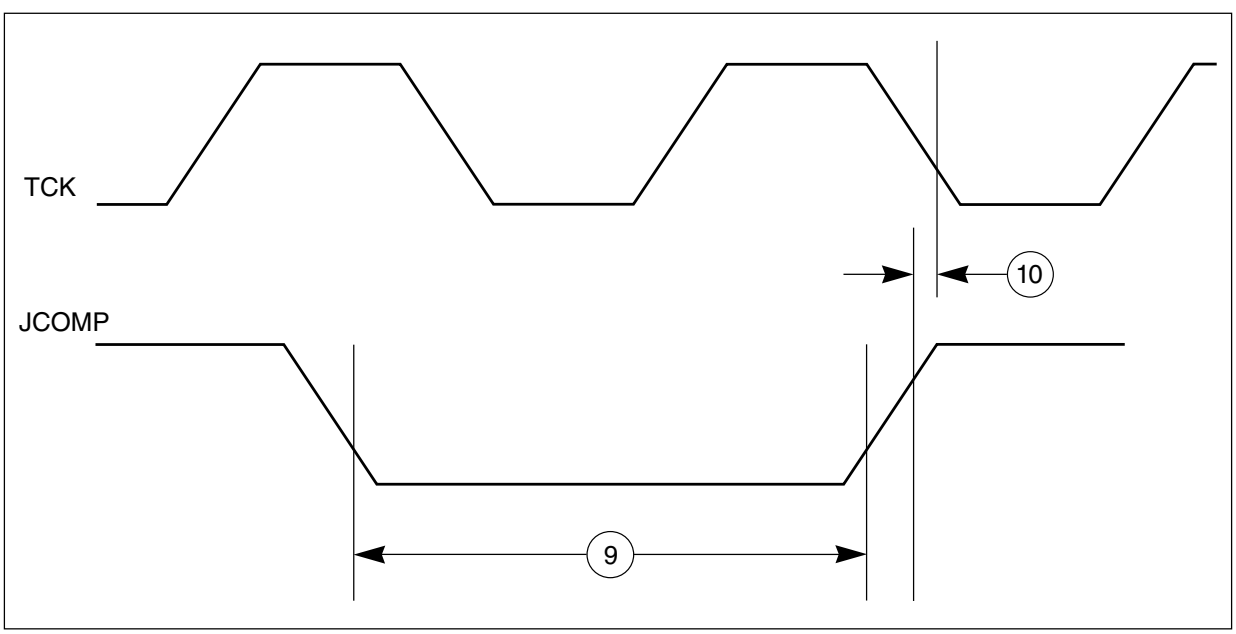


Figure 24. JTAG JCOMP timing

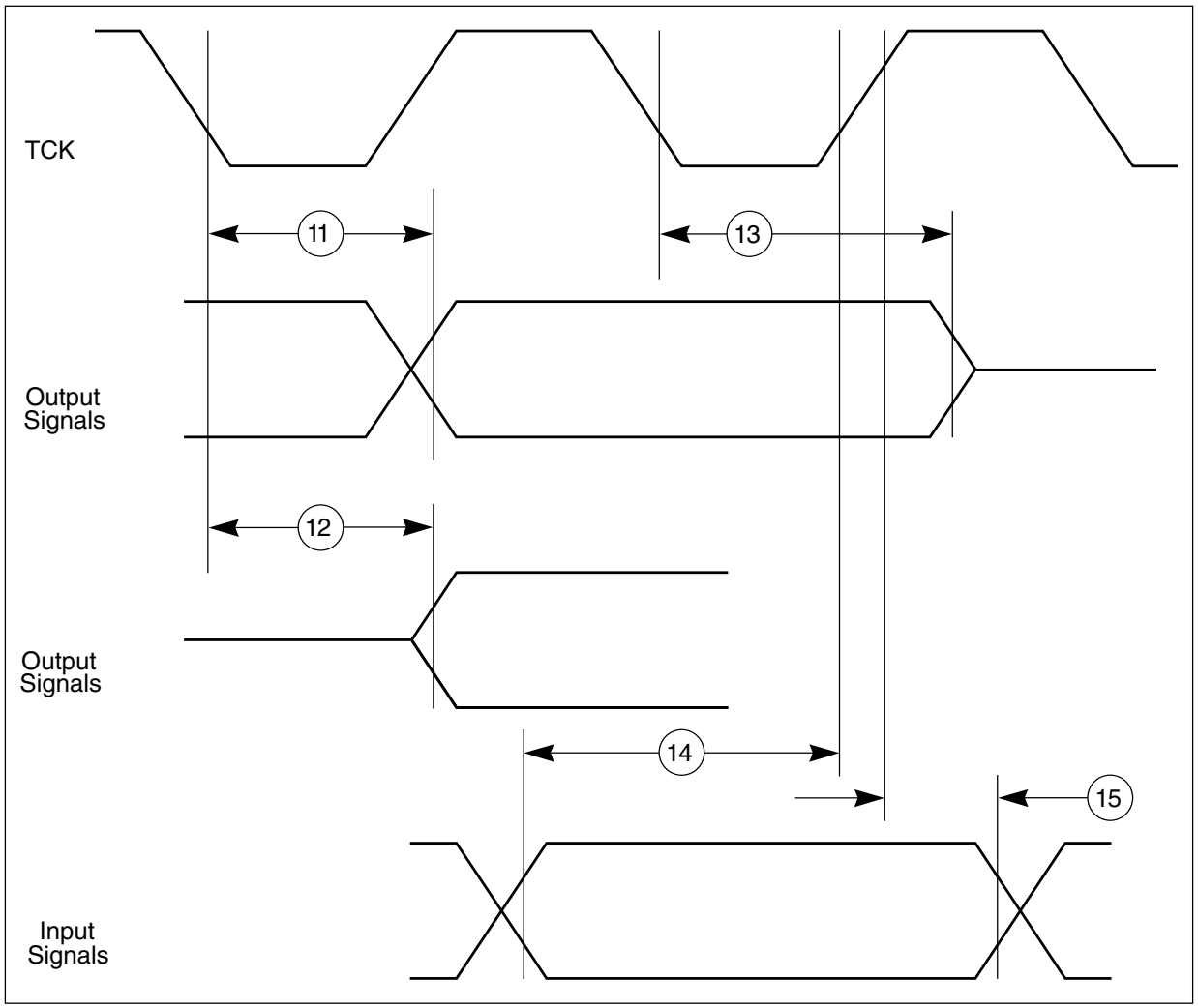


Figure 25. JTAG boundary scan timing

18.1.2 Nexus interface timing

Nexus timing specified for the whole V_{DD_LV} and $V_{DD\_HV\_IO}$ dynamic, $T_A = T_L$ to T_H, and maximum loading per pad type as specified in the I/O section of the data sheet.

Table 36. Nexus debug port timing

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{EVTIPW}	$\overline{EVTI}$ Pulse Width	4	—	t_{CYC}[1]
2	t_{EVTOPW}	$\overline{EVTO}$ Pulse Width	40	—	ns
3	t_{TCYC}	TCK cycle time	4[2, 3]	—	t_{CYC}[1]
4	t_{TCYC}	Absolute minimum TCK cycle time[4] (TDO sampled on posedge of TCK)	40[5]	—	ns

Table continues on the next page...

Table 36. Nexus debug port timing (continued)

#	Symbol	Characteristic	Value		Unit
			Min	Max	
		Absolute minimum TCK cycle time[6] (TDO sampled on negedge of TCK)	20[5]	—	
5	t_{NTDIS}	TDI data setup time	5	—	ns
6	t_{NTDIH}	TDI data hold time	5	—	ns
7	t_{NTMSS}	TMS data setup time	5	—	ns
8	t_{NTMSH}	TMS data hold time	5	—	ns
9	—	TDO propagation delay from falling edge of TCK[7]	—	16	ns
10	—	TDO hold time with respect to TCK falling edge (minimum TDO propagation delay)	2.25	—	ns

1. t_{CYC} is system clock period.
2. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual peripheral frequency being used. To ensure proper operation TCK frequency should be set to the peripheral frequency divided by a number greater than or equal to that specified here.
3. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
4. This value is TDO propagation time 36ns + 4ns setup time to sampling edge.
5. This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.
6. This value is TDO propagation time 16ns + 4ns setup time to sampling edge.
7. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.

Figure 26. Nexus output timing

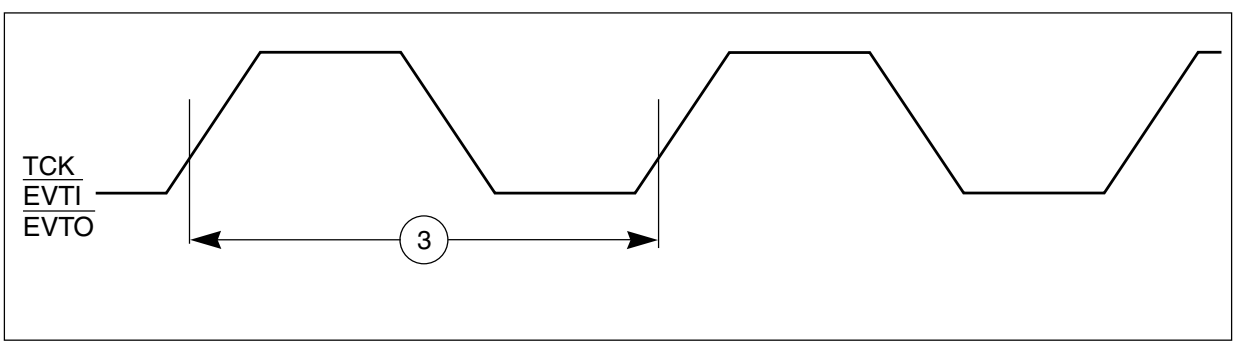


Figure 27. Nexus event trigger and test clock timings

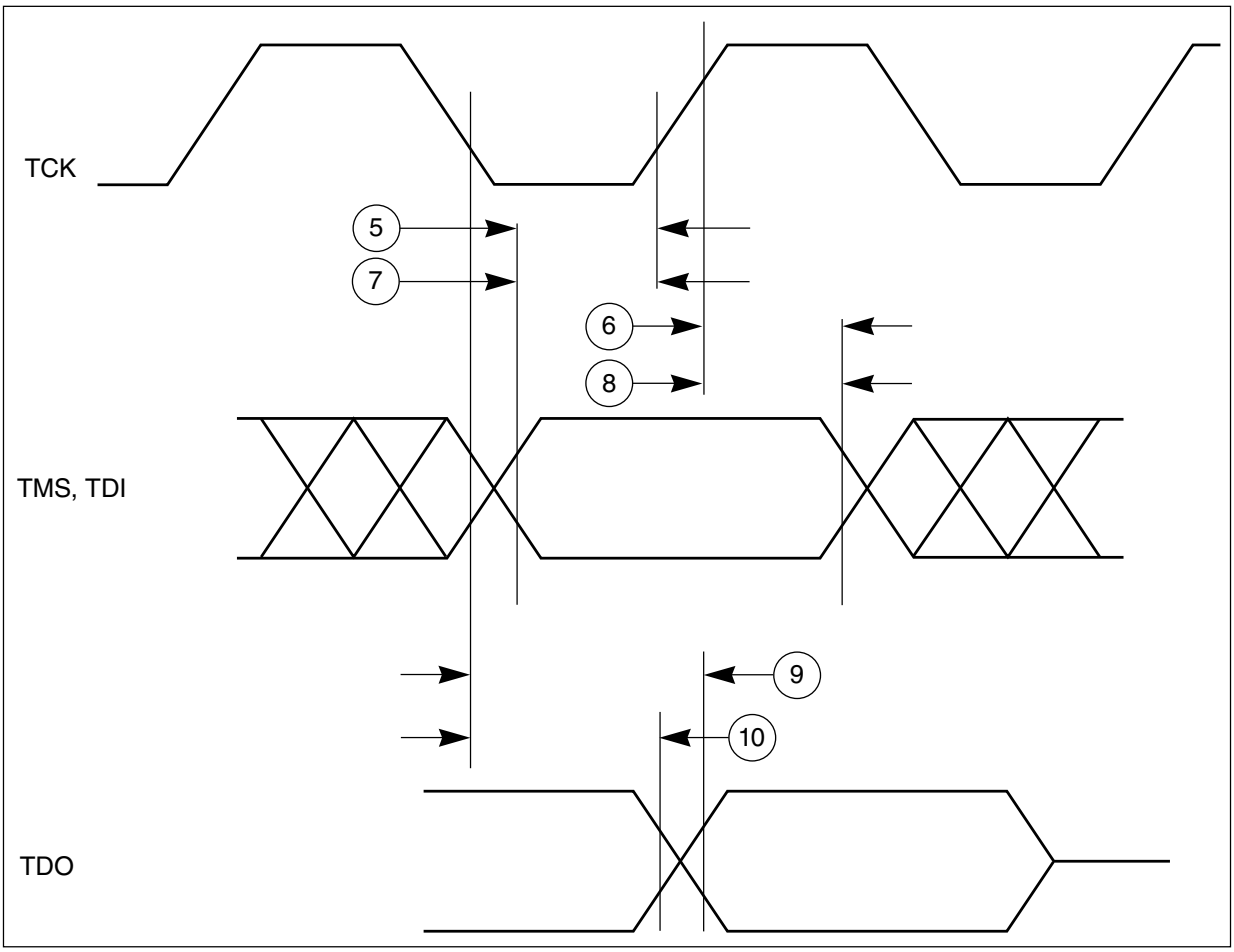


Figure 28. Nexus TDI, TMS, TDO timing

18.1.3 Aurora LVDS interface timing

Table 37. Aurora LVDS interface timing specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
Data Rate					
—	Data rate	—		1250	Mbps
STARTUP					
t_{STRT_BIAS}	Bias startup time[1]	—	—	5	µs
t_{STRT_TX}	Transmitter startup time[2]	—	—	5	µs
t_{STRT_RX}	Receiver startup time[3]	—	—	4	µs

1. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.
2. Startup time is defined as the time taken by LVDS transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

3. Startup time is defined as the time taken by LVDS receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

18.1.3.1 Aurora debug port timing

Table 38. Aurora debug port timing

#	Symbol	Parameter		Value		Unit
				Min	Max	
1	t_{REFCLK}	Reference clock frequency		625	1200	MHz
1a	t_{MCYC}	Reference clock rise/fall time		—	400	ps
2	t_{RCDC}	Reference clock duty cycle		45	55	%
3	J_{RC}	Reference clock jitter		—	40	ps
4	$t_{STABILITY}$	Reference clock stability		50	—	PPM
5	BER	Bit error rate		—	10^{-12}	—
6	J_D	Transmit lane deterministic jitter		—	0.17	OUI
7	J_T	Transmit lane total jitter		—	0.35	OUI
8	S_O	Differential output skew		—	20	ps
9	S_{MO}	Lane to lane output skew		—	1000	ps
10	OUI	Aurora lane unit interval[1]	625 Mbps	1600	1600	ps
			1.25Gbps	800	800	ps

1. ± 100 PPM

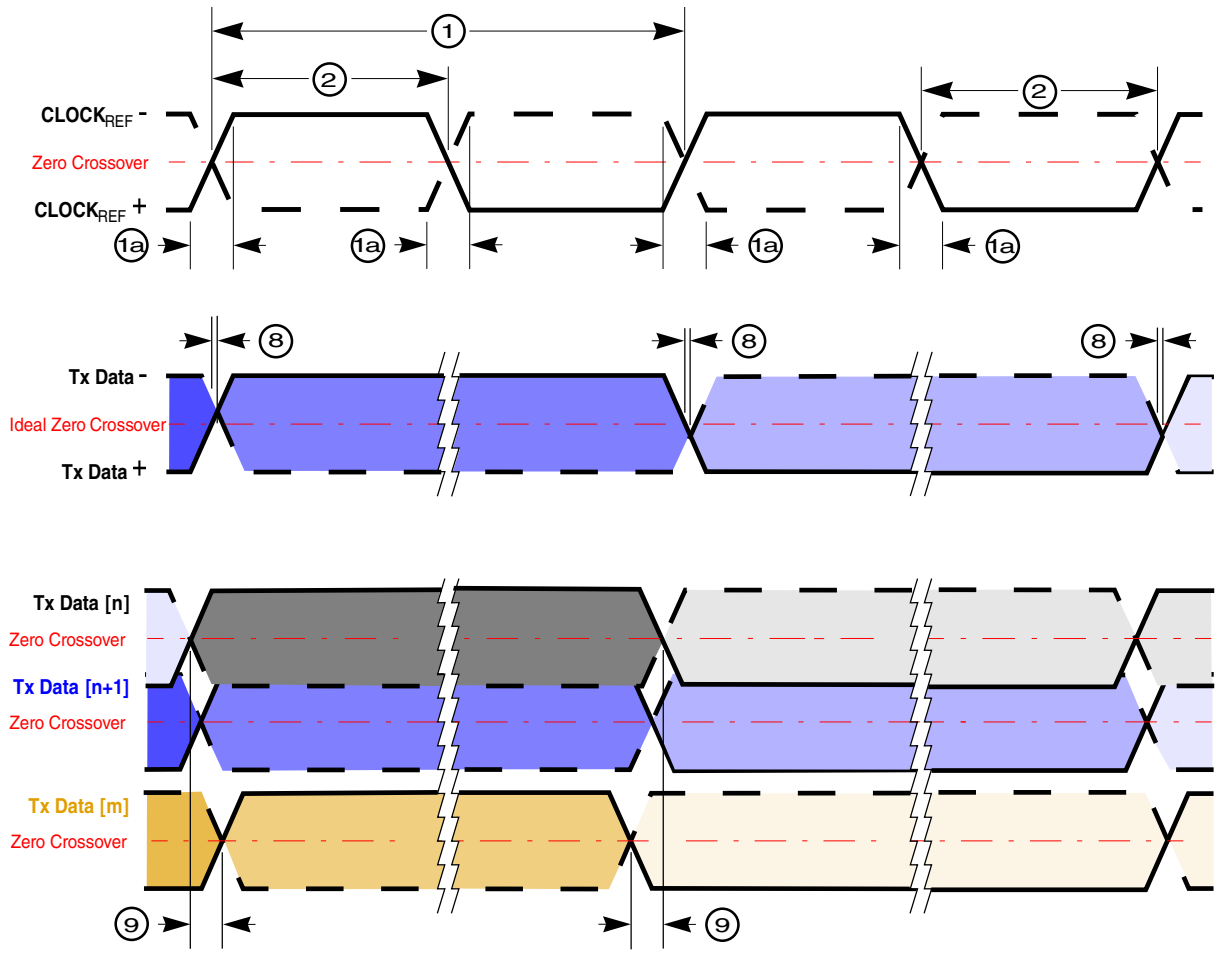


Figure 29. Aurora timings

18.2 DSPI timing with CMOS and LVDS

DSPI in TSB mode with LVDS pads can be used to implement Micro Second Channel bus protocol.

DSPI channel frequency support is shown in Table 39. Timing specifications are shown in Table 40, Table 41, Table 42, Table 43, Table 44.

Table 39. DSPI channel frequency support

DSPI use mode		Max usable frequency (MHz)[1],[2]
CMOS (Master mode)	Full duplex – Classic timing (Table 40)	17
	Full duplex – Modified timing (Table 41)	30
	Output only mode (SCK/SOUT/PCS) (Table 40 and Table 41)	30
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 44)	30
LVDS (Master mode)	Full duplex – Modified timing (Table 42)	40

1. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
2. Maximum usable frequency does not take into account external device propagation delay.

18.2.1 DSPI master mode full duplex timing with CMOS and LVDS pads

The values presented in these sections are target values. A complete performance characterization of the pads (in all configuration combinations) is required before the final specifications can be released.

18.2.1.1 DSPI CMOS master mode – classic timing

All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

NOTE

In Table 40, all output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Table 40. DSPI CMOS master classic timing (full duplex and output only) - MTFE = 0, CPHA = 0 or 1

#	Symbol	Characteristic	Condition		Value[1]		Unit
			Pad drive[2]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	SCK drive strength				
			Very strong	25 pF	33.0	—	ns
			Strong	50 pF	80.0	—	
			Medium	50 pF	200.0	—	
2	t_{CSC}	PCS to SCK delay	SCK and PCS drive strength				
			Very strong	25 pF	(N^3 x t_{SYS}, 4) - 16	—	ns
			Strong	50 pF	(N^3 x t_{SYS}, 4) - 16	—	
			Medium	50 pF	(N^3 x t_{SYS}, 4) - 16	—	
			PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	(N^3 x t_{SYS}, 4) - 29	—	
3	t_{ASC}	After SCK delay	SCK and PCS drive strength				
			Very strong	PCS = 0 pF SCK = 50 pF	(M^5 x t_{SYS}4) - 35	—	ns
			Strong	PCS = 0 pF SCK = 50 pF	(M^5 x t_{SYS}, 4) - 35	—	
			Medium	PCS = 0 pF SCK = 50 pF	(M^5 x t_{SYS}, 4) - 35	—	
			PCS medium and SCK strong	PCS = 0 pF	(M^5 x t_{SYS}, 4) - 35	—	

Table continues on the next page...

Table 40. DSPI CMOS master classic timing (full duplex and output only) - MTFE = 0, CPHA = 0 or 1 (continued)

#	Symbol	Characteristic	Condition		Value[1]		Unit
			Pad drive[2]	Load (C_L)	Min	Max	
				SCK = 50 pF			
4	t_{SDC}	SCK duty cycle[6]	SCK drive strength				
			Very strong	0 to 50 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	ns
			Strong	0 to 50 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	
			Medium	0 to 50 pF	$^1/_2t_{SCK}$ - 5	$^1/_2t_{SCK}$ + 5	
PCS strobe timing							
5	t_{PCSC}	PCSx to $\overline{PCSS}$ time[7]	PCS and PCSS drive strength				
			Strong	25 pF	13.0	—	ns
6	t_{PASC}	$\overline{PCSS}$ to PCSx time[7]	PCS and PCSS drive strength				
			Strong	25 pF	13.0	—	ns
SIN setup time							
7	t_{SUI}	SIN setup time to SCK[8]	SCK drive strength				
			Very strong	25 pF	25.0	—	ns
			Strong	50 pF	31.0	—	
			Medium	50 pF	52.0	—	
SIN hold time							
8	t_{HI}	SIN hold time from SCK[8]	SCK drive strength				
			Very strong	0 pF	-1.0	—	ns
			Strong	0 pF	-1.0	—	
			Medium	0 pF	-1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK[9]	SOUT and SCK drive strength				
			Very strong	25 pF	—	7.0	ns
			Strong	50 pF	—	8.0	
			Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK[9]	SOUT and SCK drive strength				
			Very strong	25 pF	-7.7	—	ns
			Strong	50 pF	-11.0	—	
			Medium	50 pF	-15.0	—	

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
3. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
4. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).

5. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. PCSx and PCSS using same pad configuration.
8. Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL voltage thresholds.
9. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

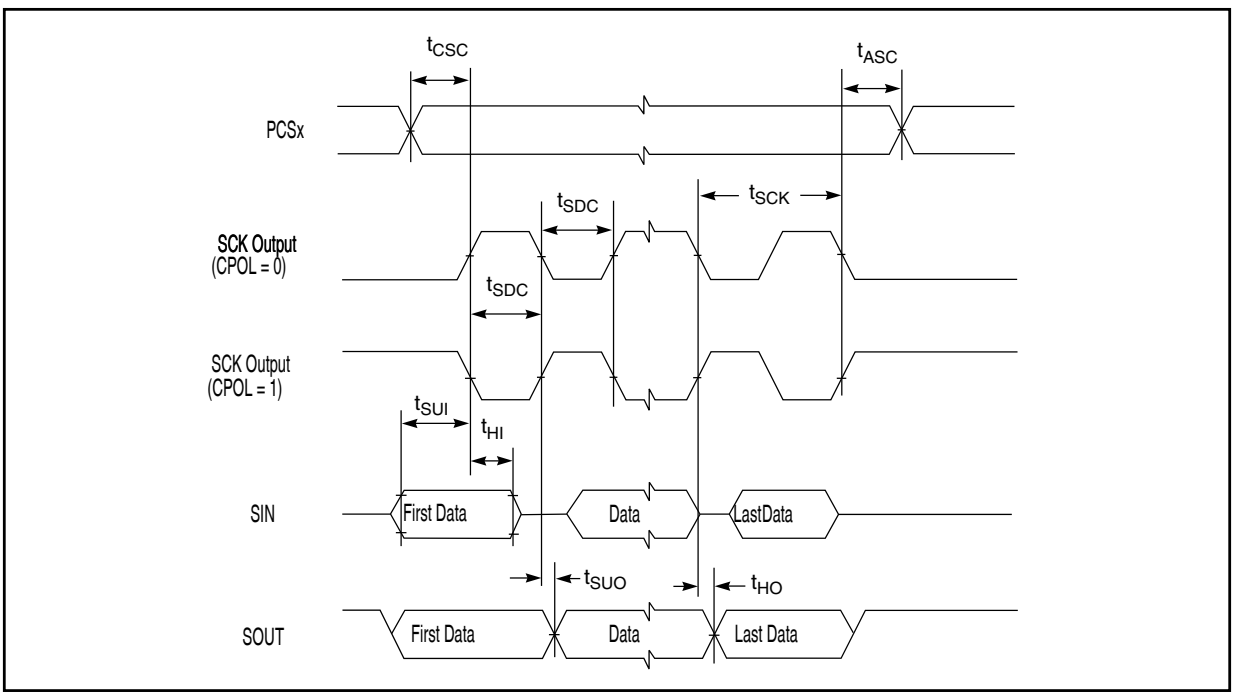


Figure 30. DSPI CMOS master mode – classic timing, CPHA = 0

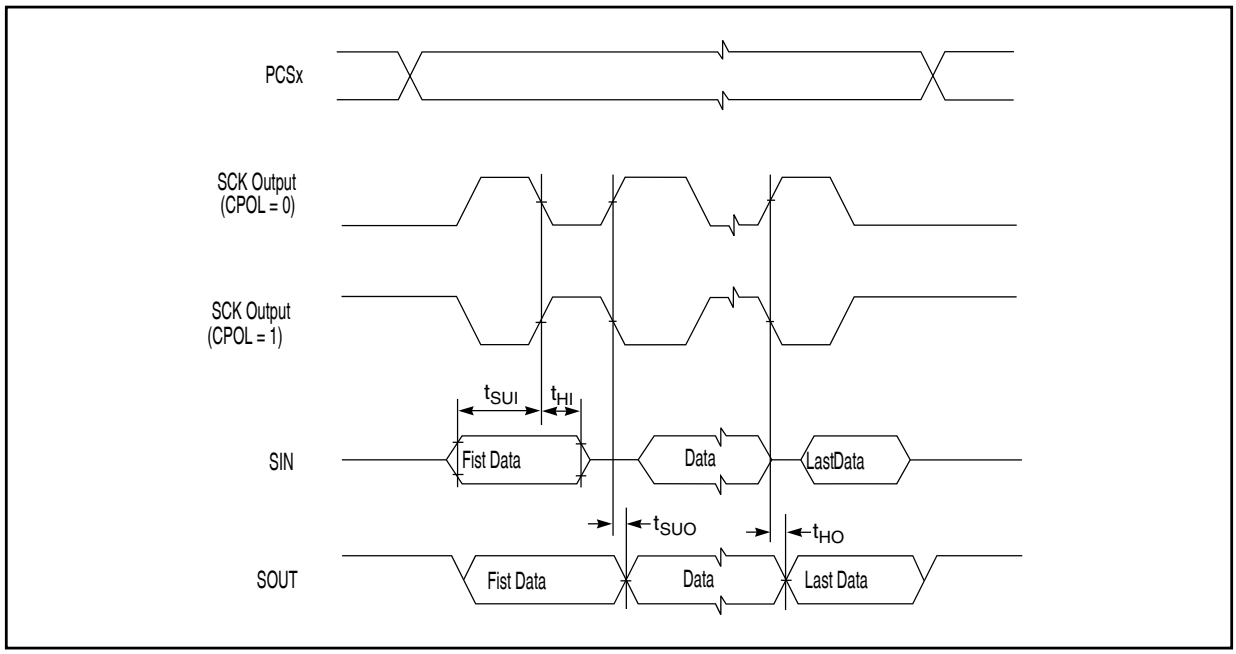


Figure 31. DSPI CMOS master mode – classic timing, CPHA = 1

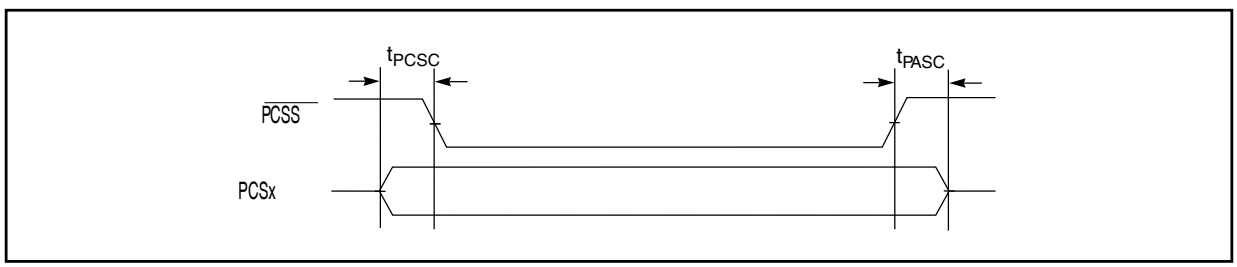


Figure 32. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)

18.2.1.2 DSPI CMOS master mode – modified timing

All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

NOTE

In Table 41, all output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Table 41. DSPI CMOS master modified timing (full duplex and output only) - MTFE = 1, CPHA = 0 or 1

#	Symbol	Characteristic	Condition		Value[1]		Unit
			Pad drive[2]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	SCK drive strength				
			Very strong	25 pF	33.0	—	ns
			Strong	50 pF	80.0	—	

Table continues on the next page...

Table 41. DSPI CMOS master modified timing (full duplex and output only) - MTFE = 1, CPHA = 0 or 1 (continued)

#	Symbol	Characteristic	Condition		Value[1]		Unit
			Pad drive[2]	Load (C_L)	Min	Max	
			Medium	50 pF	200.0	—	
2	t_{CSC}	PCS to SCK delay	SCK and PCS drive strength				
			Very strong	25 pF	(N^3 x t_{SYS}, [4]) - 16	—	ns
			Strong	50 pF	(N^3 x t_{SYS}, [4]) - 16	—	
			Medium	50 pF	(N^3 x t_{SYS}, [4]) - 16	—	
			PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	(N^3 x t_{SYS}, [4]) - 29	—	
3	t_{ASC}	After SCK delay	SCK and PCS drive strength				
			Very strong	PCS = 0 pF SCK = 50 pF	(M^5 x t_{SYS}[4]) - 35	—	ns
			Strong	PCS = 0 pF SCK = 50 pF	(M^5 x t_{SYS}, [4]) - 35	—	
			Medium	PCS = 0 pF SCK = 50 pF	(M^5 x t_{SYS}, [4]) - 35	—	
			PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	(M^5 x t_{SYS}, [4]) - 35	—	
4	t_{SDC}	SCK duty cycle[6]	SCK drive strength				
			Very strong	0 to 50 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	ns
			Strong	0 to 50 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	
			Medium	0 to 50 pF	$^1/_2t_{SCK}$ - 5	$^1/_2t_{SCK}$ + 5	
PCS strobe timing							
5	t_{PCSC}	PCSx to $\overline{PCSS}$ time[7]	PCS and PCSS drive strength				
			Strong	25 pF	13.0	—	ns
6	t_{PASC}	$\overline{PCSS}$ to PCSx time[7]	PCS and PCSS drive strength				
			Strong	25 pF	13.0	—	ns
SIN setup time							
7	t_{SUI}	SIN setup time to SCK CPHA = 0[8]	SCK drive strength				
			Very strong	25 pF	25 - (P^9 x t_{SYS}[4])	—	ns
			Strong	50 pF	31 - (P^9 x t_{SYS}, [4])	—	
			Medium	50 pF	52 - (P^9 x t_{SYS}, [4])	—	
		SIN setup time to SCK CPHA = 1[8]	SCK drive strength				
			Very strong	25 pF	25.0	—	ns
			Strong	50 pF	31.0	—	
			Medium	50 pF	52.0	—	
SIN hold time							
8	t_{HI}	SIN hold time from SCK	SCK drive strength				
			Very strong	0 pF	-1 + (P^8 x t_{SYS}, [3])	—	ns

Table continues on the next page...

Table 41. DSPI CMOS master modified timing (full duplex and output only) - MTFE = 1, CPHA = 0 or 1 (continued)

#	Symbol	Characteristic	Condition		Value[1]		Unit
			Pad drive[2]	Load (C_L)	Min	Max	
		CPHA = 0[9]	Strong	0 pF	-1 + (P[8] x t_{SYS}, [3])	—	
			Medium	0 pF	-1 + (P[8] x t_{SYS}, [3])	—	
		SIN hold time from SCK CPHA = 1[9]	SCK drive strength				
			Very strong	0 pF	-1.0	—	ns
			Strong	0 pF	-1.0	—	
			Medium	0 pF	-1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK CPHA = 0[9]	SOUT and SCK drive strength				
			Very strong	25 pF	—	7.0 + t_{SYS}[4]	ns
			Strong	50 pF	—	8.0 + t_{SYS}[4]	
			Medium	50 pF	—	16.0 + t_{SYS}[4]	
		SOUT data valid time from SCK CPHA = 1[9]	SOUT and SCK drive strength				
			Very strong	25 pF	—	7.0	ns
			Strong	50 pF	—	8.0	
			Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK CPHA = 0[10]	SOUT and SCK drive strength				
			Very strong	25 pF	-7.7 + t_{SYS}[4]	—	ns
			Strong	50 pF	-11.0 + t_{SYS}[4]	—	
			Medium	50 pF	-15.0 + t_{SYS}[4]	—	
		SOUT data hold time after SCK CPHA = 1[10]	SOUT and SCK drive strength				
			Very strong	25 pF	-7.7	—	ns
			Strong	50 pF	-11.0	—	
			Medium	50 pF	-15.0	—	

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
3. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
4. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
5. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. PCSx and PCSS using same pad configuration.
8. Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL voltage thresholds.

9. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.
10. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

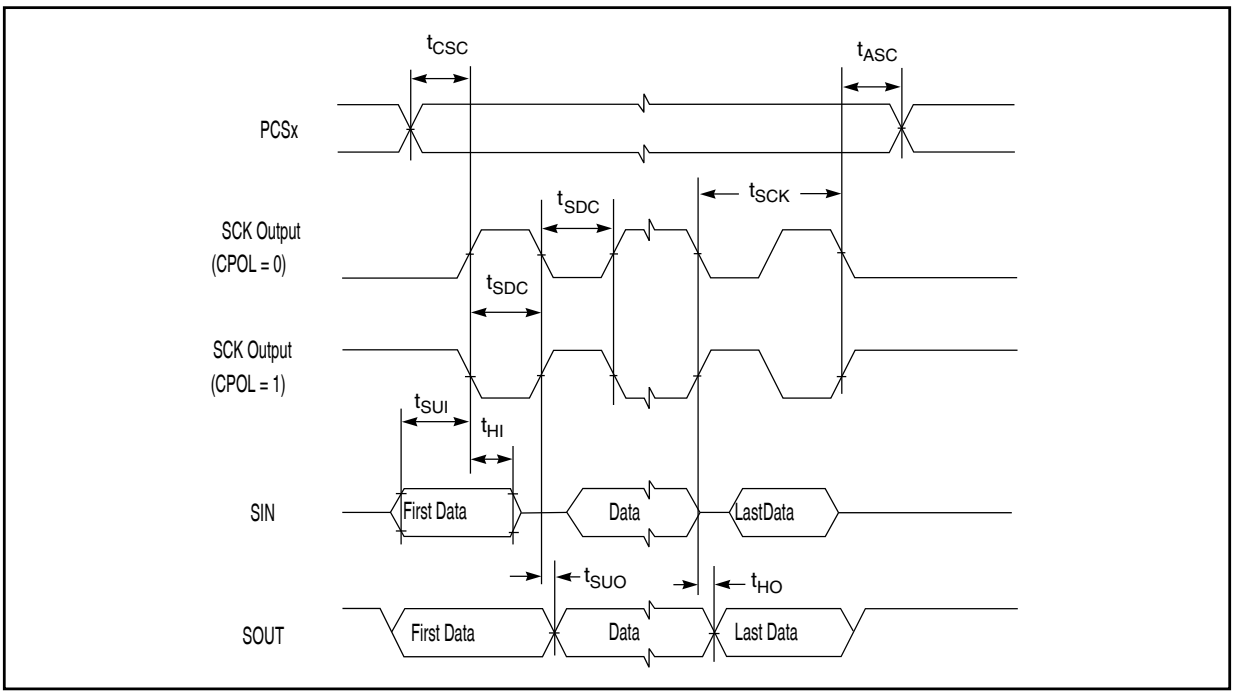


Figure 33. DSPI CMOS master mode – modified timing, CPHA = 0

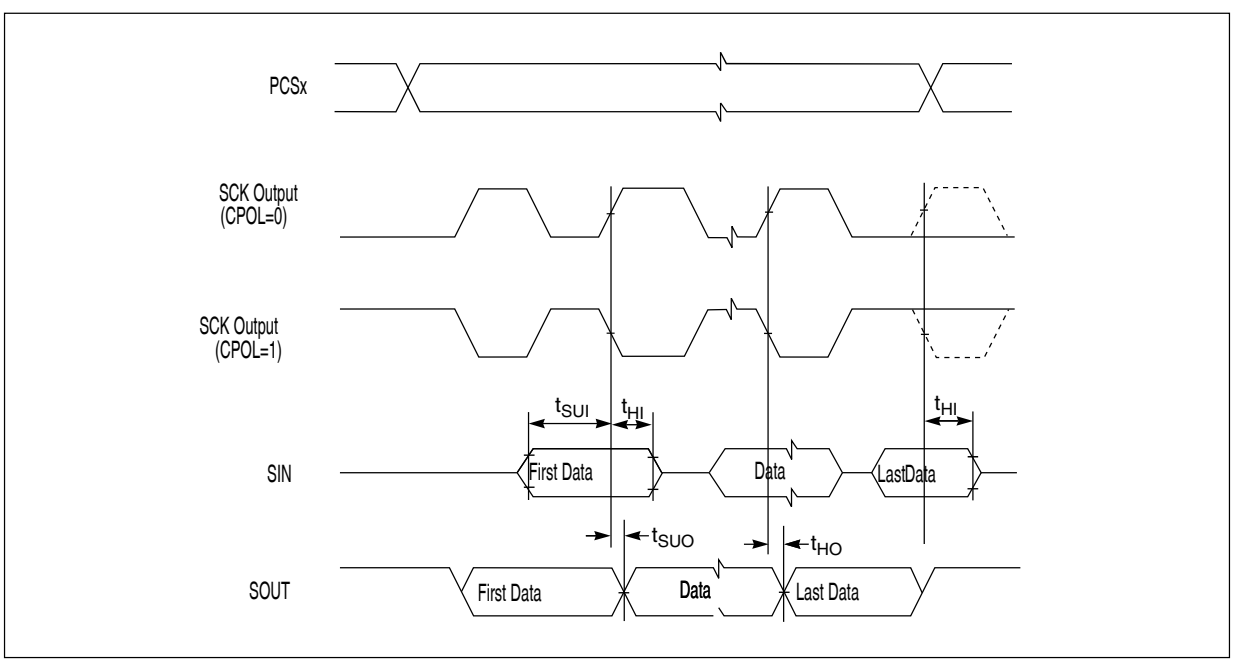


Figure 34. DSPI CMOS master mode – modified timing, CPHA = 1

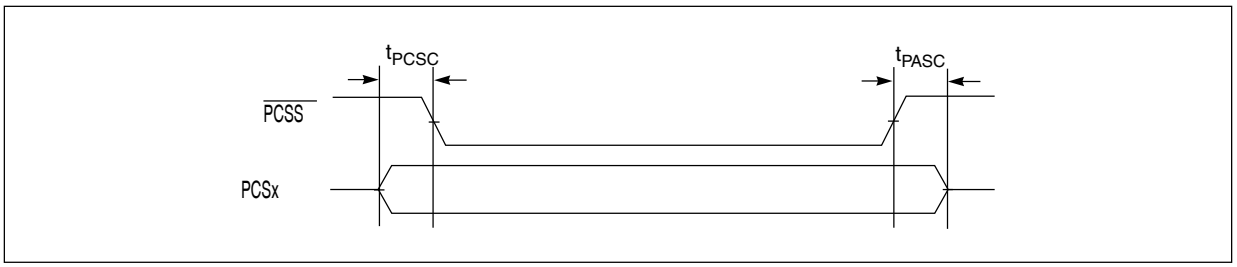


Figure 35. DSPI PCS strobe (PCSS) timing (master mode)1

18.2.1.3 DSPI LVDS master mode – modified timing

Table 42. DSPI LVDS master timing - full duplex - modified transfer format (MTFE = 1), CPHA = 0 or 1

#	Symbol	Characteristic	Condition		Value[1]		Unit
			Pad drive	Load	Min	Max	
1	t_{SCK}	SCK cycle time	LVDS	15 pF to 25 pF differential	30.0	—	ns
2	t_{CSC}	PCS to SCK delay (LVDS SCK)	PCS drive strength				
			Very strong	25 pF	$(N^2 \times t_{SYS}, ^3) - 10$	—	ns
			Strong	50 pF	$(N^2 \times t_{SYS}, ^3) - 10$	—	ns
			Medium	50 pF	$(N^2 \times t_{SYS}, ^3) - 32$	—	ns
3	t_{ASC}	After SCK delay (LVDS SCK)	Very strong	PCS = 0 pF SCK = 25 pF	$(M^4 \times t_{SYS}^3) - 8$	—	ns
			Strong	PCS = 0 pF SCK = 25 pF	$(M^4 \times t_{SYS}, ^3) - 8$	—	ns
			Medium	PCS = 0 pF SCK = 25 pF	$(M^4 \times t_{SYS}, ^3) - 8$	—	ns
4	t_{SDC}	SCK duty cycle[5]	LVDS	15 pF to 25 pF differential	$^1/_2 t_{SCK} - 2$	$^1/_2 t_{SCK} + 2$	ns
7	t_{SUI}	SIN setup time					
		SIN setup time to SCK CPHA = 0[6]	SCK drive strength				
			LVDS	15 pF to 25 pF differential	$23 - (P^7 \times t_{SYS}^3)$	—	ns
		SIN setup time to SCK CPHA = 1[6]	SCK drive strength				
			LVDS	15 pF to 25 pF differential	23	—	ns
8	t_{HI}	SIN Hold Time					

Table continues on the next page...

Table 42. DSPI LVDS master timing - full duplex - modified transfer format (MTFE = 1), CPHA = 0 or 1 (continued)

#	Symbol	Characteristic	Condition		Value[1]		Unit
			Pad drive	Load	Min	Max	
		SIN hold time from SCK CPHA = 0[6]	SCK drive strength				
			LVDS	0 pF differential	-1 + (P[7] x t_{SYS}, [3])	—	ns
		SIN hold time from SCK CPHA = 1[6]	SCK drive strength				
			LVDS	0 pF differential	-1	—	ns
9	t_{SUO}	SOUT data valid time (after SCK edge)					
		SOUT data valid time from SCK CPHA = 0[8]	SOUT and SCK drive strength				
			LVDS	15 pF to 25 pF differential	—	7.0 + t_{SYS}[3]	ns
		SOUT data valid time from SCK CPHA = 1[8]	SOUT and SCK drive strength				
			LVDS	15 pF to 25 pF differential	—	7.0	ns
10	t_{HO}	SOUT data hold time (after SCK edge)					
		SOUT data hold time after SCK CPHA = 0[8]	SOUT and SCK drive strength				
			LVDS	15 pF to 25 pF differential	-7.5 + t_{SYS}[3]	—	ns
		SOUT data hold time after SCK CPHA = 1[8]	SOUT and SCK drive strength				
			LVDS	15 pF to 25 pF differential	-7.5	—	ns

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
3. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
4. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
6. Input timing assumes an input slew rate of 1 ns (10% - 90%) and LVDS differential voltage = ±100 mV.
7. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.
8. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

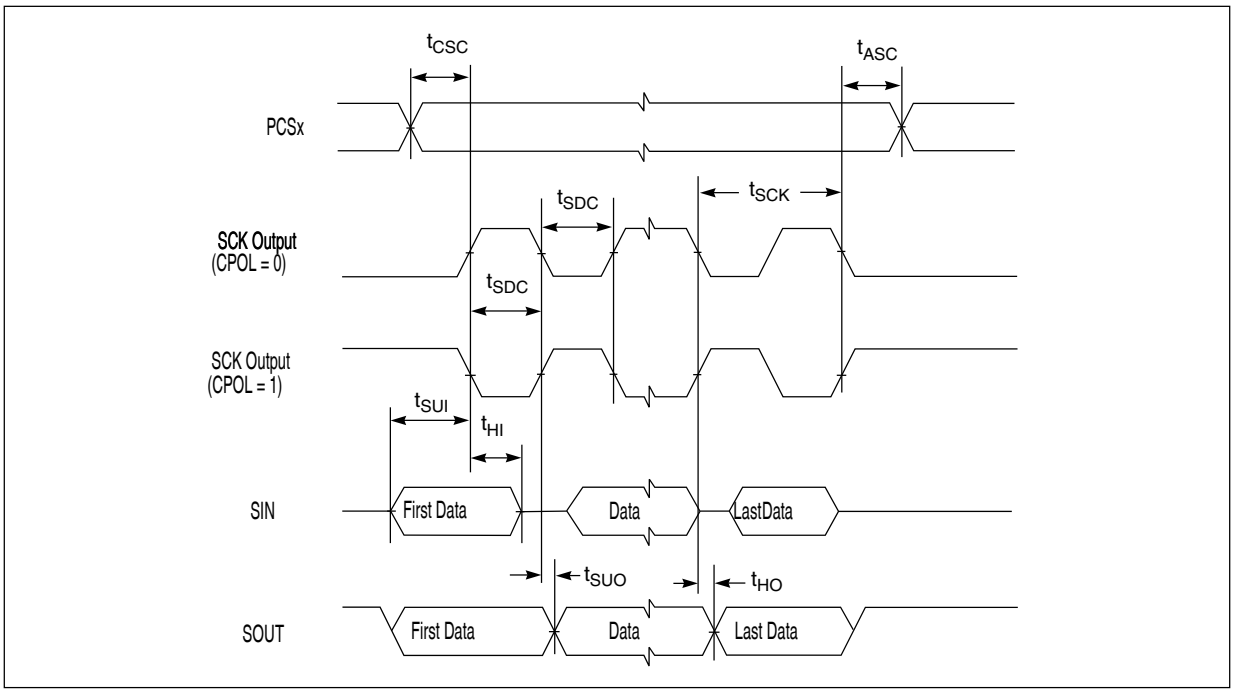


Figure 36. DSPI LVDS master mode – modified timing, CPHA = 0

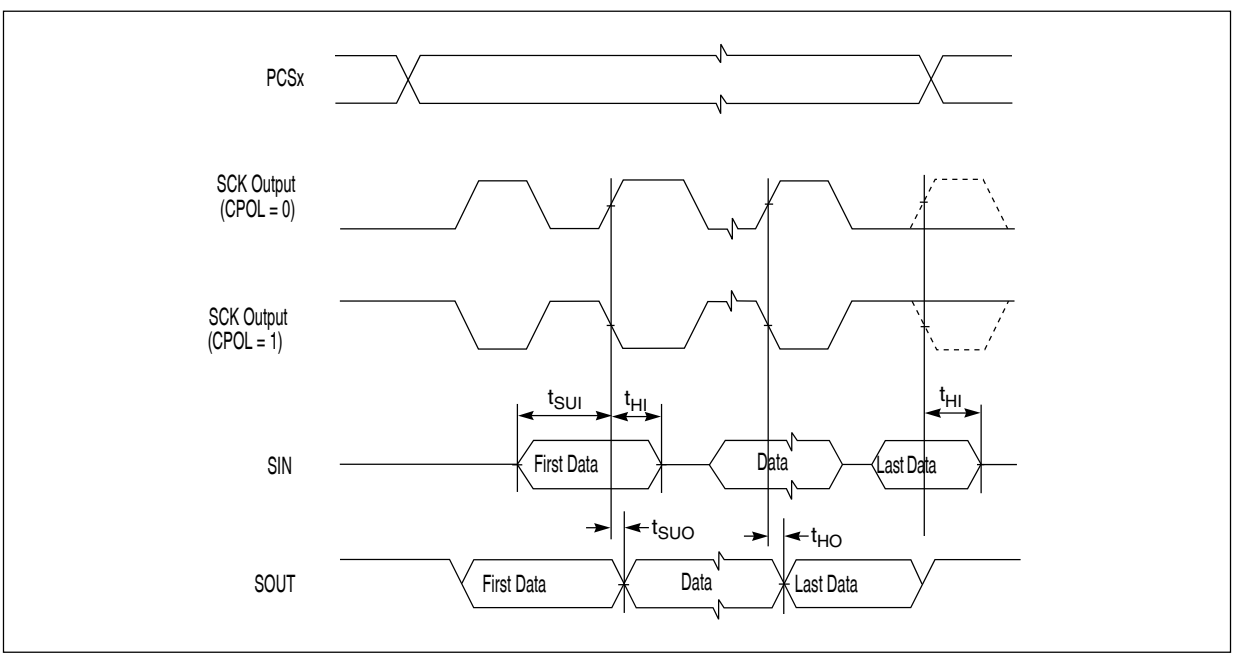


Figure 37. DSPI LVDS master mode – modified timing, CPHA = 1

18.2.1.4 DSPI master mode – output only

For Table 43 :

- All DSPI timing specifications apply to pins when using LVDS pads for SCK and SOUT and CMOS pad for PCS with pad driver strength as defined. Timing may degrade for weaker output drivers.
- TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.

Table 43. DSPI LVDS master timing - output only - timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock

#	Symbol	Characteristic	Condition		Value		Unit
			Pad drive	Load	Min	Max	
1	t_{SCK}	SCK cycle time	LVDS	15 pF to 50 pF differential	25.0	—	ns
2	t_{CSV}	PCS valid after SCK[1] (SCK with 50 pF differential load cap.)	Very strong	25 pF	—	6.0	ns
			Strong	50 pF	—	6.0	ns
3	t_{CSH}	PCS hold after SCK[1] (SCK with 50 pF differential load cap.)	Very strong	0 pF	-4.0	—	ns
			Strong	0 pF	-4.0	—	ns
4	t_{SDC}	SCK duty cycle (SCK with 50 pF differential load cap.)	LVDS	15 pF to 50 pF differential	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	ns
SOUT data valid time (after SCK edge)							
5	t_{SUO}	SOUT data valid time from SCK[2]	SOUT and SCK drive strength				
			LVDS	15 pF to 50 pF differential	—	3.5	ns
SOUT data hold time (after SCK edge)							
6	t_{HO}	SOUT data hold time after SCK[2]	SOUT and SCK drive strength				
			LVDS	15 pF to 50 pF differential	-3.5	—	ns

1. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
2. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

For Table 44 :

- TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
- All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Table 44. DSPI CMOS master timing - output only - timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock

#	Symbol	Characteristic	Condition		Value[1]		Unit
			Pad drive[2]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	SCK drive strength				
			Very strong	25 pF	33.0	—	ns
			Strong	50 pF	80.0	—	ns
			Medium	50 pF	200.0	—	ns
2	t_{CSV}	PCS valid after SCK[3]	SCK and PCS drive strength				
			Very strong	25 pF	7	—	ns
			Strong	50 pF	8	—	ns
			Medium	50 pF	16	—	ns
			PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	29	—	ns
3	t_{CSH}	PCS hold after SCK[3]	SCK and PCS drive strength				
			Very strong	PCS = 0 pF SCK = 50 pF	-14	—	ns
			Strong	PCS = 0 pF SCK = 50 pF	-14	—	ns
			Medium	PCS = 0 pF SCK = 50 pF	-33	—	ns
			PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	-35	—	ns
4	t_{SDC}	SCK duty cycle[4]	SCK drive strength				
			Very strong	0 to 50 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	ns
			Strong	0 to 50 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	ns
			Medium	0 to 50 pF	$^1/_2t_{SCK}$ - 5	$^1/_2t_{SCK}$ + 5	ns
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK CPHA = 1[5]	SOUT and SCK drive strength				
			Very strong	25 pF	—	7.0	ns
			Strong	50 pF	—	8.0	ns
			Medium	50 pF	—	16.0	ns
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK CPHA = 1[5]	SOUT and SCK drive strength				
			Very strong	25 pF	-7.7	—	ns
			Strong	50 pF	-11.0	—	ns
			Medium	50 pF	-15.0	—	ns

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
3. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.

4. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
5. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

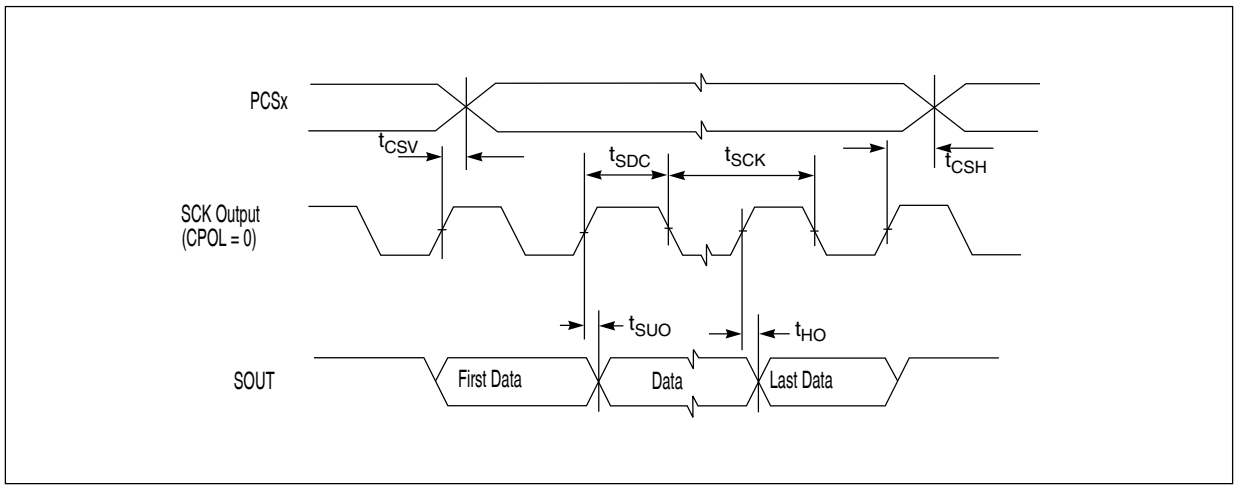


Figure 38. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1

18.2.2 DSPI CMOS slave mode

NOTE

DSPI slave operation is only supported for a single master and single slave on the device. Timing is valid for that case only.

Table 45. DSPI CMOS slave timing - Modified Transfer Format (MTFE = 0/1)

#	Symbol	Characteristic[1]	Condition		Value		Unit
			Pad drive	Load	Min	Max	
1	t_{SCK}	SCK Cycle Time	—	—	62	—	ns
2	t_{CSC}	$\overline{SS}$ to SCK Delay	—	—	16	—	ns
3	t_{ASC}	SCK to $\overline{SS}$ Delay	—	—	16	—	ns
4	t_{SDC}	SCK Duty Cycle	—	—	30	—	ns
5	t_A	Slave Access Time[2] ($\overline{SS}$ active to SOUT driven)	Very strong	25 pF	—	50	ns
			Strong	50 pF	—	50	ns
			Medium	50 pF	—	60	ns
6	t_{DIS}	Slave SOUT Disable Time[2] ($\overline{SS}$ inactive to SOUT High-Z or invalid)	Very strong	25 pF	—	5	ns
			Strong	50 pF	—	5	ns
			Medium	50 pF	—	10	ns
9	t_{SUI}	Data Setup Time for Inputs	—	—	10	—	ns

Table continues on the next page...

Table 45. DSPI CMOS slave timing - Modified Transfer Format (MTFE = 0/1) (continued)

#	Symbol	Characteristic[1]	Condition		Value		Unit
			Pad drive	Load	Min	Max	
10	t_{HI}	Data Hold Time for Inputs	—	—	10	—	ns
11	t_{SUO}	SOUT Valid Time[2] (after SCK edge)	Very strong	25 pF	—	30	ns
			Strong	50 pF	—	30	ns
			Medium	50 pF	—	50	ns
12	t_{HO}	SOUT Hold Time[2] (after SCK edge)	Very strong	25 pF	2.5	—	ns
			Strong	50 pF	2.5	—	ns
			Medium	50 pF	2.5	—	ns

1. Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL / Automotive voltage thresholds.
2. All timing values for output signals in this table, are measured to 50% of the output voltage. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

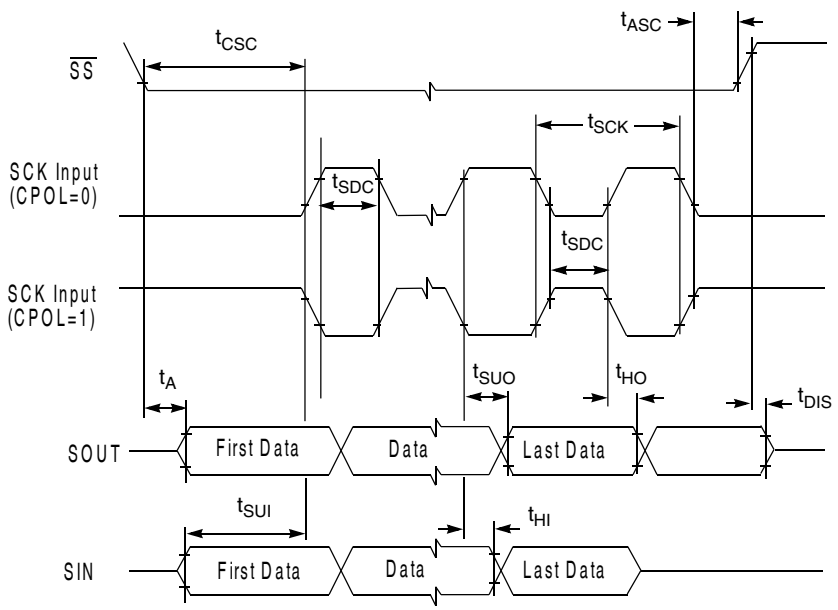


Figure 39. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 0

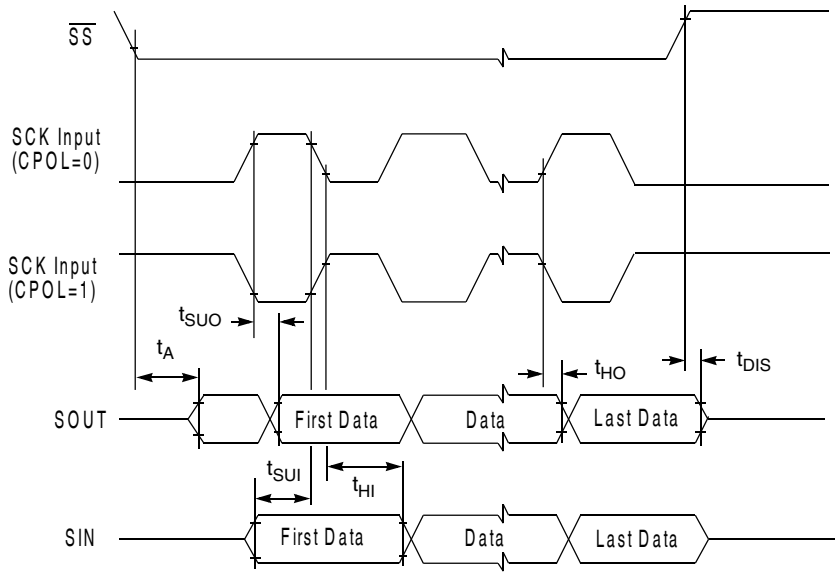


Figure 40. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 1

18.3 FEC timing

The FEC supports the 10/100 Mbps MII, 10/100 Mbps MII-lite, and the 10 Mbps-only 7-wire interface.

18.3.1 MII-lite receive signal timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

All timing specifications are referenced from RX_CLK = 1.4 V to the valid input levels.

Table 46. MII-lite receive signal timing

Spec	Characteristic	Value		Unit
		Min	Max	
M1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

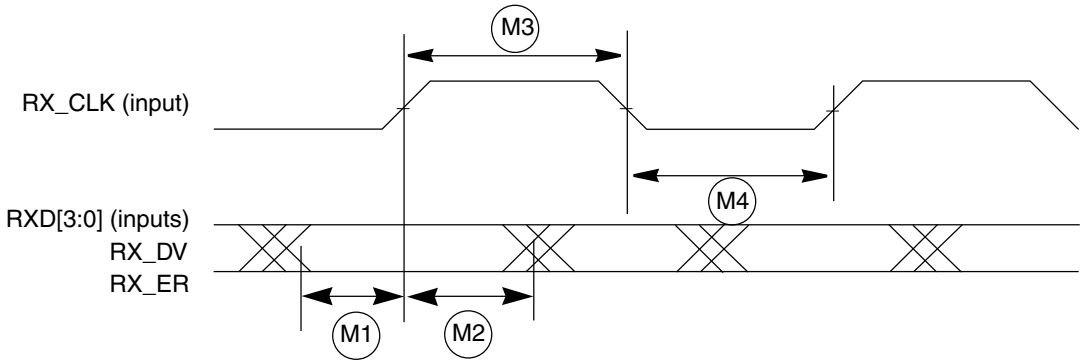


Figure 41. MII-lite receive signal timing diagram

18.3.2 MII-lite transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

All timing specifications are referenced from TX_CLK = 1.4 V to the valid output levels.

Table 47. MII-lite transmit signal timing

Spec	Characteristic	Value[1]		Unit
		Min	Max	
M5	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	TX_CLK pulse width low	35%	65%	TX_CLK period

1. Output parameters are valid for C_L = 25 p_F, where CL is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 p_F value.

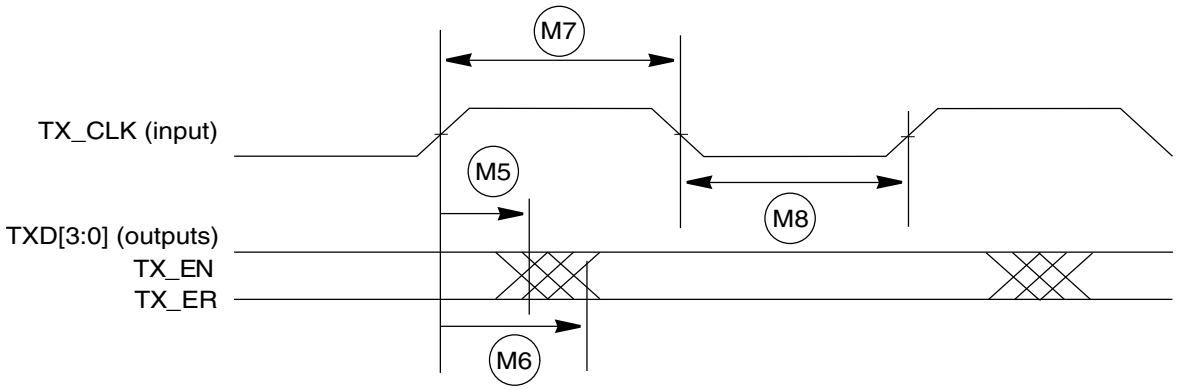


Figure 42. MII-lite transmit signal timing diagram

18.3.3 MII-lite async inputs signal timing (CRS and COL)

Table 48. MII-lite async inputs signal timing

Spec	Characteristic	Value		Unit
		Min	Max	
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

Figure 43. MII-lite async inputs timing diagram

18.3.4 MII-lite serial management channel timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

NOTE

All timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.

Table 49. MII-lite serial management channel timing

Spec	Characteristic	Value		Unit
		Min	Max	
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	10	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

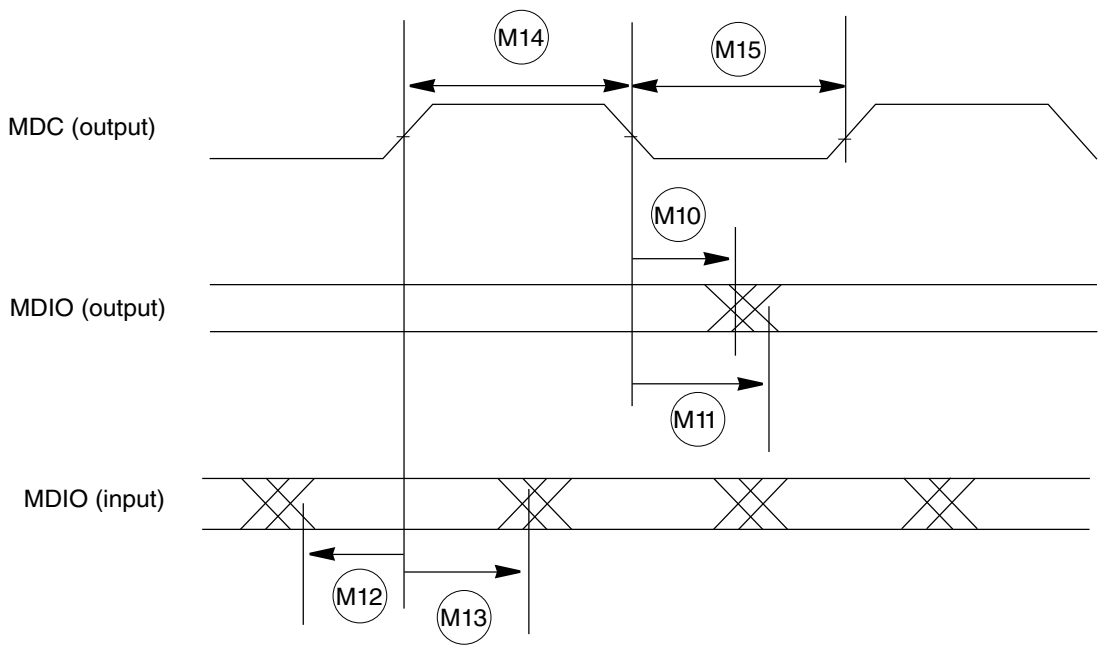


Figure 44. MII-lite serial management channel timing diagram

18.3.5 RMII serial management channel timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 50. RMII serial management channel timing

Spec	Characteristic	Value		Unit
		Min	Max	
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns

Table continues on the next page...

Table 50. RMII serial management channel timing (continued)

Spec	Characteristic	Value		Unit
		Min	Max	
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	10	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

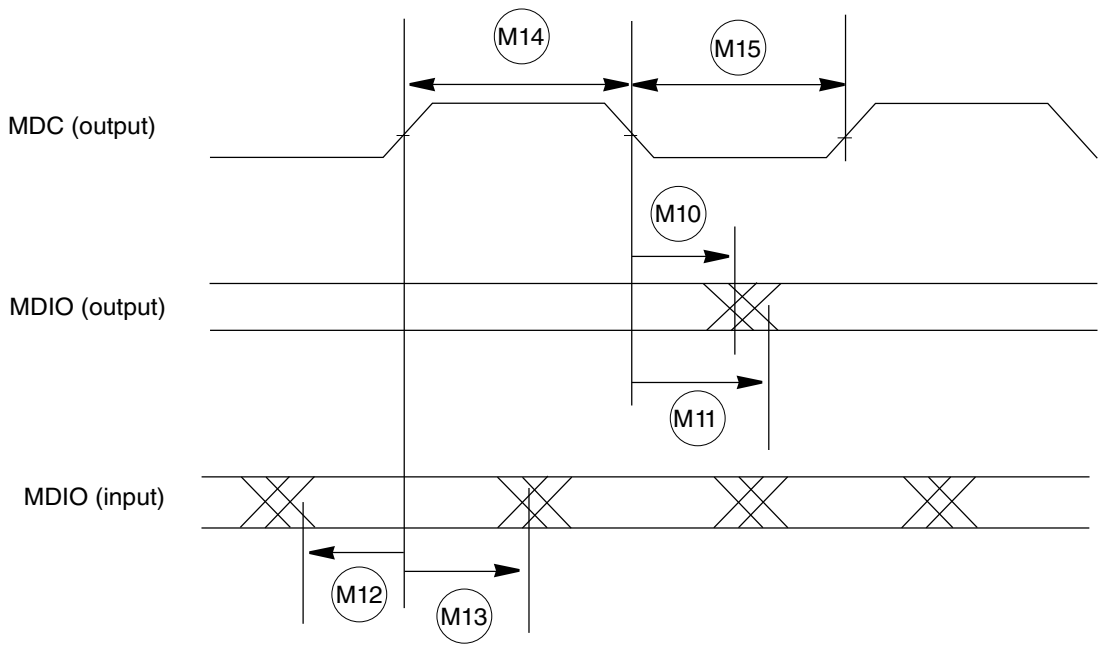


Figure 45. RMII-lite serial management channel timing diagram

18.3.6 RMII receive signal timing (RXD[1:0], CRS_DV)

The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

All timing specifications are referenced from REF_CLK = 1.4 V to the valid input levels.

Table 51. RMII receive signal timing

Spec	Characteristic	Value		Unit
		Min	Max	
R1	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	REF_CLK pulse width low	35%	65%	REF_CLK period

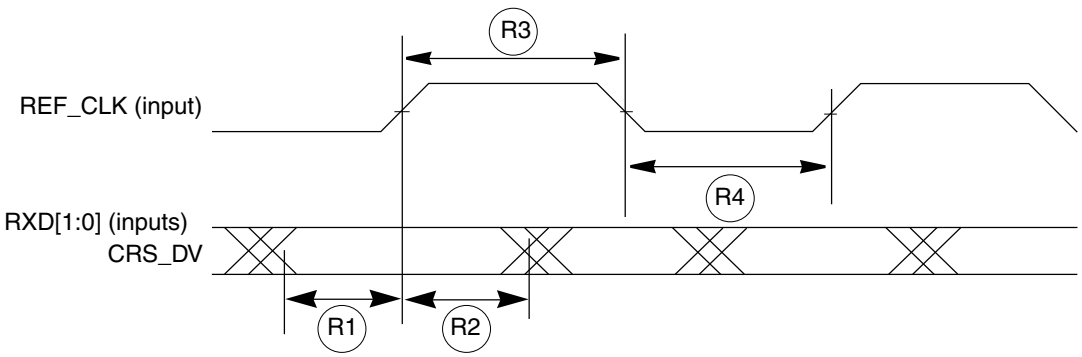


Figure 46. RMII receive signal timing diagram

18.3.7 RMII transmit signal timing (TXD[1:0], TX_EN)

The transmitter functions correctly up to a REF_CLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency, which is half that of the REF_CLK frequency.

The transmit outputs (TXD[1:0], TX_EN) can be programmed to transition from either the rising or falling edge of REF_CLK, and the timing is the same in either case. This options allows the use of non-compliant RMII PHYs.

All timing specifications are referenced from REF_CLK = 1.4 V to the valid output levels.

Table 52. RMII transmit signal timing

Spec	Characteristic	Value		Unit
		Min	Max	
R5	REF_CLK to TXD[1:0], TX_EN invalid	2	—	ns
R6	REF_CLK to TXD[1:0], TX_EN valid	—	16	ns
R7	REF_CLK pulse width high	35%	65%	REF_CLK period
R8	REF_CLK pulse width low	35%	65%	REF_CLK period

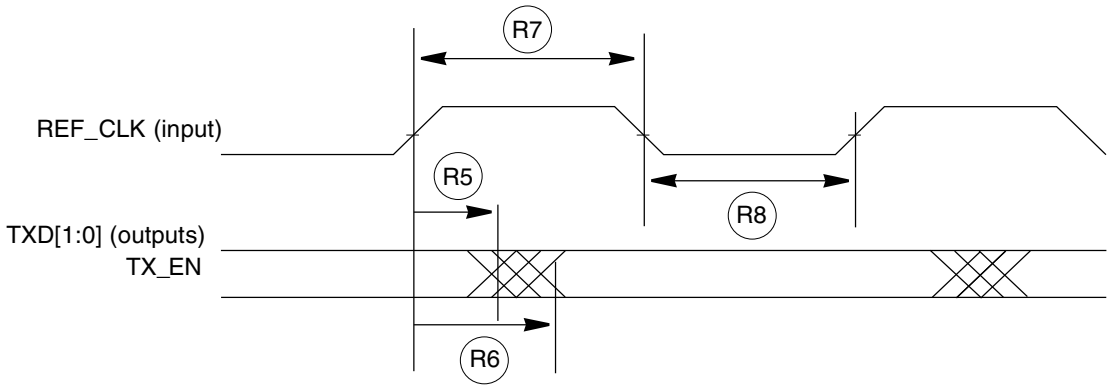


Figure 47. RMII transmit signal timing diagram

18.4 UART timings

UART channel frequency support is shown in the following table.

Table 53. UART frequency support

LINFlexD clock frequency LIN_CLK (MHz)	Oversampling rate	Voting scheme	Max usable frequency (Mbaud)
80	16	3:1 majority voting	5
	8		10
	6	Limited voting on one sample with configurable sampling point	13.33
	5		16
	4		20

18.5 eMIOS timing

Table 54. eMIOS timing

Symbol	Characteristic	Condition	Min. Value	Max. Value	Unit
t_{MIPW}	eMIOS Input Pulse Width	eMIOS_CLK = 100 MHz	2	—	cycles

19 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number.

If you want the drawing for this package	Then use this document number
LQFP 144 PD	98ASS23177W
LQFP 176 PD	98ASS23479W
MAPBGA 252 PD	98ASA00468D
MAPBGA 292 ED	98ASA00261D

20 Thermal characteristics

The following tables describe the thermal characteristics of the device.

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

Table 56. Thermal characteristics for the 144-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Junction to Ambient Natural Convection [1, 2]	Single layer board (1s)	$R_{\theta JA}$	41.3	°C/W
Junction to Ambient Natural Convection[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	33.0	°C/W
Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	32.4	°C/W
Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	26.7	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	21.5	°C/W
Junction to Case [5]	—	$R_{\theta JC}$	7.0	°C/W
Junction to Package Top[6]	Natural Convection	Ψ_{JT}	0.25	°C/W
Junction to Package Lead[7]	Natural Convection	Ψ_{JB}	16.5	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12.

Table 57. Thermal characteristics for the 176-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Junction to Ambient Natural Convection [1, 2]	Single layer board (1s)	$R_{\theta JA}$	49.9	°C/W
Junction to Ambient Natural Convection[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	33.8	°C/W

Table continues on the next page...

Table 57. Thermal characteristics for the 176-pin LQFP package (continued)

Rating	Conditions	Symbol	Value	Unit
Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	37.8	°C/W
Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	28.2	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	21.0	°C/W
Junction to Case[5]	—	$R_{\theta JC}$	7.8	°C/W
Junction to Package Top[6]	Natural Convection	ψ_{JT}	0.3	°C/W
Junction to Package Lead[7]	Natural Convection	ψ_{JB}	13.0	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12.

Table 58. Thermal characteristics for the 252-pin MAPBGA package with full solder balls

Rating	Conditions	Symbol	Value	Unit
Junction to Ambient Natural Convection [1, 2]	Single layer board (1s)	$R_{\theta JA}$	43.0	°C/W
Junction to Ambient Natural Convection[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	26.5	°C/W
Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	33.2	°C/W
Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	22.2	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	12.5	°C/W
Junction to Case[5]	—	$R_{\theta JC}$	6.3	°C/W
Junction to Package Top[6]	Natural Convection	ψ_{JT}	0.3	°C/W
Junction to Package Lead[7]	Natural Convection	ψ_{JB}	8.7	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12.

Table 59. Thermal characteristics for the 252-pin MAPBGA package 16 removed balls: 12 central, 4 corner peripheral

Rating	Conditions	Symbol	Value	Unit
Junction to Ambient Natural Convection[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	23.8	°C/W
Junction to Board[4]	Four layer board (2s2p)	$R_{\theta JB}$	15.9	°C/W
Junction to Package Lead[5]	Natural Convection	Ψ_{JB}	4.8	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12.

20.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

21 Ordering information

Table 60. Ordering information

Part Number	Device Type	Flash/SRAM	Emulation RAM	Package	Frequency
SPC5746RK1MMT5	Sample PD[1]	4M / 256 KB	-	252 MAPBGA	200 MHz
SPC5746RK1MLU3	Sample PD	4M/256KB	-	176 LQFP	150 MHz
SPC5745RK1MMT5	Sample PD	3M/192KB	-	252 MAPBGA	200 MHz
SPC5745RK1MLU3	Sample PD	3M / 192 KB	-	176 LQFP	150 MHz
SPC5743RK1MLU5	Sample PD	2M / 128KB	-	176 LQFP	200 MHz
SPC5743RK1MLQ5	Sample PD	2M / 128 KB	-	144 LQFP	200 MHz
PPC5746R2K1MMZ5A	Sample ED[2]	4M / 256 KB	1 MB	292 MAPBGA	200 MHz

1. "PD" refers to a production device, orderable in quantity.
2. “ED" refers to an emulation device, orderable in limited quantities. An emulation device (ED) is for use during system development only and is not to be used in production. An ED is a Production PD chip combined with a companion chip to form an Emulation and Debug Device (ED) and includes additional RAM memory and debug features. EDs are provided “as is" without warranty of any kind. In the event of a suspected ED failure, NXP agrees to exchange the suspected failing ED from the customer at no additional charge, however NXP will not analyze ED returns.

22 Revision history

Table 61. Revision history

Revision	Date	Description of changes
1	05/2013	Initial release.

2	12/2014	Overall:
		• Editorial changes.
		• Removed the Classification columns in spec tables and removed statements that values need to be characterized.
		• In footnotes changed cross references to figures to static text.
		
		In section Block diagram :
		• In Figure 1, changed "AIPS Bridge 0/1" to "AIPS PBridge_0/1".
		• In Figure 2 :
		  • Changed figure title (was “Peripherals block diagram”).
		  • Changed "BAF" to "BAR".
		  • Added PBRIDGE_1, EIM, XBAR, and PBRIDGE_0.
		
		In section Introduction, removed section "Parameter classification".
		
		In section Absolute maximum ratings, Table 1 :
		• VDD_HV_IO_FEC spec: removed row for "Using Ethernet Reference to VSS" condition.
		• Corrected "VIDD_HV_IO_MSC" to "VDD_HV_IO_MSC".
		• Add parameter IIOMAX.
		• Deleted IMAXSEG parameter.
		
		In section Operating conditions :
		• Deleted sentence "The ranges in this table are design targets...".
		• Added a NOTE that all power supplies need to be powered up.
		• In Table 3 :
		  • Removed VDD_HV_FLA.
		  • Changed minimum voltage of VDD_HV_ADV_SD.
		  • Modified footnote for S/D ADC supply voltage.
		  • Modified footnote for SAR ADC supply voltage.
		  • Modified VRAMP spec to two separate specs for "VRAMP_VDD_LV" and "VRAMP_VDD_HV_IO_MAIN, VRAMP_VDD_HV_PMC".
		
		In section DC electrical specifications :
		• Removed the statement that the ranges are design targets.
		• In Table 5 :
		  • Modified I_{DD_LV} to show specs depending on device model. Modified footnote.
		  • Removed the “PMC only” row of the IDD_HV_PMC “internal core reg bypassed” spec.
		  • Removed IDD_MAIN_CORE_AC.
		  • Removed IDD_LKSTP_AC.
		  • Changed I_{DDSTBY_ON} value at 40 °C.
		  • Changed I_{DDSTBY_REG} parameter to "32 KB RAM Standby Regulator Current" (was "Standby Leakage Current"); changed condition to "V_{DDSTBY} @1.2 V to 5.9 V, Tj = 150C" (was "V_{DDSTBY} @1.3 V...")

Table continues on the next page...

Table 61. Revision history

Revision	Date	Description of changes

		• Removed IDDOFF.
		• Added IDD_BD_STBY.
		• Added IVDDA.
		
		In section Input pad specifications :
		• In Table 7 :
		  • Added footnote that supported input levels vary according to pad types.
		  • Corrected VILTTL Min and Max values.
		  • Corrected VIHAUTO, VILCMOS_H and VILCMOS Min value.
		• In Table 8 :
		  • Modified |IWPU| Min values for condition Vin = VIH = 0.65 * VDD_HV_IO.
		  • Modified |IWPD| Min values for condition Vin = VIL = 0.35 * VDD_HV_IO.
		• Removed the "Analog Input Leakeage and Pull-Up/Down DC electrical characteristics" table and the preceding introductory paragraph to be moved to the ADC input description section.
		
		In section Output pad specifications, Table 9, changed VOH and VOL specs to two separate specs for 3V pads and 5V pads respectively. Corrected VOH Min and VOL Max values.
		
		In section I/O pad current specifications :
		• Added I/O Current Consumption tables.
		• Modified NOTE on Excel file attached to the Reference Manual.
		
		Added section Reset pad (PORST, RESET) electrical characteristics.
		
		In section Oscillator and FMPLL :
		• In Table 13, removed PLL0_PHI0 single period jitter row.
		• In Table 15 :
		  • Modified footnote for CS_EXTAL and CS_XTAL.
		  • Modified gm (Oscillator Transconductance) spec.
		  • Removed VHYS.
		
		In section ADC modules, revised the subsection structure and titles:
		• Added section ADC input description with content moved from the "Input pad specifications" section.
		• Section "Input impedance and ADC accuracy" renamed to Input equivalent circuit and ADC conversion characteristics with all content except Figure 11 and Table 19 removed.
		• Removed erroneous section "SAR ADC electrical specification".
		
		In section SAR ADC, Table 19 :
		• Added footnote ("SAR ADC performance is not guaranteed...") to f_{CK} symbol.
		• Changed t_{sample} specification min value to 250 ns (was 275).
		• Added footnote to OFS and GNE. Changed OFS and GNE min and max values.
		• Removed "Input (singe ADC channel)".
		• Removed injection row for "Input (double ADC channel)".
		• SNR, THD, SINAD, and ENOB specifications: changed frequency condition to 50 kHz (was 125 kHz).
		• Changed SNR Min values.
		• Added footnote to ENOB.
		• Added I_{DD_VDDA}, I_{DD_VDDR}, and V_{BG_REF} parameters.
		
		In section S/D ADC, Table 20 :
		• For V_{IN_PK2PK} parameter second and third rows, changed V_{SS} in Conditions to V_{DD}.
		• For f_{ADCD_M} specification, removed sampling frequency footnote from parameter.
		• Added footnote to RESOLUTION value.
		• For $\|\delta_{GAIN}\|$ specification added footnote to parameter and added new row with more detailed "After calibration" conditions.
		• Moved footnote "S/D ADC is functional in the range..." from the Z_{IN} to the SNR parameters.

Table continues on the next page...

Table 61. Revision history

Revision	Date	Description of changes

		• Changed all instances of “4.0 < VDD_HV_ADV_SD < 5.5” in the Conditions column to “4.5 < VDD_HV_ADV_SD < 5.5”. Modified voltage range in its footnote.
		• Changed SNR_{SE150}, GAIN = 16 condition min value to 55 dB (was 60).
		• Changed $SINAD_{SE150}$, GAIN = 16 condition min value to 54 dB (was 59).
		• Unit for SINADDIFF150, SINADDIFF333 and SINADSE150 changed from dBFs to dB.
		• For Z_{IN} specification, revised parameter footnote.
		• Added CMRR to symbol column for Common mode rejection ratio specification. Changed min value to 55 dB.
		• For δ_{GROUP} specification, revised maximum values for OSR = 24 to OSR = 256 conditions.
		• Revised entire row for $t_{LATENCY}$, $t_{SETTLING}$, and $t_{ODRECOVERY}$ specifications. Footnote added to $t_{LATENCY}$ parameter.
		• Added I_{BIAS} specification.
		• Changed IADV_D and ΣIADR_D values.
		
		In section Temperature sensor, Table 21 :
		• Changed TACC values.
		• Removed ITEMP_SENS spec item.
		
		In section LFAST interface timing diagrams, Figure 12, "|ΔVOD|" changed to "|VOD|".
		
		In section LFAST and MSC /DSPI LVDS interface electrical characteristics, Table 24, the max. value for Rise/ Fall time specs changed from 4.0 to 5.7 ns.
		
		In section LFAST PLL electrical characteristics, Table 25, ΔPER_{EYE} specification, changed Nominal value to 550 (was blank) and Max value to blank (was 400).
		
		In section Recommended power transistors, Table 27, added the specification for V_C.
		
		In section Power management integration :
		• In Figure 17 :
		  • Changed "n x C_{LV}" to "C_{LV}".
		  • Changed $C_{HV\_ADC\_S}$ to $C_{HV\_ADC\_SAR}$.
		• In Table 28 :
		  • Changed the first footnote for CHV_PMC to have the same footnote number as the first footnote for CLV as they were identical.
		  • Modified Minimum $V_{DD\_HV\_ADV\_SAR}$ external capacitance and associated footnote.
		
		Added section Regulator example for the NJD2873 transistor.
		
		Added section Regulator example for the 2SCR574d transistor.
		
		In section Device voltage monitoring, Table 29 :
		• Updated following specs:
		  • LVD_core_hot
		  • LVD_core_cold
		  • HVD_core
		  • LVD_HV
		  • HVD_HV
		  • LVD_IO
		  • LVD_SAR
		• Removed following specs:
		  • LVD_FLASH
		  • HVD_FLASH
		  • LVD_MSC_3V3
		  • LVD_MSC_5V0
		  • LVD_FEC_5V0
		  • LVD_JTAG
		  • HVD_SAR

Table continues on the next page...

Table 61. Revision history

Revision	Date	Description of changes
		• LVD_SD • HVD_SD • Corrected Voltage detector threshold crossing assertion Unit. In section Flash memory program and erase specifications, Table 30 : • Removed parenthetical phrase from table title. • Made overall updates to spec values. • Removed footnote 7. In section Flash memory Array Integrity and Margin Read specifications, Table 31 : • Removed parenthetical phrase from table title. • Made overall updates to spec values. In section Flash memory module life specifications, Table 32, removed parenthetical phrase from table title. In section Flash memory AC timing specifications, Table 33, removed parenthetical phrase from table title. Added section Flash read wait state and address pipeline control settings. In section Power management integration, Table 28, changed the footnotes for t_{TCYC} Min values to have the same footnote number as they were identical. In section DSPI timing with CMOS and LVDS, Table 39, LVDS (Master mode) specification: changed Max usuable frequency to 40 MHz (was 33 MHz). In section DSPI CMOS master mode – classic timing : • Added NOTE. • In Table 40, changed PCS strobe timing values. In section DSPI CMOS master mode – modified timing : • Added NOTE. • In Table 41, changed PCS strobe timing values. In section DSPI LVDS master mode – modified timing, Table 42, changed significant digits for some values. In section DSPI master mode – output only : • Modified format paragraphs leading the tables. Removed NOTE. • In Table 43, changed the t_{CSV} strong drive value and t_{HO} LVDS value. • In Table 44, changed significant digits for some values. In section FEC timing, corrected the title of MII-lite and RMII serial management channel timing subsections. In section MII-lite transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK), Table 47, modified footnote for output parameters. In section RMII serial management channel timing (MDIO and MDC), added Note on reference for timing specifications. In section RMII transmit signal timing (TXD[1:0], TX_EN), Table 52, modified R6 max value. In section UART timings, Table 53, removed 100 MHz specification. "Package drawings" section renamed to Obtaining package dimensions, with package drawing document numbers to search at the Freescale website. Drawings removed from this document. In section Thermal characteristics : • Added table for 144 LQFP.

Table continues on the next page...

Table 61. Revision history (continued)

Revision	Date	Description of changes
		• Moved table for 176 LQFP before 252 MAPBGA and updated table. • Replaced table for 252 MAPBGA with two separate tables for package with full solder balls and package with 16 removed balls. In section Ordering information, replaced the table.

3	09/2015	On the cover page:
		• Changed doctype from "Data Sheet: Product Preview" to "Data Sheet: Technical Data" at the upper left corner.
		• Changed statement on status of doc at the bottom of the page.
		
		Removed "Preliminary" and "Non-Disclosure Agreement required" from footers on each page.
		
		In section Electromagnetic Compatibility (EMC) removed content of entire section and replaced it with statement: "EMC measurements to IC-level IEC standards are available from Freescale on request."
		
		In section Operating conditions :
		• In Table 3
		  • For VDD_HV_PMC, removed the two footnotes.
		  • For VDDSTBY, added statement on ramp rate to footnote.
		  • For VSTBY_BO, removed Min value and added Max value.
		
		In section DC electrical specifications :
		• In Table 5 :
		  • IDD_LV spec:
		  • MPC5746R/MPC5745R Max value changed to 700 mA.
		  • MPC5743R/MPC5742R Max value changed to 610 mA.
		  • IDDSTBY_ON TA=40°C and TA=85°C values updated.
		  • IVDDA values updated.
		
		In section I/O pad specification, Table 6 Description for Input only pads, removed reference to "Automotive" input.
		
		In section Input pad specifications, Table 7 removed VIHAUTO, VILAUTO, VHYSAUTO, and VDRFTAUTO specs and references to "Automotive" input in footnotes.
		
		In section Output pad specifications :
		• In Table 9, removed footnote for tR_F spec Parameter about transition time maximum value approximation formula.
		
		In section Reset pad (PORST, RESET) electrical characteristics :
		• In Table 12 :
		  • Changed specs for VIH, VIL, and VHYS to VIH Reset, VIL Reset, and VHYS Reset respectively.
		  • Added specs for VIH PORST, VIL PORST, VHYS PORST.
		  • Generally added Conditions and updated spec values. In the Conditions column, changed all instances of "3.0 V" to "3.5 V".
		
		In section Oscillator and FMPLL :
		• In Table 13, for ΔPLL0LTJ spec, modified long term jitter Min and Max values.
		• In Table 16, values updated.
		• In Table 17, added spec for dfTRIM (IRC software trimming step).
		
		In section ADC input description :
		• In Table 18 :
		  • RPUPD 5KΩ spec Max value changed to 8.8KΩ.
		
		In section Input equivalent circuit and ADC conversion characteristics :

Table continues on the next page...

Table 61. Revision history (continued)

Revision	Date	Description of changes

		• In Table 19 :
		  • In the SNR, THD, SINAD, and ENOB rows Conditions, changed "50 kHz" to "125 kHz". Modified footnote to ENOB
		  • In IDD_VDDA and IDD_VDDR rows, modified values.
		  • In VBG_REF row's Conditions, added "INPSAMP=0xFF"
		• Added NOTE "For spec complaint operation, do not expose clock sources, including crystal oscillator, IRC, PLL0, and PLL1 on the CLKOUT pads while the SAR ADC is converting."
		• Added NOTE: "The ADC performance specifications are not guaranteed if two or more ADCs simultaneously sample the same shared channel".
		
		In section S/D ADC :
		• In Table 20 :
		  • For $THD_{DIFF333}$ GAIN = 16, updated Min value.
		  • For I_{ADV_D}, updated Max value.
		
		In section LFAST and MSC /DSPI LVDS interface electrical characteristics :
		• After table Table 24 added NOTE "For optimum LVDS performance, it is recommended to set the neighbouring GPIO pads to use Weak Drive".
		
		In section Device voltage monitoring :
		• In Table 29 :
		  • For LVD_core_hot, LVD_HV, and LVD_IO specs, removed the untrimmed Rising voltage and Falling voltage rows.
		  • For LVD_core_hot, changed Mask Opt. value to "No".
		
		In section Regulator example for the 2SCR574d transistor, figure "Regulator example", changed “5V or Vcollector” to “3.3V or Vcollector”.
		
		In section DSPI CMOS master mode – classic timing, Table 40 :
		• Changed tSDC spec's Condition SCK drive strength from "0 pF" to "0 to 50 pF".
		• In tSUI and tHI specs' footnote, removed reference to "Automotive" thresholds.
		
		In section DSPI CMOS master mode – modified timing, Table 41 :
		• Changed tSDC spec's Condition SCK drive strength from "0 pF" to "0 to 50 pF".
		• In tSUI and tHI specs' footnote, removed reference to "Automotive" thresholds.
		
		In section DSPI master mode – output only, Table 44, changed tSDC spec's Condition SCK drive strength from "0 pF" to "0 to 50 pF".
		
		Added section eMIOS timing.
		
		In section Ordering information, Table 60 :
		• Updated Part Numbers.
		• Updated Emulation device footnote.

4	03/2016	In section Block diagram, Figure 2 : • "DECIM" changed to "DECFILTER". • "SIPI" changed to "Zipwire". • I/O lines added to Zipwire, SIUL2, REACM, eTPU, eMIOS, IGF, and XOSC. In section Absolute maximum ratings table "Absolute maximum ratings", removed I_{IOMAX} spec and added I_{MAXSEG} spec. In section Operating conditions table "Device operating conditions": • For the FEC I/O supply voltage, MSC I/O supply voltage, and JTAG I/O supply voltage specs, removed the LVD enabled/disabled distinction. • Added footnote to I_{MAXSEG}. In section I/O pad current specifications :

Table continues on the next page...

Table 61. Revision history (continued)

Revision	Date	Description of changes
		• Modified the descriptions in the two paragraphs after the tables. • Removed the third paragraph after the tables and the first Note. Added section DSPI CMOS slave mode. In section Ordering information table "Ordering Information", changed Part Numbers for the 176 LQFP PD and the ED.

5	10/2016	Editorial updates.
		
		In section Operating conditions table "Device operating conditions" added foootnote to $V_{DD\_HV\_IO\_JTAG}$.
		
		In section Input pad specifications table "I/O input DC electrical characteristics" for I_{LKG} added condition "$V_{SS} < V_{IN} < V_{DD\_HV\_IO*}$"
		
		In section ADC input description table "Analog Input Leakage and Pull-Up/Down DC electrical characteristics" for ILK_AD added conditions "$V_{SS\_HV\_ADV\_SAR} < V_{IN} < V_{DD\_HV\_ADV\_SAR}$" and "$V_{SS\_HV\_ADV\_SD} < V_{IN} < V_{DD\_HV\_ADV\_SD}$".
		
		In section Recommended power transistors table "Recommended operating characteristics" for I_{CMaxDC} changed the parameter from "Minimum peak collector current" to "Maximum DC collector current".
		
		In section SAR ADC table "ADC conversion characteristics":
		• Removed the condition for t_{sample}.
		• Removed the Min and added the formula (6.02*ENOB) + 1.76 for SINAD.
		• Changed the Min value from 650 to 700 for t_{conv}.
		
		In section S/D ADC table "SDn ADC electrical specification":
		• Removed Z_{IN} specification
		• Added Z_{DIFF}, Z_{CM}, and ΔV_{INTCM} specifications
		• For R_{BIAS}:
		  • Changed Parameter description from "Bias resistance" to "Bare bias resistance"
		  • Changed Min from 100 kΩ to 110 kΩ
		  • Changed Typ from 125 kΩ to 144 kΩ
		  • Changed Max from 160 kΩ to 180 kΩ
		
		In section Flash memory AC timing specifications table "Flash memory AC timing specifications" for t_{psus}:
		• Changed Typical from 7 µs plus four system clock periods to 9.4 µs plus four system clock periods
		• Changed Max from 9.1 µs plus four system clock periods to 11.5 µs plus four system clock periods

6	05/2017	Changed Freescale to NXP throughout the datasheet. In Ordering information added rows for SPC5746RK1MLU3, SPC5745RK1MMT5 and SPC5743RK1MLU5. In Table 3 added footnote in $V_{DD\_HV\_PMC}$ In Table 28 for the rowset C_{HV_FLA} changed the Minimum and Typical values.
7	01/2020	In Table 20 : • Changed the condition of δ_{GROUP} from "Within pass band – Tclk is f_{ADCD_M}/ 2" to "Within pass band – Tclk is $2/f_{ADCD\_M}$". • In the footnote of $t_{LATENCY}$ changed the Register Latency formula from "REGISTER LATENCY = tLATENCY + 0.5/fADCD_S + 2 (~+1)/fADCD_M + 2(~+1)fPBRIDGEx_CLK where fADCD_S is the frequency of the sampling clock, fADCD_M is the frequency of the modulator" to "REGISTER LATENCY = $t_{LATENCY}$ + $0.5/f_{ADCD\_S}$ + 2 (~+1)/f_{ADCD_M} + 2(~+1)/$f_{PBRIDGEx\_CLK}$

Table 61. Revision history

Revision	Date	Description of changes
		where f_{ADCD_S} is the after-decimation ADC output data rate, $f_{ADCD\_M}/2$ is the modulator sampling rate and $f_{PBRIDGEx\_CLK}$ is the frequency of the peripheral bridge clock feeds to the ADC S/D module".

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