Features *(Continued)*

- Embedded ROM coded firmware avoids code download and allows immediate operation at startup
- Supports firmware patch code downloads for in-field upgradeability
- Two independent AGC controls for tuner's IF and RF stages
- RSSI measurement via embedded 8-bit ADC
- ACI filtering for 7 MHz channels enables use of a fixed 8 MHz SAW filter
- Time and frequency equalizer (31 taps for digital cable)
- Carrier recovery: ±0.6 MHz. Timing recovery: ±200 ppm (DVB-T/H) / ±1000 ppm (DVB-C)
- Advanced performance for SFN networks
- State-of-the-art impulsive noise protection algorithm
- CPE compensation to counteract tuner phase noise
- Ultra-fast, on-chip and automatic, UHF/VHF band scanning (QuickScan)
- BER, PER, and SNR, lock indicators
- Master TS output modes, parallel or serial (with tri-state function)
- Slave TS parallel output: external device polls data from on-chip FIFO (GPIF interface). Provides seamless interface to external controller / PHY for USB2.0, PCI-E, etc…
- On-chip PID filtering to reduce TS output bit rate (allows operation with USB1.1 microprocessor)
- Up to six GPIOs
- Two 5 V-tolerant I^2C control buses (host-side, tuner-side) with on-chip I^2C repeater (logic switch).
- Clock reference from 4, 16, 20, 24, or 27 MHz tuner output reference clock or external crystal (on-chip crystal oscillator)
- Minimal BOM using standard components
- 3.3 and 1.2 V core power supplies and variable I/O supply from 1.8 to 3.3 V
- Ultra-compact and thin QFN-36, 5x6 mm, Pb-free/RoHS-compliant package

Description *(Continued)*

Next to DVB-T's 2K and 8K FFT modes, the Si2165 includes a 4K FFT mode, compliant to DVB-H (ETSI EN 300 744 Annex F). Also both a “native” and “in-depth” interleaver are included. With these features, the Si2165 can receive DVB-H programs in fixed receiver applications (which do not require decoding of DVB-H's additional MPE FEC layer of error control coding).

With embedded smart echoes management and impulse noise reduction algorithms, demodulation performance is best-in-class while still achieving low-power operation. The Si2165 includes an IF sub-sampling mode to further reduce power consumption. For cable standards, the device implements a 31-tap equalizer to handle long echoes.

The Si2165 contains an on-chip crystal oscillator and only requires the connection of a standard crystal or a reference clock. Crystal frequencies of 16, 20, 24, and 27 MHz are supported. Alternatively, a clock signal at any of these frequencies, and additionally 4 MHz (as available, for example, from the tuner front end), can be connected to the device's clock input, eliminating the need for a dedicated crystal.

An embedded 32-bit DSP controls device operation. Sophisticated on-chip algorithms ensure optimum reception even under difficult terrestrial conditions, such as echoes outside the guard interval, pre-echoes, or strong impulsive noise. The associated DSP firmware is embedded into ROM for ease-of-use (no code download required at startup). Nevertheless, patch code can be downloaded via the I^2C interface at boot-up, for example, to adjust the demodulator for unexpected conditions that may be encountered in the field.

The Si2165 supports ultra-fast channel scanning for both cable and terrestrial DTV channels, thanks to a proprietary QuickScan feature, which is provided as a downloadable patch file (for selected supported tuners).

The use of QuickScan reduces channel discovery time at device setup and runs autonomously on the Si2165 (small software burden on the MPEG/host processor).

The user can select between serial and parallel master MPEG transport stream (TS) output modes. TS clock can be set with a constant period for CA modules.

Furthermore, a TS slave parallel mode is available in which the device signals the availability of TS data in its internal output FIFO to a host, which then reads out this data. The user can program an on-chip 32-PID hardware filter to reduce the output bit rate to only pass TS packets belonging to one or multiple programs/services. For most cases, this can reduce the data rate to below 12 Mbps, allowing the use of an USB1.x interface to carry the selected TS data from a PC peripheral to the host PC. The Si2165 provides a glueless interface to Silicon Labs MCUs with embedded USB interfaces.

A total of six general-purpose inputs/outputs are available (logic levels); Three of these GPIOs also provide Δ/Σ and interrupt output capabilities. Additionally, for a tuner that does not require RF and/or IF AGC control signals, the corresponding pins can be reconfigured as two general-purpose outputs (GPOs).

An I^2C host bus interface is used to configure and monitor all internal parameters/registers. I^2C addressing mode can be configured in either 16- or 8-bit format. An internal pass-through switch acts as an I^2C repeater and can be configured to pass I^2C commands to a secondary (tuner-side) I^2C bus, when required. This feature provides a “quiet” I^2C bus to the RF front end.

The Si2165 guarantees a low-cost system implementation due to its minimal bill of materials and PCB footprint. A maximum of 13 to 20 components (R, C, and crystal, depending on the application selected) and 15x20 mm on a 2-layer PCB are required.

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GLOSSARY

Acronym	Description
ACI	Adjacent Channel Interference
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BER	Bit Error Ratio
BOM	Bill of Materials
CCI	Co-Channel Interference
COFDM	Coded Orthogonal Frequency Division Multiplexing
CP	Continuous Pilot
CPE	Common Phase Error
CR	Code Rate
DEI	De-interleaver
DFE	Decision Feedback Equalizer
DVB	Digital Video Broadcasting
DSP	Digital Signal Processor
ETSI	European Telecommunications Standards Institute
FEC	Forward Error Correction
FFE	Feed Forward Equalizer
FFT	Fast Fourier Transform
FIFO	First In, First Out
GI	Guard Interval
GPIF	General Purpose Interface
GPIO	General Purpose Input/Output
HP	High Priority (stream)
I^2C bus	2-wire communication bus between devices
LP	Low Priority (stream)
PCI	Peripheral Component Interconnect
PER	Packet Error Rate
PID	Packet Identifier
POR	Power On and Reset
QAM	Quadrature Amplitude Modulation
QFN	Quad Flat Pack with No Leads
QPSK	Quad Phase Shift Keying Modulation
RS	Reed-Solomon Decoder
RSSI	Received Signal Strength Indicator
SNR	Signal to Noise Ratio
SP	Scattered Pilot
SR	Symbol Rate (in Mbaud)
SRC	Sample Rate Converter
TEI	Transport Error Indicator
TOP	Take Over Point (for AGC loops)

TPS	Transmission Parameter Signaling
TS	Transport Stream
USB	Universal Serial Bus

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Digital Supply Voltage	V_{DD_VCORE}	1.14	1.20	1.26	V
Analog Supply Voltage	V_{DDH_VANA}	3.00	3.30	3.60	V
ADC Supply Voltage	V_{DD_VADC}	1.14	1.20	1.26	V
Interface Supply Voltage	V_{DD_VIO}	1.62	1.80 / 2.50 / 3.30	3.60	V
Ambient Temperature	T_A	0	25	85	°C

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Unit
Digital Supply Voltage	V_{DD_VCORE}	–0.3 to 1.5	V
Analog Supply Voltage	V_{DD_VANA}	–0.3 to 3.9	V
ADC Supply Voltage	V_{DD_VADC}	–0.3 to 1.5	V
Interface Supply Voltage	V_{DD_VIO}	–0.3 to 3.9	V
Input Current[2]	I_{IN}	10	mA
Input Voltage[2]	V_{IN}	–0.3 to min (V_{DD_VIO} + 0.3, 3.9)	V
IF or I/Q inputs	$V_{ADC\_IN/IP/QN/QP}$	–0.3 to min (V_{DD_VADC} + 0.3, 1.5)	V
RSSI input	V_{RSSI_ADC}	–0.3 to min (V_{DDH_VANA} + 0.3, 3.9)	V
Operating Temperature	T_{OP}	–20 to +100	°C
Storage Temperature	T_{STG}	–55 to +150	°C

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. For input pins RESETB, ADDR, GPIO_0, GPIO_1, GPIO_2, GPIO_3, GPIO_4 and GPIO_5.

Table 3. System

Parameter	Min	Typ	Max	Unit
General				
Power-up Time	—	—	10	ms
I^2C Speed (Host side)	< 1	—	400	kHz
Input Clock Reference	—	4/16/20/24/27	—	MHz
Supported Crystal Frequency	—	16/20/24/27	—	MHz
Input ADC Sampling Clock				
ZIF Mode	18.5	48	60	MHz
IF Sub-sampling Mode	18.5	27	32.5	MHz
IF Over-sampling Mode	37	48	60	MHz
System Clock	—	—	85	MHz
TS Output Rates				
Serial Mode DVB-T	—	—	42	MHz
Serial Mode DVB-C	—	—	65	MHz
Current Supplies and Power Consumption				
DVB-T, 8 MHz, IF Mode, adc_clk = 56 MHz, Parallel TS Output				
VDD_VCORE (@ 1.2 V)	—	55	—	mA
VDD_VADC (@ 1.2 V)	—	15	—	mA
VDDH_VANA (@ 3.3 V)	—	9	—	mA
VDD_VIO (@ 3.3 V)	—	8	—	mA
Total Power	—	140	—	mW
DVB-C, 6.9 Mbauds, 256 QAM, adc_clk = 56 MHz				
VDD_VCORE (@ 1.2 V)	—	39	—	mA
VDD_VADC (@ 1.2 V)	—	15	—	mA
VDDH_VANA (@ 3.3 V)	—	9	—	mA
VDD_VIO (@ 3.3 V)	—	8	—	mA
Total Power	—	120	—	mW
Stand-by Mode				
VDDH_VANA (@ 3.3 V)	—	4	—	mA
Total Power	—	13	—	mW

Table 4. Analog Front End—I/Q A/D Converters

Parameter	Symbol	Min	Typ	Max	Unit
DC Accuracy					
Resolution	N	—	12	—	bits
Analog Signal Input					
Number of A/D Converters	N_{IQ_ADC}	—	2 (differential inputs)	—	
ADC Impedance	$Z_{in,ADC}$	—	12	—	kΩ
Input Differential Voltage Range	V_{FSR}	—	1	—	Vpp

Table 5. Analog Front End—RSSI A/D Converter

Parameter	Min	Typ	Max	Unit
Resolution	—	8	—	bit
Number of A/D Converters	—	1	—	
Input Voltage Range	—	0–2	—	V
Analog Input Bandwidth	—	500	—	Hz
Input Impedance	—	> 1	—	MΩ

2. Functional Description

The Si2165 consists of the following functional blocks: front end, demodulator, equalizer, FEC module, PID filter, TS output interface, DSP, synchro block, and control block. These functions are described in the following sections.

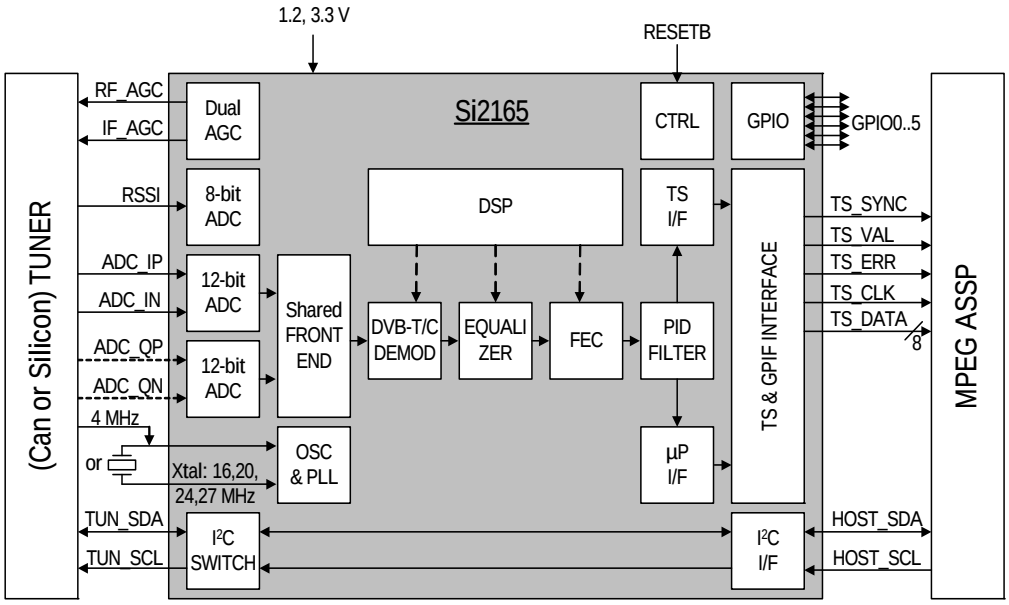

Figure 1. Functional Block Diagram

2.1. Front End

The front end interfaces the analog inputs to the digital demodulation section of the receiver. Thanks to the presence of two ADCs with differential inputs, the front end can support zero-IF or low-IF “complex” inputs next to standard-IF or low-IF “real” inputs. In case of a “real” input, a source selector switch allows the selection of either ADC; so, two RF tuners can be connected. After A/D conversion, the front end performs I and Q mismatch correction, if required. The front end further contains a separate 8-bit ADC for RSSI (Receive Strength Signal Indicator) measurement. RF and IF AGC control signals are provided to the tuner. An on-chip PLL generates ADC sampling and digital clocks from an external crystal (on-chip oscillator) or reference clock input. The front end output to the demodulator module is the digitized ADC data, down-mixed to a complex baseband signal and rate-converted from the programmable ADC sample rate to a rate equal to exactly 4 times the symbol rate.

2.2. Demodulator

For DVB-T/H, the demodulator performs successively adjacent channel filtering, impulse noise filtering, FFT processing, and echo shift compensation.

FFT window positioning is provided by the synchronization module. The demodulator provides the equalizer module with the demodulated and distorted carriers, consisting of scattered pilots, continuous pilots, TPS carriers, and carriers with QAM symbols.

For DVB-C, the demodulator performs adjacent channel filtering through a high-rejection half-Nyquist filter. An automatic digital gain control is also performed at the Nyquist filter output to compensate for power reduction within the filter such that its output signal power level remains optimized. A timing error detector provides an error signal to a second-order loop filter, which delivers a timing correction signal to control the sampling rate conversion in the front end block. The bandwidth and damping factor of the loop are programmable in order to achieve both high acquisition range and good performance during the tracking phase. A highly-programmable frequency sweep function is available to cope with large frequency offsets. The frequency correction signal is sent back to the downconverter of the front end block, which applies the proper frequency shift on the input spectrum. The overall synchronization process of the QAM demodulator is controlled by a configurable state machine, which uses status information from the different blocks to sequence the synchronization algorithms. This makes synchronization completely autonomous and, therefore, simplifies the host processor software.

2.3. Equalizer

For DVB-T/H, the equalizer estimates the channel transfer function and corrects the received signal, providing channel-corrected signal samples and confidence information to the downstream blocks. COFDM systems are designed to reduce the equalizer to its most simple expression: a single-tap filter. In order to correct each subcarrier, the equalizer has to estimate the frequency response of the channel. This task is facilitated by the insertion, at transmission, of known pilots at specific frequencies. These pilots are modulated and boosted to ensure better reception. First, the equalizer has to demodulate them. Then, it can estimate the channel response. This information is used to straighten the distorted carriers. Concurrently, the channel estimation is used to compute Channel State Information (CSI), which will be used by the demapper to weigh the soft bits information. The Si2165 also uses specific CSI algorithms to deal with high levels of Co-Channel Interference (CCI).

For DVB-C, the equalizer block implements an adaptive decision-feedback equalizer, a carrier recovery loop, and a demapper suitable for the DVB-C standard. A signal-to-noise estimator allows both the equalizer and carrier recovery loop parameters to be automatically controlled during the acquisition and tracking phases.

The DFE equalizer contains two parts:

- Feed-forward part with programmable length, which receives symbols at the symbol rate from the demodulator
- Feedback part, which receives decided symbols from the demapper

Equalizer coefficients are continuously adapted to the measured channel response.

Carrier recovery, which implements a phase detector and a programmable second-order loop filter, receives decision errors from the demapper. To optimize performance, dedicated hardware controls the operation of both equalizer and carrier recovery during the acquisition and tracking phases.

2.4. FEC Module

The FEC module consists of an **inner FEC** (for DVB-T/H) and **outer FEC** (for DVB-T/H and DVB-C). Operating on the output of the equalizer, it provides an error-corrected transport stream to the TS output interface.

The forward error correction module is compliant to broadcast cable standard EN 300 429 (DVB-C) and terrestrial standard EN 300 744 (DVB-T), also supporting Annex F (DVB-H).

This module can be configured by setting the standard and the relevant broadcast parameters: constellation, FFT mode, guard interval, code rate, hierarchy level, and stream demodulated (HP or LP). All other control registers dedicated to FEC synchronization contain default values already adapted to the mode received.

The FEC starts to synchronize once the demodulator is locked. At the end of processing, a lock indicator indicates that the FEC is locked and that the transport stream contains valid data.

For DVB-T/H, the FEC receives constellation point (I/Q) data from the DVB-T/H equalizer as well as related Channel State Information (CSI). For DVB-C, the FEC receives 4–8 bit encoded symbol data, depending on the constellation (16 to 256 QAM).

For DVB-T/H, an **inner FEC** includes a symbol (frequency) de-interleaver, de-mapper, bit de-interleaver, and Viterbi decoder. The symbol de-interleaver could be configured as native or in-depth, where the native mode is the original mode of the DVB-T specification, and the in-depth mode is the specific mode from Annex F. When the in-depth mode is selected in 2K or 4K FFT mode, the symbol de-interleaver always acts on blocks of 6048 data symbols. Rate smoothing is implemented to cancel the jitter effects of the COFDM symbol structure and of FFT window synchronization. The demapper computes soft decision bits from the frequency de-interleaved complex symbol and CSI data. Bit de-interleaving is then processed to achieve randomization at the bit stream level. The Viterbi decoder includes automatic de-puncturing of the incoming stream and systematically synchronizes to the start of the COFDM symbol.

For DVB-T/H modes, the **outer FEC** consists of a packet synchronizer, Forney De-Interleaver, Reed-Solomon Decoder, and Energy-Dispersal Descrambler. For DVB-C mode, the complete FEC section is identical to the **outer FEC** section of DVB-T/H.

Packet synchronization provides DVB packets of 204 bytes. The Si2165 offers fully-automated packet synchronization for both terrestrial and cable standards. The Forney de-interleaver spreads remaining burst errors to allow their correction by the Reed-Solomon decoder. The Reed-Solomon decoder, with a correction capacity of eight erroneous bytes per TS packet, corrects the residual errors after de-interleaving and declares the output packet un-correctable if its correction capacity is exceeded. Finally, the energy-dispersal descrambler synchronized by the inverted SYNC byte, 0xB8, retrieves the original TS.

2.5. PID Filter

The PID filter allows for optional filtering of the MPEG-TS packets. The user can specify up to 32 PID values, which are either blocked or passed. In the latter case, all other PID's are blocked except the chosen PID.

2.6. TS Output Interface

The TS output interface formats the TS into a parallel or serial MPEG-TS interface and provides various output formatting options. Two output bus modes exist: a regular master-mode synchronous interface (parallel or serial) providing clock and data, and an asynchronous parallel interface that allows an external device (typically a microcontroller) to read a burst of 512 MPEG TS data bytes out of the Si2165's internal output FIFO.

2.7. DSP

An embedded DSP supervises the entire synchronization task. Embedded ROM code is present in the Si2165. Onboard RAM provides memory space for a firmware patch download or for implementation of extra features, such as the QuickScan (blindscan) routine.

2.8. Synchro Block

The synchro block mainly consists of hardware coprocessors that aid the DSP in the synchronization task.

2.9. Control Block

The control block is mainly a clock and reset management block that generates all internal clocks and associated resets required by the Si2165. It also includes dedicated test logic for manufacturing test purposes.

3. Operational Description

3.1. Revision

The part revision is given by the die version, which can be read from the **revcode (0023h)** register.

See "3.8.2.2. Device Initialization Sequence" on page 25 for an overview of system boot information.

3.2. Definitions

The following definitions apply throughout the text of this data sheet.

- DVB_rate:
  - For DVB-T/H, DVB_rate denotes the reference frequency, i.e. 8/7 x BW (for instance, ~9.14 MSPS for an 8 MHz bandwidth).
  - For DVB-C, DVB_rate denotes the symbol rate, i.e., 1 to 7.2 MBaud for an 8 MHz bandwidth.
- The FE_clk frequency is the frequency of the front end clock.
  - If adc_clock is > 4 x DVB_rate, FE_clk frequency = adc_clk frequency.
  - Otherwise, FE_clk frequency = 2 x adc_clk frequency.

3.3. Clocks

3.3.1. Clock Reference Input: Crystal or External Clock Source

The reference clock of Si2165 is either a crystal connected between the XTAL_I and XTAL_O pins (the device has an on-chip crystal oscillator), or a sinusoidal or rectangular clock provided by an external source on pin XTAL_IN.

When Si2165 is used with a crystal, supported crystal frequencies are 16, 20, 24, and 27 MHz.

When Si2165 is used with an external clock source, supported clock frequencies are 4, 16, 20, 24, and 27 MHz.

Register **chip_mode (0000h)** has to be set to indicate whether the clock comes from the crystal or an external clock.

Note: When **chip_mode (0000h)** is set to “off”, no clock is provided to the chip, which corresponds to the Si2165 standby mode and represents the device default state after hardware reset.

The reference clock accuracy should be better than ±200 ppm for DVB-T/H while it is relaxed to ±1000 ppm maximum for DVB-C.

For DVB-T/H, the **timing_sync_range (0318h)** register adjusts the demodulator timing recovery range according to the selected crystal accuracy. A crystal with worse frequency accuracy will require a higher timing recovery range setting. However, the higher the range value, the longer the demodulator locking time will be. The value is the required local oscillator precision in ppm. For example, it should be set to 50 for a ±50 ppm crystal.

3.3.2. Clock Reference Output

The input clock reference can be routed outside Si2165 via the RSSI pin to drive an external chip (e.g. in a dual front end application). Register **rssi_pad_ctrl (0646h)** allows toggling between the two functionalities for this pin.

3.3.3. Clock Domains

Si2165 has three internal clock domains that are relevant to the user.

- **adc_clk**: ADC sampling clock. Used by ADC, dc offset correction, and I/Q mismatch correction.
- **FE_clk**: Front End clock. Used for IF frequency shift, anti-alias filtering, and timing correction.
- **sys_clk**: System clock. Used by the demodulator up to transport stream output.

adc_sampling_mode (00E0h) has to be set according to **adc_clk** frequency and **DVB_rate**; then FE_clk will be affected according to the following table:

adc_clk Divided by DVB_rate	Oversampling Mode	adc_sampling_mode (00E0h)	FE_clk Frequency	Max. adc_clk Frequency
> 4	Ovr4	If_ovr4 or zif_ovr4 (depending on tuner interface)	= adc_clk	65 MHz
≤ 4	Ovr2	If_ovr2 or zif_ovr2 (depending on tuner interface)	= adc_clk * 2	32.5 MHz

Requirements for sys_clk are 8 x DVB_rate < Sys_clk < 85 MHz. Usually, sys_clk is set around 80 MHz for DVB-T/H and around 60 MHz for DVB-C.

3.3.4. Clock Generation/PLL Dividers

Both adc_clk and sys_clk are generated from an on-chip PLL, which contains five dividers. Figure 2 shows a diagram of the embedded PLL block.

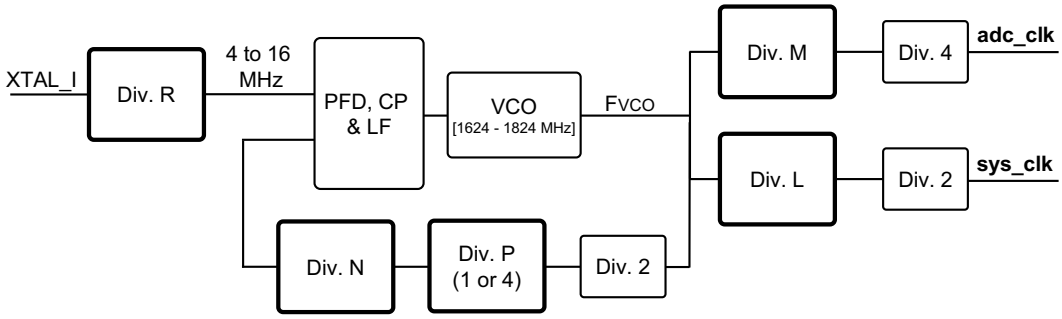

Figure 2. PLL Divider Details

For normal device operation, register **pll_enable (00A2h)** needs to be enabled.

Divider R **pll_divr (00A3h)** shall be chosen such that:

the ratio *XTAL_I / R* falls between 4 and 16 MHz.

Pre-scaler P **pll_divp (00A2h)** is selecting between a division by 1 or a division by 4.

Divider N **pll_divn (00A2h)** shall be calculated such that:

Fvco = XTAL_I / R x 2 x N x P falls in the 1624 to 1824 MHz VCO frequency range.

Divider M **pll_divm (00A1h)** and divider L **pll_divl (00A0h)** are set to ensure proper adc_clk and sys_clk frequencies.

adc_clk is programmed according to the following formula:

$$adc\_clk = F_{VCO} / (4 \times pll\_divm)$$

sys_clk is programmed according to the following formula:

$$sys\_clk = F_{VCO} / (2 \times pll\_divl)$$

There is no valid default PLL divider setting preloaded.

3.4. Tuner Interface

3.4.1. I/Q ADCs

The Si2165 analog input stage contains two 12-bit pipeline A/D converters. All voltage references and biases are included on-chip. The Si2165 basic interface scheme is ac-coupled inputs. Optimized ADC settings have to be written after software reset through registers **adc_ri0 (0129h**) to **adc_ri6 (012Fh)** and **adc_ri8 (0123h)**. See "3.8.2.2. Device Initialization Sequence" on page 25.

3.4.2. Input Configurations

Si2165 supports connection to tuners with standard IF (~36 MHz), low-IF (typically 3-4 MHz) or Zero-IF (ZIF) analog baseband I/Q outputs. The latter mode is possible thanks to the presence of two ADCs. Register **adc_sampling_mode (00E0h)** selects the ADC sampling mode (IF or ZIF).

In IF sampling mode, a single ADC is used. The ADC in function can be selected with register **iq_adc_swap (0122h)**. By default, ADC_I is used. This register can also be used to switch between two different IF sources connected to the device.

In ZIF sampling mode, both ADCs are used. If a spectrum inversion happens in the tuner or if I and Q traces are inverted on the PCB, the proper tuner connection can be restored via register **iq_adc_swap (0122h)**.

Both oversampling and sub-sampling modes are supported. In this context, sub-sampling refers to the use of an ADC clock frequency lower than the IF frequency. The advantage of sub-sampling is lower power consumption, but it may cause performance degradation especially with respect to adjacent channel immunity. The advantage of oversampling is better performance as it requires lower tuner selectivity.

For all modes, the sampling frequency has to be chosen such that ADC aliasing is minimized. This obviously depends on the selectivity of the tuner and has to be assessed for the worst-case adjacent channel scenario (typical 54 MHz sampling frequency is used in case of a 36 MHz IF scheme).

3.4.2.1. Standard IF

Figures 3 and 4 show examples of the ADC output spectrum for standard IF applications. Two cases can be distinguished, depending on whether the sampling clock is higher (oversampling) or lower (sub-sampling) than the input IF center frequency.

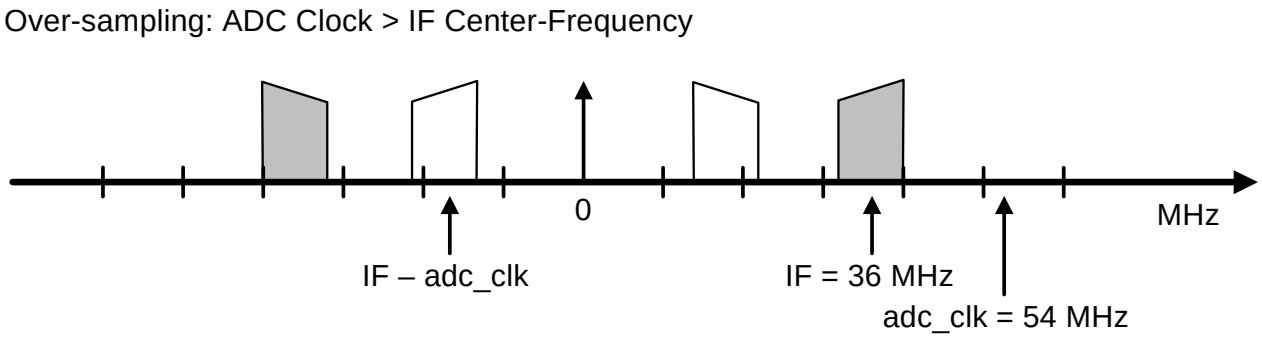

Figure 3. ADC Output Spectrum in Standard-IF Mode (Oversampling)

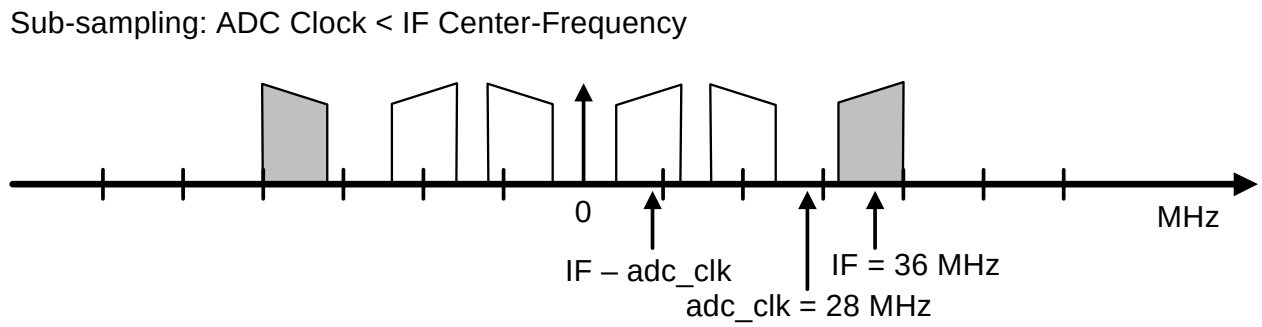

Figure 4. ADC Output Spectrum in Standard-IF Mode (Sub-sampling)

As shown in Figures 3 and 4, the A/D conversion creates replications of the IF input signal. Digital_IF indicates the frequency of the desired signal, which is located at frequency IF – adc_clk. This signal has to be downconverted to baseband. A frequency shift equal to "– digital_IF" must be applied to the input signal. This is done through register **if_freq_shift (00E8h)**.

$$if\_freq\_shift = -digital\_IF\ (in\ Hz) \times 2^{29} / FE\_clk\ (in\ Hz)$$

If a spectrum inversion happens in the tuner, the spectrum located at – digital_IF has to be selected instead of digital_IF to recover the right spectrum.

3.4.2.2. Low- IF

Low-IF denotes the case where the IF signal frequency is less than half of the ADC clock frequency (Nyquist).

Figure 5 shows an example of the ADC output spectrum for low IF applications.

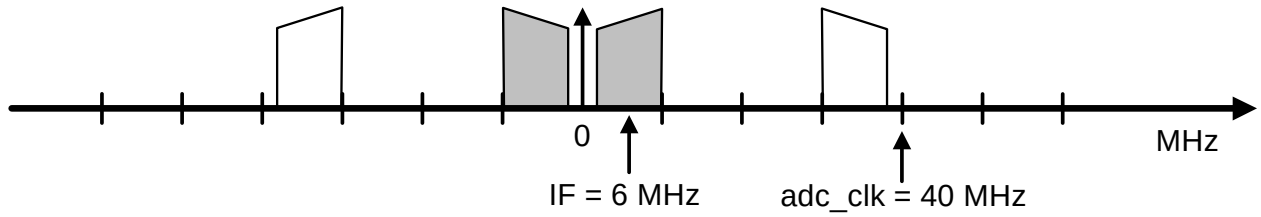

Figure 5. ADC Output Spectrum in Low-IF Mode

Since the sampling frequency is higher than twice the IF signal frequency, no downconversion occurs during sampling. Thus, digital_IF equals the low-IF frequency. This signal has to be downconverted to baseband. A frequency shift equal to "– digital_IF" must be applied to the input signal. This is done through register **if_freq_shift (00E8h)**.

$$if\_freq\_shift = – digital\_IF\ (in\ Hz) \times 2^{29} / FE\_clk\ (in\ Hz)$$

If a spectrum inversion happens in the tuner, the spectrum located at "– digital_IF" has to be selected instead of digital_IF to recover the right spectrum.

3.4.2.3. Zero IF (I/Q)

Figure 6 shows an example of the ADC output spectrum for ZIF applications.

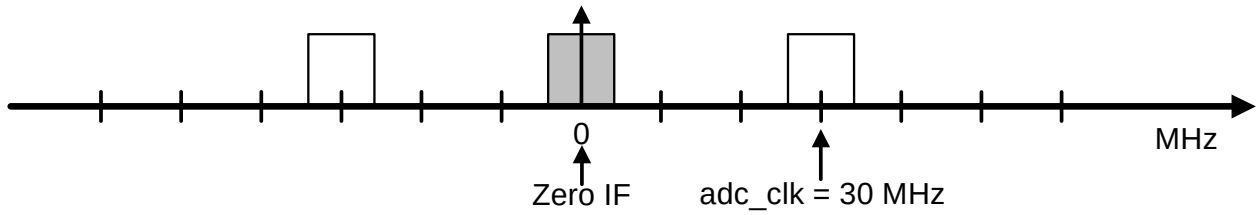

Figure 6. ADC Output Spectrum in Zero-IF

In ZIF mode, there is no need to downconvert the signal to baseband (digital_IF = 0); so, the value of the **if_freq_shift (00E8h)** register should be programmed to zero. If a spectrum inversion happens in the tuner or if I and Q traces are inverted on the PCB, the proper tuner connection can be restored via register **iq_adc_swap (0122h)**.

The following table summarizes the various tuner interface modes.

Tuner Interface	adc_sampling_mode (00E0h)	Digital_IF	Solution for Spectral Inversion
IF over-samp	IF_ovrx (x = 2 or 4 upon oversampling mode)	IF – adc_clk	Shift over Digital_IF * (-1)
IF sub-samp	IF_ovrx	IF – adc_clk	Shift over Digital_IF * (-1)
Low-IF	IF_ovrx	IF	Shift over Digital_IF * (-1)
ZIF	ZIF_ovrx	0	Invert I/Q with **iq_adc_swap(0122h)**

In DVB-C, demodulation is achieved with or without spectral inversion if register **ps_ambig_mode (0450h)** is in auto mode (default). In this case, the spectral inversion status can be read from register **ps_ambig_out (0444h)**. When in manual mode, the user should program, in register **ps_ambig_reg (0450h)**, whether or not to activate the spectral inversion.

3.4.3. RSSI ADC

If the **rssi_pad_ctrl (0646h)** register has been set to do so, the Si2165 can monitor the RSSI (Received Signal Strength Indicator) signal from tuners that provide such output. The device contains an 8-bit ADC that digitizes the RSSI signal applied to the RSSI_ADC pin. The signal is assumed to be dc-coupled. Because of the low sampling rate of the RSSI ADC, the input signal bandwidth should not be more than 500 Hz.

The RSSI ADC is turned on via register **en_rssi (0641h)**. The **start_rssi (0641h)** register allows activating or stopping RSSI measurement monitoring. When the RSSI function is active, register **rssi (0642h)** contains the most recent digitized value of the RSSI input signal.

The refresh rate of RSSI measurement can be modified by the **rssi_update_time (0641h)** register value according to the following formula:

$$RefreshRate\ (in\ Hz) = sys\_clk\ (in\ Hz) / 2^{rssi\_update\_time+5}$$

Note: There is no gain / offset control capability on this input.

3.4.4. Analog AGC

Si2165 provides RF_AGC and IF_AGC output signals, which drive the corresponding tuner inputs, to ensure that proper signal level(s) at the ADC input(s) are maintained.

Both AGC outputs are Δ/Σ outputs and need to be R-C filtered prior to use by the tuner (see Figure 7).

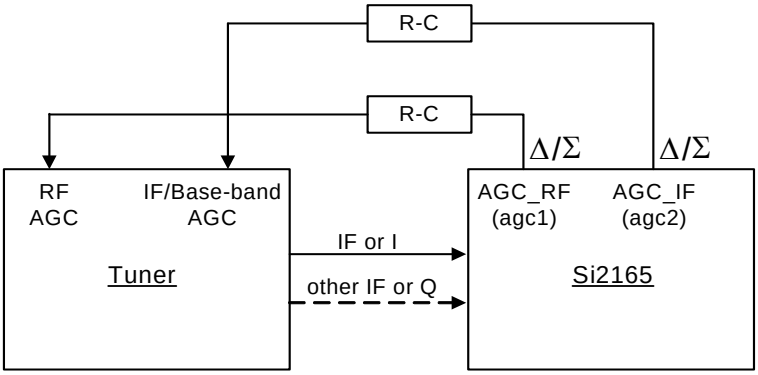

Figure 7. AGC Connection between Tuner and Si2165

Section "7.1. Typical Application with IF or Low-IF Tuner" on page 42 describes the recommended R-C circuit.

Minimum and maximum voltage swings can be set with registers **agc1_min (015Eh)** and **agc1_max (015Fh)**, and **agc2_min (016Eh)** and **agc2_max (016Fh)**.

AGC operation is performed to optimize the noise and linearity performance of the tuner. The highest gain is applied to the RF stage as long as the level is below the Takeover Point (TOP) to maximize noise performance. When the input level is higher than the TOP, the RF gain is reduced to ensure that linearity is maintained. This behavior is shown in Figure 8.

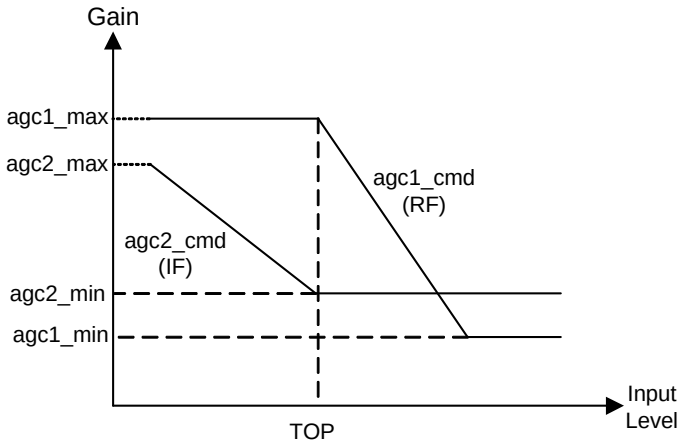

Figure 8. AGC Scheme

As shown in Figure 8, the TOP is set with register **agc2_min (016Eh)**. If the value of agc2_min is increased, the TOP is reduced. The AGC operation within Si2165 keeps the RF gain (agc1) to its maximum and adapts the IF/BB gain to ensure a proper level at the ADC input. If IF/BB gain (agc2) reaches the value set into the **agc2_min (016Eh)** register, the RF gain is reduced to reach the correct ADC level.

If the gain-versus-voltage characteristics of the amplifiers have a negative slope, the polarity of AGC controls have to be inverted via registers **agc1_pola (0160h)** and **agc2_pola (0170h)**. The default setting is a positive slope.

It should be noted that the *maximum AGC levels cannot exceed the selected V_{DD_VIO} supply voltage.*

Users can read the two agc1 and agc2 values from registers **agc1_cmd (0168h)** and **agc2_cmd (0178h)**.

For each AGC output, the AGC outputs can be set independently to push-pull or open drain modes using registers **agc1_buftyp (0160h)** and **agc2_buftyp (0170h)**. Furthermore, registers **agc_if_tri (018Bh)** and **agc_rf_tri (018Dh)** enable or tri-state the corresponding AGC outputs. Finally, the two registers, **agc_rf_slr (0192h)** and **agc_if_slr (0190h)**, allow modifying the slew rate with four settings on each AGC output pins. Register **agc_lock (0188h)** indicates when analog AGC has converged.

AGC1 and AGC2 loop bandwidths are programmable to set appropriate settling time and ensure stability for tuners with different gain versus voltage characteristics.

3.5. Digital Front End

The digital front end receives the ADC data and performs dc offset correction, I/Q mismatch correction, anti-alias filtering, and sample rate conversion.

3.5.1. DC Offset Correction

A dc removal function has been implemented to remove potential dc offset on I and Q input signals. Register **dc_bypass (0131h)** enables or disables this feature.

When enabled, the current dc offset correction values can be read from registers **dc_offset_i (0132h)** and **dc_offset_q (0133h)**, and the correction loop can be frozen to the current correction values via register **dc_freeze (0131h)**. Register **dc_coeff (0131h)** enables setting of the loop bandwidth.

If **iq_adc_swap (0122h)** is set to “swapped”, **dc_offset_i (0132h)** indicates the ADC Q offset and vice-versa.

3.5.2. I/Q Mismatch Correction

In ZIF applications, impairments in the tuner can lead to phase and amplitude mismatches on I/Q complex input signals; so, correction functions have been implemented to compensate for these.

Amplitude mismatch correction is applied to the Q branch and is enabled via register **iq_freeze (0134h)**. The gain currently applied to the Q branch can be read from register **q_gain (013Ch)**. If **iq_adc_swap (0122h)** is set to “swapped”, **q_gain (013Ch)** indicates the gain applied to the I branch. Register **iq_kagc (0135h)** enables setting of the loop bandwidth.

Phase mismatch correction is enabled via register **phase_freeze (0140h)**. The current phase correction can be read from register **phi_cor (0144h)**. Register **phase_kloop (0141h)** enables setting of the loop bandwidth.

3.5.3. Anti-Alias Filtering

Low-pass filtering has to be performed on the signal to remove unwanted images in order to avoid aliasing during the sample rate conversion that follows.

A digital AGC function allows compensating for the removed power. Register **aaf_crestf_dbx8 (01A0h)** sets the reference level for the filter's average output power level. The corresponding gain applied to the signal (after AGC convergence) can be read from register **aaf_agc_cmd (01B0h)**.

3.5.4. Bandwidth Setting For DVB-T/H

The user should select the DVB-T/H broadcast channel bandwidth (5, 6, 7, or 8 MHz) into the **bandwidth (0308h)** register.

Note: Where value = received bandwidth / 10 kHz i.e. 700 for 7 MHz (default value being 800 i.e. 8 MHz)

3.5.5. Sample Rate Conversion

The ratio between FE_clk and DVB_rate has to be programmed such that the sample rate converter can perform the timing recovery function. This is done through register **oversamp (00E4h)** with the following calculation:

$$oversamp = FE\_clk\ (in\ Hz) / DVB\_rate\ (in\ Hz) \times 2^{23}$$

3.5.6. ACI Filtering

Low-pass filtering has to be performed on the signal to remove adjacent channels and allow proper demodulation. In DVB-C, this filter is a square root raised cosine filter (Nyquist filter).

A digital AGC function allows the chip to compensate for removed power. Register **aci_crestf_dbx8 (01C8h)** sets the reference level for the filter's average output power level. The corresponding gain applied to the signal (after AGC convergence) can be read from register **aci_agc_cmd (01D8h)**.

3.6. Demodulator

Register **standard (00ECh)** configures the demodulator for either DVB-T/H or DVB-C demodulation. After power-on reset DVB-T/H is the default standard.

3.6.1. DVB-T/H

3.6.1.1. Normal Operation via TPS (Transmission Pilot Signaling)

In DVB-T/H, parameters needed for device synchronization are broadcast in the TPS carriers. Register **tps_lock (0394h)** signals whether the Si2165 has detected this information in the TPS carriers.

The TPS word length (33 bits for DVB-H, 31 bits for DVB-T, 23 bits for DVB-T without Cell-ID) can be read from register **tps_length (0418h)**.

Choice of high-priority (HP) or low-priority (LP) streams is achieved through programming the **req_stream (02E4h)** register.

When the TPS are found, the demodulator is automatically configured with the parameters detected in the TPS stream. When automatic synchronization is active, detected modulation parameters can be read from the following registers:

Registers	Definition	Read-only Values
auto_fft_mode (03F0h)	FFT mode	2K, 4K, 8K
auto_guard_int (03F4h)	Guard Interval type	1/32, 1/16, 1/8, 1/4
auto_constellation (03F8h)	Constellation type	QPSK, 16 QAM, 64 QAM
auto_rate_HP (0400h)	Code Rate for HP stream	1/2, 2/3, 3/4, 5/6, 7/8
auto_rate_LP (0404h)	Code Rate for LP stream	1/2, 2/3, 3/4, 5/6, 7/8
auto_hierarchy (0408h)	Hierarchical level	None, Alpha 1, Alpha 2, Alpha 4

Automatic synchronization can be disabled using register **automatic_synchro (02E8h)**. When turned off, individual DVB-T/H parameters need to be programmed using registers **req_fft_mode (02ECh)**, **req_guard_int (02F0h)**, **req_constellation (02F4h)**, **req_rate_HP (02F8h)**, **req_rate_LP (0300h)**, and **req_hierarchy (0304h)**.

3.6.1.2. Cell ID

Cell-ID is the identifier of the broadcasting DVB-T/H transmitter. The **cell_id (040Ch)** register provides the TPS decoded cell-ID value.

3.6.1.3. DVB-H Specifics

Next to standard 2K and 8K FFT modes for DVB-T, Si2165 also includes a 4K FFT mode for DVB-H reception. DVB-H transmission can also use a different kind of inner symbol deinterleaver. If the device detects within the TPS that the DVB-H specific in-depth deinterleaver is used, the DSP unit will automatically activate this function within the FEC block. The detected deinterleaver mode can be read from register **dvbh_interleaver (041Ch)**.

If register **automatic_synchro (02E8h)** is not set in automatic mode, the user should manually set the de-interleaver mode using register **symb_deint_mode (04C0h)**.

Extended TPS information is available in DVB-H mode and signals whether MPE-FEC coding and time slicing are used on either the low- or high-priority stream(s).

Registers	Indications
lp_mpe_fec (0415h)	MPE-F.E.C. is used on minimum one elementary LP stream
hp_mpe_fec (0417h)	MPE-F.E.C. is used on minimum one elementary HP stream
lp_time_slicing (0414h)	Time slicing is used on minimum one elementary LP stream
hp_time_slicing (0416h)	Time slicing is used on minimum one elementary HP stream

3.6.1.4. Common Phase Error (CPE) Compensation

To correct for a phase noise component common across the COFDM carriers, the Si2165 implements some CPE compensation. Register **cpe_req (0310h)** enables this feature, which is recommended to be left activated.

3.6.1.5. Impulsive Noise Protection

Special algorithms have been implemented to counteract most of the impulsive noise impairments on the DVB-T/H spectrum. Register **impulsive_noise_remover (031Ch)** enables this feature, which is recommended to be left activated.

3.6.1.6. Demod Status

Si2165 indicates if the DVB-T/H demodulator is locked in register **demod_lock_t (0390h)**. Register **freq_lock_t (0398h)** indicates whether carrier recovery is achieved. Register **timing_lock_t (039Ch)** indicates whether timing recovery is achieved. Register **fft_lock_t (03A0h)** indicates whether fft window synchronization is achieved.

For DVB-T/H demodulation, after any change to the RF setting(s) on the tuner, it is recommended to apply a "start_synchro" command via register **start_synchro (02E0h)**.

3.6.1.7. Timing Recovery

Timing offset can be computed from the **timing_corr_t (03B0h)** register according to the following formula:

$$TimingOffset\ (in\ ppm) = 4 \times 10^6 \times timing\_corr\_t \times DVB\_rate\ (in\ Hz) / (FE\_clk\ (in\ Hz) \times 2^{23})$$

With the default values of the loop parameters, the timing acquisition range of this loop is typically ±50 ppm. The acquisition range can be modified up to ±200 ppm thanks to register **timing_sync_range (0318h)**. Note, however, that the acquisition time may increase with the timing recovery range enlargement.

3.6.1.8. Carrier Recovery

The carrier recovery range can be adjusted with register **freq_sync_range (030Ch)**. The default value is set for 50 kHz offset.

Frequency offset can be computed from the **freq_corr_t (03B4h)** register according to the following formula:

$$FrequencyOffset\ (in\ Hz) = FE\_clk\ (in\ Hz) \times freq\_corr\_t / 2^{29}$$

3.6.1.9. DVB-T/H Equalizer

Time and frequency equalizers have been optimized for fixed/portable terrestrial channel recovery. The onboard firmware continually optimizes the behavior of both equalizers to the measured channel response. The current measured channel length can be computed from register **channel_length (03A4h)**.

An estimation of the signal-to-noise ratio can be computed from registers **sigma2_est (02A4h)** and **ref_signal_power (02C0)**. Actual value of C/N in dB is given by the following formula:

$$C/N\ (in\ dB) = 10 \times (log10\ (sigma2\_est / 2) / (ref\_signal\_power \times 64))$$

3.6.1.10. Reacquisition (Auto Re-lock) for DVB-T/H

Si2165 will relock automatically after an interruption to the RF input signal as e.g. the result of an antenna disconnect or RF signal interruption.

3.6.1.11. Scanning Procedure for DVB-T/H

- Fast scanning (host processor assisted)

During channel scanning, Si2165 can inform via register **check_signal (03A8h)** whether or not a COFDM DVB-T/H signal is present on a given RF channel. This improves channel scan time significantly as it provides a faster readout than waiting for the complete DVB-T/H lock process for those channels where no (or analog) modulation is present.

- QuickScan (on-chip, ultra-fast automatic channel scan)

The complete channel scan procedure is detailed in a forthcoming application note.

3.6.2. DVB-C

3.6.2.1. Constellation

The constellation format (from 16 QAM to 256 QAM, including rectangular constellations 32 & 128) shall be user-defined into the register, **req_constellation (02F4h)**.

3.6.2.2. Symbol Rate

Programming of the symbol rate is achieved via the **oversamp (00E4h)** register as defined in "3.5.5. Sample Rate Conversion".

3.6.2.3. Timing Recovery Loop

The timing recovery block implements a timing error detector and a second-order loop filter, for which loop bandwidth and damping factor are programmable for both acquisition and tracking modes.

The damping factor formula is:

$$Df = 13 \times 2^{(KP - (KI/2) - 11)}$$

The normalized bandwidth formula is:

$$Bl.Ts = 13 \times 2^{((KI/2) - 11)} \times (Df + 0.25 / Df)$$

KP is user-defined by two registers, **tim_kp_acq (0201h)** and **tim_kp_loc (0203h)**, while KI is similarly set by two registers, **tim_ki_acq (0200h)** and **tim_ki_loc (0202h)**. Depending on whether the device operates in acquisition or locked mode either "_acq" or "_lock" registers are selected. Register **demod_lock_c (023Eh)** is used internally to automatically switch from acquisition parameters to lock parameters.

Timing offset can be computed from the **timing_corr_c (0208h)** register according to the following formula:

$$TimingOffset\ (in\ ppm) = -10^6 \times timing\_corr\_c / (timing\_corr\_c + 2^{20})$$

With the default values of the loop parameters, the timing acquisition range of this loop is typically ±3000 ppm.

In addition to the above mentioned loop, a coarse timing recovery function is also provided which allows enlarging the timing acquisition range up to ±25% of the symbol rate. This feature is used for blind scanning of the band and its use is described in a forthcoming application note.

3.6.2.4. Carrier Recovery Loop

The carrier recovery block implements a phase detector and a programmable second-order loop filter and allows recovery of the carrier phase at the output of the equalizer. The loop parameters (loop bandwidth & damping factor) are programmable for acquisition and tracking modes:

The damping factor formula is:

$$Df = 2^{(KP - (KI/2) - 11)} \times SQRT(\pi \times 360)$$

The normalized loop bandwidth formula is:

$$Bl.Ts = 2^{((KI/2) - 10)} \times (Df + 0.25 / Df) \times SQRT(\pi \times 90)$$

KP is user-defined by two registers, **kp_acq (0238h)** and **kp_lock (023Ah)**, while KI is similarly set by two registers, **ki_acq (0239h)** and **ki_lock (023Bh)**. Depending on whether the device operates in acquisition or locked mode, either "_acq" or "_lock" registers are selected. Register **demod_lock_c (023Eh)** is used internally to automatically switch from acquisition parameters to lock parameters.

A readout for carrier frequency offset is available and given by the **phase_cor_c (0240h)** register according to the following formula:

$$FrequencyOffset\ (in\ Hz) = DVB\_rate\ (in\ Hz) \times phase\_cor\_c / 2^{16}$$

In addition to this loop, a programmable frequency sweep can be performed to enlarge the maximum frequency offset that the device is able to recover (up to 11% of the required symbol rate). The initial value of the carrier frequency sweep is set via register **sweep_init (0230h)** according to the following formula:

$$SweepInit\ (in\ Hz) = DVB\_rate\ (in\ Hz) \times sweep\_init / 256$$

The range of the carrier frequency sweep is set via register **sweep_range (0231h)** according to the following formula:

$$SweepRange\ (in\ Hz) = DVB\_rate\ (in\ Hz) \times sweep\_range / 256$$

The speed of the carrier frequency sweep is set via register **sweep_step (0232h)**. For each symbol, the frequency is incremented by:

$$SweepStep\ (in\ Hz) = DVB\_rate\ (in\ Hz) \times sweep\_step / 2^{24}$$

When the carrier recovery loop has converged, the sweep carrier frequency offset correction is given by register **freq_corr_c (0234h)**:

$$SweepFrequencyOffset\ (in\ Hz) = FE\_clk\ (in\ Hz) \times freq\_corr\_c / 2^{16}$$

The total carrier frequency offset is the sum of FrequencyOffset + SweepFrequencyOffset.

3.6.2.5. Demod Status

Si2165 indicates if the DVB-C demodulator is locked in register **demod_lock_c (023Eh)**.

3.6.2.6. Reacquisition (Auto Re-lock) for DVB-C

In DVB-C mode, if lock is lost for a time longer than a programmable timeout value, the device performs an automatic soft reset. The reset time after unlock is programmable via the **lock_timeout (00C4h)** register. The auto relock function is enabled via the **auto_reset (00CBh)** register.

3.6.2.7. Equalizer for DVB-C

The time equalizer operates on 32 QAM symbols (31 taps) and consists of a feed-forward part (FFE) and a feed-back part (DFE).

The length of the FFE part is programmable via register **ffe_length (0260h)**, and the DFE part uses the remaining taps. The central tap position of the FFE is set with register **central_tap (0261h)** and must be less than the FFE length.

Equalizer coefficient adaptation is performed by two different algorithms depending on whether the carrier has been recovered:

- As long as the carrier recovery is not locked, a Constant Modulus Algorithm is used, and FFE coefficients are adapted using the adaptation step programmed in register **gain_cma (0264h)**.
- Once the carrier has been recovered a Decision Directed Algorithm is used, and both FFE and DFE coefficients are adapted using the adaptation steps programmed in registers **gain_ddffe (0264h)** and **gain_dddfe (0265h)**.

It is strongly recommended to set the **auto_algo (0278h)** register to “dfe_init” value, in order to automatically recover lock status in case of any de-synchronization.

An estimation of the signal-to-noise ratio at the output of the equalizer is provided in register **c_n (026Ch)**, and the actual value of C/N in dB is given by the following formula:

$$C/N\ (in\ dB) = 10 \times log10\ (2^{24} / c\_n)$$

3.6.2.8. Scanning Procedure for DVB-C

The complete digital cable channel scan procedure is detailed in a forthcoming application note.

3.7. Forward Error Correction

3.7.1. DVB-T/H

For DVB-T/H, the FEC section consists of inner and outer FEC. Refer to Functional Description for additional detail. Si2165 does not include decoding of the additional MPE-FEC layer for mobile DVB-H reception. However for DVB-H reception with fixed receivers, decoding of the MPE FEC layer is not required. The FEC for DVB-T/H is automatically configured.

3.7.2. DVB-C

For DVB-C, the FEC section does not require any user-specific configuration (unless changing default settings of packet synchronization).

3.7.3. Lock Status and Performance Indicators

3.7.3.1. Device Status

The Si2165 provides readouts for both packet and FEC lock. In DVB-C mode, packet synchronization is performed via a correlation search on the SYNC (0x47 / 0xB8) byte of the TS packet.

In DVB-C mode, packet synchronization searches for the regular occurrence of 0x47/0xB8 SYNC bytes within the stream. The number of consecutive occurrences to generate a lock status can be set in register **ps_sync_thr (044Dh)**. Once locked, register **ps_superv_thr (044Eh)** sets the number of consecutive missed occurrences to generate an unlock status. If required when locked, register **ps_stay_locked (0448h)** allows the lock state to be maintained.

Lock Indicators	Registers
Packet Synchronization lock	**ps_lock (0440h)**
F.E.C. lock	**fec_lock (04E0h)**

In DVB-T/H mode, packet synchronization is automatically achieved since the frame contains an integral number of TS packets.

Register **ts_before_lock (04E4h)** can be programmed to optionally hold the TS output bus quiet, forcing it to 0, when there is no FEC lock. In that case, the signalization signals (TS_SYNC, TS_VAL) are also forced to 0, but then TS_CLK remains active.

3.7.3.2. Performance Indicators

- CBER

The Viterbi decoder provides Channel Bit Error Rate (CBER) monitoring information. The computation method consists of re-encoding the output of the Viterbi decoder and comparing the re-encoded bits to the delayed hard decisions at the input of the Viterbi decoder.

The error rate monitoring mechanism is as follows:

- **cber_bit (0428h)** register value provides the number of bits to take into account for one computation period.
- **cber_err (0430h)** register value provides the number of erroneous bits found over the computation period.
- The final CBER ratio computation is then defined by the following formula:

$$CBER = \frac{CBER\_ERR}{CBER\_BIT}$$

- Register **cber_rst (0424h)** is used to reset the error counters and start a new computation period.
- Status register **cber_avail (0434h)** indicates that the computation period is over after a CBER reset (or after device reset).

- BER

The Reed-Solomon decoder allows monitoring of input Bit Error Rate (BER).

The error rate monitoring mechanism is as follows:

- **ber_pkt (0470h)** register value provides the number of RS packets to take into account for one computation period.
- **ber_bit (0478h)** register value provides the number of erroneous bits found over the computation period.
- The final BER computation is then defined by the following formula:

$$BER = \frac{BER\_BIT}{BER\_PKT \times 204 \times 8}$$

- Register **ber_rst (046Ch)** is used to reset the error counter and start a new computation period.
- Status register **ber_avail (047Ch)** indicates that the computation period is over after a BER reset (or a device reset).

- PER

The Reed-Solomon decoder allows monitoring of output Packet Error Rate (PER).

The error rate monitoring mechanism is as follows:

- **per_pkt (0484h)** register value provides the number of RS packets to take into account for one computation period.
- **per (048Ch)** register value provides the number of erroneous packets found over the computation period
- The final PER computation is then defined by the following formula:

$$PER = \frac{PER}{PER\_PKT}$$

- Register **per_rst (0480h)** is used to reset the error counter and start a new computation period.
- Status register **per_avail (0490h)** indicates that the computation period is over after a PER reset (or a device reset).

- UNCOR Counter

In addition, the Reed Solomon decoder also offers a way to monitor the occurrence of uncorrectable packets over a flexible period of time.

Register **uncor_cnt (0468h)** provides the number of uncorrectable RS packets after a reset up to its saturation value of 255, until the next reset via register **uncor_rst (0464h)**.

3.8. System Control

3.8.1. Power Supply Ramp-Up / Ramp-Down Sequence

Si2165 requires only two industry-standard power supplies: 1.2 and 3.3 V. V_{DD_VIO} is usually set to 3.3 V, but 1.8 or 2.5 V can be substituted as well. There is no specific power-up/power-down sequencing with regards to V_{DD_VCORE}, V_{DD_VIO}, V_{DDH_VANA}, and V_{DD_VADC} supplies. However, it is recommended that RESETB be held low while the supplies are powered up in order to prevent potential bus conflicts on the I/O pins of the Si2165. Once the supplies have stabilized to their nominal voltages, RESETB can be brought high. Also, if V_{DD_VCORE} is turned off to enter a low power state, the RESETB pin must be brought and held low while V_{DD_VCORE} is off to put the Si2165 into a state with the lowest possible power consumption.

3.8.2. Initialization Procedure

3.8.2.1. Hard Reset

Pin RESETB, active low, resets all the logic and *sets all internal registers to their respective default values*. Any pre-loaded DSP firmware patch would need to be reloaded.

After power-on reset, all output signals i.e. TS_DATA[0..7], AGC_IF, AGC_RF and GPIO_0 are left in high-impedance (tri-state) mode.

The following registers provide individual output-enable control of output signals on pins TS_DATA[0..7], TS_SYNC, TS_ERR, TS_VAL, TS_CLK, AGC_IF, AGC_RF and GPIO_0: **ts_data0_tri (04EFh)** to **ts_data7_tri (04EFh)**, **ts_sync_tri (04F0h)**, **ts_err_tri (04F0h)**, **ts_val_tri (04F0h)**, **ts_clk_tri (04F0h)**, **agc_if_tri (018Bh)**, **agc_rf_tri (018Dh)**, and **gpio0_tri (05C1h)**.

3.8.2.2. Device Initialization Sequence

Si2165 device requires an initialization procedure that includes internal calibration. This must be done after each power-on reset and will take less than 10 ms to be completed.

Step 1: System Configuration

Consists of programming the **chip_mode (0000h)** register. This register releases the Si2165 from standby mode and specifies the clock source type on which the chip will rely.

Step 2: PLL Setup

Internal clocks frequencies have to be set properly according to the frequency of the reference clock/crystal. This is done by enabling the PLL via **pll_enable (00A2h)**, then accessing the **pll_divl (00A0h)**, **pll_divm (00A1h)**, **pll_divn (00A2h)**, **pll_divp (00A2h)**, and **pll_divr (00A3h)** registers.

Step 3: Initialization Procedure

In order to launch the initialization mode, user should activate register **chip_init (0050h)** then **start_init (0096h)**.

The user should then either monitor register **init_done (0054h)** until the status shows “completed” or wait for a fixed timeout (5 ms typical, depending on the sys_clk frequency).

Then, the user should return to normal device functional mode by again appropriately programming the **chip_init (0050h)** register and issue one software reset via register **rst_all (00C0h)**.

Step 4: Start DSP

For DVB-T/H operation, the DSP should now be started by programming register **addr_jump (0348h)**. This 32-bit register determines the memory address to jump to, when the firmware is available in memory (default value is F4000000h).

In case a DSP firmware patch is necessary, it should be downloaded via I^2C transactions after the DSP boot (refer to “3.8.3.1. DSP Boot” for the indication of DSP boot completion).

For DVB-C demodulation, usually, no firmware patch is necessary, and, in this case, the DSP can be parked by setting register **addr_jump (0348h)** to 0. The DSP block can also be turned off, thus saving some power consumption, by modifying register **dsp_clock (0104h)**. If a downloaded firmware patch is recommended for DVB-C demodulation, then the on-chip DSP shall always remain active.

Step 5: Demodulation Parameters and ADC Settings

Finally, the desired standard and appropriate related IF parameters must be set using registers:

standard (00ECh), **adc_sampling_mode (00E0h)**, **if_freq_shift (00E8h)**, and **oversamp (00E4h)**, which are common to both DVB standards.

The recommended and optimized ADC settings are as follows:

1. Set **adc_ri1 (012Ah)**: 0x46
2. Set **adc_ri3 (012Ch)**: 0x00
3. Set **adc_ri5 (012Eh)**: 0x0A
4. Set **adc_ri6 (012Fh)**: 0xFF
5. Set **adc_ri8 (0123h)**: 0x70

Then, **bandwidth (0308h)** is specific to DVB-T/H, or **req_constellation (02F4h)** is specific to DVB-C.

End the procedure by applying a soft reset procedure as described in “3.8.2.3. Soft Reset Procedure”.

The startup sequence is summarized in Figure 9.

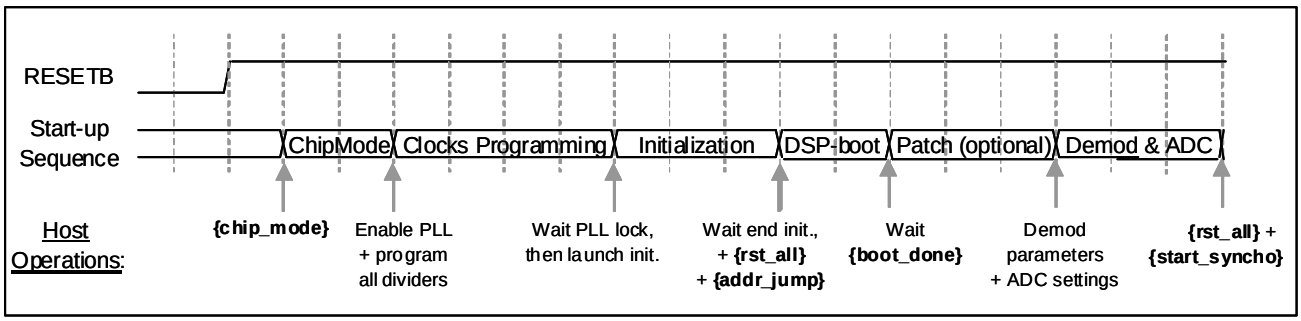

Figure 9. Initialization Sequence

3.8.2.3. Soft Reset Procedure

Register **rst_all (00C0h)** is used to perform a soft reset that re-initializes all the Si2165 logic, except the internal registers. Any preloaded DSP firmware patch is not affected by a soft reset. A soft reset is mandatory before attempting to achieve the first demodulator lock.

Then, a new synchronization has to be launched via the **start_synchro (02E0h)** register.

Note: Intensively applying soft reset commands on the Si2165 device will not freeze its proper operation (after the next synchronization start).

3.8.3. DSP Operations

3.8.3.1. DSP Boot

Register **boot_done (0341h)** indicates whether the DSP boot process has been successful or is still in-progress.

3.8.3.2. DSP Watchdog

In the unlikely event that the DSP locks and automatically reboots as the result of an action from the internal watchdog, the **wdog_error (0341h)** register provides an indicator that such a reboot has occurred.

The user can reset this error using the **rst_wdog_error (0341h)** register.

3.8.3.3. Patch Identification

In case a firmware patch has been downloaded into RAM, the patch code version can be identified by reading register **patch_version (0344h)**.

DSP patch compilation generates a CRC key that can be compared, after downloading, to the CRC key computed inside Si2165. Readout of the 16-bit key is found in register **crc (037Ah)**.

Register **rst_crc (0379h)** allows resetting the CRC key within the device.

3.8.4. Standby Mode

3.8.4.1. Software Power-down

Register **chip_mode (0000h)** allows configuration of the Si2165 in such a way that all logic inside the device becomes inactive with the exception of the I^2C block (but not affecting the programmed register values or any pre-loaded DSP firmware patch).

The proper sequence to set Si2165 in power down mode is as follows:

1. Stop the clock of the DSP through register **dsp_clock (0104h)**.
2. Set Si2165 in stand-by mode via register **chip_mode (0000h)**.

The proper sequence to recover from above power-down mode is as follows:

1. Set Si2165 in operating mode via register **chip_mode (0000h)**.
2. Start the clock of the DSP through register **dsp_clock (0104h)**.

3.8.4.2. Shutting Off V_{DD_VCORE} Alone

If the application needs to power down only the V_{DD_VCORE} (1.2 V) supply while still keeping the V_{DD_VIO} (typically 1.8, 2.5, or 3.3 V) active, the *RESETB pin must stay low at all times while V_{DD_VCORE} is turned-off*.

4. MPEG Transport Stream Bus

Si2165 supports three output modes. However, only one output bus mode can be active at any given time:

- TS master parallel: Si2165 outputs TS_CLK and TS_DATA over an 8-bit parallel data bus
- TS master serial: Si2165 outputs TS_CLK and TS_DATA over a 1-bit serial data bus
- TS slave parallel GPIF (general purpose interface): Si2165 indicates when data is buffered in its internal FIFO. An external device polls data by providing a clock/strobe signal. Si2165 provides data over an 8-bit parallel data bus.

The MPEG Transport Stream (TS) output interface carries the decoded terrestrial/cable data to external devices for further MPEG decoding. The MPEG-TS output interface consists of the following pins for each mode:

Table 6. Three Main TS Modes and Pin Assignment

Pin	Pin Name	TS Serial Mode	TS Parallel Mode	GPIF: TS Slave Parallel Mode
7	TS_VAL / GPIF_CLK	TS valid data signal	TS valid data signal	GPIF clock
8	TS_SYNC / GPIF_RDY	TS synchro / frame start signal	TS synchro / frame start signal	GPIF ready signal
9	TS_CLK / GPIF_CTL	TS clock	TS clock	GPIF control signal
11	TS_DATA[0] / TS_SER	TS serial data stream	TS parallel output bit #0	TS parallel output bit #0
12	TS_DATA[1] / GPIO_1	Unused (can be GPIO #1)	TS parallel output bit #1	TS parallel output bit #1
13	TS_DATA[2] / GPIO_3	Unused (can be GPIO #3)	TS parallel output bit #2	TS parallel output bit #2
14	TS_DATA[3] / GPIO_4	Unused (can be GPIO #4)	TS parallel output bit #3	TS parallel output bit #3
16	TS_DATA[4] / GPIO_5	Unused (can be GPIO #5)	TS parallel output bit #4	TS parallel output bit #4
17	TS_DATA[5]	Unused	TS parallel output bit #5	TS parallel output bit #5
18	TS_DATA[6]	Unused	TS parallel output bit #6	TS parallel output bit #6
20	TS_DATA[7]	Unused	TS parallel output bit #7	TS parallel output bit #7
21	TS_ERR / GPIO_2	TS packet error indicator or GPIO #2	TS packet error indicator or GPIO #2	Unused signal or GPIO #2

In parallel mode, TS_DATA[0..7] carries the TS stream. In serial mode, TS_SER / TS_DATA[0] carries the TS stream.

In master mode: TS_CLK, TS_SYNC, TS_VAL, and TS_ERR signals are available.

- TS_CLK is the MPEG TS clock output.
- TS_SYNC output is active during the first byte of each TS packet. TS_SYNC is only active when TS synchronization exists.
- TS_VAL output is used to indicate when valid data is present. TS_VAL is active during the MPEG-TS payload packet data (188 bytes per TS packet) and inactive during Reed-Solomon parity packet data (16 bytes per TS packet) or when there is no TS synchronization. Note also that there will be clock periods during which TS_VAL will signal that no valid data is present, due to the fact that TS_CLK does not equal the actual TS bit or byte clock.
- TS_ERR output indicates that an uncorrectable error has been detected in the RS decoding stage and that the current TS data packet contains uncorrectable errors. The TS_ERR output is active during the entire erroneous TS packet.

4.1. General TS Output Programmability (Available in All Bus Modes)

The programmability described in this section is available for all modes (master parallel, master serial, slave parallel).

Register **ts_data_sync_overwr (04E4h)** provides the option to overwrite the sync byte. When enabled, all sync bytes received are replaced by 0x47 value. When “disabled”, they are left unchanged.

Reed-Solomon parity bytes may be optionally forced to zero via register **ts_data_parity (04E4h)**.

Register **ts_before_lock (04E4h)** provides the option to force TS data to zero as long as no FEC lock is obtained.

Register **ts_data_dir (04E4h)** allows changing the MSB-to-LSB bit order on the TS_DATA bus in parallel mode. This ensures an easy routing of the Si2165 output irrespective of pin order on the host device. In serial mode, this register allows a selection between MSB-first and LSB-first serial output.

Register **ts_tei (04E4h)** enables signaling of the Transport Error Indicator (TEI) bit, the MSB of the second byte of each TS packet. When signaling is “enabled”, the TEI bit is set to “1” when an unrecoverable packet error has occurred. When “disabled”, the TEI bit is always left unchanged.

After device power-on reset, all TS data and control signals are in tri-state mode as default.

The MPEG-TS data output pins are individually released from tri-state by using registers **ts_data0_tri (04EFh)** to **ts_data7_tri (04EFh)**.

Similarly, registers **ts_clk_tri (04F0h)**, **ts_sync_tri (04F0h)**, **ts_err_tri (04F0h)**, and **ts_val_tri (04F0h)** provide release from tri-state for control signals TS_CLK, TS_SYNC, TS_ERR, and TS_VAL.

Note that the tri-state release and slew rate controls are implemented in the output drivers, and, thus, these settings affect the corresponding pins in every configuration. In other words, these registers also affect tri-state output and slew rate selection when the pins are configured for use as GPIO or when using GPIF mode.

Eight registers on two bytes, from **ts_data0_slr (04F4h)** to **ts_data7_slr (04F5h)** enable to adjust slew rate for the TS_DATA[0..7] pins. Four different options (slowest, moderate, fast, fastest) are user-selectable.

Similarly, the four registers on one byte **ts_clk_slr (04F6h)** / **ts_err_slr (04F6h)** / **ts_sync_slr (04F6h)** / **ts_val_slr (04F6h)** enable to modify the TS control signals (TS_CLK, TS_ERR, TS_SYNC, TS_VAL) slew rate.

Si2165 supports both master and slave TS bus modes. The slave TS bus mode is also called GPIF (general purpose interface bus) mode. Register **ts_mux (04E9h)** configures the bus mode. In master TS bus mode, both parallel and serial outputs are supported while slave TS bus (GPIF) mode is only compatible with parallel output.

4.2. TS Master Mode

Both master parallel (default setting) and master serial modes are supported. The programmability described in this paragraph is available for all TS master modes (parallel and serial).

The active edge of TS_CLK can be programmed such that data is transitioning either on the rising or falling edge of TS_CLK using register **ts_clk_edge (04E5h)**.

Polarities of TS_SYNC, TS_VAL, and TS_ERR can be programmed independently using registers **ts_sync_pola (04E6h)**, **ts_val_pola (04E6h)**, and **ts_err_pola (04E6h)**.

TS data can be output in either a parallel byte-wide mode or a serial bit-wide mode for system-level flexibility. Register **ts_data_mode (04E4h)** controls the selection of the interface mode. Both modes are discussed in the following sections.

4.2.1. TS Master Parallel Modes

Si2165-D device proposes various modes of operations for parallel output modes, as described in Table 7:

Table 7. TS Master Parallel Output Mode Settings

TS Parallel Output Mode	Register Setting for ts_clk_mode (04E5h)	Register Setting for ts_parallel_mode (08F8h)
Mode1 gapped	Gapped	Mode1
Mode1 continuous	Continuous	Mode1
Mode2_div_6	X	Mode2_div_6
Mode2_div_8	X	Mode2_div_8
Mode2_div_12	X	Mode2_div_12
Mode2_div_16	X	Mode2_div_16

In both mode1 output cases, the TS clock period is not regular and its average value is adapted to the received data rate.

- In mode1 continuous, TS_CLK remains active during the parity bytes. TS_VAL is used to distinguish between valid TS data and parity bytes. Figures 11 and 12 provide output timing waveforms.
- In mode1 gapped, TS_CLK is only active during payload bytes. Figures 13 and 14 provide output timing waveforms.

In mode2_div_N (N=6/8/12/16), the TS clock frequency is fixed and is equal to sys_clk/N. In this case, TS_CLK remains active during the parity bytes. In these four specific modes, the **ts_clk_mode (04E5h)** register has no effect, and TS_VAL is used to select valid data bytes. Figure 10 provides output timing waveforms.

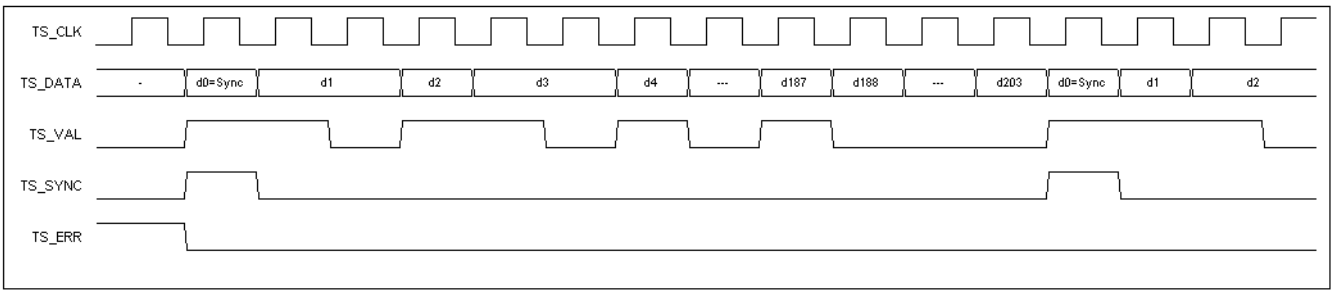

Figure 10. Mode2_div_N TS Parallel Mode with Enabled Parity Bytes and Active High Polarities

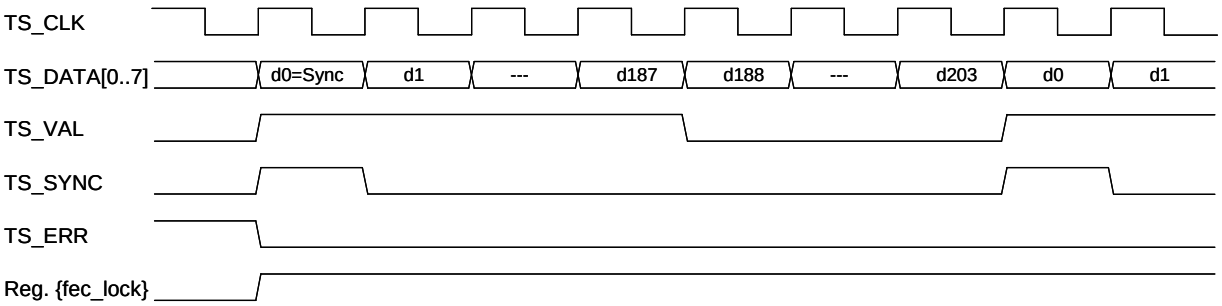

Figure 11. Continuous TS Parallel Mode with Rising Active Clock Edge and Enabled Parity Bytes

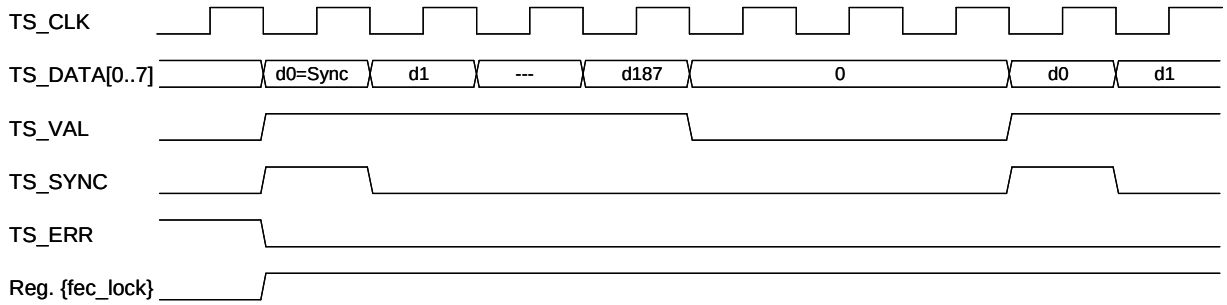

Figure 12. Continuous TS Parallel Mode with Falling Active Clock Edge and Disabled Parity Bytes

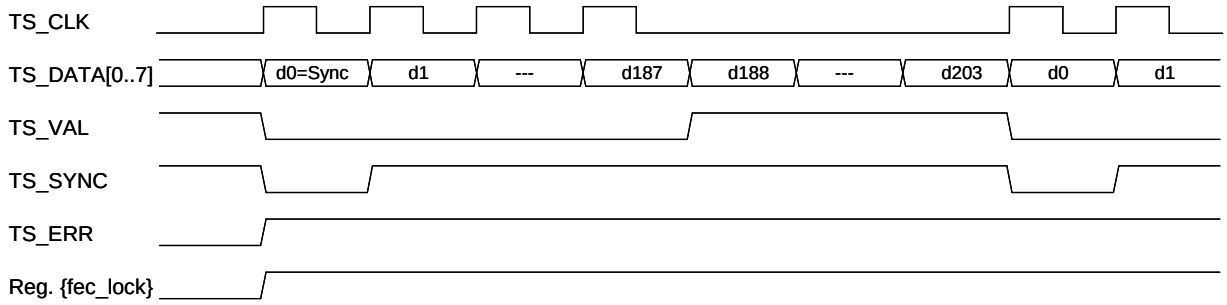

Figure 13. Gapped TS Parallel Mode with Rising Active Clock Edge, Enabled Parity Bytes, and Active Low Polarities

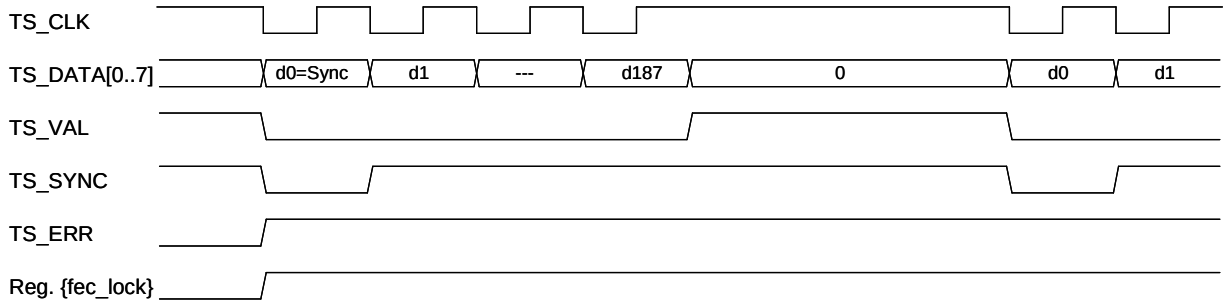

Figure 14. Gapped TS Parallel Mode with Falling Active Clock Edge, Disabled Parity Bytes, and Active Low Polarities

4.2.2. TS Master Serial Mode

The TS_CLK frequency in serial mode is fixed to:

- For DVB-T/H: TS_CLK = sys_clk/2
- For DVB-C: TS_CLK = sys_clk

In TS master serial mode, the TS_SYNC pulse can be programmed to be active for the whole byte or the first bit only, via register **ts_sync_length (04E6h)**.

Both continuous and gapped clock modes are supported by programming register **ts_clk_mode (04E5h)** accordingly.

4.2.2.1. Continuous TS Serial Mode

In continuous TS serial mode, TS_CLK remains active during parity bytes and during TS_CLK cycles between bytes (payload or parity). TS_VAL frames valid bytes. Figures 15 and 16 show the output timing waveforms.

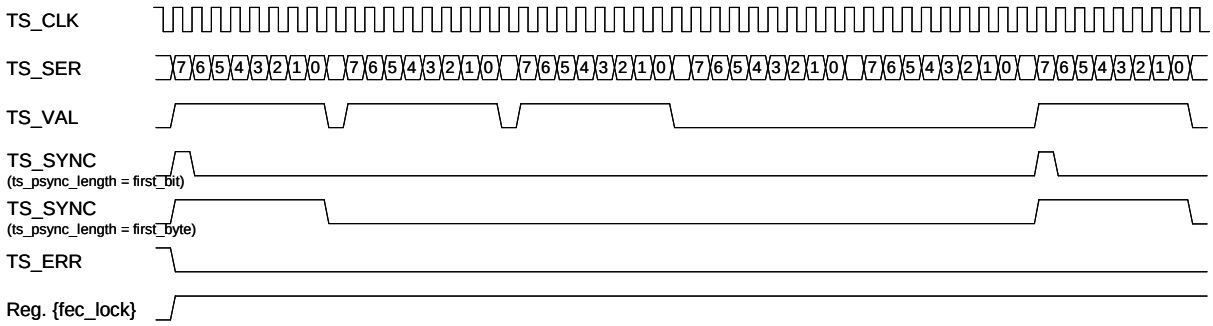

Figure 15. Continuous TS Serial Mode with Rising Active Clock Edge, Enabled Parity, and Active High Polarities

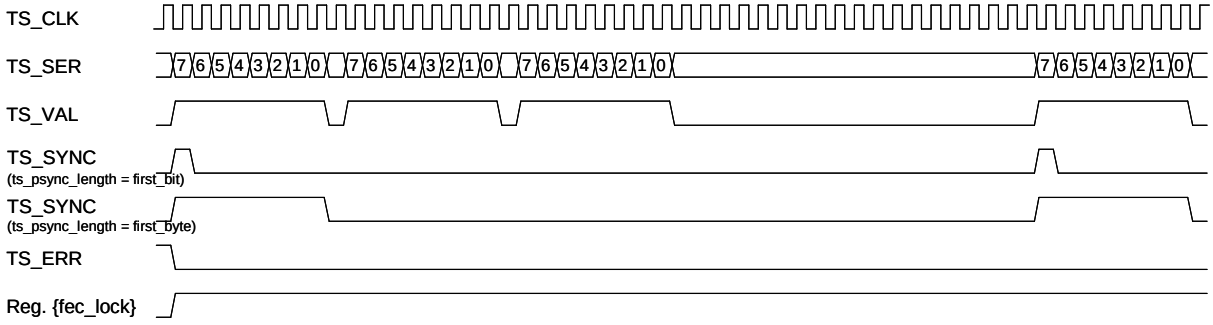

Figure 16. Continuous TS Serial Mode with Falling Active Clock Edge, Disabled Parity, and Active High Polarities

4.2.2.2. Gapped TS Serial Mode

In gapped TS serial mode, TS_CLK is only active during payload bits (when register **ts_data_parity (04E4h)** is disabled) or during payload plus parity bits (when register **ts_data_parity (04E4h)** is enabled). Figures 17 and 18 show the output timing waveforms.

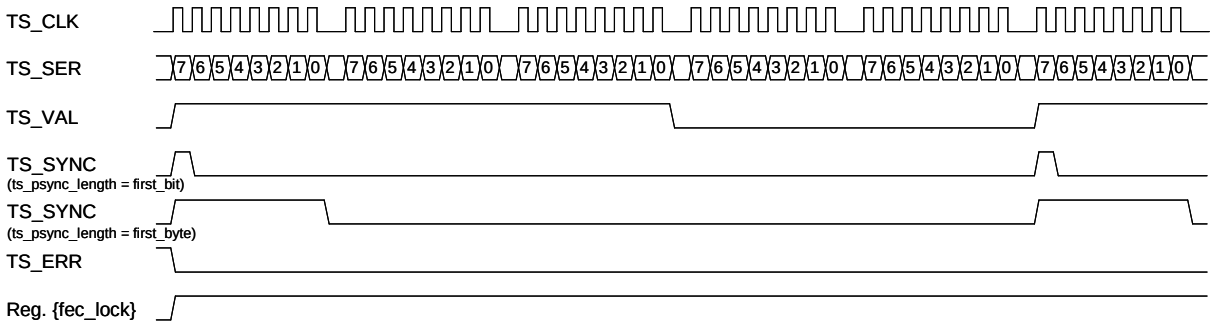

Figure 17. Gapped TS Serial Mode with Rising Active Clock Edge, Enabled Parity Bytes, and Active High Polarities

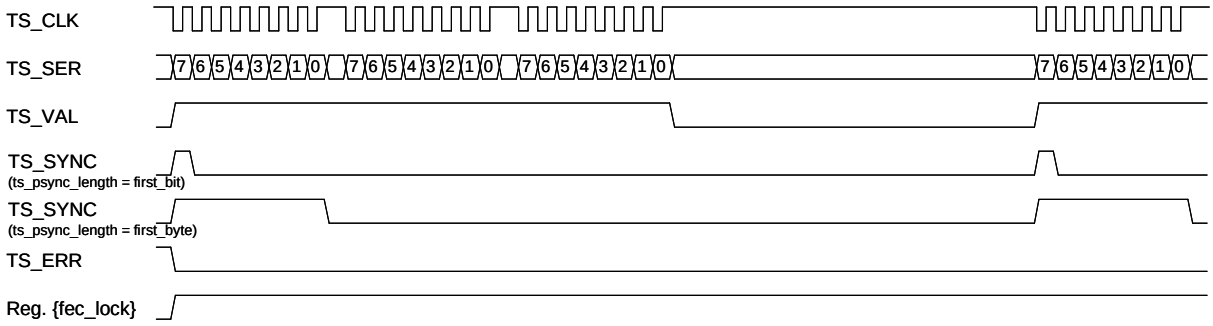

Figure 18. Gapped TS Serial Mode with Falling Active Clock Edge, Disabled Parity Bytes, and Active High Polarities

4.3. TS Slave Parallel Mode (Microprocessor Interface Mode)

Si2165 can seamlessly connect to any standard microcontroller bus. A specific bridge to interface parallel MPEG-TS output to a GPIF bus has been implemented. Only parallel mode transfer is supported. Data transfer from the GPIF interface is controlled by the microcontroller. GPIF is the suggested interface to controllers implementing specific bus protocols, such as USB and PCI-Express.

An embedded RAM (1024 bytes) is used to buffer the MPEG TS before it is read via the GPIF bus.

To enable/disable the GPIF transfer mode, the user should select the GPIF bus mode via register **ts_mux (04E9h)** and activate it via register **gpif_standby (0500h)**.

The GPIF clock signal from the microcontroller/USB device should be connected to the GPIF_CLK pin. Once Si2165 detects a data block of 512 bytes internally buffered in RAM (this data buffer size is not user-changeable), pin GPIF_RDY is set high to signal availability of output data to the controller.

The controller should provide a high logic level on pin GPIF_CTL to indicate that it is ready to receive the packet data. Then, two clock cycles later, the 512 bytes of data are sent to the TS output pins on successive GPIF_CLK cycles. Si2165 outputs a low logic level on pin GPIF_RDY two cycles before the end of data to signal the end of data transfer.

Finally, the microcontroller sets pin GPIF_CTL back to a low logic level and starts waiting for the next available block of data.

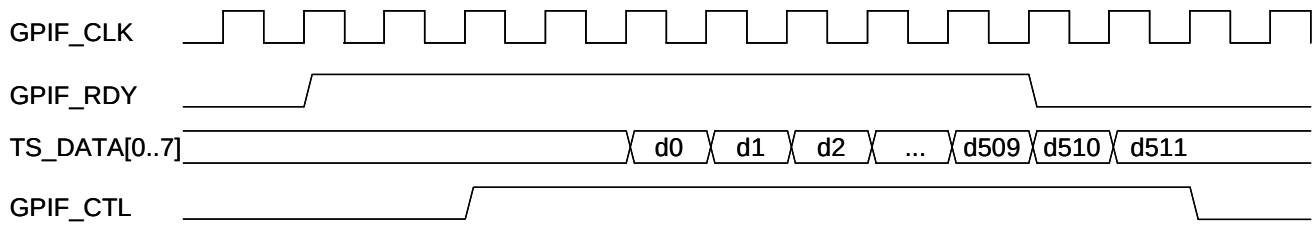

Figure 19. GPIF Timing Waveform

Internal GPIF data buffering consists of an internal RAM and an input FIFO to this RAM. When overflow occurs on any of these, registers **gpif_in_fifo_overflow (0500h)** and **gpif_ram_overflow (0500h)** are flagged. To reset both registers, the user should write register **gpif_alarm_reset (0504h)**.

As noted previously, registers **ts_data_dir (04E4h)**, **ts_tei (04E4h)**, and **ts_data_sync_overwr (04E4h)** have similar effects on the GPIF interface as on the MPEG-TS interface. Other MPEG-TS control registers are not available in GPIF mode.

4.4. TS PID Filtering

In order to reduce the MPEG TS data rate, users can filter the transport stream such that Si2165 only outputs TS packets with programmable PIDs (packet IDs). The PID filter allows filtering of the MPEG-TS packets according to a maximum of 32 programmable PID values (13-bits each). The filtering can be positive/inclusive (i.e. TS packets with PIDs in the PID filter list are included in the TS output) or negative/exclusive (i.e. TS packets with PIDs in the PID filter list are excluded from the TS output).

The PID filtering function (bypassed as default setting) is enabled via register **pid_filter_en (0510h)**.

Then, up to 32 PID filters can be switched on; registers **pid_en_0 (0514h)**, **pid_en_1 (0514h)**, **pid_en_2 (0514h)**, …. **pid_en_31 (0517h)** enable each individual filter.

For each enabled PID filter, the user should write the actual PID value to filter into the corresponding registers, **pid_0 (0518h)**, **pid_1 (051Ch)**, **pid_2 (0520h)**, ... **pid_31 (0594h)**.

Finally, register **pid_p (0510h)** determines whether to apply a positive/inclusive or a negative/exclusive filtering.

4.5. TS Timing Diagrams

Output timing depends on output bus loading as well as on the applied V_{DD_VIO} voltage.

4.5.1. Timings

The jitter specification for the TS_CLK signal varies depending on the selected TS output mode:

- In TS master serial mode, TS_CLK has virtually no jitter.
- In TS mode1 master parallel modes, the TS_CLK exhibits typically about 270 ns of peak-to-peak jitter.
- In TS mode2 master parallel modes, the TS_CLK has virtually no jitter.

4.5.2. V_{DD_VIO} Impact on TS Outputs

When V_{DD_VIO} is reduced to 1.8 or 2.5 V, the maximum TS frequency (for a given load) or the maximum capacitive load (for a given output frequency) varies proportionally as follows:

Table 8. Maximum Output Bus Frequency vs. Load

V_{DD_VIO} (V)	Max. Frequency @ 20 pF Load	Max. Load @ 70 MHz
3.30	100 MHz	30 pF
2.50	80 MHz	24 pF
1.80	50 MHz	12 pF

5. I²C Control Bus

5.1. I²C Device Address Selection

Four device I²C addresses are available, allowing up to four Si2165 to share the same I²C bus. The 7-bit device address consists of a fixed part (5 MSBs), followed by a programmable 2-bit part. The LSB of the device address signals whether a read or write I²C operation occurs.

The voltage on the ADDR pin is used to set the programmable 2-bit part of the device address. The ADDR pin embeds both internal pull-down and pull-up resistors (210 kΩ each) to ground and V_{DDH_VANA}. The various I²C device addresses can be selected with a single external resistor as summarized in Table 9.

Table 9. I²C Device Address Selection

device_address[7..3]	device_address[2:1]	ADDR Voltage (V) (Pin Connection)	device_address[0]
1 1 0 0 1	*1 1*	V_{DDH_VANA} (ADDR tied to V_{DDH_VANA})	R = 1 / W = 0
1 1 0 0 1	*1 0*	2/3 x V_{DDH_VANA} ± 10% (220 kΩ pull-up to V_{DDH_VANA})	R = 1 / W = 0
1 1 0 0 1	*0 1*	1/3 x V_{DDH_VANA} ± 10% (220 kΩ pull-down to ground)	R = 1 / W = 0
1 1 0 0 1	*0 0*	0 (ADDR tied to ground)	R = 1 / W = 0

The value of the detected device_address[2:1] can be read via register **i2c_addr (0013h)**.

5.2. I²C Bus Architecture and Operation Modes

Si2165 contains two independent I²C control buses (5 V compatible when V_{DD_VIO} is set to 3.3 V): one host-side bus and one tuner-side bus. Both buses implement a FAST (400 kHz) I²C interface.

The tuner-side bus can provide a quiet control bus, carrying only tuner commands, to the RF front end.

The internal I²C state machine runs from the SCL clock; so, there is no need for a high-speed clock. The I²C section always remains active, even if the device is in standby mode. However, only the two registers, **chip_mode (0000h)** and **i2c_passthru (0001h)**, are modifiable during standby.

5.2.1. I²C Standard Operation

The I²C bus interface is provided for configuration and monitoring of all internal registers. The Si2165 supports a 7-bit device addressing procedure and is capable of operating at rates up to 400 kbps. Individual data transfers to and from the device are 8-bits. The I²C bus consists of two wires: a serial clock line (SCL) and a serial data line (SDA). The device always operates as a bus slave. In order to be active, the I²C block requires that V_{DD_VIO} and V_{DD_VCORE} supplies be turned-on.

Read and write operations are performed in accordance with the I²C bus specification and the following sequences:

- The first byte after the START condition consists of the slave address (SLAVE ADR, 7-bits) of the target device. The R/W bit determines the direction of data transfer. During a read operation, data is sent from the device to the bus master. During a write operation, data is sent from the bus master to the device.
- The field labeled "ADDR" (in the graphs below) must contain the 8 or 16 bit address of the target register. The data to be transferred to or from the target register must be placed in the following 8-bit "DATA" field(s).
- An auto-increment address feature is implemented so that the target register address is automatically incremented for subsequent data transfers until a STOP condition ends the operation.

5.3. I²C Register Addressing Modes (8 or 16-bit)

Two I²C register addressing modes are available for Si2165.

5.3.1. 16-bit Mode

This is the native mode for read/write register addresses and follows the format: (NNNNh).

In this mode, the I²C write and read command sequences consist of a first two bytes carrying the register address followed by additional data bytes, as shown in Figures 20 and 21.

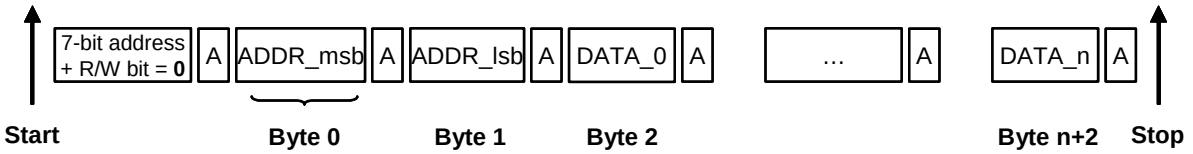

Figure 20. I²C Write Command Sequence in 16-Bit Addressing Mode

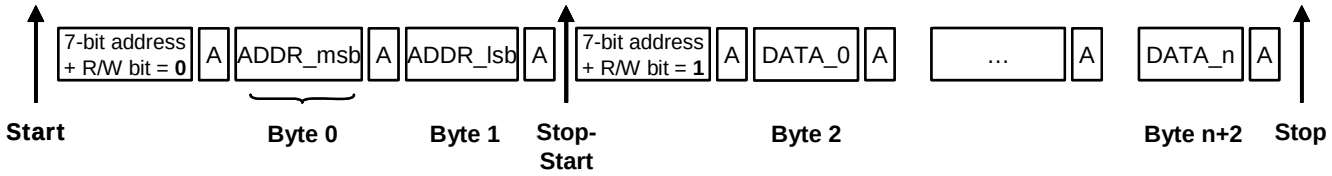

Figure 21. I²C Read Command Sequence in 16-Bit Addressing Mode

5.3.2. 8-bit Mode

In this mode, the I²C write and read command sequences consist of a first single byte carrying the register address followed by additional data bytes, as shown in Figure 22 and Figure 23.

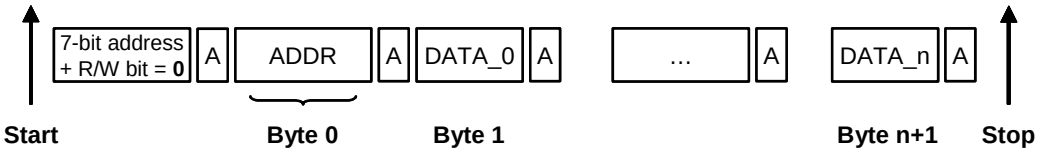

Figure 22. I²C Write Command Sequence in 8-Bit Addressing Mode

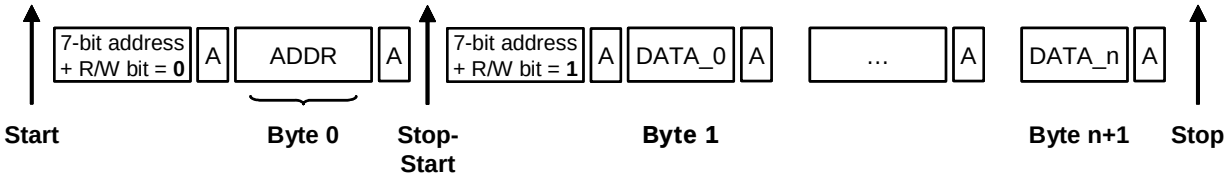

Figure 23. I²C Read Command Sequence in 8-Bit Addressing Mode

Note: A = acknowledge

5.3.3. Address Mode Change

At any time, the I²C master can signal a change in I²C addressing mode during the two bytes immediately following the 7-bit device address and r/w bit. It does not matter whether the part is currently in 8-bit or 16-bit mode, the two bytes are interpreted the same way in either case. The first byte is called "byte 0" and the second, "byte 1":

When "byte 0" equals 0xFF, then the addressing mode will be changed to the value specified by "byte 1".

- If "byte 1" equals 0x00 to 0xFE, then 8-bit mode is chosen, and the page (upper 8 bits of physical address) is set to the value of "byte 1".
- If "byte 1" equals 0xFF, then 16-bit addressing mode is chosen.

Note a change in addressing mode can be accomplished with host software designed for either 8 or 16-bit

addressing mode, since any "extra" bytes that are written will be ignored by the device.

If an 8-bit register address scheme is preferred, the following I^2C commands should be sent immediately after power-up:

Table 10. 16-Bit vs. 8-Bit Address Mode Selection

Host Controller	Si2165	Action Required	Register Address	Value
16-bit mode	16-bit mode	Change Si2165 to 8-bit address mode	(FF00h)	00h
8-bit mode	16-bit mode	Change Si2165 to 8-bit address mode	(FFh)	00h
8-bit mode	8-bit mode	Host controller changing address page	(FFh)	Page (hexa)

After a hardware reset (using RESETB pin), the Si2165 returns to 16-bit register addressing mode.

5.4. I^2C Switch Operation

Si2165 incorporates a logic pass-through switch. Despite not being a physical switch, this logic switch should be considered a standard switch. This switch can be used to pass incoming I^2C transactions from the host controller to the tuner's I^2C bus. An internal state machine is used to control the SDA drive direction such that acknowledge replies from the tuner-side bus are passed back to the host-side bus.

The host software controls the switch open/close position by programming register **i2c_passthru (0001h)**:

Table 11. I^2C Switch Operation

I^2C Command	Register	Value
CONNECT logic switch to communicate with tuner	**i2c_passthru (0001h)**	01h
DISCONNECT logic switch to isolate tuner from I^2C bus		00h

Important Note:

One I^2C STOP condition is required after writing this register in order for the switch status to be updated!

The SDA pad delays output data by 600 ns, for non pass-through traffic only. This ensures that all devices on the bus see an SDA change only when SCL is “low” if Si2165 is driving data or acknowledge.

5.5. I^2C Pull-up Resistors and Bus Voltage Compatibility

Both host and tuner-side I^2C buses do not include any internal pull-up resistors on either clock or data signals. Thus, signals on pins SDA_MAST, SCL_MAST, SCL_HOST, and SDA_HOST must always be pulled-high (to either 1.8, 2.5, 3.3, or 5 V) by weak pull-up resistors on the board. Note that the rise times of both the SCL_HOST and SDA_HOST signals can be as high as 1000 ns in both standard mode and fast mode of I^2C, provided that the other I^2C timing specification are met.

For proper I^2C operation, the various combinations allowed for power supply "V_{DD_VIO}" and I^2C bus pull-up supply called "VPU" are shown in the following table:

Table 12. I/O Voltage vs. Supply Compatibility[1,2]

VPU (V) V_{DD_VIO} (V)	1.80 (±10%)	2.50 (±10%)	3.30 (±10%)	5.00 (±10%)
1.80 (±10%)	✓	✓	x	x
2.50 (±10%)	x	✓	✓	x
3.30 (±10%)	x	x	✓	✓

Notes:
1. ✓ = compatible
2. x = not allowed

6. General Purpose I/O (GPIO)

The Si2165 includes two types of GPIO ports: full-function GPIO and logic level-only GPIO.

A full-function GPIO port, configured as an output, can provide (after R-C filtering of its Δ/Σ output) any analog value from 0 V to V_{DD_VIO} with 256 step increments (actual value being user-defined by an 8-bit register) in addition to operation as a logic-level I/O.

Logic level-only I/O is limited to providing “high” or “low” output levels or providing readback of the logic level present on a pin when used as an input.

6.1. Full-function GPIOs: GPIO_0, GPIO_1, GPIO_2

GPIO_0 is completely independent from any other device function.

GPIO_1 is muxed with TS_DATA[1] onto the same pin. Consequently, this port is only available when the serial TS interface is used.

GPIO_2 is muxed with TS_ERR onto the same pin. Consequently, this port is only available when the TS_ERR signal is not used by the host processor.

The registers listed in Table 13 control operations of these GPIOs:

Table 13. GPIO_0/1/2 Functionality

GPIO	Functionality	Register
GPIO_0	Tri-state GPIO_0 pin.	**gpio0_tri (05C1h)**
GPIO_0 GPIO_1 GPIO_2	Enable/disable GPIO mode.	**gp0_en (05B1h)** **gp1_en (05D1h)** **gp2_en (05F1h)**
	Select GPIO mode: general-purpose (logic) output, interrupt output, Δ/Σ encoded output.	**gp0_sel (05B1h)** **gp1_sel (05D1h)** **gp2_sel (05F1h)**
	Select polarity: inverted vs. non-inverted.	**gp0_p (05B1h)** **gp1_p (05D1h)** **gp2_p (05F1h)**
	Select electrical output type: CMOS vs. open-drain.	**gp0_t (05B1h)** **gp1_t (05D1h)** **gp2_t (05F1h)**
	Set output level, when in logic output mode.	**gp0_o (05B1h)** **gp1_o (05D1h)** **gp2_o (05F1h)**
	Read input level (read only).	**gp0_i (05B4h)** **gp1_i (05D4h)** **gp2_i (05F4h)**
	Set Δ/Σ value (user defined 8-bit value) when in Δ/Σ output mode.	**gp0_deltasigma (05B0h)** **gp1_deltasigma (05D0h)** **gp2_deltasigma (05F0h)**

6.2. Logic-Level GPIOs: GPIO_3, GPIO_4, and GPIO_5

GPIO_3, GPIO_4, and GPIO_5 are muxed with TS_DATA[2], TS_DATA[3], and TS_DATA[4]. Therefore, these ports are only available when the serial TS interface is used.

To enable tri-state mode for these two ports, refer to the MPEG TS section.

The following registers control operations of these three GPIOs:

Table 14. GPIO_3/4/5 Functionality

GPIO	Functionality	Register
GPIO_3 GPIO_4 GPIO_5	Enable/disable GPIO mode	**gp3_en (0610h)** **gp4_en (0621h)** **gp5_en (0632h)**
	Select polarity: inverted vs. non-inverted	**gp3_p (0610h)** **gp4_p (0621h)** **gp5_p (0632h)**
	Select electrical output type: CMOS vs. open-drain	**gp3_t (0610h)** **gp4_t (0621h)** **gp5_t (0632h)**
	Set output level, when in logic output mode	**gp3_o (0610h)** **gp4_o (0621h)** **gp5_o (0632h)**
	Read input level (read only)	**gp3_i (0614h)** **gp4_i (0625h)** **gp5_i (0636h)**

6.3. Selection of the Multiplexed GPIO Ports

For the shared GPIOs, Table 15 specifies the registers that determine the output signals on the respective TS/ GPIO pins.

Table 15. Multiplexed GPIO Port Selection

Pin	Functions Muxed	Register
12	GPIO_1 or TS_DATA[1]	**sel_gpio_ts_data1 (04EBh)**
13	GPIO_3 or TS_DATA[2]	**sel_gpio_ts_data2 (04EBh)**
14	GPIO_4 or TS_DATA[3]	**sel_gpio_ts_data3 (04EBh)**
16	GPIO_5 or TS_DATA[4]	**sel_gpio_ts_data4 (04EBh)**
21	GPIO_2 or TS_ERR	**sel_gpio_ts_err (04EBh)**

6.4. Activation of GPIO Ports

Step 1. Release the tri-state condition of the corresponding GPIO port(s).

Step 2. For GPIO_0, this GPIO port can be enabled directly.
The output signal slew rate is modifiable, with four settings, via register **gpio0_slr (05CAh)**.
For GPIO_1 / _2 / _3 / _4/ _5, first the proper muxing should be selected; then, the corresponding GPIO port can be enabled.

- **Input Capability:**
  If GPIO port <n> is to be used as an input, the pin must be configured according to Table 16.

Table 16. Input Capability

Registers	Settings for Input Capability
gp<n>_t	Set to “Open_drain” type
gp<n>_o	Set to “high” status
gp<n>_sel	Set to “gp_o” mode
gp<n>_p	Set to “non_inverted” polarity

As soon as the above four registers are properly set, the input value becomes available in register **gp<n>_i**.

6.5. Additional General-Purpose Output (GPO)

If the signals are not required by the application, AGC_RF and AGC_IF can also be reconfigured to output a user-defined analog level (after R-C filtering of its Δ/Σ output) from 0 V to V_{DD_VIO} with 256 step increments.

- The AGC_RF output level is controlled by setting both **agc1_min (015Eh)** and **agc1_max (015Fh)** registers to the desired 8-bit value.
- The AGC_IF output level is controlled by setting both **agc2_min (016Eh)** and **agc2_max (016Fh)** registers to the desired 8-bit value.

Note: interrupt outputs and input modes are not supported on these two pins.

6.6. Interrupts

Si2165 is equipped with an interrupt to signal indication of FEC lock. When the FEC is locked, all prior steps in the demodulator chain have been completed successfully; so, FEC lock is an efficient indicator for the overall final lock of the demodulator.

To enable FEC lock output on any of the three full-function GPIO pins, the user should configure GPIO_0, GPIO_1, and/or GPIO_2 as the interrupt output(s) and explicitly enable “FEC_lock” as an interrupt source on the corresponding output using registers **fecl0_e (05B6h)**, **fecl1_e (05D6h)**, and/or **fecl2_e (05F6h)**.

When the corresponding interrupt is enabled, it is also possible to have a readout of the interrupt status using registers **fecl0_i (05BAh)**, **fecl1_i (05DAh)**, and/or **fecl2_i (05FAh)**, depending on the affected GPIO port.

To reset interrupts, use registers **rst_interrupt_gp0 (05BCh)**, **rst_interrupt_gp1 (05DCh)**, and/or **rst_interrupt_gp2 (0600h)**.

7. Typical Application Schematics

7.1. Typical Application with IF or Low-IF Tuner

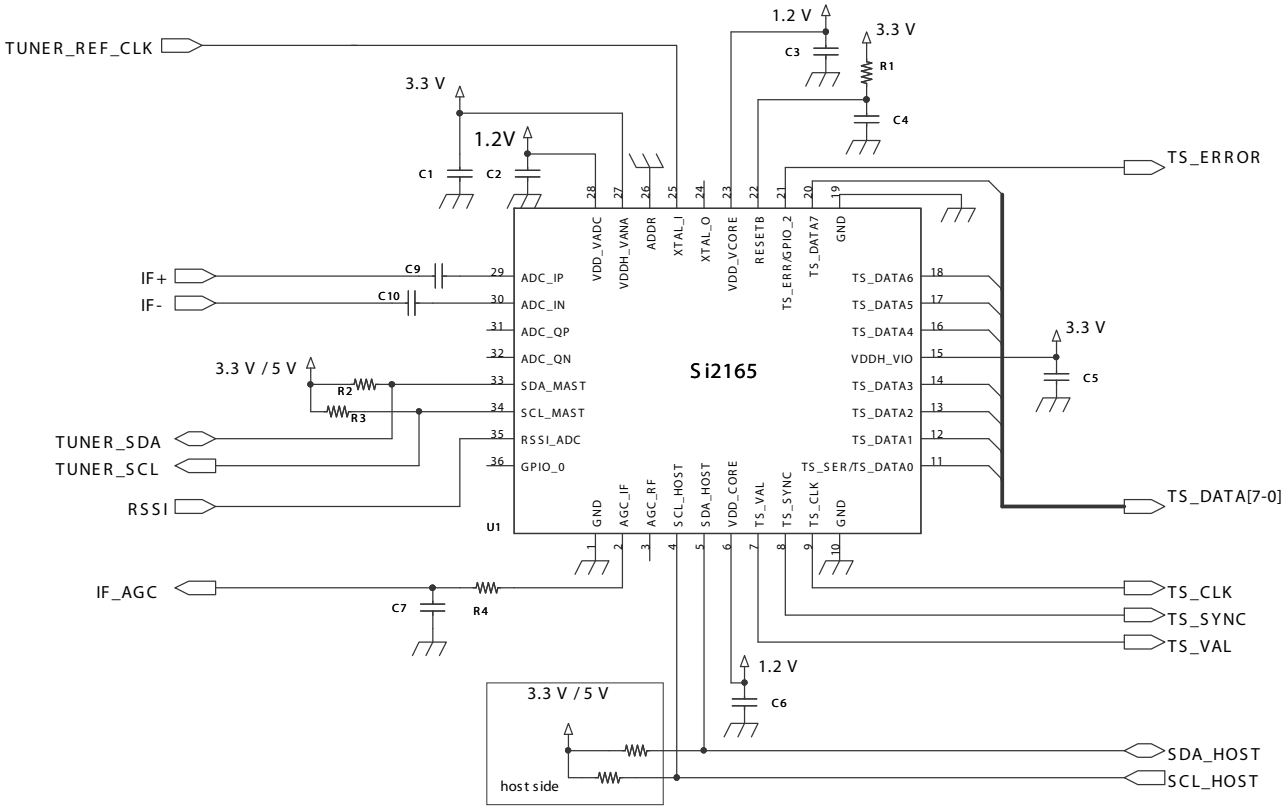

Figure 24. Application Schematic #1 (36 MHz IF/IF AGC), External Clock Reference, and Parallel TS Output

7.2. Typical Application with ZIF Silicon Tuner

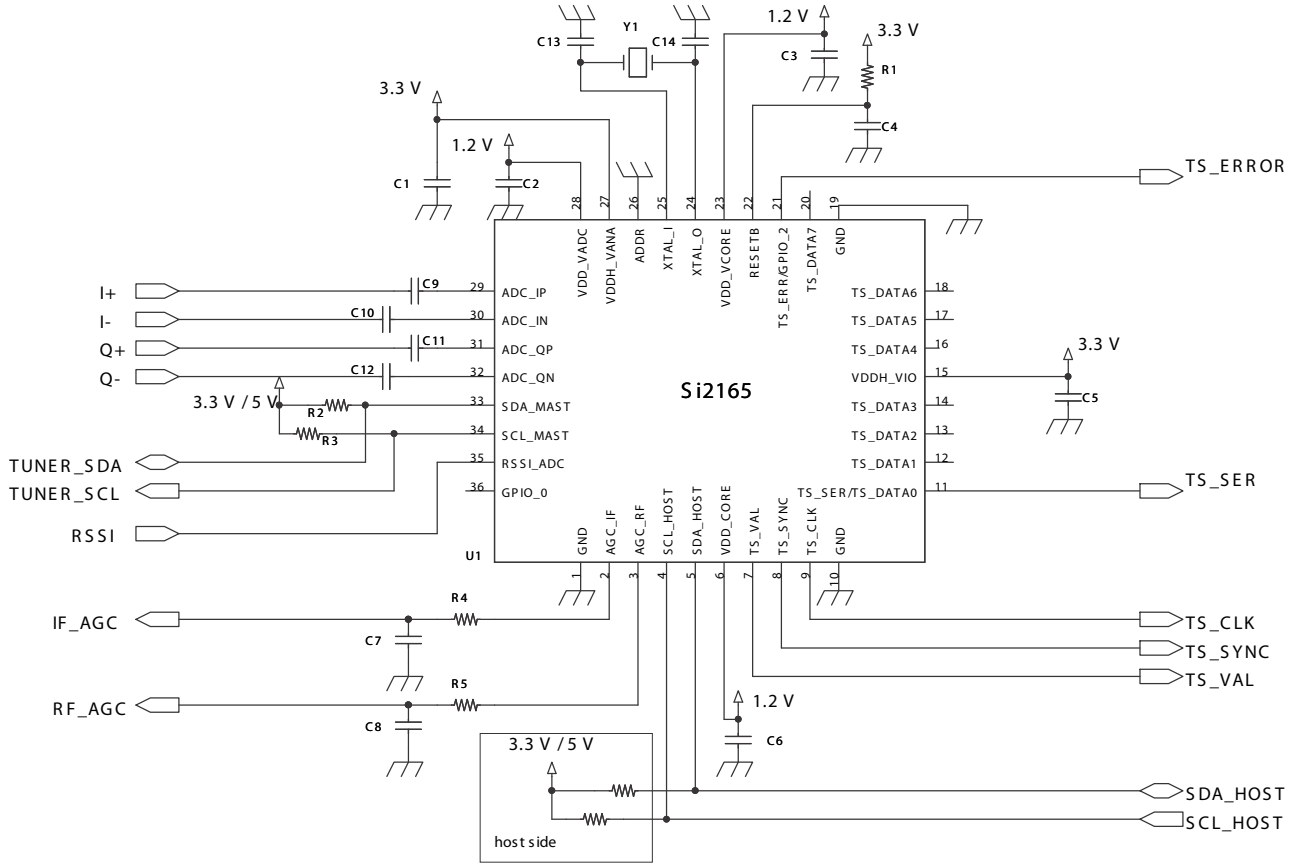

Figure 25. Application Schematic #2 (Zero IF) with Crystal, Dual AGC Loops, and Serial TS Output

7.3. Typical Bill Of Materials

Table 17. Si2165 Bill of Materials

Components	Description	Comment
IC1	Si2165-D-GM	
Y1	Crystal 16, 20, 24, or 27 MHz ±100 ppm (additionally, Cload = 12 pF)	Application #2 only
C1	100 nF, ±20%	
C2	100 nF, ±20%	
C3	100 nF, ±20%	
C4	100 nF, ±20%	
C5	100 nF, ±20%	
C6	100 nF, ±20%	
C7	100 nF, ±20%	
C8	100 nF, ±20%	Application #2 only
C9	100 nF, ±20%	
C10	100 nF, ±20%	
C11	100 nF, ±20%	Application #2 only
C12	100 nF, ±20%	Application #2 only
C13	20 pF, ±10%	Application #2 only
C14	20 pF, ±10%	Application #2 only
R1	47 kΩ, ±20%	
R2	4.7 kΩ, ±20%	
R3	4.7 kΩ, ±20%	
R4	4.7 kΩ, ±20%	
R5	4.7 kΩ, ±20%	Application #2 only

8. Additional Reference Information for Design

Upon request, Silicon Laboratories' application team can provide customers with the following documents:

- EVB Si2165 GUI User Manual (and USB Driver Installation note)
- Schematics of Evaluation Board (four layer PCB)
- Si216x Schematics Guideline
- DVB-T Scan
- RSSI ADC
- BER Settings

9. Programming Guide

9.1. API Example

Several documents related to software support are available upon request from the Silicon Laboratories' application team.

- SW Si2165 Getting Started
- SW Si2165 Layer 1
- SW Si2165 Layer 2
- SW Si2165 Layer 3

10. Register Map Summary

Table 18. Register Map Summary

I2C Addr	D7	D6	D5	D4	D3	D2	D1	D0
I2C Slave Registers (SCL Domain Only)								
0000		chip_mode						
0001								i2c_passthru
I2C Slave Registers								
0013							i2c_addr	
IP Version								
0023	revcode							
Initialization								
0050								chip_init
0054								init_done
0096								start_init
Clocks								
00A0				pll_divl				
00A1				pll_divm				
00A2	pll_enable	pll_divp	pll_divn					
00A3						pll_divr		
Resets								
00C0								rst_all
00C4	lock_timeout (LSB)							
00C5	lock_timeout							
00C6	lock_timeout							
00C7							lock_timeout (MSB)	
00CB								auto_reset
General Parameters								
00E0							adc_sampling_mode	
00E4	oversamp (LSB)							
00E5	oversamp							
00E6	oversamp							
00E7			oversamp (MSB)					
00E8	if_freq_shift (LSB)							
00E9	if_freq_shift							
00EA	if_freq_shift							
00EB				if_freq_shift (MSB)				
00EC			standard					

Table 18. Register Map Summary

I2C Addr	D7	D6	D5	D4	D3	D2	D1	D0
00F8			constellation					
0104								dsp_clock
ADC Interface								
0122								iq_adc_swap
0123	adc_ri8							
0129	adc_ri0							
012A	adc_ri1							
012B	adc_ri2							
012C	adc_ri3							
012D	adc_ri4							
012E	adc_ri5							
012F	adc_ri6							
IQ Mismatch Correction								
0131				dc_freeze	dc_bypass	dc_coeff		
0132	dc_offset_i							
0133	dc_offset_q							
0134								iq_freeze
0135						iq_kagc		
0136	q_gain_ext (LSB)							
0137							q_gain_ext (MSB)	
013C	q_gain (LSB)							
013D							q_gain (MSB)	
0140								phase_freeze
0141						phase_kloop		
0144	phi_cor (LSB)							
0145							phi_cor (MSB)	
Analog AGC								
0150	agc_crestf_dbx8							
0154				agc_alpha_acq				
0155				agc_alpha_loc				
0156	agc_dicho_rate							
0157								agc_acq_mode
0158					agc_coarse2fine_thr			
0159					agc_fine2coarse_thr			
015A					agc_freeze_thr			

Table 18. Register Map Summary

I2C Addr	D7	D6	D5	D4	D3	D2	D1	D0
015B					agc_unfreeze_thr			
015C				agc1_kacq				
015D				agc1_kloc				
015E	agc1_min							
015F	agc1_max							
0160						agc1_buftype	agc1_pola	agc1_freeze
0161						agc1_clkdiv		
0164	agc1_ext							
0168	agc1_cmd							
016C				agc2_kacq				
016D				agc2_kloc				
016E	agc2_min							
016F	agc2_max							
0170						agc2_buftype	agc2_pola	agc2_freeze
0171						agc2_clkdiv		
0174	agc2_ext							
0178	agc2_cmd							
0180	agc_pow_max (LSB)							
0181								agc_pow_max (MSB)
0184								agc_pow_max_init
0188							agc_freeze_int	agc_lock
018B								agc_if_tri
018D								agc_rf_tri
0190							agc_if_slr	
0192							agc_rf_slr	
Digital AGC								
01A0	aaf_crestf_dbx8							
01A4				aaf_alpha_acq				
01A5				aaf_alpha_loc				
01A6					aaf_agc_step			
01A7							aaf_update_sel	aaf_agc_freeze
01A8			aaf_coarse2fine_thr					
01A9			aaf_fine2coarse_thr					

Table 18. Register Map Summary

I2C Addr	D7	D6	D5	D4	D3	D2	D1	D0
01AA	aaf_freeze_thr							
01AB	aaf_unfreeze_thr							
01AC	aaf_agc_ext							
01B0	aaf_agc_cmd							
01B8	aaf_pow_fil (LSB)							
01B9							aaf_pow_fil (MSB)	
01BE	aaf_pow_max (LSB)							
01BF								aaf_pow_max (MSB)
01C0								aaf_pow_max_init
01C4							aaf_freeze_int	aaf_lock
01C8	aci_crestf_dbx8							
01CC				aci_alpha_acq				
01CD				aci_alpha_loc				
01CE					aci_agc_step			
01CF							aci_agc_update_sel	aci_agc_freeze
01D0	aci_coarse2fine_thr							
01D1	aci_fine2coarse_thr							
01D2	aci_freeze_thr							
01D3	aci_unfreeze_thr							
01D4	aci_agc_ext							
01D8	aci_agc_cmd							
01E0	aci_pow_fil (LSB)							
01E1							aci_pow_fil (MSB)	
01E6	aci_pow_max (LSB)							
01E7								aci_pow_max (MSB)
01E8								aci_pow_max_init
01EC							aci_freeze_int	aci_lock
Cable Timing Recovery								
0200				tim_ki_acq				
0201					tim_kp_acq			
0202				tim_ki_loc				
0203					tim_kp_loc			

Table 18. Register Map Summary

I2C Addr	D7	D6	D5	D4	D3	D2	D1	D0
0208	timing_corr_c (LSB)							
0209	timing_corr_c (Middle)							
020A							timing_corr_c (MSB)	
020D							tim_update_period	
0211			range_baud_rate					
0214	coarsetim_corr (LSB)							
0215					coarsetim_corr (MSB)			
0219					timing_unfrz_cond		baud_rate_unfrz_cond	
Cable Carrier Recovery								
0230	sweep_init							
0231		sweep_range						
0232			sweep_step					
0234	freq_corr_c (LSB)							
0235	freq_corr_c (MSB)							
0238					kp_acq			
0239				ki_acq				
023A					kp_lock			
023B				ki_lock				
023E								demod_lock_c
0240	phase_cor_c (LSB)							
0241	phase_cor_c (MSB)							
Cable Equalizer								
0260		ffe_length						
0261	central_tap							
0264	gain_ddffe				gain_cma			
0265					gain_dddfe			
026C	c_n (LSB)							
026D	c_n (Middle)							
026E	c_n (MSB)							
0278							auto_algo	auto_control
DVB-T Equalizer.								
02A4	sigma2_est (LSB)							
02A5	sigma2_est (Middle)							
02A6	sigma2_est (MSB)							
02C0	ref_signal_power (LSB)							
02C1			ref_signal_power (MSB)					

Table 18. Register Map Summary

I2C Addr	D7	D6	D5	D4	D3	D2	D1	D0
DVB-T Synchonisation								
02E0								start_synchro
02E4								req_stream
02E8								automatic_synchro
02EC					req_fft_mode			
02F0						req_guard_int		
02F4			req_constellation					
02F8					req_rate_HP			
0300					req_rate_LP			
0304						req_hierarchy		
0308	bandwidth (LSB)							
0309			bandwidth (MSB)					
030C	freq_sync_range (LSB)							
030D					freq_sync_range (MSB)			
0310								cpe_req
0318	timing_sync_range							
031C								impulsive_noise_remover
0320					check_signal_thres			
0324				relock_on_per_thres				
0328				stay_lock_ber_thres				
0334					freq_bw_acq			
0336					freq_bw_track			
0338					timing_bw_acq			
033A					timing_bw_track			
Firmware								
0341						wdog_error	rst_wdog_error	boot_done
0344	patch_version							
0348	addr_jump (LSB)							
0349	addr_jump							
034A	addr_jump							
034B	addr_jump (MSB)							
035C							errorn	en_rst_error
0364	dcom_control_byte (LSB)							
0365	dcom_control_byte							

Table 18. Register Map Summary

I2C Addr	D7	D6	D5	D4	D3	D2	D1	D0
0366	dcom_control_byte							
0367	dcom_control_byte (MSB)							
0368	dcom_addr (LSB)							
0369	dcom_addr							
036A	dcom_addr							
036B	dcom_addr (MSB)							
036C	dcom_data (LSB)							
036D	dcom_data							
036E	dcom_data							
036F	dcom_data (MSB)							
0379								rst_crc
037A	crc (LSB)							
037B	crc (MSB)							
0384	gp_reg0 (LSB)							
0385	gp_reg0							
0386	gp_reg0							
0387	gp_reg0 (MSB)							
0388	gp_reg1 (LSB)							
0389	gp_reg1							
038A	gp_reg1							
038B	gp_reg1 (MSB)							
038C	gp_reg2 (LSB)							
038D	gp_reg2							
038E	gp_reg2							
038F	gp_reg2 (MSB)							
DVB-T Lock Status								
0390								demod_lock_t
0394								tps_lock
0398								freq_lock_t
039C								timing_lock_t
03A0								fft_lock_t
03A4	channel_length (LSB)							
03A5				channel_length (MSB)				
03A8							check_signal	
03B0	timing_corr_t (LSB)							
03B1	timing_corr_t (Middle)							

Table 18. Register Map Summary

I2C Addr	D7	D6	D5	D4	D3	D2	D1	D0
03B2					timing_corr_t (MSB)			
03B4	freq_corr_t (LSB)							
03B5	freq_corr_t							
03B6	freq_corr_t							
03B7							freq_corr_t (MSB)	
TPS								
03F0					auto_fft_mode			
03F4						auto_guard_int		
03F8			auto_constellation					
0400					auto_rate_HP			
0404					auto_rate_LP			
0408						auto_hierarchy		
040C	cell_id (LSB)							
040D	cell_id (MSB)							
0410					tps_reserved1			
0411					tps_reserved2			
0412					tps_reserved3			
0413					tps_reserved4			
0414								lp_time_slicing
0415								lp_mpe_fec
0416								hp_time_slicing
0417								hp_mpe_fec
0418			tps_length					
041C								dvbh_interleaver
Viterbi Decoder								
0420								stream
0424								cber_rst
0428	cber_bit (LSB)							
0429	cber_bit (Middle)							
042A	cber_bit (MSB)							
0430	cber_err (LSB)							
0431	cber_err (Middle)							
0432	cber_err (MSB)							
0434								cber_avail
Packet Synchronization								
0440								ps_lock

Table 18. Register Map Summary

I2C Addr	D7	D6	D5	D4	D3	D2	D1	D0
0444								ps_ambig_out
0448								ps_stay_locked
044D					ps_sync_thr			
044E	ps_superv_thr							
044F	ps_ambig_thr							
0450							ps_ambig_reg	ps_ambig_mode
Reed Solomon Decoder								
0461								rs_bypass
0464								uncor_rst
0468	uncor_cnt							
046C								ber_rst
0470	ber_pkt (LSB)							
0471	ber_pkt (MSB)							
0478	ber_bit (LSB)							
0479	ber_bit (Middle)							
047A	ber_bit (MSB)							
047C								ber_avail
0480								per_rst
0484	per_pkt (LSB)							
0485	per_pkt (MSB)							
048C	per (LSB)							
048D	per (MSB)							
0490								per_avail
Inner And Outer Deinterleaver								
04C0								symb_deint_mode
Descrambler								
04D0								desc_enable
MPEG Transport Stream Interface								
04E0								fec_lock
04E4			ts_before_lock	ts_tei	ts_data_sync_overwr	ts_data_parity	ts_data_dir	ts_data_mode
04E5						ts_clk_duty_cycle	ts_clk_mode	ts_clk_edge
04E6					ts_err_pola	ts_val_pola	ts_sync_pola	ts_sync_length
04E9						ts_mux		

Table 18. Register Map Summary

I2C Addr	D7	D6	D5	D4	D3	D2	D1	D0
04EB				sel_gpio_ts_data4	sel_gpio_ts_data3	sel_gpio_ts_data2	sel_gpio_ts_data1	sel_gpio_ts_err
04EF	ts_data7_tri	ts_data6_tri	ts_data5_tri	ts_data4_tri	ts_data3_tri	ts_data2_tri	ts_data1_tri	ts_data0_tri
04F0					ts_clk_tri	ts_err_tri	ts_sync_tri	ts_val_tri
04F4	ts_data3_slr		ts_data2_slr		ts_data1_slr		ts_data0_slr	
04F5	ts_data7_slr		ts_data6_slr		ts_data5_slr		ts_data4_slr	
04F6	ts_clk_slr		ts_err_slr		ts_sync_slr		ts_val_slr	
Bridge From MPEG-TS To GPIF Interface								
0500						gpif_standby	gpif_ram_overflow	gpif_in_fifo_overflow
0504								gpif_alarm_reset
PID Filter								
0510							pid_p	pid_filter_en
0514	pid_en_7	pid_en_6	pid_en_5	pid_en_4	pid_en_3	pid_en_2	pid_en_1	pid_en_0
0515	pid_en_15	pid_en_14	pid_en_13	pid_en_12	pid_en_11	pid_en_10	pid_en_9	pid_en_8
0516	pid_en_23	pid_en_22	pid_en_21	pid_en_20	pid_en_19	pid_en_18	pid_en_17	pid_en_16
0517	pid_en_31	pid_en_30	pid_en_29	pid_en_28	pid_en_27	pid_en_26	pid_en_25	pid_en_24
0518	pid_0 (LSB)							
0519				pid_0 (MSB)				
051C	pid_1 (LSB)							
051D				pid_1 (MSB)				
0520	pid_2 (LSB)							
0521				pid_2 (MSB)				
0524	pid_3 (LSB)							
0525				pid_3 (MSB)				
0528	pid_4 (LSB)							
0529				pid_4 (MSB)				
052C	pid_5 (LSB)							
052D				pid_5 (MSB)				
0530	pid_6 (LSB)							
0531				pid_6 (MSB)				
0534	pid_7 (LSB)							
0535				pid_7 (MSB)				
0538	pid_8 (LSB)							

Table 18. Register Map Summary

I2C Addr	D7	D6	D5	D4	D3	D2	D1	D0
0539				pid_8 (MSB)				
053C	pid_9 (LSB)							
053D				pid_9 (MSB)				
0540	pid_10 (LSB)							
0541				pid_10 (MSB)				
0544	pid_11 (LSB)							
0545				pid_11 (MSB)				
0548	pid_12 (LSB)							
0549				pid_12 (MSB)				
054C	pid_13 (LSB)							
054D				pid_13 (MSB)				
0550	pid_14 (LSB)							
0551				pid_14 (MSB)				
0554	pid_15 (LSB)							
0555				pid_15 (MSB)				
0558	pid_16 (LSB)							
0559				pid_16 (MSB)				
055C	pid_17 (LSB)							
055D				pid_17 (MSB)				
0560	pid_18 (LSB)							
0561				pid_18 (MSB)				
0564	pid_19 (LSB)							
0565				pid_19 (MSB)				
0568	pid_20 (LSB)							
0569				pid_20 (MSB)				
056C	pid_21 (LSB)							
056D				pid_21 (MSB)				
0570	pid_22 (LSB)							
0571				pid_22 (MSB)				
0574	pid_23 (LSB)							
0575				pid_23 (MSB)				
0578	pid_24 (LSB)							
0579				pid_24 (MSB)				
057C	pid_25 (LSB)							
057D				pid_25 (MSB)				
0580	pid_26 (LSB)							

Table 18. Register Map Summary

I2C Addr	D7	D6	D5	D4	D3	D2	D1	D0
0581				pid_26 (MSB)				
0584	pid_27 (LSB)							
0585				pid_27 (MSB)				
0588	pid_28 (LSB)							
0589				pid_28 (MSB)				
058C	pid_29 (LSB)							
058D				pid_29 (MSB)				
0590	pid_30 (LSB)							
0591				pid_30 (MSB)				
0594	pid_31 (LSB)							
0595				pid_31 (MSB)				
General Purpose I/O GPIO_0								
05B0	gp0_deltasigma							
05B1			gp0_o	gp0_en	gp0_t	gp0_p	gp0_sel	
05B4								gp0_i
05B6								fecl0_e
05BA								fecl0_i
05BC								rst_interrupt_gp0
05C1								gpio0_tri
05CA							gpio0_slr	
General Purpose I/O GPIO_1								
05D0	gp1_deltasigma							
05D1			gp1_o	gp1_en	gp1_t	gp1_p	gp1_sel	
05D4								gp1_i
05D6								fecl1_e
05DA								fecl1_i
05DC								rst_interrupt_gp1
General Purpose I/O GPIO_2								
05F0	gp2_deltasigma							
05F1			gp2_o	gp2_en	gp2_t	gp2_p	gp2_sel	
05F4								gp2_i
05F6								fecl2_e
05FA								fecl2_i
0600								rst_interrupt_gp2

Table 18. Register Map Summary

I2C Addr	D7	D6	D5	D4	D3	D2	D1	D0
General Purpose I/O GPIO_3								
0610					gp3_o	gp3_en	gp3_t	gp3_p
0614								gp3_i
General Purpose I/O GPIO_4								
0621					gp4_o	gp4_en	gp4_t	gp4_p
0625								gp4_i
General Purpose I/O GPIO_5								
0632					gp5_o	gp5_en	gp5_t	gp5_p
0636								gp5_i
RSSI (Received Signal Strength Indication)								
0641		rssi_update_time					start_rssi	en_rssi
0642	rssi							
0646							rssi_pad_ctrl	
08F8						ts_parallel_mode		

11. Register Descriptions

Register 0000h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		chip_mode						
Type	R/W							

Bit	Name	Function
6:0	chip_mode[6:0]	**Chip Mode Selection.** 00h = off (default) 20h = pll_ext 21h = pll_xtal 22h = pll_rssi Other = Reserved Selects chip clocking mode.

Register 0001h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								i2c_passthru
Type	R/W							

Bit	Name	Function
0	i2c_passthru	**I^2C Pass-through Selection.** 0 = disabled (default) 1 = enabled Enables digital pass-through between I^2C slave and master buses. Note that a STOP condition is required after writing this register so that the pass-through is effectively enabled.

Register 0013h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							i2c_addr	
Type	R							

Bit	Name	Function
1:0	i2c_addr[1:0]	**I^2C Address LSB.** Unsigned Value. I^2C ADDR configuration

Register 0023h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	revcode							
Type	R							

Bit	Name	Function
7:0	revcode[7:0]	**Hardware Revision Code.** 00h = rev_A 01h = rev_B 02h = rev_C 03h = rev_D (default)

Register 0050h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								chip_init
Type								R/W

Bit	Name	Function
0	chip_init	**Chip Initialization.** 0 = func (default) 1 = init Once this register is set to ‘init‘, the initialization sequence is automatically launched. The register init_done indicates when the initialization is completed.

Register 0054h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								init_done
Type								R

Bit	Name	Function
0	init_done	**Initialization Status.** 0 = pending (default) 1 = completed This register is set when device initialization is completed.

Register 0096h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								start_init
Type								R/W

Bit	Name	Function
0	start_init	**Start Initialization.** 0 = reset (default) 1 = run Once chip_init has been set to 1 start_init must be set to 1 to start initialization procedure.

Register 00A0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				pll_divl				
Type				R/W				

Bit	Name	Function
4:0	pll_divl[4:0]	**PLL L-divider.** Unsigned Value. Default Value: 07h

Register 00A1h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				pll_divm				
Type				R/W				

Bit	Name	Function
4:0	pll_divm[4:0]	**PLL M-divider.** Unsigned Value. Default Value: 05h

Register 00A2h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	pll_enable	pll_divp	pll_divn					
Type	R/W	R/W	R/W					

Bit	Name	Function
5:0	pll_divn[5:0]	**PLL N-divider.** Unsigned Value. Default Value: 87h
6	pll_divp	**PLL P-divider.** 0 = prescaler_4 (default) 1 = prescaler_1
7	pll_enable	**PLL Enable.** 0 = disable (default) 1 = enable pll_enable has to be set to enable for normal operation

Register 00A3h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						pll_divr		
Type	R/W							

Bit	Name	Function
2:0	pll_divr[2:0]	**PLL R-divider.** Unsigned Value. Default Value: 001

Register 00C0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								rst_all
Type	R/W							

Bit	Name	Function
0	rst_all	**Software Reset.** Auto Return register 0 = reset 1 = run (default) Resets all the logic except internal registers. For DVB-T mode, after rst_all, a start_synchro is required.

Register 00C4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	00C4h lock_timeout (LSB)							
Type	R/W							
Name	00C5h lock_timeout							
Type	R/W							
Name	00C6h lock_timeout							
Type	R/W							
Name							00C7h lock_timeout (MSB)	
Type							R/W	

Bit	Name	Function
25:0	lock_timeout[25:0]	**Lock Timeout For Auto Reset Feature.** Unsigned Value. Default Value: 0000000h Timeout value is equal to: lock_timeout x xtal_period x 2

Register 00CBh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								auto_reset
Type								R/W

Bit	Name	Function
0	auto_reset	**Auto Reset Enable.** 0 = off (default) 1 = on When auto_reset is ‘on‘, the chip resets itself after a timeout period. The timeout counter starts after a rst_all command or after the demodulator unlocks.

Register 00E0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							adc_sampling_mode	
Type	R/W							

Bit	Name	Function
1:0	adc_sampling_mode[1:0]	**ADC Sampling Scheme.** 00 = if_ovr4 (default) 01 = if_ovr2 10 = zif_ovr4 11 = zif_ovr2 if_yy modes must be used for IF input signal (real) whereas zif_yy modes must be used for baseband I & Q input signal. xx_ovr4 modes must be used when the sampling frequency is higher than 4 times DVB_rate, else xx_ovr2 modes must be used. DVB_rate is the symbol rate in DVB-C and the DVB-T frequency (9.142857 MHz in 8 MHz bandwidth) in DVB-T.

Register 00E4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	00E4h oversamp (LSB)							
Type	R/W							
Name	00E5h oversamp							
Type	R/W							
Name	00E6h oversamp							
Type	R/W							
Name			00E7h oversamp (MSB)					
Type	R/W							

Bit	Name	Function
29:0	oversamp[29:0]	**Over-sampling Rate Parameter.** Unsigned Value. Default Value: 02800000h OVERSAMP = 2^{23} x FE_clk / DVB_rate

Register 00E8h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	00E8h if_freq_shift (LSB)							
Type	R/W							
Name	00E9h if_freq_shift							
Type	R/W							
Name	00EAh if_freq_shift							
Type	R/W							

Register 00E8h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				00EBh if_freq_shift (MSB)				
Type	R/W							

Bit	Name	Function
28:0	if_freq_shift[28:0]	**Frequency Shift Applied To Input Signal.** Signed Value. Default Value: 00000000h Value of frequency shift applied to input signal. IF_FREQ_SHIFT = IF_shift (Hz) x 2^{29} / FE_clk (Hz)

Register 00ECh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			standard					
Type	R/W							

Bit	Name	Function
5:0	standard[5:0]	**DVB Standard.** 01h = DVB_T (default) 05h = DVB_C Other = Reserved

Register 00F8h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			constellation					
Type	R							

Bit	Name	Function
5:0	constellation[5:0]	**Constellation.** 03h = QPSK 07h = QAM16 08h = QAM32 09h = QAM64 (default) 0Ah = QAM128 0Bh = QAM256 Indicates the constellation received according to the enumerated values.

Register 0104h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								dsp_clock
Type								R/W

Bit	Name	Function
0	dsp_clock	**DSP Clock Enable.** 0 = disable 1 = enable (default) Enable or disable the DSP clock to save power in DVB-C mode.

Register 0122h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								iq_adc_swap
Type								R/W

Bit	Name	Function
0	iq_adc_swap	**I/Q Input Channels Swap.** 0 = not_swapped (default) 1 = swapped Allows swapping I & Q inputs.

Register 0123h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	adc_ri8							
Type	R/W							

Bit	Name	Function
7:0	adc_ri8[7:0]	**ADC Control Register 8.** Unsigned Value. Default Value: 00h Must be set to 70h.

Register 0129h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	adc_ri0							
Type	R/W							

Bit	Name	Function
7:0	adc_ri0[7:0]	**ADC Control Register 0.** Unsigned Value. Default Value: 00h

Register 012Ah.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	adc_ri1							
Type	R/W							

Bit	Name	Function
7:0	adc_ri1[7:0]	**ADC Control Register 1.** Unsigned Value. Default Value: 00h Must be set to 46h.

Register 012Bh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	adc_ri2							
Type	R/W							

Bit	Name	Function
7:0	adc_ri2[7:0]	**ADC Control Register 2.** Unsigned Value. Default Value: 00h

Register 012Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	adc_ri3							
Type	R/W							

Bit	Name	Function
7:0	adc_ri3[7:0]	**ADC Control Register 3.** Unsigned Value. Default Value: 00h

Register 012Dh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	adc_ri4							
Type	R/W							

Bit	Name	Function
7:0	adc_ri4[7:0]	**ADC Control Register 4.** Unsigned Value. Default Value: 00h

Register 012Eh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	adc_ri5							
Type	R/W							

Bit	Name	Function
7:0	adc_ri5[7:0]	**ADC Control Register 5.** Unsigned Value. Default Value: 00h Must be set to 0Ah.

Register 012Fh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	adc_ri6							
Type	R/W							

Bit	Name	Function
7:0	adc_ri6[7:0]	**ADC Control Register 6.** Unsigned Value. Default Value: 00h Must be set to FFh.

Register 0131h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				dc_freeze	dc_bypass	dc_coeff		
Type				R/W	R/W	R/W		

Bit	Name	Function
2:0	dc_coeff[2:0]	**DC Offset Compensation Loop Coefficient.** Unsigned Value. Default Value: 010 Loop coefficient for dc offset compensation loop.
3	dc_bypass	**DC Offset Compensation Bypass.** 0 = not_bypassed (default) 1 = bypassed
4	dc_freeze	**DC Offset Compensation Freeze.** 0 = unfrozen (default) 1 = frozen When frozen, dc offset is corrected with current offset estimation, but the compensation loop is frozen.

Register 0132h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	dc_offset_i							
Type	R							

Bit	Name	Function
7:0	dc_offset_i[7:0]	**DC Offset On I Channel.** Signed Value. Input dc offset on real branch (I) is equal to dc_offset_i/8 LSB.

Register 0133h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	dc_offset_q							
Type	R							

Bit	Name	Function
7:0	dc_offset_q[7:0]	**DC Offset On Q Channel.** Signed Value. Input dc offset on imaginary branch (Q) is equal to dc_offset_q/8 LSB.

Register 0134h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								iq_freeze
Type								R/W

Bit	Name	Function
0	iq_freeze	**I/Q Gain Mismatch Correction Freeze Control.** 0 = unfrozen 1 = frozen (default) Allows freezing the gain correction loop to the current value: Q gain is corrected but the loop is not updated anymore.

Register 0135h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						iq_kagc		
Type						R/W		

Bit	Name	Function
2:0	iq_kagc[2:0]	**Gain Mismatch Correction Loop Coefficient.** Unsigned Value. Default Value: 010 Loop coefficient for amplitude mismatch compensation loop.

Register 0136h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0136h q_gain_ext (LSB)							
Type	R/W							
Name							0137h q_gain_ext (MSB)	
Type							R/W	

Bit	Name	Function
9:0	q_gain_ext[9:0]	**Forced Gain Correction On Q Channel.** Unsigned Value. Default Value: 200h Each time q_gain_ext is written, corresponding gain value is loaded and applied on Q branch. If the loop has been frozen with iq_freeze register then this gain value is always applied. This value is also applied after reset. Gain (linear) = q_gain_ext / 512

Register 013Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	013Ch q_gain (LSB)							
Type	R							
Name							013Dh q_gain (MSB)	
Type							R	

Bit	Name	Function
9:0	q_gain[9:0]	**Current Gain Correction Applied To Q Channel.** Unsigned Value. Gain (linear) = q_gain / 512

Register 0140h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								phase_freeze
Type								R/W

Bit	Name	Function
0	phase_freeze	**I/Q Phase Mismatch Correction Loop Freeze Control.** 0 = unfrozen 1 = frozen (default) Allows freezing the phase mismatch correction loop to the current value: phase mismatch is corrected but the loop is not updated anymore.

Register 0141h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						phase_kloop		
Type	R/W							

Bit	Name	Function
2:0	phase_kloop[2:0]	**I/Q Phase Mismatch Correction Loop Coefficient.** Unsigned Value. Default Value: 010 Loop coefficient for phase mismatch compensation loop.

Register 0144h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0144h phi_cor (LSB)							
Type	R							
Name							0145h phi_cor (MSB)	
Type	R							

Bit	Name	Function
9:0	phi_cor[9:0]	**Current Phase Mismatch Correction Value.** Signed Value. phase (rad) = phi_cor x π / 2^{12}

Register 0150h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	agc_crestf_dbx8							
Type	R/W							

Bit	Name	Function
7:0	agc_crestf_dbx8[7:0]	**AGC Reference.** Unsigned Value. Default Value: 78h Crest factor reference for AGC: crest_factor (in dB) = AGC_CRESTF_DBX8 / 8 The AGC loop will adjust RF_AGC and IF_AGC outputs such that input signal average power is crest_factor dB below ADC full scale. To avoid saturation crest_factor must be greater than the signal crest factor, defined as the ratio between its maximum peak power and its average power.

Register 0154h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				agc_alpha_acq				
Type	R/W							

Bit	Name	Function
4:0	agc_alpha_acq[4:0]	**Alpha_acq Coefficient Of AGC Loop.** Unsigned Value. Default Value: 0Dh alpha coefficient of IIR used to filter AGC error, during the acquisition phase (alpha = $2^{(-AGC\_ALPHA\_ACQ)}$). It has to be chosen so that convergence time of IIR is in the same order of magnitude as the selected external RC filter.

Register 0155h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				agc_alpha_loc				
Type	R/W							

Bit	Name	Function
4:0	agc_alpha_loc[4:0]	**Alpha_loc Coefficient For AGC Loop.** Unsigned Value. Default Value: 12h alpha coefficient of IIR used to filter AGC error, during the tracking phase(alpha = $2^{(-AGC\_ALPHA\_LOC)}$) It has to be chosen in order to sufficiently filter input signal maximum amplitude variation, so that AGC loop stays frozen in normal operating conditions.

Register 0156h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	agc_dicho_rate							
Type	R/W							

Bit	Name	Function
7:0	agc_dicho_rate[7:0]	**Dichotomy Rate For AGC Loop.** Unsigned Value. Default Value: 3Ah Update rate of the dichotomy algorithm (only used in dicho_mode). When the dichotomy is selected the AGC command is first set to 128 (middle of the range) and the resulting input signal power is tested. If it is too high then the AGC command is set to 64, if it is too low the AGC command is set to 192 and the signal power is tested again to determine the next value to be tried. This procedure is reiterated until the signal power is as expected. AGC_DICHO_RATE allows programming the time between two trials, which depends on the time constant of external RC filters and must be greater than the settling time of the AGC command. AGC_DICHO_RATE = time (s) x adc_clk (Hz) / 1024.

Register 0157h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								agc_acq_mode
Type								R/W

Bit	Name	Function
0	agc_acq_mode	**AGC Loop Acquisition Mode.** 0 = loop_mode (default) 1 = dicho_mode For AGC acquisition, 2 modes are possible: a standard first order loop mode and a dichotomy search algorithm.

Register 0158h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					agc_coarse2fine_thr			
Type	R/W							

Bit	Name	Function
3:0	agc_coarse2fine_thr[3:0]	**Coarse To Fine AGC Threshold.** Unsigned Value. Default Value: 0011 AGC loop switches from coarse AGC to fine AGC when filtered AGC error becomes less than AGC_COARSE2FINE_THR.

Register 0159h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					agc_fine2coarse_thr			
Type	R/W							

Bit	Name	Function
3:0	agc_fine2coarse_thr[3:0]	**Fine To Coarse AGC Threshold.** Unsigned Value. Default Value: 1000 AGC loop switches from fine AGC to coarse AGC when filtered AGC error becomes higher than AGC_FINE2COARSE_THR.

Register 015Ah.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					agc_freeze_thr			
Type	R/W							

Bit	Name	Function
3:0	agc_freeze_thr[3:0]	**AGC Freeze Threshold.** Unsigned Value. Default Value: 0001 AGC loop is frozen when filtered AGC error becomes less than AGC_FREEZE_THR.

Register 015Bh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					agc_unfreeze_thr			
Type	R/W							

Bit	Name	Function
3:0	agc_unfreeze_thr[3:0]	**AGC Unfreeze Threshold.** Unsigned Value. Default Value: 0010 AGC loop is unfrozen when filtered AGC error becomes higher than AGC_UNFREEZE_THR.

Register 015Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				agc1_kacq				
Type	R/W							

Bit	Name	Function
4:0	agc1_kacq[4:0]	**AGC1 Loop Bandwidth Coefficient During Acquisition.** Unsigned Value. Default Value: 0Ch

Register 015Dh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				agc1_kloc				
Type	R/W							

Bit	Name	Function
4:0	agc1_kloc[4:0]	**AGC1 Loop Coefficient During Tracking.** Unsigned Value. Default Value: 0Eh

Register 015Eh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	agc1_min							
Type	R/W							

Bit	Name	Function
7:0	agc1_min[7:0]	**Lower Bound Of AGC1 Command.** Unsigned Value. Default Value: 00h

Register 015Fh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	agc1_max							
Type	R/W							

Bit	Name	Function
7:0	agc1_max[7:0]	**Upper Bound Of AGC1 Command.** Unsigned Value. Default Value: FFh

Register 0160h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						agc1_buftype	agc1_pola	agc1_freeze
Type						R/W	R/W	R/W

Bit	Name	Function
0	agc1_freeze	**AGC1 Loop Freeze Control.** 0 = unfrozen (default) 1 = frozen First AGC loop is forced in frozen mode when AGC1_FREEZE = 1, else it is in normal mode.
1	agc1_pola	**Polarity Of AGC1 Output.** 0 = non_inverted (default) 1 = inverted
2	agc1_buftype	**AGC1 Output Type.** 0 = push_pull (default) 1 = open_drain It can be either a push-pull output or an open-drain output.

Register 0161h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						agc1_clkdiv		
Type	R/W							

Bit	Name	Function
2:0	agc1_clkdiv[2:0]	**Frequency Of AGC1 Output.** Unsigned Value. Default Value: 000 Sets the division factor between the sampling clock and AGC1 delta/sigma output frequency: division factor = AGC1_CLKDIV + 1.

Register 0164h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	agc1_ext							
Type	R/W							

Bit	Name	Function
7:0	agc1_ext[7:0]	**External Value For AGC1 Command.** Unsigned Value. Default Value: 01h Each time agc1_ext is written, corresponding value is loaded on agc1_cmd. If the loop has been frozen with agc1_freeze register then this value is maintained on AGC1 command.

Register 0168h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	agc1_cmd							
Type	R							

Bit	Name	Function
7:0	agc1_cmd[7:0]	**AGC1 Command Current Value.** Unsigned Value.

Register 016Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				agc2_kacq				
Type	R/W							

Bit	Name	Function
4:0	agc2_kacq[4:0]	**AGC2 Loop Bandwidth Coefficient During Acquisition.** Unsigned Value. Default Value: 0Ch

Register 016Dh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				agc2_kloc				
Type	R/W							

Bit	Name	Function
4:0	agc2_kloc[4:0]	**AGC2 Loop Bandwidth Coefficient During Tracking.** Unsigned Value. Default Value: 0Fh

Register 016Eh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	agc2_min							
Type	R/W							

Bit	Name	Function
7:0	agc2_min[7:0]	**Lower Bound Of AGC2 Command.** Unsigned Value. Default Value: 01h

Register 016Fh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	agc2_max							
Type	R/W							

Bit	Name	Function
7:0	agc2_max[7:0]	**Upper Bound Of AGC2 Command.** Unsigned Value. Default Value: FFh

Register 0170h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						agc2_buftype	agc2_pola	agc2_freeze
Type						R/W	R/W	R/W

Bit	Name	Function
0	agc2_freeze	**AGC2 Loop Freeze Control.** 0 = unfrozen (default) 1 = frozen Second AGC loop is forced in frozen mode when AGC2_FREEZE = 1, else it is in normal mode.
1	agc2_pola	**Polarity Of AGC2 Output.** 0 = non_inverted (default) 1 = inverted
2	agc2_buftype	**AGC2 Output Type.** 0 = push_pull (default) 1 = open_drain It can be either a push-pull output or an open-drain output.

Register 0171h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						agc2_clkdiv		
Type						R/W		

Bit	Name	Function
2:0	agc2_clkdiv[2:0]	**Frequency Of AGC2 Output.** Unsigned Value. Default Value: 000 Sets the division factor between the sampling clock and AGC2 delta/sigma output frequency: division factor = AGC2_CLKDIV + 1

Register 0174h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	agc2_ext							
Type	R/W							

Bit	Name	Function
7:0	agc2_ext[7:0]	**External Value For AGC1 Command.** Unsigned Value. Default Value: 01h Each time agc2_ext is written, corresponding value is loaded on agc2_cmd. If the loop has been frozen with agc2_freeze register then this value is maintained on AGC2 command.

Register 0178h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	agc2_cmd							
Type	R							

Bit	Name	Function
7:0	agc2_cmd[7:0]	**AGC2 Command Current Value.** Unsigned Value.

Register 0180h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0180h agc_pow_max (LSB)							
Type	R							
Name								0181h agc_pow_max (MSB)
Type	R							

Bit	Name	Function
8:0	agc_pow_max[8:0]	**Peak Power Of Input Signal.** Unsigned Value. AGC maximum (peak) input power indicator. saturation margin (in dB, relative to full scale) = 10 x log(AGC_POW_MAX / 510)

Register 0184h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								agc_pow_max_init
Type	R/W							

Bit	Name	Function
0	agc_pow_max_init	**Peak Power Indicator Reset.** Unsigned Value. Default Value: 0. (Auto Return register) Each time AGC_POW_MAX_INIT is set high, maximum power detector AGC_POW_MAX is reinitialized to 0.

Register 0188h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							agc_freeze_int	agc_lock
Type							R	R

Bit	Name	Function
0	agc_lock	**AGC Loop Lock Indicator.** 0 = unlocked (default) 1 = locked “locked“ means in tracking or frozen mode.
1	agc_freeze_int	**AGC Freeze Indicator.** 0 = unfrozen (default) 1 = frozen Indicates whether AGC loop is frozen or not. The loop is frozen when AGC error becomes lower than AGC_FREEZE_THR and unfrozen when AGC error becomes higher than AGC_UNFREEZE_THR.

Register 018Bh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								agc_if_tri
Type								R/W

Bit	Name	Function
0	agc_if_tri	**Tristate Control Of AGC_IF Pin.** 0 = normal 1 = tristate (default)

Register 018Dh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								agc_rf_tri
Type								R/W

Bit	Name	Function
0	agc_rf_tri	**Tristate Control Of AGC_RF Pin.** 0 = normal 1 = tristate (default)

Register 0190h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							agc_if_slr	
Type	R/W							

Bit	Name	Function
1:0	agc_if_slr[1:0]	**Slew Rate Control Of AGC_IF Pin.** 00 = fastest_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges

Register 0192h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							agc_rf_slr	
Type	R/W							

Bit	Name	Function
1:0	agc_rf_slr[1:0]	**Slew Rate Control Of AGC_RF Pin.** 00 = fastest_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges

Register 01A0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	aaf_crestf_dbx8							
Type	R/W							

Bit	Name	Function
7:0	aaf_crestf_dbx8[7:0]	**AAF Filter Digital AGC Reference.** Unsigned Value. Default Value: 78h Crest factor reference for anti-alias filter digital AGC: AAF_CRESTF_DBX8 = 8 x CrestFactor (in dB) Sets the ratio between the wanted average signal power and full scale at anti-alias filter output. This reference must be higher than the maximum possible crest factor of the signal, to avoid saturation.

Register 01A4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				aaf_alpha_acq				
Type	R/W							

Bit	Name	Function
4:0	aaf_alpha_acq[4:0]	**Alpha_acq Coefficient Of AAF Digital AGC.** Unsigned Value. Default Value: 0Fh “alpha“ coefficient of IIR used to filter signal power at anti-alias filter output, during acquisition phase.

Register 01A5h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				aaf_alpha_loc				
Type	R/W							

Bit	Name	Function
4:0	aaf_alpha_loc[4:0]	**Alpha_loc Coefficient Of AAF Digital AGC.** Unsigned Value. Default Value: 10h “alpha“ coefficient of IIR used to filter signal power at anti-alias filter output, during tracking phase.

Register 01A6h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					aaf_agc_step			
Type	R/W							

Bit	Name	Function
3:0	aaf_agc_step[3:0]	**Step Of AAF Digital AGC.** Unsigned Value. Default Value: 0001 Step parameter of anti-alias filter digital AGC loop. In fine AGC mode the gain is corrected by steps equal to: step = AAF_AGC_STEP / 16.

Register 01A7h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							aaf_update_sel	aaf_agc_freeze
Type							R/W	R/W

Bit	Name	Function
0	aaf_agc_freeze	**AAF Digital AGC Freeze Control.** 0 = unfrozen (default) 1 = frozen Anti-alias filter digital AGC loop is forced in frozen mode when AAF_AGC_FREEZE = 1, else it is in normal mode.
1	aaf_update_sel	**Reserved.** Unsigned Value. Default Value: 0 Must be set to 0.

Register 01A8h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			aaf_coarse2fine_thr					
Type	R/W							

Bit	Name	Function
5:0	aaf_coarse2fine_thr[5:0]	**AAF Coarse To Fine AGC Threshold.** Unsigned Value. Default Value: 1Eh When power error is lower than AAF_COARSE2FINE_THR, digital AGC goes from coarse mode to fine mode. - In coarse mode, AGC error is directly used to correct the gain. - In fine mode, the gain is corrected by steps equal to ±AAF_AGC_STEP / 16 AAF_COARSE2FINE_THR is a multiple of 1/16 dB.

Register 01A9h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			aaf_fine2coarse_thr					
Type	R/W							

Bit	Name	Function
5:0	aaf_fine2coarse_thr[5:0]	**AAF Fine To Coarse AGC Threshold.** Unsigned Value. Default Value: 30h When power error is greater than AAF_FINE2COARSE_THR, digital AGC goes from fine mode to coarse mode - In coarse mode, AGC error is directly used to correct the gain - In fine mode, the gain is corrected by steps equal to ±AAF_AGC_STEP / 16 AAF_FINE2COARSE_THR is a multiple of 1/16 dB.

Register 01AAh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			aaf_freeze_thr					
Type	R/W							

Bit	Name	Function
5:0	aaf_freeze_thr[5:0]	**AAF AGC Loop Freeze Threshold.** Unsigned Value. Default Value: 02h Anti-alias filter digital AGC loop is frozen when AGC error becomes less than AAF_FREEZE_THR. AAF_FREEZE_THR is a multiple of 1/16 dB.

Register 01ABh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			aaf_unfreeze_thr					
Type	R/W							

Bit	Name	Function
5:0	aaf_unfreeze_thr[5:0]	**AAF AGC Loop Unfreeze Threshold.** Unsigned Value. Default Value: 0Ch Anti-alias filter digital AGC loop is unfrozen when AGC error becomes larger than AAF_UNFREEZE_THR. AAF_UNFREEZE_THR is a multiple of 1/16 dB.

Register 01ACh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	aaf_agc_ext							
Type	R/W							

Bit	Name	Function
7:0	aaf_agc_ext[7:0]	**External Value For AAF AGC Command.** Unsigned Value. Default Value: 40h Each time aaf_agc_ext is written, corresponding value is loaded on aaf_agc_cmd. If the loop has been frozen with aaf_agc_freeze register then this value is maintained on aaf_agc_cmd command.

Register 01B0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	aaf_agc_cmd							
Type	R							

Bit	Name	Function
7:0	aaf_agc_cmd[7:0]	**AAF AGC Command Current Value.** Unsigned Value. Anti-alias filter current digital gain command. Gain (dB) = AAF_AGC_CMD / 8 – 1.9

Register 01B8h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	01B8h aaf_pow_fil (LSB)							
Type	R							
Name							01B9h aaf_pow_fil (MSB)	
Type	R							

Bit	Name	Function
9:0	aaf_pow_fil[9:0]	**AAF Output Mean Power.** Unsigned Value. Anti-alias filter output average power. Signal crest factor at anti-alias filter output is equal to 10 x log(2 x AAF_POW_MAX / AAF_POW_FIL) dB

Register 01BEh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	01BEh aaf_pow_max (LSB)							
Type	R							
Name								01BFh aaf_pow_max (MSB)
Type								R

Bit	Name	Function
8:0	aaf_pow_max[8:0]	**AAF Output Peak Power.** Unsigned Value. Saturation margin (in dB, relative to full scale) = 10 x log(aaf_pow_max / 510)

Register 01C0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								aaf_pow_max_init
Type								R/W

Bit	Name	Function
0	aaf_pow_max_init	**AAF Output Peak Power Indicator Reset.** Unsigned Value. Default Value: 0. (Auto Return register) Each time AAF_POW_MAX_INIT is set high, maximum power detector (AAF_POW_MAX) is reinitialized to 0.

Register 01C4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							aaf_freeze_int	aaf_lock
Type							R	R

Bit	Name	Function
0	aaf_lock	**AAF AGC Loop Lock Indicator.** 0 = unlocked (default) 1 = locked “locked“ means in fine or frozen mode.
1	aaf_freeze_int	**AAF AGC Loop Freeze Indicator.** 0 = unfrozen (default) 1 = frozen Indicates whether anti-alias filter digital AGC loop is frozen or not. The loop is frozen when AGC error is lower than AAF_FREEZE_THR and unfrozen when AGC error is higher than AAF_UNFREEZE_THR.

Register 01C8h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	aci_crestf_dbx8							
Type	R/W							

Bit	Name	Function
7:0	aci_crestf_dbx8[7:0]	**ACI Filter Digital AGC Reference.** Unsigned Value. Default Value: 68h Crest factor reference for ACI filter digital AGC: aci_crestf_dbx8 = 8 x CrestFactor (in dB) Sets the ratio between the wanted average signal power and full scale at ACI filter output. This reference must be higher than the maximum possible crest factor of the signal, to avoid saturation.

Register 01CCh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				aci_alpha_acq				
Type	R/W							

Bit	Name	Function
4:0	aci_alpha_acq[4:0]	**Alpha_acq Coefficient Of ACI Digital AGC.** Unsigned Value. Default Value: 0Ah “alpha“ coefficient of IIR used to filter signal power at anti-alias filter output, during acquisition phase.

Register 01CDh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				aci_alpha_loc				
Type	R/W							

Bit	Name	Function
4:0	aci_alpha_loc[4:0]	**Alpha_loc Coefficient Of ACI Digital AGC.** Unsigned Value. Default Value: 0Bh “alpha“ coefficient of IIR used to filter signal power at anti-alias filter output, during tracking phase.

Register 01CEh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					aci_agc_step			
Type	R/W							

Bit	Name	Function
3:0	aci_agc_step[3:0]	**Step Of ACI Digital AGC.** Unsigned Value. Default Value: 0001 Step parameter of anti-alias filter digital AGC loop. In fine AGC mode the gain is corrected by steps equal to: step = aci_agc_step / 16.

Register 01CFh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							aci_agc_update_sel	aci_agc_freeze
Type	R/W						R/W	R/W

Bit	Name	Function
0	aci_agc_freeze	**ACI Digital AGC Freeze Control.** 0 = unfrozen (default) 1 = frozen Anti-alias filter digital AGC loop is forced in frozen mode when aci_agc_freeze = 1, else it is in normal mode.
1	aci_agc_update_sel	**Reserved.** 0 = internal (default) 1 = external Must be set to 0.

Register 01D0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			aci_coarse2fine_thr					
Type	R/W							

Bit	Name	Function
5:0	aci_coarse2fine_thr[5:0]	**ACI Coarse To Fine AGC Threshold.** Unsigned Value. Default Value: 08h When power error is lower than aci_coarse2fine_thr, digital AGC goes from coarse mode to fine mode. - In coarse mode, AGC error is directly used to correct the gain. - In fine mode, the gain is corrected by steps equal to ±aci_agc_step / 16 aci_coarse2fine_thr is a multiple of 1/16 dB.

Register 01D1h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			aci_fine2coarse_thr					
Type	R/W							

Bit	Name	Function
5:0	aci_fine2coarse_thr[5:0]	**ACI Fine To Coarse AGC Threshold.** Unsigned Value. Default Value: 30h When power error is greater than aci_fine2coarse_thr, digital AGC goes from fine mode to coarse mode. - In coarse mode, AGC error is directly used to correct the gain. - In fine mode, the gain is corrected by steps equal to ±aci_agc_step / 16 aci_fine2coarse_thr is a multiple of 1/16 dB.

Register 01D2h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			aci_freeze_thr					
Type	R/W							

Bit	Name	Function
5:0	aci_freeze_thr[5:0]	**ACI AGC Loop Freeze Threshold.** Unsigned Value. Default Value: 03h Anti-alias filter digital AGC loop is frozen when AGC error becomes less than aci_freeze_thr. aci_freeze_thr is a multiple of 1/16 dB.

Register 01D3h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			aci_unfreeze_thr					
Type	R/W							

Bit	Name	Function
5:0	aci_unfreeze_thr[5:0]	**ACI AGC Loop Unfreeze Threshold.** Unsigned Value. Default Value: 08h Anti-alias filter digital AGC loop is unfrozen when AGC error becomes larger than aci_unfreeze_thr. aci_unfreeze_thr is a multiple of 1/16 dB.

Register 01D4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	aci_agc_ext							
Type	R/W							

Bit	Name	Function
7:0	aci_agc_ext[7:0]	**External Value For ACI AGC Command.** Unsigned Value. Default Value: 70h Each time aci_agc_ext is written, corresponding value is loaded on aci_agc_cmd. If the loop has been frozen with aci_agc_freeze register then this value is maintained on aci_agc_cmd command.

Register 01D8h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	aci_agc_cmd							
Type	R							

Bit	Name	Function
7:0	aci_agc_cmd[7:0]	**ACI AGC Command Current Value.** Unsigned Value. Anti-alias filter current digital gain command. Gain (dB) = ACI_AGC_CMD / 8 – 1.9

Register 01E0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	01E0h aci_pow_fil (LSB)							
Type	R							
Name							01E1h aci_pow_fil (MSB)	
Type	R							

Bit	Name	Function
9:0	aci_pow_fil[9:0]	**ACI Output Mean Power.** Unsigned Value. ACI filter output average power. Signal crest factor at ACI filter output is equal to 10 x log(2 x aci_pow_max / aci_pow_fil) dB

Register 01E6h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	01E6h aci_pow_max (LSB)							
Type	R							
Name								01E7h aci_pow_max (MSB)
Type								R

Bit	Name	Function
8:0	aci_pow_max[8:0]	**ACI Output Peak Power.** Unsigned Value. Saturation margin (in dB, relative to full scale) = 10 x log(aci_pow_max / 510).

Register 01E8h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								aci_pow_max_init
Type								R/W

Bit	Name	Function
0	aci_pow_max_init	**ACI Output Peak Power Indicator Reset.** Unsigned Value. Default Value: 0. (Auto Return register) Each time aci_pow_max_init is set high, maximum power detector (aci_pow_max) is reinitialized to 0.

Register 01ECh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							aci_freeze_int	aci_lock
Type							R	R

Bit	Name	Function
0	aci_lock	**ACI AGC Loop Lock Indicator.** 0 = unlocked (default) 1 = locked Anti-alias filter AGC loop lock indicator. “locked“ means in fine or frozen mode.
1	aci_freeze_int	**ACI AGC Loop Freeze Indicator.** 0 = unfrozen (default) 1 = frozen Indicates whether anti-alias filter digital AGC loop is frozen or not. The loop is frozen when AGC error is lower than aci_freeze_thr and unfrozen when AGC error is higher than aci_unfreeze_thr.

Register 0200h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				tim_ki_acq				
Type	R/W							

Bit	Name	Function
4:0	tim_ki_acq[4:0]	**Integral Coefficient Of QAM Timing Loop (Acquisition Phase).** Signed Value. Default Value: 1Ah Sets integral coefficient (KI) of the QAM timing loop filter to $2^{TIM\_KI\_ACQ}$ during acquisition phase.

Register 0201h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					tim_kp_acq			
Type	R/W							

Bit	Name	Function
3:0	tim_kp_acq[3:0]	**Proportional Coefficient Of QAM Timing Loop (Acquisition Phase).** Signed Value. Default Value: 0100 Sets proportional coefficient (KP) of the QAM timing loop filter to $2^{TIM\_KP\_ACQ}$ during acquisition phase.

Register 0202h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				tim_ki_loc				
Type	R/W							

Bit	Name	Function
4:0	tim_ki_loc[4:0]	**Integral Coefficient Of QAM Timing Loop (Tracking Phase).** Signed Value. Default Value: 13h Sets integral coefficient (KI) of the QAM timing loop filter to $2^{TIM\_KI\_LOC}$ during tracking phase.

Register 0203h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					tim_kp_loc			
Type	R/W							

Bit	Name	Function
3:0	tim_kp_loc[3:0]	**Proportional Coefficient Of QAM Timing Loop (Tracking Phase).** Signed Value. Default Value: 0001 Sets proportional coefficient (KP) of the QAM timing loop filter to $2^{TIM\_KP\_LOC}$ during tracking phase.

Register 0208h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0208h timing_corr_c (LSB)							
Type	R							
Name	0209h timing_corr_c (Middle)							
Type	R							
Name							020Ah timing_corr_c (MSB)	
Type	R							

Bit	Name	Function
17:0	timing_corr_c[17:0]	**Timing Offset Correction For QAM.** Signed Value. Timing offset recovered by the timing loop. The timing offset, in ppm, is equal to: -10^6 x TIMING_CORR_C / (TIMING_CORR_C + 2^{20})

Register 020Dh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							tim_update_period	
Type	R/W							

Bit	Name	Function
1:0	tim_update_period[1:0]	**Update Period Of Coarse Timing Sweep For QAM.** Unsigned Value. Default Value: 10 Update period of each step of the coarse timing sweep which is equal to $2^{(12 + TIM\_UPDATE\_PERIOD)}$ symbols.

Register 0211h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			range_baud_rate					
Type	R/W							

Bit	Name	Function
5:0	range_baud_rate[5:0]	**Coarse Timing Sweep Range For QAM.** Unsigned Value. Default Value: 20h The range, in ppm, is equal to: 10^6 x RANGE_BAUD_RATE / 256. The time to perform the complete sweep is equal to: $2^{(12 + TIM\_UPDATE\_PERIOD)}$ x RANGE_BAUD_RATE / 3 symbols.

Register 0214h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0214h coarsetim_corr (LSB)							
Type	R							
Name					0215h coarsetim_corr (MSB)			
Type	R							

Bit	Name	Function
11:0	coarsetim_corr[11:0]	**Coarse Timing Correction For QAM.** Signed Value. Coarse timing correction. The baud rate correction, in ppm, is equal to: 10^6 x COARSETIM_CORR / 4096.

Register 0219h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					timing_unfrz_cond		baud_rate_unfrz_cond	
Type	R/W						R/W	

Bit	Name	Function
1:0	baud_rate_unfrz_cond[1:0]	**Baud Rate Scan Unfreeze Condition For QAM.** 00 = disable (default) 01 = agc_lock 10 = all_agc_lock Other = Reserved Condition to start baud rate scan: 00 = No condition, it stays frozen. 01 = It starts when analog AGC has converged. 10 = It starts when all AGCs have converged (analog AGC, AAF AGC and ACI AGC).
3:2	timing_unfrz_cond[1:0]	**Timing Recovery Loop Unfreeze Condition For QAM.** 00 = disable 01 = agc_lock 10 = all_agc_lock (default) 11 = baud_rate_lock Condition to start the timing recovery loop: 00 = No condition, it stays frozen. 01 = It starts when analog AGC has converged. 10 = It starts when all AGCs have converged (analog AGC, AAF AGC and ACI AGC). 11 = It starts when the extended baud rate loop has converged.

Register 0230h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	sweep_init							
Type	R/W							

Bit	Name	Function
7:0	sweep_init[7:0]	**Initial Value Of Carrier Frequency Sweep For QAM.** Signed Value. Default Value: FAh The carrier frequency sweep starts from SweepInit percent of the symbol rate where: SweepInit = 100 x SWEEP_INIT / 256

Register 0231h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		sweep_range						
Type	R/W							

Bit	Name	Function
6:0	sweep_range[6:0]	**Carrier Frequency Sweep Range For QAM.** Unsigned Value. Default Value: 1Ch The carrier frequency sweep range is ±SweepRange percent of the symbol rate where: SweepRange = 100 x SWEEP_RANGE / 256

Register 0232h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			sweep_step					
Type	R/W							

Bit	Name	Function
5:0	sweep_step[5:0]	**Carrier Frequency Sweep Step For QAM.** Signed Value. Default Value: 03h Step of the carrier frequency sweep. Each symbol the frequency is incremented by SweepStep percent of the symbol rate where: SweepStep = 100 x SWEEP_STEP / 2^{24}

Register 0234h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0234h freq_corr_c (LSB)							
Type	R							
Name	0235h freq_corr_c (MSB)							
Type	R							

Bit	Name	Function
15:0	freq_corr_c[15:0]	**Frequency Offset Correction For QAM.** Signed Value. Sweep carrier frequency offset correction: SweepOffsetFrequency(Hz) = FE_clk(Hz) x FREQ_CORR_C / 2^{16}

Register 0238h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					kp_acq			
Type	R/W							

Bit	Name	Function
3:0	kp_acq[3:0]	**Proportional Coefficient Of Carrier Loop During Acquisition.** Signed Value. Default Value: 0110

Register 0239h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				ki_acq				
Type	R/W							

Bit	Name	Function
4:0	ki_acq[4:0]	**Integral Coefficient Of Carrier Loop During Acquisition.** Signed Value. Default Value: 1Dh

Register 023Ah.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					kp_lock			
Type	R/W							

Bit	Name	Function
3:0	kp_lock[3:0]	**Proportional Coefficient Of Carrier Loop During Tracking.** Signed Value. Default Value: 0101

Register 023Bh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				ki_lock				
Type	R/W							

Bit	Name	Function
4:0	ki_lock[4:0]	**Integral Coefficient Of Carrier Loop During Tracking.** Signed Value. Default Value: 1Eh

Register 023Eh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								demod_lock_c
Type	R							

Bit	Name	Function
0	demod_lock_c	**Demodulator Lock Indicator.** 0 = unlocked (default) 1 = locked

Register 0240h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0240h phase_cor_c (LSB)							
Type	R							
Name	0241h phase_cor_c (MSB)							
Type	R							

Bit	Name	Function
15:0	phase_cor_c[15:0]	**Frequency Offset Recovered By The Phase Loop.** Signed Value. FrequencyOffset (Hz) = SymbolRate (Hz) x phase_cor_c / 2^{16}

Register 0260h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		ffe_length						
Type	R/W							

Bit	Name	Function
6:0	ffe_length[6:0]	**Length Of Equalizer FFE Part.** Unsigned Value. Default Value: 0Ah The number of taps of FFE part is equal to (1 + 2 x ffe_length).

Register 0261h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	central_tap							
Type	R/W							

Bit	Name	Function
7:0	central_tap[7:0]	**Position Of Equalizer Central Tap.** Unsigned Value. Default Value: 0Bh It must be less or equal to the length of equalizer FFE part.

Register 0264h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	gain_ddffe				gain_cma			
Type	R/W				R/W			

Bit	Name	Function
3:0	gain_cma[3:0]	**Adaptation Gain Of The Equalizer In CMA Mode.** 0000 = auto (default) 0001 = 1 0010 = 2 0011 = 4 0100 = 8 0101 = 16 0110 = 32 0111 = 64 1000 = 128 Other = Reserved The higher the gain, the faster the equalizer convergence and the noisier the equalizer coefficients. This value is taken into account only if different from 0, otherwise, a default value, adapted to broadcast parameters, is automatically set internally. This default internal CMA gain value is equal to 16.
7:4	gain_ddffe[3:0]	**Adaptation Gain Of FFE Part In Decision Directed Mode.** 0000 = auto (default) 0001 = 1 0010 = 2 0011 = 4 0100 = 8 0101 = 16 0110 = 32 0111 = 64 1000 = 128 Other = Reserved The higher the gain, the faster the equalizer convergence and the noisier the equalizer coefficients. This value is taken into account only if different from 0, otherwise, a default value, adapted to broadcast parameters, is automatically set internally. This default internal DD FFE gain value is equal to 8.

Register 0265h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					gain_dddfe			
Type	R/W							

Bit	Name	Function
3:0	gain_dddfe[3:0]	**Adaptation Gain Of DFE Part.** 0000 = auto (default) 0001 = 1 0010 = 2 0011 = 4 0100 = 8 0101 = 16 0110 = 32 0111 = 64 1000 = 128 Other = Reserved The higher the gain, the faster the equalizer convergence and the noisier are the equalizer coefficients. This value is taken into account only if different from 0, otherwise, a default value, adapted to broadcast parameters, is automatically set internally. This default internal DD DFE gain value is equal to 8.

Register 026Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	026Ch c_n (LSB)							
Type	R							
Name	026Dh c_n (Middle)							
Type	R							
Name	026Eh c_n (MSB)							
Type	R							

Bit	Name	Function
23:0	c_n[23:0]	**C/N Indicator For DVB-C.** Unsigned Value. C/N value in dB is given by the following relation: C/N (dB) = 10 x log(2^{24} / c_n).

Register 0278h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							auto_algo	auto_control
Type							R/W	R/W

Bit	Name	Function
0	auto_control	**Equalizer Automatic Control Setting.** 0 = off 1 = on (default) When equals to 1, the equalizer is controlled automatically, else it is controlled through the epb interface (cma_dd, init_ffe, freeze_ffe, init_dfe, freeze_dfe).
1	auto_algo	**Equalizer Automatic Reinitialization Setting.** 0 = dfe_init 1 = dfe_freeze (default) Determines the algorithm used by the control state machine. When 'auto_algo'=0, the DFE coefficients are re-initialized to 0 each time the equalizer switches from full_dfe state to another state, else the DFE coefficients are frozen.

Register 02A4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	02A4h sigma2_est (LSB)							
Type	R							
Name	02A5h sigma2_est (Middle)							
Type	R							
Name	02A6h sigma2_est (MSB)							
Type	R							

Bit	Name	Function
23:0	sigma2_est[23:0]	**Noise Power Output Value.** Unsigned Value. The mean noise power estimated on the received data, allowing computing an estimation of the signal to noise ratio (C/N) in DVB-T. C/N (in dB) = 10 x log(128 x ref_signal_power / sigma2_est)

Register 02C0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	02C0h ref_signal_power (LSB)							
Type	R							
Name			02C1h ref_signal_power (MSB)					
Type	R							

Bit	Name	Function
13:0	ref_signal_power[13:0]	**Reference Signal Power.** Unsigned Value. Provides the value of the signal power for the selected constellation, for C/N estimation. C/N (in dB) = 10 x log(128 x ref_signal_power / sigma2_est)

Register 02E0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								start_synchro
Type	R/W							

Bit	Name	Function
0	start_synchro	**Start DVB-T Signal Acquisition.** 0 = running 1 = start (default) Writing “start“ in this register resets and starts a complete DVB-T signal acquisition. This should be done after the RF tuner has locked onto a new channel and after each rst_all command in DVB-T mode. It returns automatically to the value “running“.

Register 02E4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								req_stream
Type	R/W							

Bit	Name	Function
0	req_stream	**Hierarchical Stream Selection.** 0 = HP (default) 1 = LP This register sets the hierarchical stream to be decoded by the FEC.

Register 02E8h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								automatic_synchro
Type	R/W							

Bit	Name	Function
0	automatic_synchro	**DVB-T Parameters Automatic Configuration.** 0 = on (default) 1 = off When activated the demodulator is automatically configured by the DVB-T parameters found in the TPS stream. When off the proper configuration has to be entered in the following registers (req_fft_mode, req_guard_int, req_constellation, req_rate_HP, req_rate_LP, req_hierarchy).

Register 02ECh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					req_fft_mode			
Type	R/W							

Bit	Name	Function
3:0	req_fft_mode[3:0]	**Required FFT Mode.** 1011 = 2K 1100 = 4K 1101 = 8K (default) Other = Reserved Required fft mode used when automatic_synchro register is off.

Register 02F0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						req_guard_int		
Type	R/W							

Bit	Name	Function
2:0	req_guard_int[2:0]	**DVB-T Required Guard Interval.** 001 = 1_32 (default) 010 = 1_16 011 = 1_8 100 = 1_4 Other = Reserved Required guard interval mode used when automatic_synchro register is off.

Register 02F4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			req_constellation					
Type	R/W							

Bit	Name	Function
5:0	req_constellation[5:0]	**Required Constellation.** 03h = QPSK (default) 07h = QAM16 08h = QAM32 09h = QAM64 0Ah = QAM128 0Bh = QAM256 Other = Reserved In DVB-T, sets the required constellation when automatic_synchro register is off. In DVB-C, sets the wanted constellation.

Register 02F8h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					req_rate_HP			
Type	R/W							

Bit	Name	Function
3:0	req_rate_HP[3:0]	**Required HP Stream Rate.** 0001 = 1_2 (default) 0010 = 2_3 0011 = 3_4 0101 = 5_6 0111 = 7_8 Other = Reserved Required HP stream rate used when automatic_synchro register is off.

Register 0300h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					req_rate_LP			
Type	R/W							

Bit	Name	Function
3:0	req_rate_LP[3:0]	**Required LP Stream Rate.** 0001 = 1_2 (default) 0010 = 2_3 0011 = 3_4 0101 = 5_6 0111 = 7_8 Other = Reserved Required LP stream rate used when automatic_synchro register is off.

Register 0304h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						req_hierarchy		
Type	R/W							

Bit	Name	Function
2:0	req_hierarchy[2:0]	**Required Hierarchy Level.** 001 = NONE (default) 010 = ALFA1 011 = ALFA2 101 = ALFA4 Other = Reserved Required hierarchy mode used when automatic_synchro register is off.

Register 0308h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0308h bandwidth (LSB)							
Type	R/W							
Name			0309h bandwidth (MSB)					
Type	R/W							

Bit	Name	Function
13:0	bandwidth[13:0]	**DVB-T Bandwidth.** Unsigned Value. Default Value: 0320h Enter the desired DVB-T bandwidth in 10 KHz resolution. For example: 8 MHz = 800

Register 030Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	030Ch freq_sync_range (LSB)							
Type	R/W							
Name					030Dh freq_sync_range (MSB)			
Type	R/W							

Bit	Name	Function
11:0	freq_sync_range[11:0]	**Frequency Recovery Range.** Unsigned Value. Default Value: 000h Enter the frequency recovery detection range in ±kHz (in DVB-T applications). When set to zero the range is ±50 kHz. When set to 200, the range is ±200 kHz. Frequency recovery time is function of the search range. Use ±200 kHz to include ±166 kHz frequency offset(s) recovery during scanning and switch to ±50 kHz range for normal operation.

Register 0310h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								cpe_req
Type								R/W

Bit	Name	Function
0	cpe_req	**CPE Activation Request.** 0 = off 1 = on (default) Activation of Common Phase Error compensation.

Register 0318h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	timing_sync_range							
Type	R/W							

Bit	Name	Function
7:0	timing_sync_range[7:0]	**Timing Recovery Range In DVB-T.** Unsigned Value. Default Value: 64h Enter, in ppm, the local oscillator precision (for DVB-T applications only). For example 50 for a ±50 ppm crystal. Maximum value is 200.

Register 031Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								impulsive_noise_remover
Type	R/W							

Bit	Name	Function
0	impulsive_noise_remover	**Impulsive Noise Remover.** 0 = off (default) 1 = on Activates the impulsive noise remover algorithm.

Register 0320h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					check_signal_thres			
Type	R/W							

Bit	Name	Function
3:0	check_signal_thres[3:0]	**Check Signal Threshold.** Unsigned Value. Default Value: 0010 “Check_signal“ register detector speed. Adjusts the time during which the demodulator checks channel status and after which it returns channel detection status in the ‘check_signal‘ register.

Register 0324h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				relock_on_per_thres				
Type	R/W							

Bit	Name	Function
4:0	relock_on_per_thres[4:0]	**Automatic Relock On Packet Error Rate.** Unsigned Value. Default Value: 06h When different from 0 an automatic DVB-T relock is performed if the RS Packet Error Rate is above $1 / 2^{relock\_on\_per\_thres}$ (ex: 10: 1E-3). Firmware is measuring RS Packet Error Rate and Viterbi output BER every second. If BER is below the threshold set in stay_lock_ber_thres register, the demodulator will stay locked irrespective of the PER value (avoiding problems due to short impairments).

Register 0328h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				stay_lock_ber_thres				
Type	R							

Bit	Name	Function
4:0	stay_lock_ber_thres[4:0]	**Automatic Relock BER Threshold.** Unsigned Value. Default Value: 08h According to the register relock_on_per_thres this threshold blocks any automatic relock if the Viterbi output BER is below 1 / $2^{stay\_lock\_ber\_thres}$ (ex: 8: 3.9E-3).

Register 0334h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					freq_bw_acq			
Type	R/W							

Bit	Name	Function
3:0	freq_bw_acq[3:0]	**Frequency Acquisition Bandwidth.** Unsigned Value. Default Value: 1101 Sets the frequency loop gain in acquisition phase (DVB-T only).

Register 0336h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					freq_bw_track			
Type	R/W							

Bit	Name	Function
3:0	freq_bw_track[3:0]	**Frequency Tracking Bandwidth.** Unsigned Value. Default Value: 1001 Sets the frequency loop gain in tracking phase (DVB-T only).

Register 0338h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					timing_bw_acq			
Type	R/W							

Bit	Name	Function
3:0	timing_bw_acq[3:0]	**Timing Acquisition Bandwidth.** Unsigned Value. Default Value: 1011 Timing loop acquisition bandwidth (DVB-T only).

Register 033Ah.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					timing_bw_track			
Type	R/W							

Bit	Name	Function
3:0	timing_bw_track[3:0]	**Timing Tracking Bandwidth.** Unsigned Value. Default Value: 0110 The timing loop gain in tracking phase (DVB-T only)..

Register 0341h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						wdog_error	rst_wdog_error	boot_done
Type	R/W					R	R/W	R

Bit	Name	Function
0	boot_done	**Boot Status.** 0 = in_progress (default) 1 = done Indicates if the boot program is in progress or if now done.
1	rst_wdog_error	**Watch Dog Error Reset.** Auto Return register 0 = run (default) 1 = reset
2	wdog_error	**Watch Dog Error Indicator.** 0 = no_error (default) 1 = error

Register 0344h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	patch_version							
Type	R/W							

Bit	Name	Function
7:0	patch_version[7:0]	**Patch Version.** Unsigned Value. Default Value: 00h

Register 0348h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0348h addr_jump (LSB)							
Type	R/W							
Name	0349h addr_jump							
Type	R/W							
Name	034Ah addr_jump							
Type	R/W							
Name	034Bh addr_jump (MSB)							
Type	R/W							

Bit	Name	Function
31:0	addr_jump[31:0]	**DSP Jump Address.** Unsigned Value. Default Value: 00000000h Jump address at DSP boot.

Register 035Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							errorn	en_rst_error
Type							R	R/W

Bit	Name	Function
0	en_rst_error	**Processor Reset Enable.** 0 = no_reset_on_errorn 1 = reset_on_errorn (default) Selects whether the processor is reset or not when a processor internal error occurs.
1	errorn	**Processor Internal Error.** 0 = error_state (default) 1 = no_error This active low register is asserted when the processor has entered error state and is halted.

Register 0364h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0364h dcom_control_byte (LSB)							
Type	R/W							
Name	0365h dcom_control_byte							
Type	R/W							
Name	0366h dcom_control_byte							
Type	R/W							
Name	0367h dcom_control_byte (MSB)							
Type	R/W							

Bit	Name	Function
31:0	dcom_control_byte[31:0]	**Patch Download Control.** Unsigned Value. Default Value: 00000000h Used for patch download only. Indicates type and length of next patch data download.

Register 0368h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0368h dcom_addr (LSB)							
Type	R/W							
Name	0369h dcom_addr							
Type	R/W							
Name	036Ah dcom_addr							
Type	R/W							
Name	036Bh dcom_addr (MSB)							
Type	R/W							

Bit	Name	Function
31:0	dcom_addr[31:0]	**Patch Download Address.** Unsigned Value. Default Value: 00000000h Used for patch download only. Indicates address of next patch data word.

Register 036Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	036Ch dcom_data (LSB)							
Type	R/W							
Name	036Dh dcom_data							
Type	R/W							
Name	036Eh dcom_data							
Type	R/W							
Name	036Fh dcom_data (MSB)							
Type	R/W							

Bit	Name	Function
31:0	dcom_data[31:0]	**Patch Download Data.** Unsigned Value. Default Value: 00000000h Used for patch download only. Patch data word.

Register 0379h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								rst_crc
Type								R/W

Bit	Name	Function
0	rst_crc	**CRC Reset Register.** Auto Return register 0 = run (default) 1 = reset

Register 037Ah.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	037Ah crc (LSB)							
Type	R							
Name	037Bh crc (MSB)							
Type	R							

Bit	Name	Function
15:0	crc[15:0]	**CRC Of Downloaded Patch.** Unsigned Value.

Register 0384h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0384h gp_reg0 (LSB)							
Type	R/W							
Name	0385h gp_reg0							
Type	R/W							
Name	0386h gp_reg0							
Type	R/W							
Name	0387h gp_reg0 (MSB)							
Type	R/W							

Bit	Name	Function
31:0	gp_reg0[31:0]	**First General Purpose DSP Register.** Unsigned Value. Default Value: 00000000h

Register 0388h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0388h gp_reg1 (LSB)							
Type	R/W							
Name	0389h gp_reg1							
Type	R/W							
Name	038Ah gp_reg1							
Type	R/W							
Name	038Bh gp_reg1 (MSB)							
Type	R/W							

Bit	Name	Function
31:0	gp_reg1[31:0]	**Second General Purpose DSP Register.** Unsigned Value. Default Value: 00000000h

Register 038Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	038Ch gp_reg2 (LSB)							
Type	R/W							
Name	038Dh gp_reg2							
Type	R/W							
Name	038Eh gp_reg2							
Type	R/W							
Name	038Fh gp_reg2 (MSB)							
Type	R/W							

Bit	Name	Function
31:0	gp_reg2[31:0]	**Third General Purpose DSP Register.** Unsigned Value. Default Value: 00000000h

Register 0390h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								demod_lock_t
Type								R

Bit	Name	Function
0	demod_lock_t	**DVB-T Demodulator Lock Status.** 0 = unlocked (default) 1 = locked Goes to ‘locked‘ when the demodulator has locked onto a valid DVB-T signal.

Register 0394h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								tps_lock
Type								R

Bit	Name	Function
0	tps_lock	**TPS Lock Status.** 0 = unlocked (default) 1 = locked TPS decoder lock indicator.

Register 0398h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								freq_lock_t
Type								R

Bit	Name	Function
0	freq_lock_t	**DVB-T Frequency Lock Status.** 0 = unlocked (default) 1 = locked Indicates ‘locked‘ when the DVB-T frequency recovery loop has converged.

Register 039Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								timing_lock_t
Type								R

Bit	Name	Function
0	timing_lock_t	**DVB-T Timing Loop Status.** 0 = unlocked (default) 1 = locked Indicates ‘locked‘ when the DVB-T timing recovery loop has converged.

Register 03A0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								fft_lock_t
Type								R

Bit	Name	Function
0	fft_lock_t	**DVB-T FFT Window Positioning Status.** 0 = unlocked (default) 1 = locked Indicates ‘locked‘ when the DVB-T FFT window recovery loop has converged.

Register 03A4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	03A4h channel_length (LSB)							
Type	R							
Name				03A5h channel_length (MSB)				
Type	R							

Bit	Name	Function
12:0	channel_length[12:0]	**Channel Length.** Unsigned Value. Default Value: 0000h FFT window recovery loop returns the received channel length estimation in time. The bit resolution is Tu/256 (where Tu is 896 us in 8K mode and 224 us in 2K mode).

Register 03A8h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							check_signal	
Type							R	

Bit	Name	Function
1:0	check_signal[1:0]	**Fast Signal Type Detection.** 00 = searching (default) 01 = nothing 10 = digital Gives a fast feedback of the channel type to help scanning loop. After writing “start“ in the start_synchro register it goes to “searching“. Then as soon as possible and much faster than a complete DVB_T lock process returns the signal type. When the value “nothing“ is returned, the scanning loop can leave this frequency to check the next one. When the value “digital“ is returned, this indicates a DVB-T or DVB-H signal.

Register 03B0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	03B0h timing_corr_t (LSB)							
Type	R							
Name	03B1h timing_corr_t (Middle)							
Type	R							
Name					03B2h timing_corr_t (MSB)			
Type	R							

Bit	Name	Function
19:0	timing_corr_t[19:0]	**Timing Offset.** Signed Value. DVB-T Timing correction to the front-end. The timing offset, in ppm, is equal to: 10^6 x TIMING_CORR_T x DVB_rate / FE_clk / 2^{21}

Register 03B4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	03B4h freq_corr_t (LSB)							
Type	R							
Name	03B5h freq_corr_t							
Type	R							
Name	03B6h freq_corr_t							
Type	R							
Name							03B7h freq_corr_t (MSB)	
Type	R							

Bit	Name	Function
25:0	freq_corr_t[25:0]	**Frequency Offset.** Signed Value. DVB-T frequency correction to the front-end. FrequencyOffset (Hz) = FE_clk (Hz) x FREQ_CORR_T / 2^{29}

Register 03F0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					auto_fft_mode			
Type	R							

Bit	Name	Function
3:0	auto_fft_mode[3:0]	**Detected FFT Mode.** 1011 = 2K (default) 1100 = 4K 1101 = 8K FFT mode detected in the TPS stream by the demodulator.

Register 03F4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						auto_guard_int		
Type	R							

Bit	Name	Function
2:0	auto_guard_int[2:0]	**Detected Guard Interval.** 001 = 1_32 (default) 010 = 1_16 011 = 1_8 100 = 1_4 Guard interval mode detected in the TPS stream by the demodulator.

Register 03F8h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			auto_constellation					
Type	R							

Bit	Name	Function
5:0	auto_constellation[5:0]	**Detected DVB-T Constellation.** 03h = QPSK 07h = QAM16 09h = QAM64 (default) Constellation detected in the TPS stream by the demodulator.

Register 0400h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					auto_rate_HP			
Type	R							

Bit	Name	Function
3:0	auto_rate_HP[3:0]	**Detected HP Stream Rate.** 0001 = 1_2 (default) 0010 = 2_3 0011 = 3_4 0101 = 5_6 0111 = 7_8 HP stream rate detected in the TPS stream by the demodulator.

Register 0404h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					auto_rate_LP			
Type	R							

Bit	Name	Function
3:0	auto_rate_LP[3:0]	**Detected LP Stream Rate.** 0001 = 1_2 (default) 0010 = 2_3 0011 = 3_4 0101 = 5_6 0111 = 7_8 LP stream rate detected in the TPS stream by the demodulator.

Register 0408h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						auto_hierarchy		
Type	R							

Bit	Name	Function
2:0	auto_hierarchy[2:0]	**Detected Hierarchical Level.** 001 = NONE (default) 010 = ALFA1 011 = ALFA2 101 = ALFA4 Hierarchy mode detected in the TPS stream by the demodulator.

Register 040Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	040Ch cell_id (LSB)							
Type	R							
Name	040Dh cell_id (MSB)							
Type	R							

Bit	Name	Function
15:0	cell_id[15:0]	**Received DVB-T Signal Cell Id.** Unsigned Value. Default Value: 0000h Contains the TPS decoded Cell-ID value.

Register 0410h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					tps_reserved1			
Type	R							

Bit	Name	Function
3:0	tps_reserved1[3:0]	**Spare TPS Bit Part 1.** Unsigned Value. Default Value: 0000 Contains the decoded TPS bit [50:53] from frame 1.

Register 0411h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					tps_reserved2			
Type	R							

Bit	Name	Function
3:0	tps_reserved2[3:0]	**Spare TPS Bit Part 2.** Unsigned Value. Default Value: 0000 Contains the decoded TPS bit [50:53] from frame 2.

Register 0412h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					tps_reserved3			
Type	R							

Bit	Name	Function
3:0	tps_reserved3[3:0]	**Spare TPS Bit Part 3.** Unsigned Value. Default Value: 0000 Contains the decoded TPS bit [50:53] from frame 3.

Register 0413h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					tps_reserved4			
Type	R							

Bit	Name	Function
3:0	tps_reserved4[3:0]	**Spare TPS Bit Part 4.** Unsigned Value. Default Value: 0000 Contains the decoded TPS bit [50:53] from frame 4.

Register 0414h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								lp_time_slicing
Type								R

Bit	Name	Function
0	lp_time_slicing	**Time Slicing Used On LP Stream.** 0 = off (default) 1 = on Indicates if time slicing is used on minimum one elementary stream or not (DVB-H only).

Register 0415h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								lp_mpe_fec
Type								R

Bit	Name	Function
0	lp_mpe_fec	**MPE FEC Used On LP Stream.** 0 = off (default) 1 = on Indicates if MPE FEC is used on minimum one elementary stream or not (DVB-H only).

Register 0416h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								hp_time_slicing
Type								R

Bit	Name	Function
0	hp_time_slicing	**Time Slicing Used On HP Stream.** 0 = off (default) 1 = on Indicates if time slicing is used on minimum one elementary stream or not (DVB-H only).

Register 0417h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								hp_mpe_fec
Type								R

Bit	Name	Function
0	hp_mpe_fec	**MPE FEC Used On HP Stream.** 0 = off (default) 1 = on Indicates if MPE FEC is used on minimum one elementary stream or not (DVB-H only).

Register 0418h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			tps_length					
Type	R							

Bit	Name	Function
5:0	tps_length[5:0]	**TPS Word Length.** Unsigned Value. Default Value: 00h TPS length indicator: 33 in DVB-H, 31 in DVB-T with cell identification, 23 in DVB-T without cell identification.

Register 041Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								dvbh_interleaver
Type								R

Bit	Name	Function
0	dvbh_interleaver	**TPS In-depth Inner Interleaver.** 0 = native (default) 1 = in_depth Signaling format for inner interleaver: native or in-depth (DVB-H only).

Register 0420h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								stream
Type								R

Bit	Name	Function
0	stream	**Hierarchical Stream Status (DVB-T).** 0 = HP (default) 1 = LP Indicates which stream, HP or LP, is decoded when in hierarchical mode. When in non-hierarchical mode, is always HP.

Register 0424h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								cber_rst
Type								R/W

Bit	Name	Function
0	cber_rst	**CBER Reset.** Auto Return register 0 = run (default) 1 = reset Resets CBER and CBER_AVAIL and starts a new computation period.

Register 0428h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0428h cber_bit (LSB)							
Type	R/W							
Name	0429h cber_bit (Middle)							
Type	R/W							
Name	042Ah cber_bit (MSB)							
Type	R/W							

Bit	Name	Function
23:0	cber_bit[23:0]	**CBER Bit Number.** Unsigned Value. Default Value: 0186A0h Sets the number of bits per computation period.

Register 0430h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0430h cber_err (LSB)							
Type	R							
Name	0431h cber_err (Middle)							
Type	R							
Name	0432h cber_err (MSB)							
Type	R							

Bit	Name	Function
23:0	cber_err[23:0]	**CBER Bit Error Number.** Unsigned Value. Provides the number of bit errors after a CBER computation period. After a reset, wait until CBER_AVAIL goes high before reading CBER. CBER = cber_err / cber_bit

Register 0434h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								cber_avail
Type								R

Bit	Name	Function
0	cber_avail	**CBER Available Status.** 0 = unavailable (default) 1 = available When ‘available‘, indicates that CBER_BIT bits are counted since last CBER_RST and that CBER_ERR is available.

Register 0440h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								ps_lock
Type								R

Bit	Name	Function
0	ps_lock	**Packet Synchronization Lock Status.** 0 = unlocked (default) 1 = locked Provides the status of packet synchronization lock mechanism.

Register 0444h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								ps_ambig_out
Type								R

Bit	Name	Function
0	ps_ambig_out	**Packet Synchronization (DVB-C Only): Ambiguity Status.** Unsigned Value. Provides the spectral inversion ambiguity found and applied by packet synchronization once locked. 0 : no spectral inversion 1 : spectral inversion

Register 0448h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								ps_stay_locked
Type								R/W

Bit	Name	Function
0	ps_stay_locked	**Packet Synchronization Stay Locked.** 0 = unstay (default) 1 = stay When ‘stay‘, forces the Packet Synchronization to remain locked once it locks.

Register 044Dh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					ps_sync_thr			
Type					R/W			

Bit	Name	Function
3:0	ps_sync_thr[3:0]	**Packet Synchronization (DVB-C Only): Synchronization Threshold.** Unsigned Value. Default Value: 0000 Sets the number of consecutive correct correlations on SYNC symbol (0x47/0xB8) that the controller has to find to switch from synchronization to supervision state (lock). If the register value is 0, then an internal default value equal to 4 is used, else the register value is applied.

Register 044Eh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ps_superv_thr							
Type	R/W							

Bit	Name	Function
7:0	ps_superv_thr[7:0]	**Packet Synchronization (DVB-C Only): Supervision Threshold.** Unsigned Value. Default Value: 00h Sets the number of consecutive correlations with errors on the SYNC symbol (0x47/0xB8) that the controller has to find to switch from supervision to tracking state (unlock). If the register value is 0, an internal default value equal to 5 is used; else the register value is applied.

Register 044Fh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ps_ambig_thr							
Type	R/W							

Bit	Name	Function
7:0	ps_ambig_thr[7:0]	**Packet Synchronization (DVB-C Only): Ambiguity Threshold.** Unsigned Value. Default Value: 00h Sets the maximum number of SYNC periods (or packet trials) that the controller will test before considering that there is no lock possible with the received data (due to a spectral inversion) and then trying the opposite configuration. If ps_ambig_thr=0, then a default value of 40 packet trials is applied internally, else the value set on ps_ambig_thr is applied.

Register 0450h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							ps_ambig_reg	ps_ambig_mode
Type							R/W	R/W

Bit	Name	Function
0	ps_ambig_mode	**Packet Synchronization (DVB-C Only): Ambiguity Mode.** 0 = manual 1 = auto (default) Defines whether the control of spectral inversion ambiguity comes from packet synchronization (automatic) or is programmed (manual). When ‘manual‘, ambiguity control output is the copy of register ‘ps_ambig_reg‘.
1	ps_ambig_reg	**Packet Synchronization (DVB-C Only): Ambiguity Register.** Unsigned Value. Default Value: 0 Ambiguity value for manual mode. Value applied on the ambiguity control output when ps_ambig_mode = manual. 0 : no spectral inversion 1 : spectral inversion

Register 0461h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								rs_bypass
Type								R/W

Bit	Name	Function
0	rs_bypass	**RS Decoder Bypass.** 0 = not_bypassed (default) 1 = bypassed

Register 0464h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								uncor_rst
Type								R/W

Bit	Name	Function
0	uncor_rst	**UNCOR Counter Reset.** Auto Return register 0 = run (default) 1 = reset Resets UNCOR_CNT and starts a new period of time to count occurrences of uncorrectable packets.

Register 0468h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	uncor_cnt							
Type	R							

Bit	Name	Function
7:0	uncor_cnt[7:0]	**UNCOR Counter Number.** Unsigned Value. Provides the number of uncorrectable packets counted since the last UNCOR reset. This number saturates to 255 in case of too many uncorrectable packets went through the Decoder.

Register 046Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								ber_rst
Type								R/W

Bit	Name	Function
0	ber_rst	**BER Reset.** Auto Return register 0 = run (default) 1 = reset Resets BER_BIT, BER_AVAIL and starts a new computation period.

Register 0470h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0470h ber_pkt (LSB)							
Type	R/W							
Name	0471h ber_pkt (MSB)							
Type	R/W							

Bit	Name	Function
15:0	ber_pkt[15:0]	**BER Packet Number.** Unsigned Value. Default Value: FFFFh Sets the number of RS packets per BER computation period.

Register 0478h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0478h ber_bit (LSB)							
Type	R							
Name	0479h ber_bit (Middle)							
Type	R							
Name	047Ah ber_bit (MSB)							
Type	R							

Bit	Name	Function
23:0	ber_bit[23:0]	**BER Bit Error Number.** Unsigned Value. Provides the number of bit errors found per BER computation period. After a reset, wait until BER_AVAIL goes high before reading BER_BIT. BER = ber_bit / (ber_pkt x 204 x 8)

Register 047Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								ber_avail
Type								R

Bit	Name	Function
0	ber_avail	**BER Available.** 0 = unavailable (default) 1 = available When available, indicates that BER_PKT packets are counted since the last reset and that BER_BIT can be read.

Register 0480h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								per_rst
Type								R/W

Bit	Name	Function
0	per_rst	**PER Reset.** Auto Return register 0 = run (default) 1 = reset Resets PER_BIT, PER_AVAIL and starts a new computation period.

Register 0484h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0484h per_pkt (LSB)							
Type	R/W							
Name	0485h per_pkt (MSB)							
Type	R/W							

Bit	Name	Function
15:0	per_pkt[15:0]	**PER Packet Number.** Unsigned Value. Default Value: FFFFh Sets the number of RS packets per PER computation period.

Register 048Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	048Ch per (LSB)							
Type	R							
Name	048Dh per (MSB)							
Type	R							

Bit	Name	Function
15:0	per[15:0]	**PER Error Number.** Unsigned Value. Provides the number of packet errors per PER computation period. After a reset, wait until PER_AVAIL goes high before reading PER.

Register 0490h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								per_avail
Type								R

Bit	Name	Function
0	per_avail	**PER Available.** 0 = unavailable (default) 1 = available When high, indicates that PER_PKT packets have been counted since the last reset and that PER is now available.

Register 04C0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								symb_deint_mode
Type								R

Bit	Name	Function
0	symb_deint_mode	**Inner Symbol Deinterleaver Mode (DVB-T).** 0 = native (default) 1 = in_depth Indicates the Inner Symbol Interleaver mode. Automatically set with the TPS info when automatic_synchro register is on.

Register 04D0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								desc_enable
Type								R/W

Bit	Name	Function
0	desc_enable	**Descrambler Enable.** 0 = disabled 1 = enabled (default)

Register 04E0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								fec_lock
Type								R

Bit	Name	Function
0	fec_lock	**FEC Lock Status.** 0 = unlocked (default) 1 = locked Indicates whether the complete FEC is locked or not. When locked, the Transport Stream carries valid TS packets.

Register 04E4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			ts_before_lock	ts_tei	ts_data_sync_overwr	ts_data_parity	ts_data_dir	ts_data_mode
Type			R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
0	ts_data_mode	**Transport Stream Data Mode.** 0 = serial 1 = parallel (default) Sets Data output mode. When ‘serial‘, the data is provided on pin TS_DATA[0].
1	ts_data_dir	**Transport Stream Data Bit Direction.** 0 = msb_first (default) 1 = lsb_first In parallel mode, the byte is provided unchanged (when msb first) or bit-swapped (when lsb_first) on ‘ts_data‘ byte output. In serial mode, the byte is provided either MSB or LSB first on ‘ts_data(0)‘ bit output.
2	ts_data_parity	**Transport Stream Data Parity.** 0 = enabled (default) 1 = disabled When ‘enabled‘, the parity bytes (or bits) are provided. When ‘disabled‘, the parity is forced to 0‘s.
3	ts_data_sync_overwr	**Transport Stream Synchronization Byte Overwrite.** 0 = enabled (default) 1 = disabled When ‘enabled‘, all Sync bytes received are replaced by 0x47. When ‘disabled‘, they are left unchanged.
4	ts_tei	**Transport Stream Error Indicator.** 0 = enabled (default) 1 = disabled When ‘enabled‘, the MSB of the second byte of each uncorrectable packet is forced to 1. When ‘disabled‘, the MSB of the second byte is always left unchanged.
5	ts_before_lock	**Transport Stream Mode Before Lock.** 0 = active 1 = quiet (default) When ‘quiet‘, the Transport Stream is made quiet until FEC locks or when it unlocks, which means data are forced to 0‘s and signalization (TS_SYNC, TS_VAL) is forced to the inactive state. Nevertheless the clock remains always active. When ‘active‘, the Transport Stream is provided as it is.

Register 04E5h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						ts_clk_duty_cycle	ts_clk_mode	ts_clk_edge
Type						R/W	R/W	R/W

Bit	Name	Function
0	ts_clk_edge	**Transport Stream Clock Edge.** 0 = rising 1 = falling (default) When ‘rising‘, Data are provided on the rising edge of clock ‘ts_clk‘. When ‘falling‘, on the falling edge.
1	ts_clk_mode	**Transport Stream Clock Mode.** 0 = gapped 1 = continuous (default) Sets clock mode. When ‘continuous‘, the clock runs without regard to data bytes (or bits) being output and the signal TS_VAL must be used as a strobe. When ‘gapped‘, the clock is only active during payload bytes (in parallel mode), or during payload bits (in serial mode when ts_data_parity=DISABLED) or during payload plus redundancy bits (in serial mode when ts_data_parity=ENABLED).
2	ts_clk_duty_cycle	**Reserved.** Unsigned Value. Default Value: 0 Must be set to 0.

Register 04E6h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					ts_err_pola	ts_val_pola	ts_sync_pola	ts_sync_length
Type					R/W	R/W	R/W	R/W

Bit	Name	Function
0	ts_sync_length	**Transport Stream Sync Signal Length.** 0 = first_byte (default) 1 = first_bit Sets Sync byte signalization mode (serial mode only). When ‘first_byte‘, the TS_SYNC signal is active during the whole byte. When ‘first_bit‘ the TS_SYNC signal is active during the first bit provided (MSB or LSB of Sync byte depending on ‘ts_data_dir‘).
1	ts_sync_pola	**Transport Stream Sync Signal Polarity.** 0 = active_high (default) 1 = active_low Sets TS_SYNC signal polarity.
2	ts_val_pola	**Transport Stream Data Valid Signal Polarity.** 0 = active_high (default) 1 = active_low Sets TS_VAL signal polarity.
3	ts_err_pola	**Transport Stream Error Signal Polarity.** 0 = active_high (default) 1 = active_low Sets TS_ERR signal polarity.

Register 04E9h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						ts_mux		
Type						R/W		

Bit	Name	Function
2:0	ts_mux[2:0]	**TS Pins Configuration.** 000 = ts (default) 001 = gpif Controls TS output configuration, either standard or GPIF modes.

Register 04EBh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				sel_gpio_ ts_data4	sel_gpio_ ts_data3	sel_gpio_ ts_data2	sel_gpio_ ts_data1	sel_gpio_ ts_err
Type				R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
0	sel_gpio_ts_err	**TS_ERR / GPIO Selection.** 0 = ts_err (default) 1 = gpio_2 Configure TS_ERR pin to be either TS error flag or GPIO_2 function.
1	sel_gpio_ts_data1	**TS_DATA1 / GPIO Selection.** 0 = ts_data (default) 1 = gpio_1 Configure TS_DATA[1] pin to be either ts_data bit or GPIO_1 function.
2	sel_gpio_ts_data2	**TS_DATA2 / GPIO Selection.** 0 = ts_data (default) 1 = gpio_3 Configure TS_DATA[2] pin to be either ts_data bit or GPIO_3 function.
3	sel_gpio_ts_data3	**TS_DATA3 / GPIO Selection.** 0 = ts_data (default) 1 = gpio_4 Configure TS_DATA[3] pin to be either ts_data bit or GPIO_4 function.
4	sel_gpio_ts_data4	**TS_DATA4 / GPIO Selection.** 0 = ts_data (default) 1 = gpio_5 Configure TS_DATA[4] pin to be either ts_data bit or GPIO_5 function.

Register 04EFh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ts_data7_tri	ts_data6_tri	ts_data5_tri	ts_data4_tri	ts_data3_tri	ts_data2_tri	ts_data1_tri	ts_data0_tri
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
0	ts_data0_tri	**Tristate Control Of TS_DATA[0] Pin.** 0 = normal 1 = tristate (default)
1	ts_data1_tri	**Tristate Control Of TS_DATA[1] Pin.** 0 = normal 1 = tristate (default)
2	ts_data2_tri	**Tristate Control Of TS_DATA[2] Pin.** 0 = normal 1 = tristate (default)
3	ts_data3_tri	**Tristate Control Of TS_DATA[3] Pin.** 0 = normal 1 = tristate (default)
4	ts_data4_tri	**Tristate Control Of TS_DATA[4] Pin.** 0 = normal 1 = tristate (default)
5	ts_data5_tri	**Tristate Control Of TS_DATA[5] Pin.** 0 = normal 1 = tristate (default)
6	ts_data6_tri	**Tristate Control Of TS_DATA[6] Pin.** 0 = normal 1 = tristate (default)
7	ts_data7_tri	**Tristate Control Of TS_DATA[7] Pin.** 0 = normal 1 = tristate (default)

Register 04F0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					ts_clk_tri	ts_err_tri	ts_sync_tri	ts_val_tri
Type					R/W	R/W	R/W	R/W

Bit	Name	Function
0	ts_val_tri	**Tristate Control Of TS_VAL Pin.** 0 = normal 1 = tristate (default)
1	ts_sync_tri	**Tristate Control Of TS_SYNC Pin.** 0 = normal 1 = tristate (default)
2	ts_err_tri	**Tristate Control Of TS_ERR Pin.** 0 = normal 1 = tristate (default)
3	ts_clk_tri	**Tristate Control Of TS_CLK Pin.** 0 = normal 1 = tristate (default)

Register 04F4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ts_data3_slr		ts_data2_slr		ts_data1_slr		ts_data0_slr	
Type	R/W		R/W		R/W		R/W	

Bit	Name	Function
1:0	ts_data0_slr[1:0]	**Slew Rate Configuration Of TS_DATA[0] Pin.** 00 = fastes_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges
3:2	ts_data1_slr[1:0]	**Slew Rate Configuration Of TS_DATA[1] Pin.** 00 = fastest_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges
5:4	ts_data2_slr[1:0]	**Slew Rate Configuration Of TS_DATA[2] Pin.** 00 = fastest_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges
7:6	ts_data3_slr[1:0]	**Slew Rate Configuration Of TS_DATA[3] Pin.** 00 = fastest_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges

Register 04F5h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ts_data7_slr		ts_data6_slr		ts_data5_slr		ts_data4_slr	
Type	R/W		R/W		R/W		R/W	

Bit	Name	Function
1:0	ts_data4_slr[1:0]	**Slew Rate Configuration Of TS_DATA[4] Pin.** 00 = fastest_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges
3:2	ts_data5_slr[1:0]	**Slew Rate Configuration Of TS_DATA[5] Pin.** 00 = fastest_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges Slew rate configuration of TS_DATA[5] pin.
5:4	ts_data6_slr[1:0]	**Slew Rate Configuration Of TS_DATA[6] Pin.** 00 = fastest_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges
7:6	ts_data7_slr[1:0]	**Slew Rate Configuration Of TS_DATA[7] Pin.** 00 = fastest_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges

Register 04F6h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ts_clk_slr		ts_err_slr		ts_sync_slr		ts_val_slr	
Type	R/W		R/W		R/W		R/W	

Bit	Name	Function
1:0	ts_val_slr[1:0]	**Slew Rate Configuration Of TS_VAL Pin.** 00 = fastest_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges
3:2	ts_sync_slr[1:0]	**Slew Rate Configuration Of TS_SYNC Pin.** 00 = fastest_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges
5:4	ts_err_slr[1:0]	**Slew Rate Configuration Of TS_ERR Pin.** 00 = fastest_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges
7:6	ts_clk_slr[1:0]	**Slew Rate Configuration Of TS_CLK Pin.** 00 = fastest_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges

Register 0500h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						gpif_standby	gpif_ram_overflow	gpif_in_fifo_overflow
Type						R/W	R	R

Bit	Name	Function
0	gpif_in_fifo_overflow	**GPIF Input FIFO Overflow.** 0 = none (default) 1 = overflow
1	gpif_ram_overflow	**GPIF RAM Overflow.** 0 = none (default) 1 = overflow
2	gpif_standby	**GPIF Standby.** 0 = run 1 = standby (default)

Register 0504h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								gpif_alarm_reset
Type								R/W

Bit	Name	Function
0	gpif_alarm_reset	**GPIF Alarm Reset.** Auto Return register 0 = run (default) 1 = reset GPIF reset for the FIFO and RAM overflow alarms.

Register 0510h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							pid_p	pid_filter_en
Type							R/W	R/W

Bit	Name	Function
0	pid_filter_en	**PID Filter Enable.** 0 = bypass (default) 1 = on
1	pid_p	**PID Filtering Mode.** 0 = negative (default) 1 = positive When positive, if a PID in the stream matches the programmed PID, then it is sent to the output. When negative, if a PID in the stream matches, then it is not sent to the output.

Register 0514h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	pid_en_7	pid_en_6	pid_en_5	pid_en_4	pid_en_3	pid_en_2	pid_en_1	pid_en_0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
0	pid_en_0	**PID Filtering Status On Branch 0.** 0 = off (default) 1 = enable
1	pid_en_1	**PID Filtering Status On Branch 1.** 0 = off (default) 1 = enable
2	pid_en_2	**PID Filtering Status On Branch 2.** 0 = off (default) 1 = enable
3	pid_en_3	**PID Filtering Status On Branch 3.** 0 = off (default) 1 = enable
4	pid_en_4	**PID Filtering Status On Branch 4.** 0 = off (default) 1 = enable
5	pid_en_5	**PID Filtering Status On Branch 5.** 0 = off (default) 1 = enable
6	pid_en_6	**PID Filtering Status On Branch 6.** 0 = off (default) 1 = enable
7	pid_en_7	**PID Filtering Status On Branch 7.** 0 = off (default) 1 = enable

Register 0515h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	pid_en_15	pid_en_14	pid_en_13	pid_en_12	pid_en_11	pid_en_10	pid_en_9	pid_en_8
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
0	pid_en_8	**PID Filtering Status On Branch 8.** 0 = off (default) 1 = enable
1	pid_en_9	**PID Filtering Status On Branch 9.** 0 = off (default) 1 = enable
2	pid_en_10	**PID Filtering Status On Branch 10.** 0 = off (default) 1 = enable
3	pid_en_11	**PID Filtering Status On Branch 11.** 0 = off (default) 1 = enable
4	pid_en_12	**PID Filtering Status On Branch 12.** 0 = off (default) 1 = enable
5	pid_en_13	**PID Filtering Status On Branch 13.** 0 = off (default) 1 = enable
6	pid_en_14	**PID Filtering Status On Branch 14.** 0 = off (default) 1 = enable
7	pid_en_15	**PID Filtering Status On Branch 15.** 0 = off (default) 1 = enable

Register 0516h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	pid_en_23	pid_en_22	pid_en_21	pid_en_20	pid_en_19	pid_en_18	pid_en_17	pid_en_16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
0	pid_en_16	**PID Filtering Status On Branch 16.** 0 = off (default) 1 = enable
1	pid_en_17	**PID Filtering Status On Branch 17.** 0 = off (default) 1 = enable
2	pid_en_18	**PID Filtering Status On Branch 18.** 0 = off (default) 1 = enable
3	pid_en_19	**PID Filtering Status On Branch 19.** 0 = off (default) 1 = enable
4	pid_en_20	**PID Filtering Status On Branch 20.** 0 = off (default) 1 = enable
5	pid_en_21	**PID Filtering Status On Branch 21.** 0 = off (default) 1 = enable
6	pid_en_22	**PID Filtering Status On Branch 22.** 0 = off (default) 1 = enable
7	pid_en_23	**PID Filtering Status On Branch 23.** 0 = off (default) 1 = enable

Register 0517h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	pid_en_31	pid_en_30	pid_en_29	pid_en_28	pid_en_27	pid_en_26	pid_en_25	pid_en_24
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
0	pid_en_24	**PID Filtering Status On Branch 24.** 0 = off (default) 1 = enable
1	pid_en_25	**PID Filtering Status On Branch 25.** 0 = off (default) 1 = enable
2	pid_en_26	**PID Filtering Status On Branch 26.** 0 = off (default) 1 = enable
3	pid_en_27	**PID Filtering Status On Branch 27.** 0 = off (default) 1 = enable
4	pid_en_28	**PID Filtering Status On Branch 28.** 0 = off (default) 1 = enable
5	pid_en_29	**PID Filtering Status On Branch 29.** 0 = off (default) 1 = enable
6	pid_en_30	**PID Filtering Status On Branch 30.** 0 = off (default) 1 = enable
7	pid_en_31	**PID Filtering Status On Branch 31.** 0 = off (default) 1 = enable

Register 0518h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0518h pid_0 (LSB)							
Type	R/W							
Name				0519h pid_0 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_0[12:0]	**PID Number On Branch 0.** Unsigned Value. Default Value: 0000h

Register 051Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	051Ch pid_1 (LSB)							
Type	R/W							
Name				051Dh pid_1 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_1[12:0]	**PID Number On Branch 1.** Unsigned Value. Default Value: 0000h

Register 0520h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0520h pid_2 (LSB)							
Type	R/W							
Name				0521h pid_2 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_2[12:0]	**PID Number On Branch 2.** Unsigned Value. Default Value: 0000h

Register 0524h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0524h pid_3 (LSB)							
Type	R/W							
Name				0525h pid_3 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_3[12:0]	**PID Number On Branch 3.** Unsigned Value. Default Value: 0000h

Register 0528h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0528h pid_4 (LSB)							
Type	R/W							
Name				0529h pid_4 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_4[12:0]	**PID Number On Branch 4.** Unsigned Value. Default Value: 0000h

Register 052Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	052Ch pid_5 (LSB)							
Type	R/W							
Name				052Dh pid_5 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_5[12:0]	**PID Number On Branch 5.** Unsigned Value. Default Value: 0000h

Register 0530h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0530h pid_6 (LSB)							
Type	R/W							
Name				0531h pid_6 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_6[12:0]	**PID Number On Branch 6.** Unsigned Value. Default Value: 0000h

Register 0534h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0534h pid_7 (LSB)							
Type	R/W							
Name				0535h pid_7 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_7[12:0]	**PID Number On Branch 7.** Unsigned Value. Default Value: 0000h

Register 0538h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0538h pid_8 (LSB)							
Type	R/W							
Name				0539h pid_8 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_8[12:0]	**PID Number On Branch 8.** Unsigned Value. Default Value: 0000h

Register 053Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	053Ch pid_9 (LSB)							
Type	R/W							
Name				053Dh pid_9 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_9[12:0]	**PID Number On Branch 9.** Unsigned Value. Default Value: 0000h

Register 0540h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0540h pid_10 (LSB)							
Type	R/W							
Name				0541h pid_10 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_10[12:0]	**PID Number On Branch 10.** Unsigned Value. Default Value: 0000h

Register 0544h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0544h pid_11 (LSB)							
Type	R/W							
Name				0545h pid_11 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_11[12:0]	**PID Number On Branch 11.** Unsigned Value. Default Value: 0000h

Register 0548h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0548h pid_12 (LSB)							
Type	R/W							
Name				0549h pid_12 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_12[12:0]	**PID Number On Branch 12.** Unsigned Value. Default Value: 0000h

Register 054Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	054Ch pid_13 (LSB)							
Type	R/W							
Name				054Dh pid_13 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_13[12:0]	**PID Number On Branch 13.** Unsigned Value. Default Value: 0000h

Register 0550h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0550h pid_14 (LSB)							
Type	R/W							
Name				0551h pid_14 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_14[12:0]	**PID Number On Branch 14.** Unsigned Value. Default Value: 0000h

Register 0554h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0554h pid_15 (LSB)							
Type	R/W							
Name				0555h pid_15 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_15[12:0]	**PID Number On Branch 15.** Unsigned Value. Default Value: 0000h

Register 0558h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0558h pid_16 (LSB)							
Type	R/W							
Name				0559h pid_16 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_16[12:0]	**PID Number On Branch 16.** Unsigned Value. Default Value: 0000h

Register 055Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	055Ch pid_17 (LSB)							
Type	R/W							
Name				055Dh pid_17 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_17[12:0]	**PID Number On Branch 17.** Unsigned Value. Default Value: 0000h

Register 0560h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0560h pid_18 (LSB)							
Type	R/W							
Name				0561h pid_18 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_18[12:0]	**PID Number On Branch 18.** Unsigned Value. Default Value: 0000h

Register 0564h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0564h pid_19 (LSB)							
Type	R/W							
Name				0565h pid_19 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_19[12:0]	**PID Number On Branch 19.** Unsigned Value. Default Value: 0000h

Register 0568h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0568h pid_20 (LSB)							
Type	R/W							
Name				0569h pid_20 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_20[12:0]	**PID Number On Branch 20.** Unsigned Value. Default Value: 0000h

Register 056Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	056Ch pid_21 (LSB)							
Type	R/W							
Name				056Dh pid_21 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_21[12:0]	**PID Number On Branch 21.** Unsigned Value. Default Value: 0000h

Register 0570h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0570h pid_22 (LSB)							
Type	R/W							
Name				0571h pid_22 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_22[12:0]	**PID Number On Branch 22.** Unsigned Value. Default Value: 0000h

Register 0574h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0574h pid_23 (LSB)							
Type	R/W							
Name				0575h pid_23 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_23[12:0]	**PID Number On Branch 23.** Unsigned Value. Default Value: 0000h

Register 0578h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0578h pid_24 (LSB)							
Type	R/W							
Name				0579h pid_24 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_24[12:0]	**PID Number On Branch 24.** Unsigned Value. Default Value: 0000h

Register 057Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	057Ch pid_25 (LSB)							
Type	R/W							
Name				057Dh pid_25 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_25[12:0]	**PID Number On Branch 25.** Unsigned Value. Default Value: 0000h

Register 0580h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0580h pid_26 (LSB)							
Type	R/W							
Name				0581h pid_26 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_26[12:0]	**PID Number On Branch 26.** Unsigned Value. Default Value: 0000h

Register 0584h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0584h pid_27 (LSB)							
Type	R/W							
Name				0585h pid_27 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_27[12:0]	**PID Number On Branch 27.** Unsigned Value. Default Value: 0000h

Register 0588h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0588h pid_28 (LSB)							
Type	R/W							
Name				0589h pid_28 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_28[12:0]	**PID Number On Branch 28.** Unsigned Value. Default Value: 0000h

Register 058Ch.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	058Ch pid_29 (LSB)							
Type	R/W							
Name				058Dh pid_29 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_29[12:0]	**PID Number On Branch 29.** Unsigned Value. Default Value: 0000h

Register 0590h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0590h pid_30 (LSB)							
Type	R/W							
Name				0591h pid_30 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_30[12:0]	**PID Number On Branch 30.** Unsigned Value. Default Value: 0000h

Register 0594h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0594h pid_31 (LSB)							
Type	R/W							
Name				0595h pid_31 (MSB)				
Type	R/W							

Bit	Name	Function
12:0	pid_31[12:0]	**PID Number On Branch 31.** Unsigned Value. Default Value: 0000h

Register 05B0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	gp0_deltasigma							
Type	R/W							

Bit	Name	Function
7:0	gp0_deltasigma[7:0]	**Delta/sigma Reference Value For GPIO_0.** Unsigned Value. Default Value: 00h

Register 05B1h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			gp0_o	gp0_en	gp0_t	gp0_p	gp0_sel	
Type			R/W	R/W	R/W	R/W	R/W	

Bit	Name	Function
1:0	gp0_sel[1:0]	**GPIO_0 Mode Selection.** 00 = gp_o (default) 01 = interrupt 10 = deltasigma 11 = clock
2	gp0_p	**GPIO_0 Polarity Inversion.** 0 = non_inverted (default) 1 = inverted
3	gp0_t	**GPIO_0 Output Type.** 0 = CMOS (default) 1 = Open_drain
4	gp0_en	**GPIO_0 Enable.** 0 = disable (default) 1 = enable
5	gp0_o	**GPIO_0 Output Control.** 0 = low (default) 1 = high Sets the value of GPIO_0 output when gp0_sel = gp_o

Register 05B4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								gp0_i
Type								R

Bit	Name	Function
0	gp0_i	**GPIO_0 Input Value.** 0 = low (default) 1 = high

Register 05B6h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								fecl0_e
Type								R/W

Bit	Name	Function
0	fecl0_e	**FEC Lock Interrupt Enable On GPIO_0.** 0 = disable (default) 1 = enable

Register 05BAh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								fecl0_i
Type								R

Bit	Name	Function
0	fecl0_i	**FEC Lock Interrupt Status On GPIO_0.** 0 = unlocked (default) 1 = locked

Register 05BCh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								rst_interrupt_gp0
Type								R/W

Bit	Name	Function
0	rst_interrupt_gp0	**Interrupts Reset For GPIO_0.** Auto Return register 0 = run (default) 1 = reset

Register 05C1h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								gpio0_tri
Type								R/W

Bit	Name	Function
0	gpio0_tri	**Tristate Control Of GPIO_0 Pin.** 0 = normal 1 = tristate (default)

Register 05CAh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							gpio0_slr	
Type	R/W							

Bit	Name	Function
1:0	gpio0_slr[1:0]	**Slew Rate Control Of GPIO_0 Pin.** 00 = fastest_edges (default) 01 = slowest_edges 10 = moderate_edges 11 = fast_edges

Register 05D0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	gp1_deltasigma							
Type	R/W							

Bit	Name	Function
7:0	gp1_deltasigma[7:0]	**Delta/sigma Reference Value For GPIO_1.** Unsigned Value. Default Value: 00h

Register 05D1h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			gp1_o	gp1_en	gp1_t	gp1_p	gp1_sel	
Type			R/W	R/W	R/W	R/W	R/W	

Bit	Name	Function
1:0	gp1_sel[1:0]	**GPIO_1 Mode Selection.** 00 = gp_o (default) 01 = interrupt 10 = deltasigma 11 = clock
2	gp1_p	**GPIO_1 Polarity Inversion.** 0 = non_inverted (default) 1 = inverted
3	gp1_t	**GPIO_1 Output Type.** 0 = CMOS (default) 1 = Open_drain
4	gp1_en	**GPIO_1 Enable.** 0 = disable (default) 1 = enable
5	gp1_o	**GPIO_1 Output Control.** 0 = low (default) 1 = high Sets the value of GPIO_1 output when gp1_sel = gp_o

Register 05D4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								gp1_i
Type								R

Bit	Name	Function
0	gp1_i	**GPIO_1 Input Value.** 0 = low (default) 1 = high

Register 05D6h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								fecl1_e
Type								R/W

Bit	Name	Function
0	fecl1_e	**FEC Lock Interrupt Enable On GPIO_1.** 0 = disable (default) 1 = enable

Register 05DAh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								fecl1_i
Type								R

Bit	Name	Function
0	fecl1_i	**FEC Lock Interrupt Status On GPIO_1.** 0 = unlocked (default) 1 = locked

Register 05DCh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								rst_interrupt_gp1
Type								R/W

Bit	Name	Function
0	rst_interrupt_gp1	**Interrupts Reset For GPIO_1.** Auto Return register 0 = run (default) 1 = reset

Register 05F0h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	gp2_deltasigma							
Type	R/W							

Bit	Name	Function
7:0	gp2_deltasigma[7:0]	**Delta/sigma Reference Value For GPIO_2.** Unsigned Value. Default Value: 00h

Register 05F1h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			gp2_o	gp2_en	gp2_t	gp2_p	gp2_sel	
Type			R/W	R/W	R/W	R/W	R/W	

Bit	Name	Function
1:0	gp2_sel[1:0]	**GPIO_2 Mode Selection.** 00 = gp_o (default) 01 = interrupt 10 = deltasigma 11 = clock
2	gp2_p	**GPIO_2 Polarity Inversion.** 0 = non_inverted (default) 1 = inverted
3	gp2_t	**GPIO_2 Output Type.** 0 = CMOS (default) 1 = Open_drain
4	gp2_en	**GPIO_2 Enable.** 0 = disable (default) 1 = enable
5	gp2_o	**GPIO_2 Output Control.** 0 = low (default) 1 = high Sets the value of GPIO_2 output when gp2_sel = gp_o

Register 05F4h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								gp2_i
Type								R

Bit	Name	Function
0	gp2_i	**GPIO_2 Input Value.** 0 = low (default) 1 = high Level of the GPIO_2 pin. GPIO_2 must be configured in tri-state when it is used as an input.

Register 05F6h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								fecl2_e
Type								R/W

Bit	Name	Function
0	fecl2_e	**FEC Lock Interrupt Enable On GPIO_2.** 0 = disable (default) 1 = enable

Register 05FAh.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								fecl2_i
Type								R

Bit	Name	Function
0	fecl2_i	**FEC Lock Interrupt Status On GPIO_2.** 0 = unlocked (default) 1 = locked

Register 0600h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								rst_interrupt_gp2
Type								R/W

Bit	Name	Function
0	rst_interrupt_gp2	**Interrupts Reset For GPIO_2.** Auto Return register 0 = run (default) 1 = reset

Register 0610h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					gp3_o	gp3_en	gp3_t	gp3_p
Type					R/W	R/W	R/W	R/W

Bit	Name	Function
0	gp3_p	**GPIO_3 Polarity Inversion.** 0 = non_inverted (default) 1 = inverted
1	gp3_t	**GPIO_3 Output Type.** 0 = CMOS (default) 1 = Open_drain
2	gp3_en	**GPIO_3 Enable.** 0 = disable (default) 1 = enable
3	gp3_o	**GPIO_3 Output Control.** 0 = low (default) 1 = high Sets the value of GPIO_3 output when enabled.

Register 0614h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								gp3_i
Type								R

Bit	Name	Function
0	gp3_i	**GPIO_3 Input Value.** 0 = low (default) 1 = high

Register 0621h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					gp4_o	gp4_en	gp4_t	gp4_p
Type					R/W	R/W	R/W	R/W

Bit	Name	Function
0	gp4_p	**GPIO_4 Polarity Inversion.** 0 = non_inverted (default) 1 = inverted
1	gp4_t	**GPIO_4 Output Type.** 0 = CMOS (default) 1 = Open_drain
2	gp4_en	**GPIO_4 Enable.** 0 = disable (default) 1 = enable
3	gp4_o	**GPIO_4 Output Control.** 0 = low (default) 1 = high Sets the value of GPIO_4 output when enabled.

Register 0625h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								gp4_i
Type								R

Bit	Name	Function
0	gp4_i	**GPIO_4 Input Value.** 0 = low (default) 1 = high

Register 0632h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					gp5_o	gp5_en	gp5_t	gp5_p
Type					R/W	R/W	R/W	R/W

Bit	Name	Function
0	gp5_p	**GPIO_5 Polarity Inversion.** 0 = non_inverted (default) 1 = inverted
1	gp5_t	**GPIO_5 Output Type.** 0 = CMOS (default) 1 = Open_drain General Purpose pin type.
2	gp5_en	**GPIO_5 Enable.** 0 = disable (default) 1 = enable
3	gp5_o	**GPIO_5 Output Control.** 0 = low (default) 1 = high Sets the value of GPIO_5 output when enabled.

Register 0636h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								gp5_i
Type								R

Bit	Name	Function
0	gp5_i	**GPIO_5 Input Value.** 0 = low (default) 1 = high

Register 0641h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		rssi_update_time					start_rssi	en_rssi
Type	R/W						R/W	R/W

Bit	Name	Function
0	en_rssi	**RSSI Enable.** 0 = off (default) 1 = on
1	start_rssi	**Start RSSI.** Unsigned Value. Default Value: 0 Must be set to 1 to start RSSI feature. (Automatically set to 1 after DSP boot)
6:2	rssi_update_time[4:0]	**SAR Algorithm Update Frequency.** Unsigned Value. Default Value: 00h Update frequency = sys_clk / $2^{rssi\_update\_time+5}$

Register 0642h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	rssi							
Type	R							

Bit	Name	Function
7:0	rssi[7:0]	**RSSI Value.** Unsigned Value. RSSI value at the output of the 8-bit ADC.

Register 0646h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							rssi_pad_ctrl	
Type	R/W							

Bit	Name	Function
1:0	rssi_pad_ctrl[1:0]	**RSSI Pad Control.** 00 = adc_in (default) 01 = xtal_out Other = Reserved Selects whether RSSI pin is used as RSSI ADC input (normal mode) or as a reference clock output. This clock output can be use as the reference clock for a second device.

Register 08F8h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						ts_parallel_mode		
Type	R/W							

Bit	Name	Function
2:0	ts_parallel_mode [2:0]	**Selection of TS Parallel Mode.** 000 = mode1 (default) 100 = mode2_div6 101 = mode2_div8 110 = mode2_div12 111 = mode2_div16 Other = Reserved Selects between TS parallel mode1 and mode2. In mode1, the TS clock is not regular and its average frequency is adapted to the received data rate. In mode2, the TS clock is a fixed division of the system clock. (When “mode2_divN” is selected, TS_CLK is equal to sys_clk/N).

12. Pin Descriptions

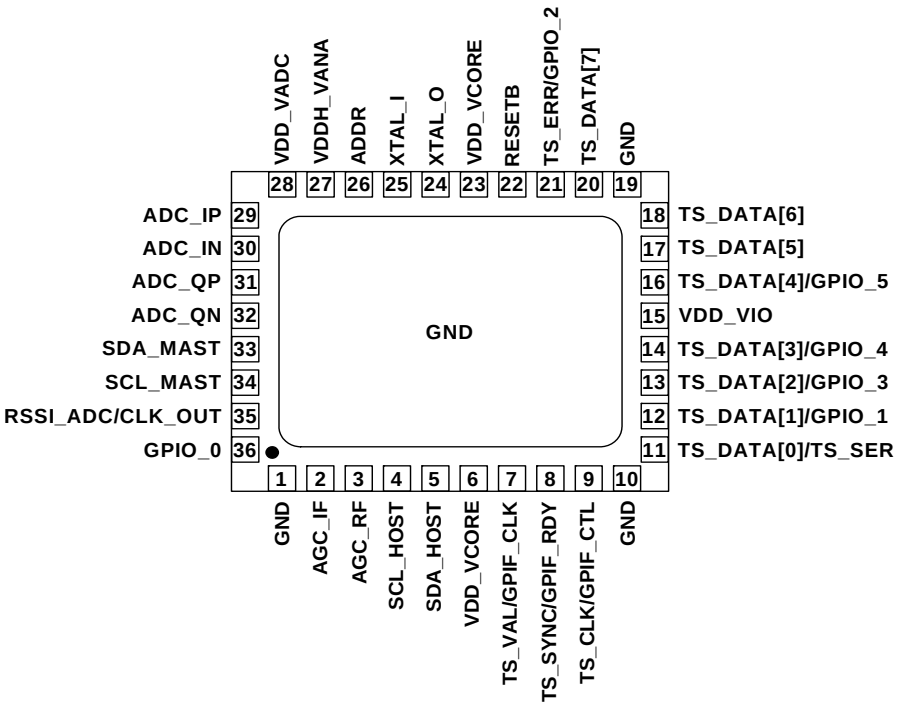

Table 19. Si2165 Pin Descriptions

Pin #	Pin Name	I/O	Description	V max
29	ADC_IP	I	12-bit ADC input (differential +) for IF or I in ZIF mode	1.2
30	ADC_IN	I	12-bit ADC input (differential –) for IF or I in ZIF mode	1.2
31	ADC_QP	I	12-bit ADC input (differential +) for Q in ZIF mode	1.2
32	ADC_QN	I	12-bit ADC input (differential –) for Q in ZIF mode	1.2
35	RSSI_ADC/ CLK_OUT	I/O	RSSI level monitoring muxed with reference clock output (or input)	3.3
22	RESETB	I	Hardware RESET (active low)	V_{DD_VIO}
26	ADDR	I	I^2C responding address (4 possible addresses)	4 levels between 0–3.3 V
36	GPIO_0	I/O	Full function GPIO	V_{DD_VIO}
2	AGC_IF	O	Tuner's IF AGC control	V_{DD_VIO}
3	AGC_RF	O	Tuner's RF AGC control	V_{DD_VIO}
24	XTAL_O	O	Crystal pin 2 or grounded	3.3
25	XTAL_I	I	Crystal pin 1 or external clock input	3.3
4	SCL_HOST	I/O	I^2C clock from MPEG decoder	2.5, 3.3, and 5 V tolerant*
5	SDA_HOST	I/O	I^2C data from MPEG decoder	2.5, 3.3, and 5 V tolerant*
***Note:** 5 Volts tolerance is only supported when V_{DD_VIO} = 3.3 V.				

Table 19. Si2165 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Description	V max
33	SDA_MAST	I/O	I^2C data to tuner	2.5, 3.3, and 5 V tolerant*
34	SCL_MAST	I/O	I^2C clock to tuner	2.5, 3.3, and 5 V tolerant*
7	TS_VAL/GPIF_CLK	I/O	TS valid indicator muxed with GPIF clock signal	V_{DD_VIO}
8	TS_SYNC/ GPIF_RDY	O	TS synchronization muxed with GPIF ready signal	V_{DD_VIO}
9	TS_CLK/GPIF_CTL	I/O	TS clock muxed with GPIF control signal	V_{DD_VIO}
11	TS_DATA[0]/TS_SER	O	TS serial output muxed with TS parallel output bit #0	V_{DD_VIO}
12	TS_DATA[1]/GPIO_1	I/O	TS parallel output bit #1 muxed with full function GPIO_1	V_{DD_VIO}
13	TS_DATA[2]/GPIO_3	I/O	TS parallel output bit #2 muxed with logic level GPIO_3	V_{DD_VIO}
14	TS_DATA[3]/GPIO_4	I/O	TS parallel output bit #3 muxed with logic level GPIO_4	V_{DD_VIO}
16	TS_DATA[4]/GPIO_5	O	TS parallel output bit #4 muxed with logic level GPIO_5	V_{DD_VIO}
17	TS_DATA[5]	O	TS parallel output bit #5	V_{DD_VIO}
18	TS_DATA[6]	O	TS parallel output bit #6	V_{DD_VIO}
20	TS_DATA[7]	O	TS parallel output bit #7	V_{DD_VIO}
21	TS_ERR/GPIO_2	I/O	TS error indicator muxed with full function GPIO_2	V_{DD_VIO}
6, 23	VDD_VCORE	S	Core logic digital supply pins	1.2
15	VDD_VIO	S	Pad I/O supply	1.8–3.3
27	VDDH_VANA	S	3.3 V supply	3.3
28	VDD_VADC	S	1.2 V supply	1.2
1	GND	S	Ground connection	0
10	GND	S	Ground connection	0
19	GND	S	Ground connection	0
	Exposed die pad	EDP	Ground connection	0

***Note:** 5 Volts tolerance is only supported when V_{DD_VIO} = 3.3 V.

13. Ordering Guide

Part Number	Description	Temperature	Package
Si2165-D-GM	Multi-Standard DVB-T/C Demodulator	0 to 85 °C	36-pin QFN, RoHS compliant
Si2165-D-GMR	Multi-Standard DVB-T/C Demodulator (tape and reel packing option)	0 to 85 °C	36-pin QFN, RoHS compliant

14. Package Marking

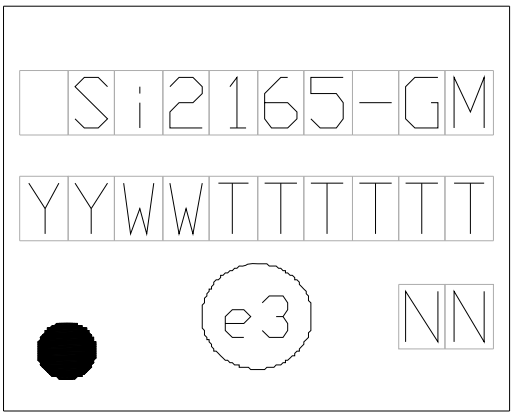

Figure 26. Top Mark

Table 20. Package Marking

Mark Method:	Laser	
Font Size	1.75 point (0.62 mm) Right-justified	
Line 1 Marking	Customer Part Number	**Si2165-GM**
Line 2 Marking	YY = year WW = work week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release.
	TTTTTT = mfg code	Manufacturing code from the Assembly Purchase Order form.
Line 3 Marking	Circle = 0.7 mm diameter Lower left-justified	Pin 1 Identifier
	Circle = 1.3 mm diameter Center-justified	“e3” Pb-free symbol
	NN = Country of origin ISO code abbreviation	Assigned by the Assembly House.

15. Package Outline

Figure 27 and Table 21 illustrate and detail the package dimensions for the Si2165.

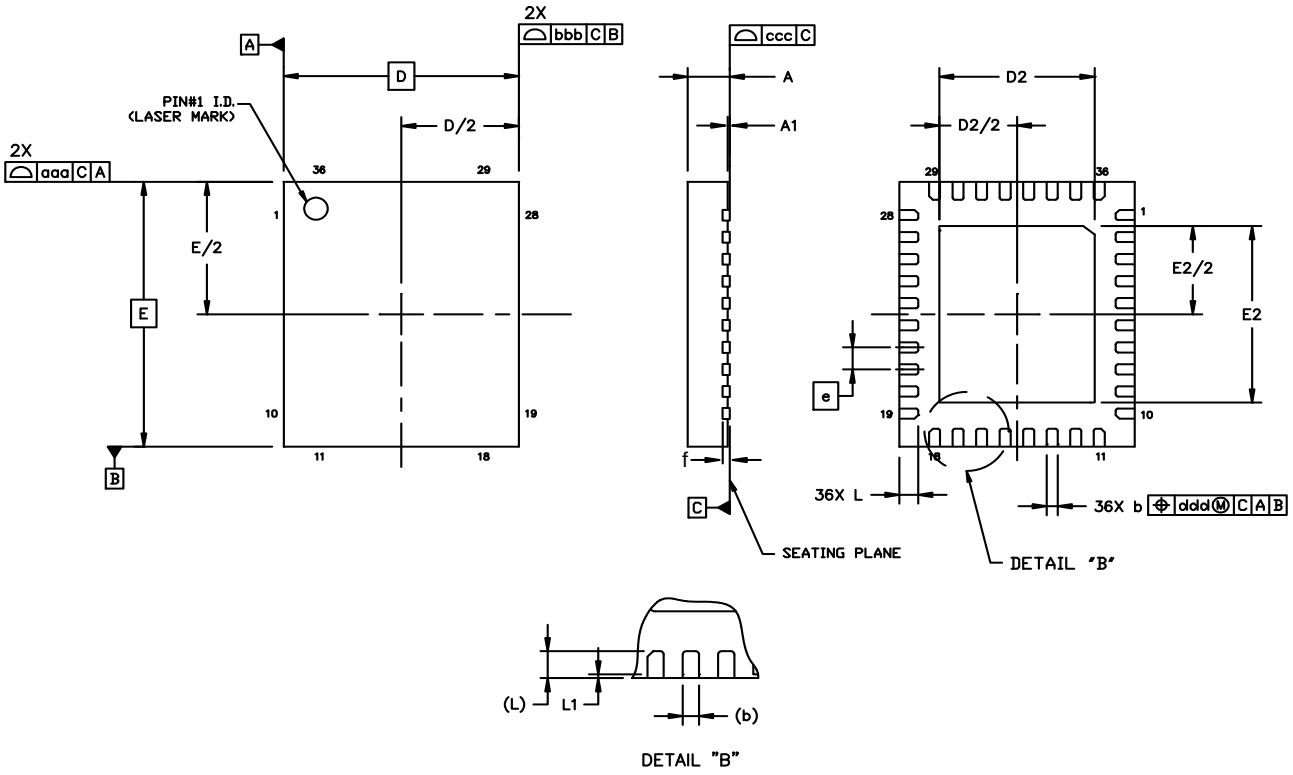

Figure 27. 36-Pin Quad Flat No-Lead (QFN) Package

Table 21. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
D		5.00 BSC.	
D2	3.55	3.60	3.65
e		0.50 BSC.	
E		6.00 BSC.	
E2	4.05	4.10	4.15
f	—	0.203 BSC.	—
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VHJD.

16. PCB Land Pattern

Figure 28 and Table 22 illustrate and detail the printed circuit board land pattern for the selected 36-pin QFN.

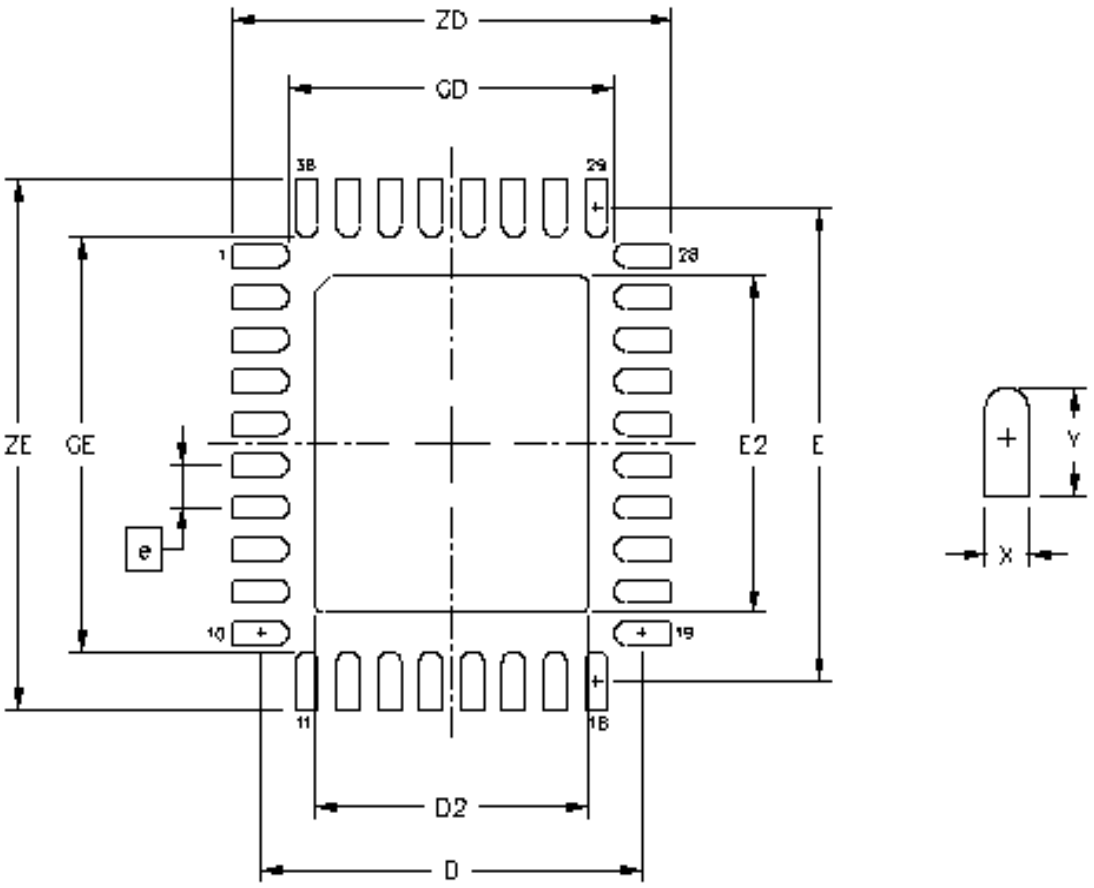

Figure 28. PCB Land Pattern Details for the Si2165 Package

Table 22. PCB Land Pattern Dimensions

Dimension	Min	Max
e	0.50 BSC.	
E	5.62 REF.	
D	4.62 REF.	
E2	4.05	4.15
D2	3.55	3.65
GE	5.2	—
GD	4.2	—
X	—	0.3
Y	0.69 REF.	
ZE	—	6.31
ZD	—	5.31

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder-mask-defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all around the pad.

Stencil Design

6. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 3x4 array of 0.90x0.85 mm rectangular openings on 1.05 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.5 to Revision 1.0

- NorDig Unified 2.0 replacing NorDig 1.0.3 on page 1.
- 7.2MBaud symbol rate replacing 7MBaud on page 1.
- Register req_constellation (02F4h) replacing register constellation (00F8h) on page 21, section 3.6.2.1 and on page 26, section 3.8.2.2.
- New Figure 9, “Initialization Sequence,” on page 26.
- Corrected dsp_clock hexadecimal address in "3.8.4.1. Software Power-down" on page 27.
- New paragraph "4.2.1. TS Master Parallel Modes" on page 29.
- New paragraph "4.5.1. Timings" on page 35.
- Register constellation (00F8h) description and usage changes on page 64.
- Register req_constellation (02F4h) description and usage changes on page 103.
- Addition of register ts_parallel_mode (08F8h) on page 167.
- New package marking drawing on page 170.

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