PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM48754	SOIC-14	-40℃ to +85℃	SGM48754YS14G/TR	SGM48754YS14 XXXXX	Tape and Reel, 2500
	TSSOP-14	-40℃ to +85℃	SGM48754YTS14G/TR	SGM48754 YTS14 XXXXX	Tape and Reel, 4000

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... -0.3V to 6V
Voltage into Any Terminal (1) ..... -0.3V to (V_{CC} + 0.3V)
Continuous Current into Any Terminal ..... ±20mA
Peak Current
(Pulsed at 1ms, 10% duty cycle) ..... ±40mA
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
MM 300V

NOTE:
1. Voltages exceeding V_{CC} or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 2.5V to 5.5V
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

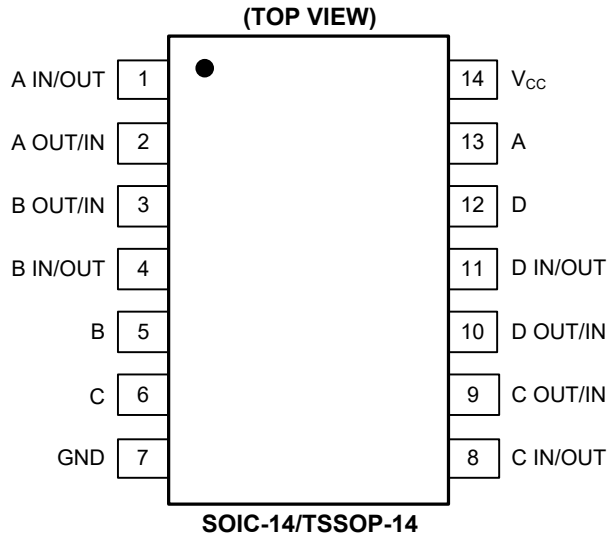
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	A IN/OUT	Switch A Input/Output.
2	A OUT/IN	Switch A Input/Output.
3	B OUT/IN	Switch B Input/Output.
4	B IN/OUT	Switch B Input/Output.
5	B	Switch B Control.
6	C	Switch C Control.
7	GND	Ground.
8	C IN/OUT	Switch C Input/Output.
9	C OUT/IN	Switch C Input/Output.
10	D OUT/IN	Switch D Input/Output.
11	D IN/OUT	Switch D Input/Output.
12	D	Switch D Control.
13	A	Switch A Control.
14	V_{CC}	Power Supply.

FUNCTION TABLE

SELECT INPUTS A/B/C/D	SWITCH STATUS
High	All Switches Close
Low	All Switches Open

NOTE: Input and output pins are identical and interchangeable. Any may be considered an input or output; signals pass equally well in both directions.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, Full = -40℃ to +85℃, x = A, B, C and D switch in/out or out/in, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{X\_}$, V_X		Full	GND		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 5V, I_X = 1mA	+25℃		24	30	Ω
			Full			35	
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 5V, I_X = 1mA	+25℃		1	2.6	Ω
			Full			3	
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{CC} = 5V, I_X = 1mA	+25℃		8	11	Ω
			Full			14	
X_ Off Leakage Current	$I_{X\_(OFF)}$	V_{CC} = 5V, $V_{X\_}$ = 4.5V or 0V, V_X = 4.5V or 0V	+25℃		1	1000	nA
X Off Leakage Current	$I_{X(OFF)}$	V_{CC} = 5V, $V_{X\_}$ = 4.5V or 0V, V_X = 4.5V or 0V	+25℃		1	1000	nA
X On Leakage Current	$I_{X(ON)}$	V_{CC} = 5V, V_X = 4.5V or 0V	+25℃		1	1000	nA
DIGITAL I/O							
Logic Input Logic Threshold High	V_{AH}, V_{BH}, V_{CH},V_{DH}		+25℃	1.7			V
Logic Input Logic Threshold Low	V_{AL}, V_{BL}, $V_{CL,}$ V_{DL}		+25℃			0.5	V
Input-Current High	I_{AH}, I_{BH}, $I_{CH,}$ I_{DH}	V_A, V_B, V_C, V_D = V_{CC}	+25℃		1		nA
Input-Current Low	I_{AL}, I_{BL}, $I_{CL,}$ I_{DL}	V_A, V_B, V_C, V_D = 0V	+25℃		1		nA
DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{X\_}$, $V_{Y\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 1	+25℃		40		ns
Turn-Off Time	t_{OFF}	$V_{X\_}$, $V_{Y\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 1	+25℃		100		ns
Input Transition Rise or Fall Rate	Δt/ΔV		+25℃			20	ns/V
Charge Injection	Q	R_S = 0Ω, C = 1nF, V_S = 0V, Test Circuit 2	+25℃		7		pC
Input Off-Capacitance	$C_{X\_(OFF)}$	$V_{X\_}$ = 0V, f = 1MHz, Test Circuit 3	+25℃		9		pF
Output Off-Capacitance	$C_{X(OFF)}$	$V_{X\_}$ = 0V, f = 1MHz, Test Circuit 3	+25℃		9		pF
Output On-Capacitance	$C_{X(ON)}$	$V_{X\_}$ = 0V, f = 1MHz, Test Circuit 3	+25℃		18		pF
Off Isolation	O_{ISO}	R_L = 50Ω, f = 1MHz, Test Circuit 4	+25℃		-80		dB
Crosstalk	X_{TALK}	f = 1MHz, Test Circuit 4	+25℃		-95		dB
-3dB Bandwidth	BW	R_L = 50Ω	+25℃		180		MHz
Total Harmonic Distortion	THD	R_L = 600Ω, $5V_{P-P}$, f = 20Hz to 20kHz	+25℃		0.35		%
POWER SUPPLY							
Power Supply Range	V_{CC}		Full	2.5		5.5	V
Power Supply Current	I_{CC}	V_{CC} = 5V, V_A, V_B, V_C, V_D = V_{CC} or 0	+25℃		0.001	6	μA

ELECTRICAL CHARACTERISTICS (continued)

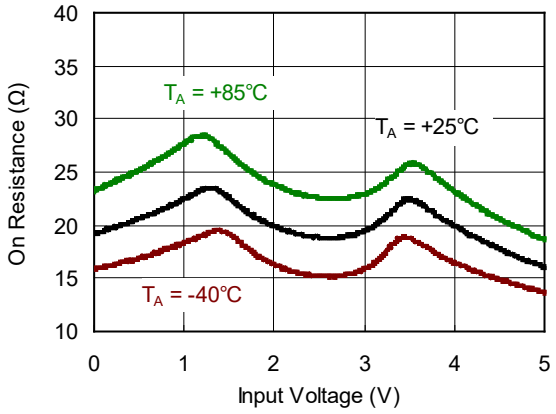
(V_{CC} = 3.3V, Full = -40℃ to +85℃, x = A, B, C and D switch in/out or out/in, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{X\_}$, V_X		Full	GND		V_{CC}	V
On-Resistance	R_{ON}	I_X = 1mA	+25℃		40	55	Ω
			Full			58	
Off Leakage Current	$I_{X\_(OFF)}$	$V_{X\_}$ = 1V, 3V, V_X = 3V, 1V	+25℃		1	1000	nA
Off Leakage Current	$I_{X(OFF)}$	$V_{X\_}$ = 1V, 3V, V_X = 3V, 1V	+25℃		1	1000	nA
On Leakage Current	$I_{X(ON)}$	V_X = 3V, 1V	+25℃		1	1000	nA
DIGITAL I/O							
Logic Input Logic Threshold High	V_{AH}, V_{BH}, V_{CH}, V_{DH}		+25℃	1.7			V
Logic Input Logic Threshold Low	V_{AL}, V_{BL}, V_{CL}, V_{DL}		+25℃			0.5	V
Input-Current High	I_{AH}, I_{BH}, I_{CH} I_{DH}	V_A, V_B, V_C, V_D = V_{CC}	+25℃		1		nA
Input-Current Low	I_{AL}, I_{BL}, I_{CL} I_{DL}	V_A, V_B, V_C, V_D = 0V	+25℃		1		nA
DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{X\_}$, $V_{Y\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 1	+25℃		75		ns
Turn-Off Time	t_{OFF}	$V_{X\_}$, $V_{Y\_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 1	+25℃		125		ns
Input Transition Rise or Fall Rate	Δt/ΔV		+25℃			100	ns/V
-3dB Bandwidth	BW	R_L = 50Ω	+25℃		180		MHz
Charge Injection	Q	R_S = 0Ω, C = 1nF, V_S = 0V, Test Circuit 2	+25℃		3.5		pC
POWER SUPPLY							
Power Supply Current	I_{CC}	V_A, V_B, V_C, V_D = V_{CC} or 0	+25℃		0.001	3	μA

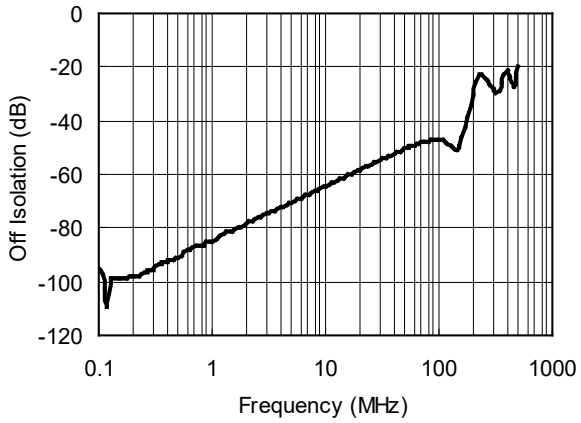
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, unless otherwise noted.

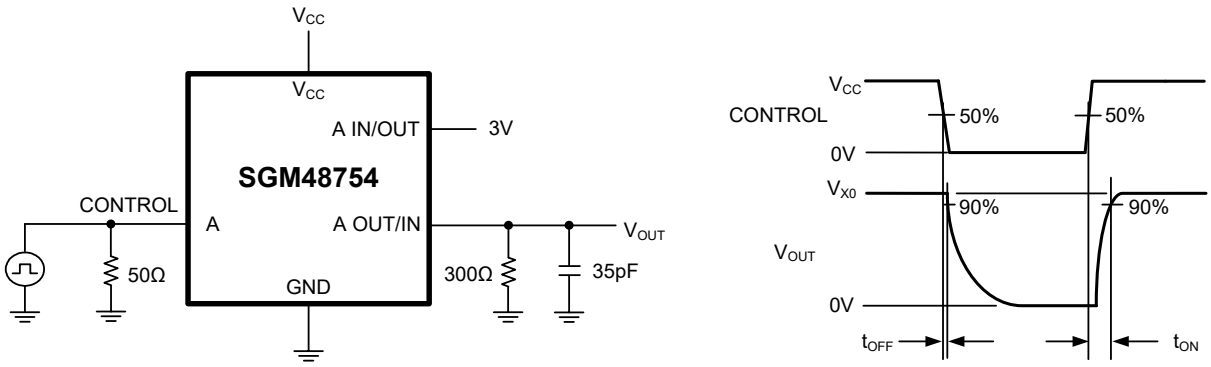
On-Resistance vs. Input Voltage



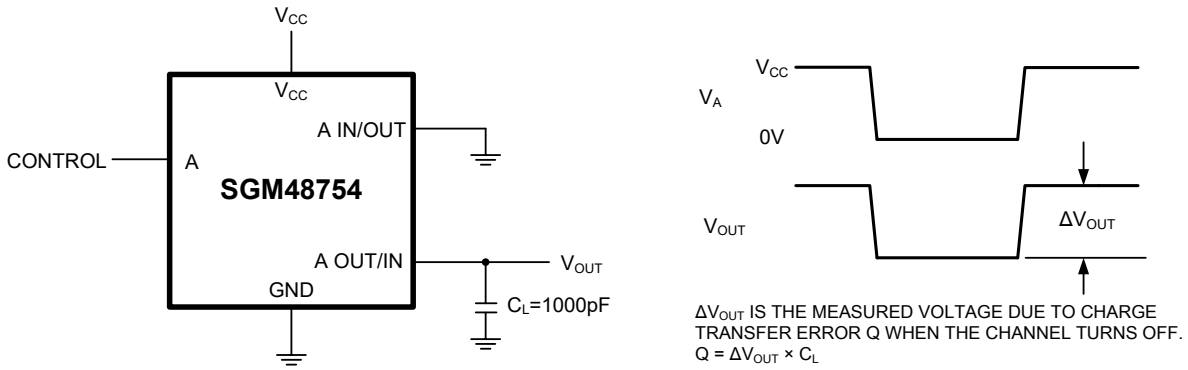
Off Isolation vs. Frequency



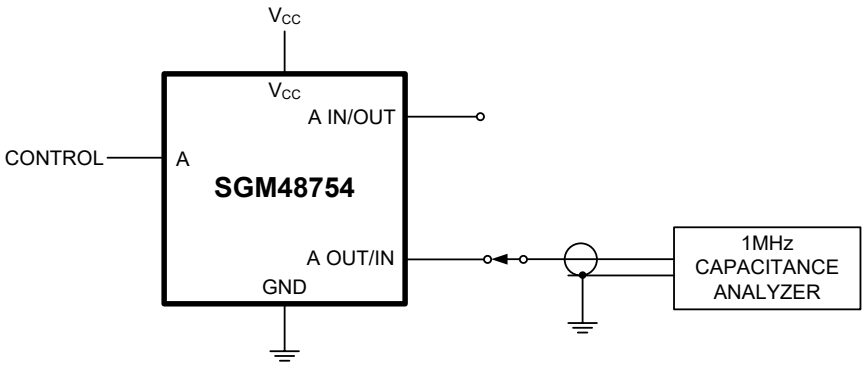
TEST CIRCUITS



Test Circuit 1. Switching Times (t_{ON}, t_{OFF})

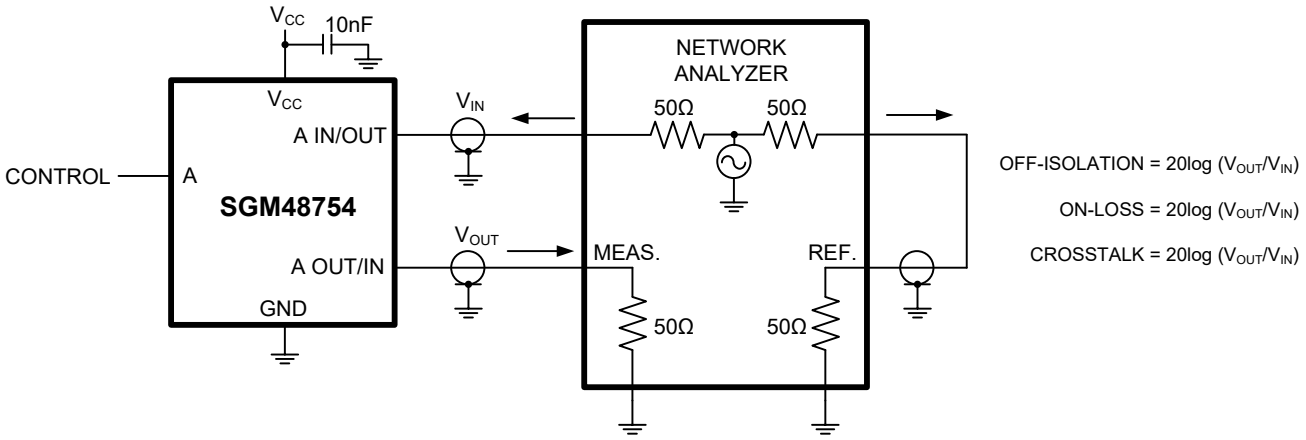


Test Circuit 2. Charge Injection (Q)



Test Circuit 3. Capacitance

TEST CIRCUITS (continued)



MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AT SOCKET TERMINALS.
OFF-ISOLATION IS MEASURED BETWEEN COM AND "OFF" NO TERMINAL ON EACH SWITCH.
ON-LOSS IS MEASURED BETWEEN COM AND "ON" NO TERMINAL ON EACH SWITCH.
CROSSTALK IS MEASURED FROM ONE CHANNEL (A, B, C, D) TO ALL OTHER CHANNELS.
SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.

Test Circuit 4. Off Isolation, On Loss and Crosstalk

APPLICATION INFORMATION

Power-Supply Considerations

Overview

The SGM48754 construction is typical of most CMOS analog switch. It supports single power supply. V_{CC} and GND are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD protection diodes are internally connected between each analog-signal pin and both V_{CC} and GND. If any analog signal exceeds V_{CC} or GND, one of these diodes will conduct. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from V_{CC} or GND.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V_{CC} or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V_{CC} and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

Over-Voltage Protection

Proper power-supply sequencing is recommended for the CMOS device. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_{CC} on first, followed by the logic inputs and analog signals. If power-supply sequencing is not possible, add one 100Ω resistor in series with the supply V_{CC} pin for over-voltage protection (Figure 1).

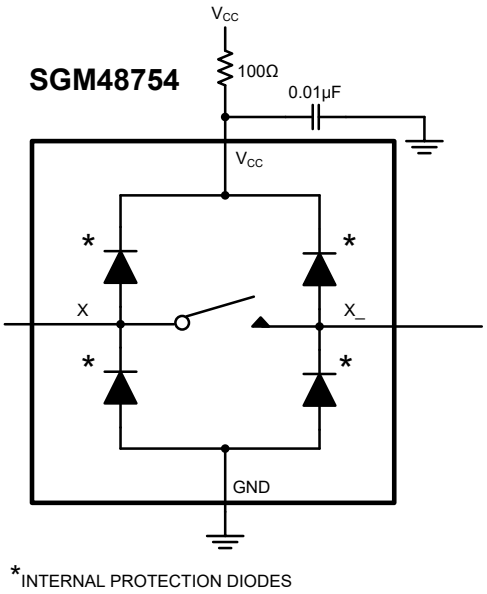


Figure 1. Over-Voltage Protection Using External Resistor

REVISION HISTORY

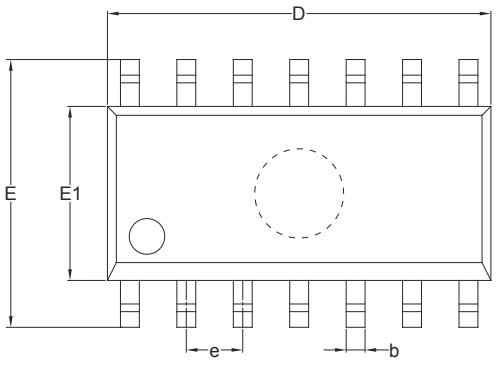
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

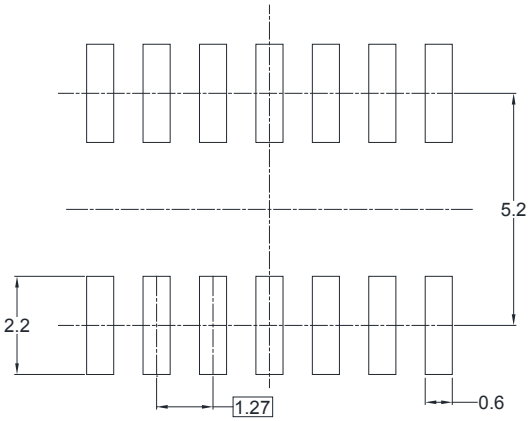
Changes from Original (JANUARY 2015) to REV.A

Changed from product preview to production data	All

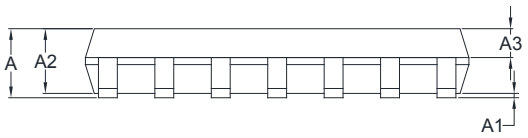
PACKAGE OUTLINE DIMENSIONS

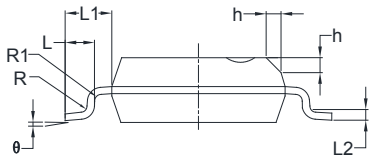
SOIC-14





RECOMMENDED LAND PATTERN (Unit: mm)

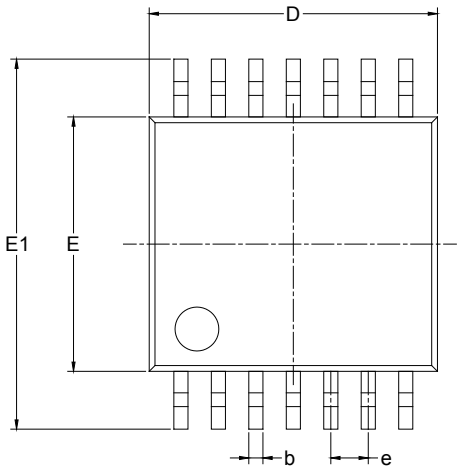


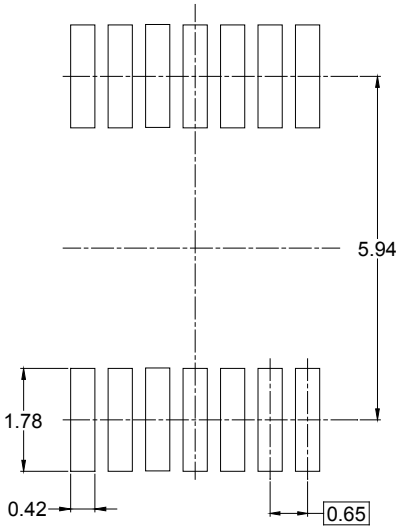


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.049	0.065
A3	0.55	0.75	0.022	0.030
b	0.36	0.49	0.014	0.019
D	8.53	8.73	0.336	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.45	0.80	0.018	0.032
L1	1.04 REF		0.040 REF	
L2	0.25 BSC		0.01 BSC	
R	0.07		0.003	
R1	0.07		0.003	
h	0.30	0.50	0.012	0.020
θ	0°	8°	0°	8°

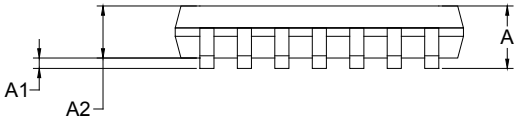
PACKAGE OUTLINE DIMENSIONS

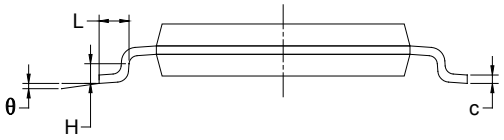
TSSOP-14





RECOMMENDED LAND PATTERN (Unit: mm)

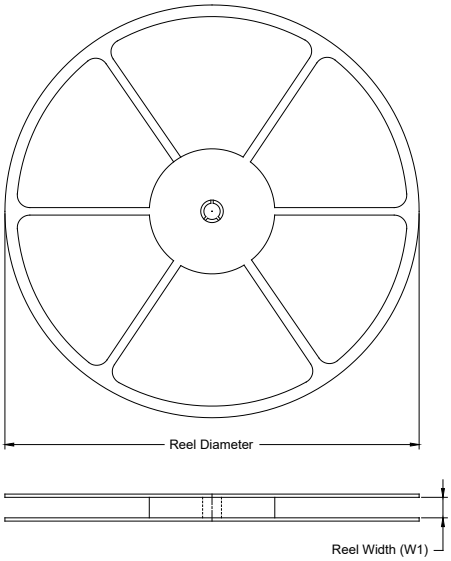




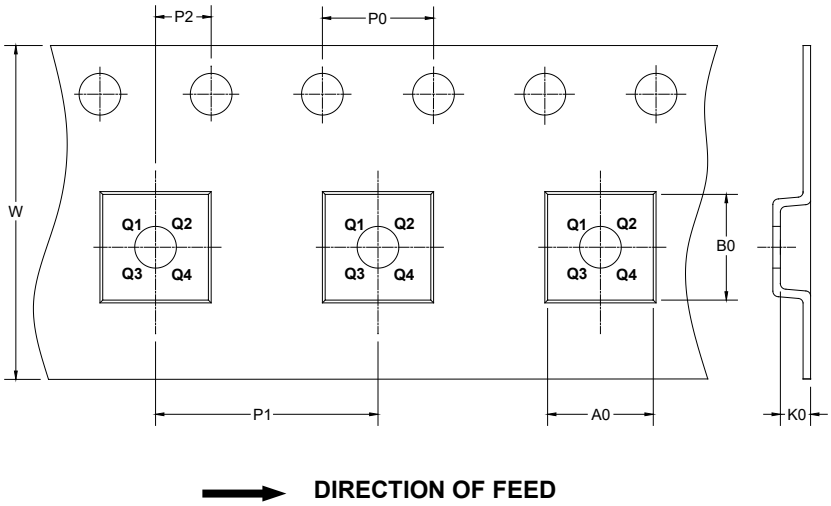
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



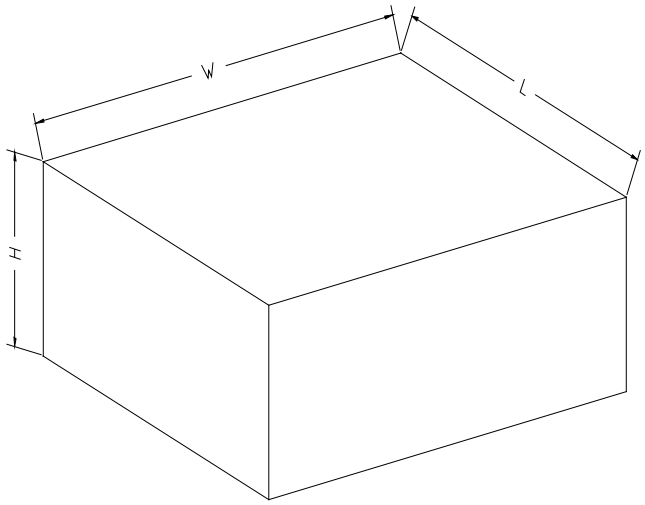
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-14	13″	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP-14	13″	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002