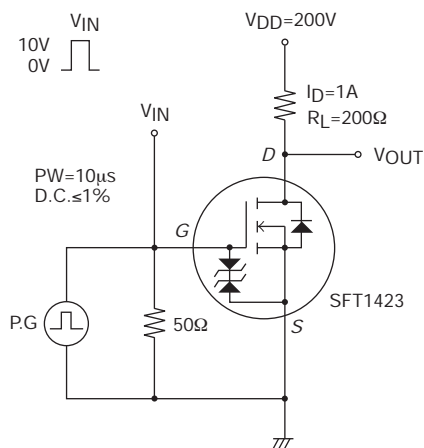


SFT1423

Electrical Characteristics at Ta=25°C

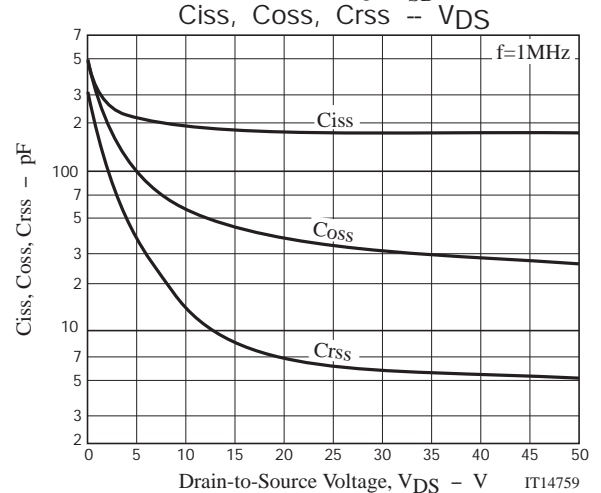
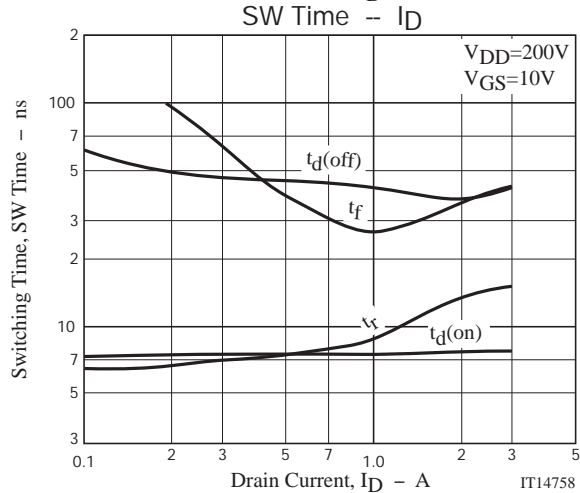
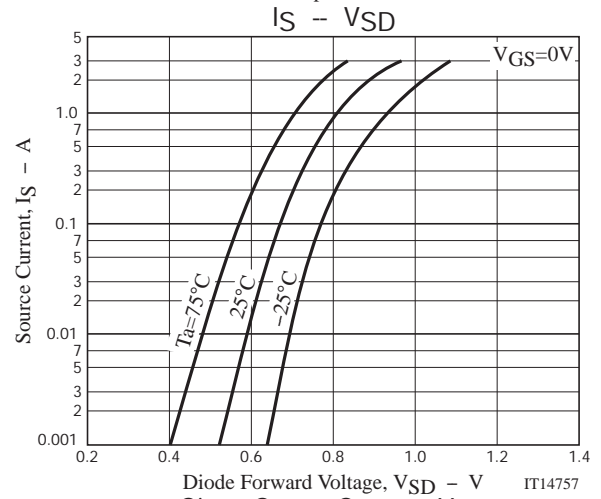
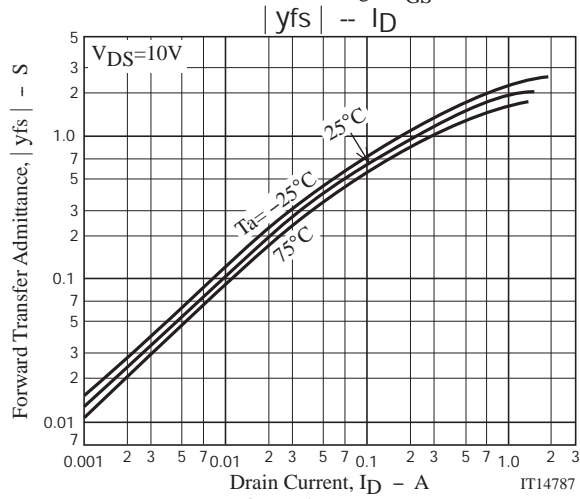
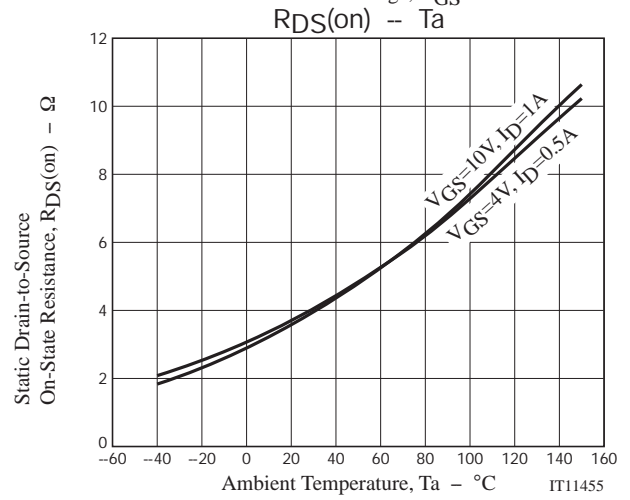
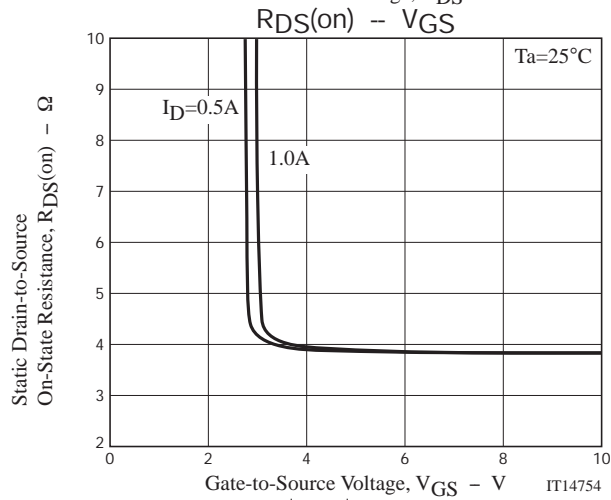
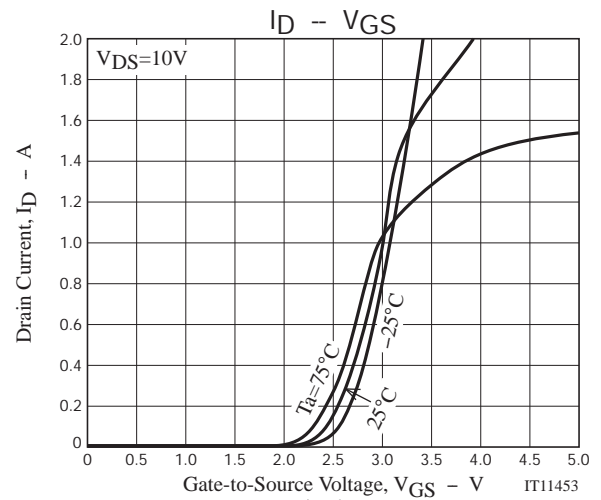
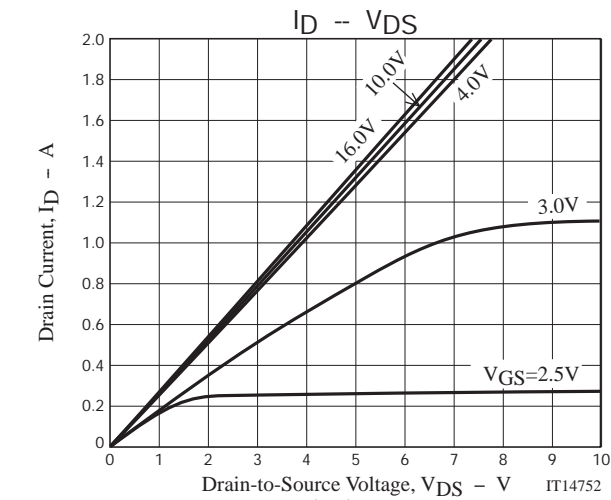
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=10mA, V_{GS}=0V$	500			V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS}=400V, V_{GS}=0V$			100	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 16V, V_{DS}=0V$			± 10	μA
Cutoff Voltage	$V_{GS(off)}$	$V_{DS}=10V, I_D=1mA$	1.2		2.6	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS}=10V, I_D=1A$	1.1	1.9		S
Static Drain-to-Source On-State Resistance	$R_{DS(on)1}$	$I_D=1A, V_{GS}=10V$		3.8	4.9	Ω
	$R_{DS(on)2}$	$I_D=0.5A, V_{GS}=4V$		3.9	5	Ω
Input Capacitance	C_{iss}	$V_{DS}=30V, f=1MHz$		175		pF
Output Capacitance	C_{oss}			32		pF
Reverse Transfer Capacitance	C_{rss}			6		pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit.		7.4		ns
Rise Time	t_r			8.8		ns
Turn-OFF Delay Time	$t_{d(off)}$			42		ns
Fall Time	t_f			27		ns
Total Gate Charge	Q_g	$V_{DS}=200V, V_{GS}=10V, I_D=2A$		8.7		nC
Gate-to-Source Charge	Q_{gs}			1.1		nC
Gate-to-Drain "Miller" Charge	Q_{gd}			2.9		nC
Diode Forward Voltage	V_{SD}	$I_S=2A, V_{GS}=0V$		0.9	1.2	V

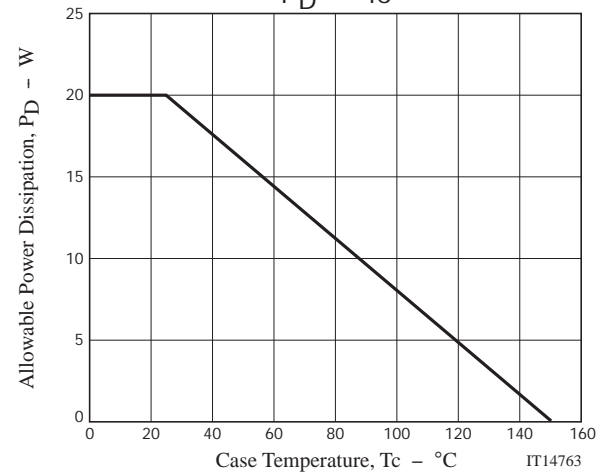
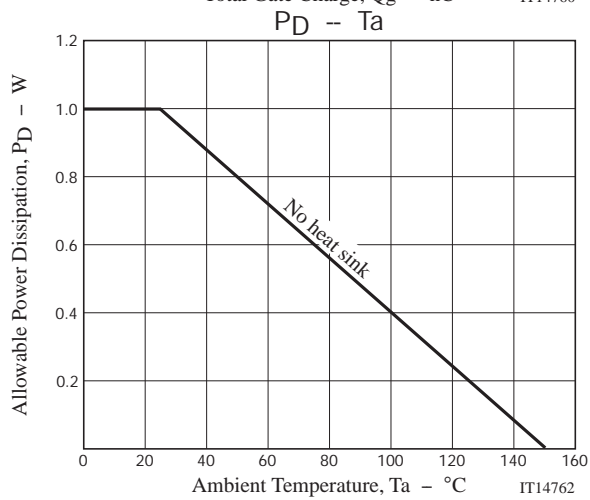
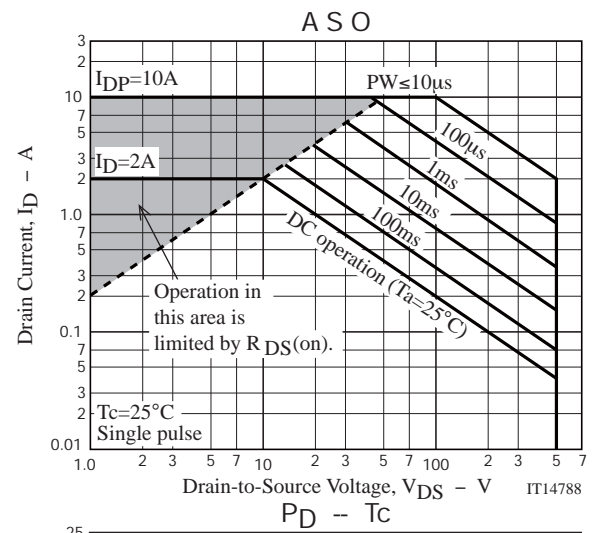
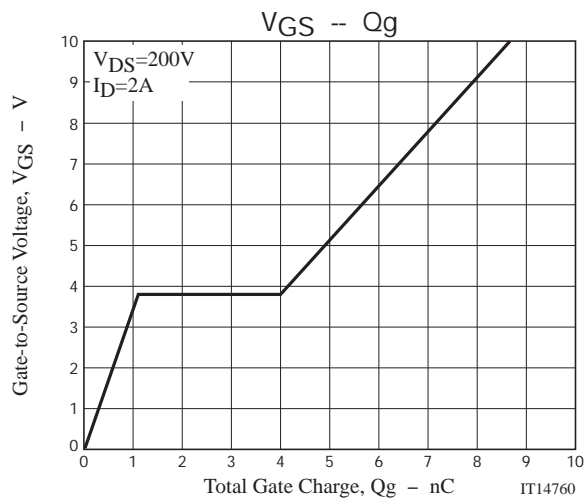
Switching Time Test Circuit



Ordering Information

Device	Package	Shipping	memo
SFT1423-E	TP	500pcs./bag	Pb Free
SFT1423-TL-E	TP-FA	700pcs./reel	





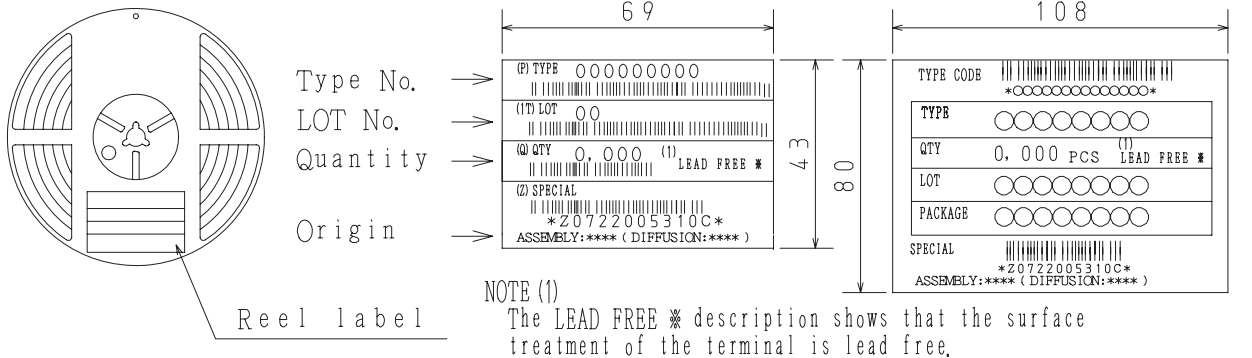
Taping Specification

SFT1423-TL-E

Packing Format

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
TP-FA	TP	700	2,100	12,600	3 reels contained Dimensions:mm (external) 183×72×185	6 inner boxes contained Dimensions:mm (external) 440×195×210

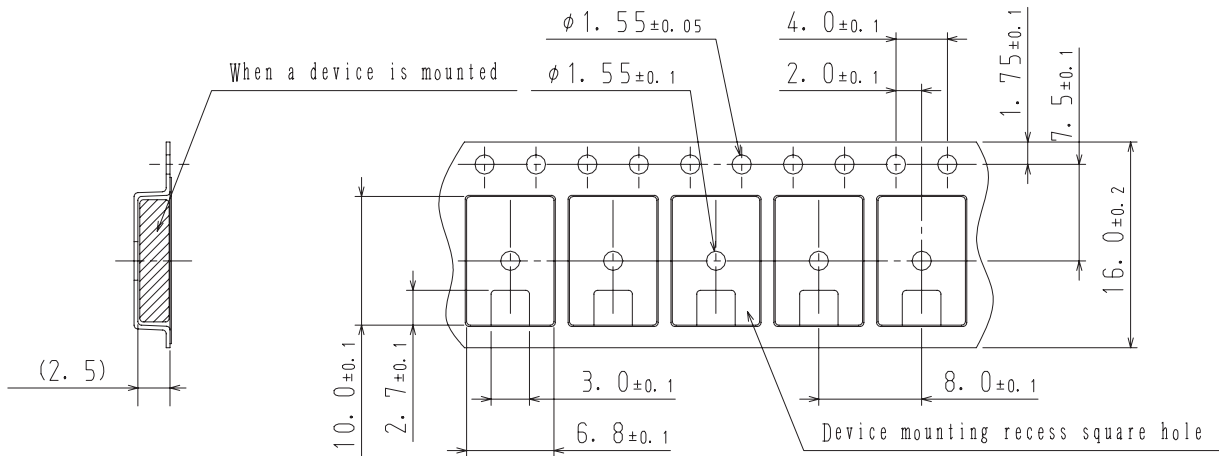
Packing method



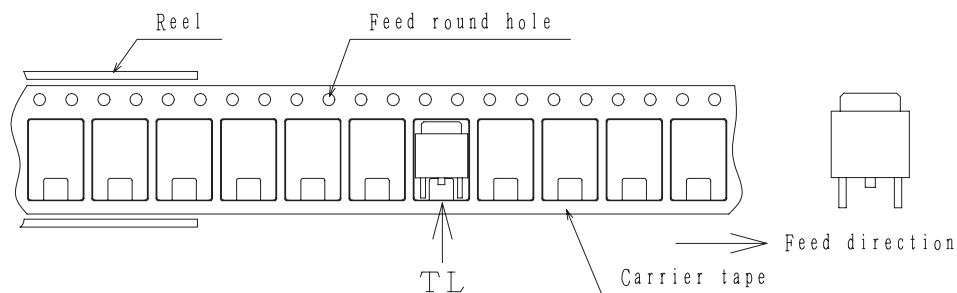
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

Taping configuration

1. Carrier tape size (unit:mm)



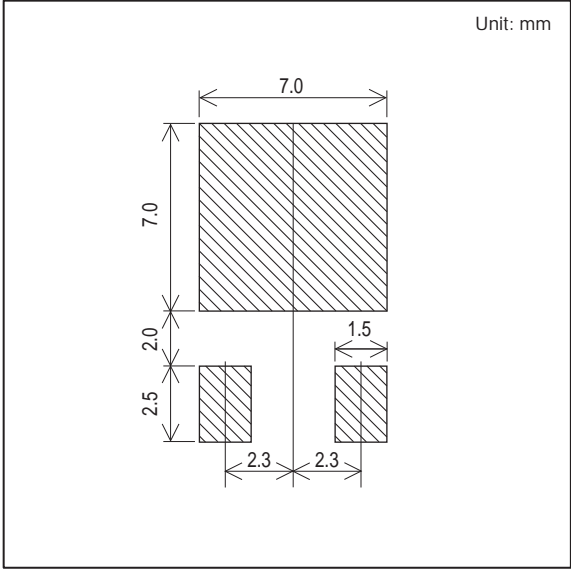
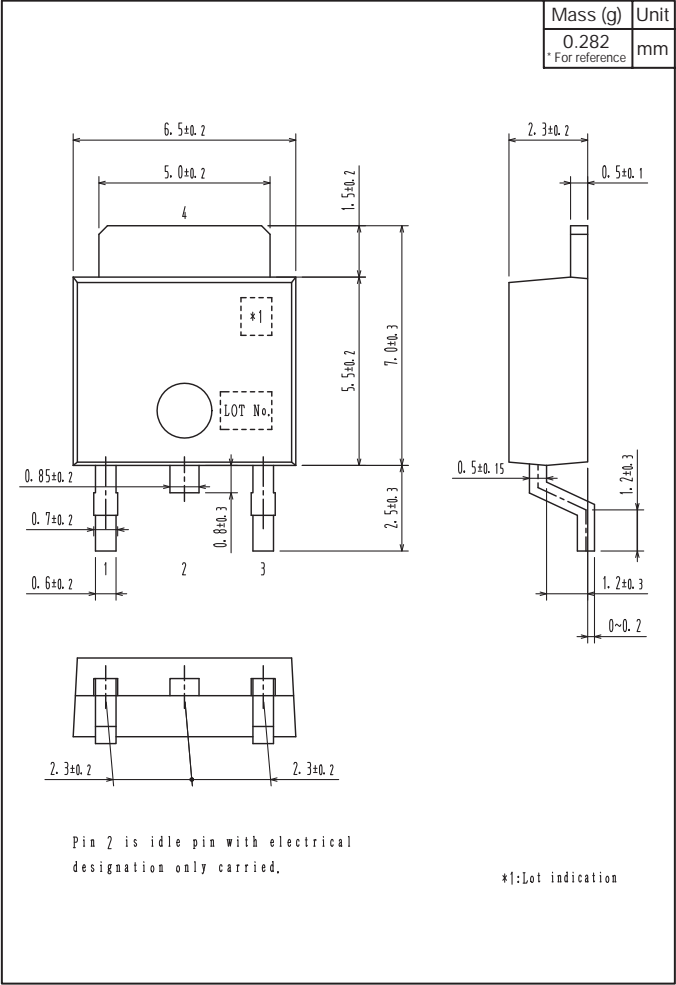
2. Device placement direction



Those with one electrode terminal on the feed hole side.....TL

Outline Drawing
SFT1423-TL-E

Land Pattern Example

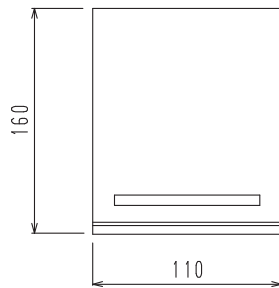
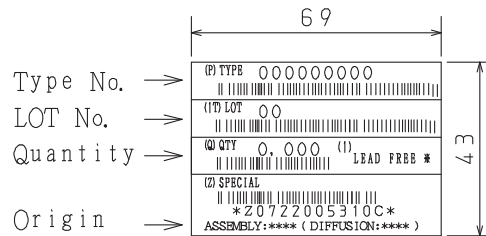


Bag Packing Specification

SFT1423-E

1. Packing Format

Package Name	Maximum Number of devices contained (pcs)			
	Bag	Inner box	Outer box	
TP	500	B-1	A-1	A-2
		10, 000	50, 000	30, 000
		Packing format (Dimensions:mm (external))		
		Inner box	Outer box	
		B-1	A-1	A-2
		445×225×55	470×250×300	470×250×190

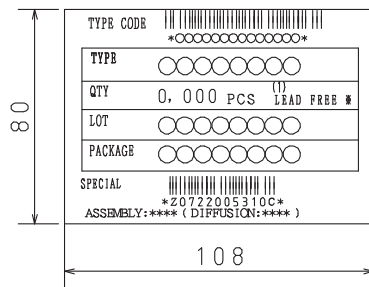
2. Bag dimensions
(unit:mm)3. Bag label, Inner box label
(unit:mm)4. Outer box label
(unit:mm)

It is a label at the time of factory shipments.
The form of a label may change in physical
distribution process.

NOTE (1)

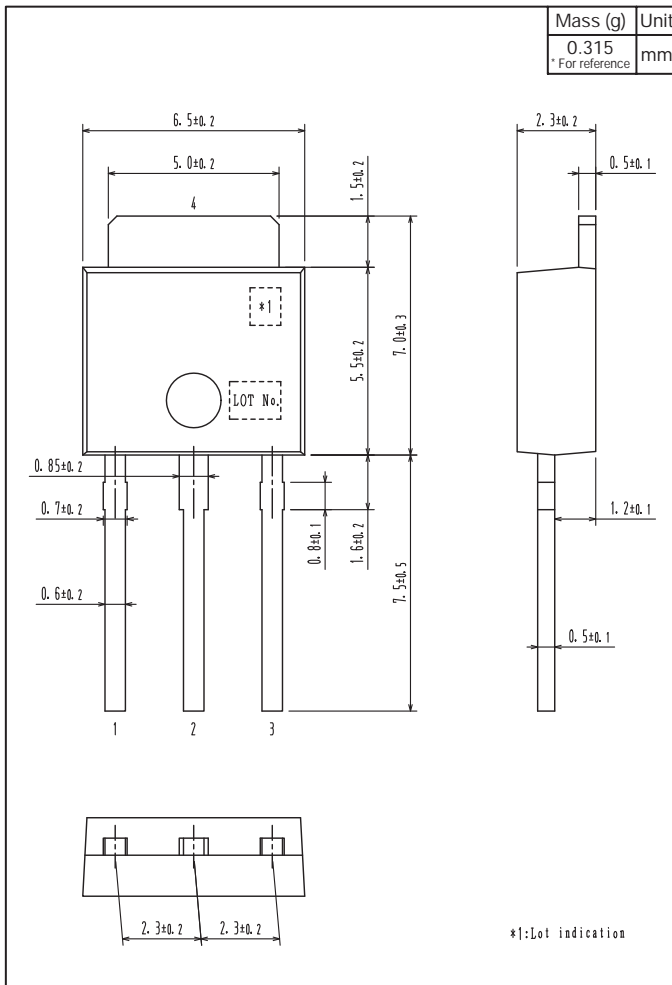
The LEAD FREE * description shows that the
surface treatment of the terminal is lead free.

Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3



Outline Drawing

SFT1423-E



Note on usage : Since the SFT1423 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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