Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage	V_{CC}	-0.5 to18	V
Supply Current	I_{CC}	20	mA
SYNC, RC,CS, LUVLO, REF to GND		-0.5 to 7	V
FB to GND	V_{FB}	-0.5 to (V_{REF}+ 0.5)	V
REF Current	I_{REF}	10	mA
OUTA/OUTB to GND	$V_{OUTA/B}$	-0.5 to 18	V
OUTA/OUTB Source Current (peak)	I_{source}	-250	mA
OUTA/OUTB Sink Current (peak)	I_{sink}	250	mA
Power Dissipation at T_A = 25°C	P_D	1.105	W
Thermal Resistance	θ_{JA}	113.1	°C/W
Junction Temperature	T_J	-40 to 150	℃
Storage Temperature Range	T_{STG}	-65 to 150	℃
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	+300	℃
ESD Rating (Human Body Model)	V_{ESD}	2	kV

Electrical Characteristics

Unless specified: VCC = 12V; CL = 100pF; T_A = -40°C to 105°C

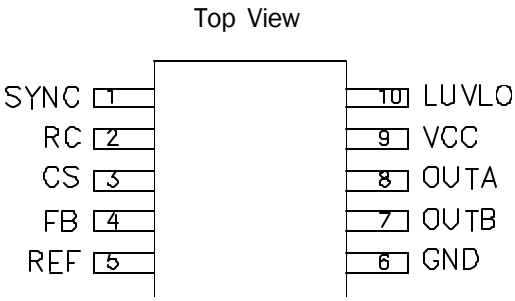
Parameter	Test Conditions	Min	Typ	Max	Unit
PWM					
Maximum Duty Cycle	Fosc = 50kHz, FB = 5V, Measured at OUTA or OUTB	48	49	50	%
Minimum Duty Cycle	Fosc = 50kHz, FB = 1.5V, Measured at OUTA or OUTB			0	%
Current Sense					
Gain			3		
Maximum Input Signal		475	525	575	mV
CS to Output Delay			100		ns
Over Current Threshold		.850	.950	1	V
Internal Slope Compensation Resistor			25		kΩ
FB to CS Offset		1.30	1.50	1.70	V
Output					
OUT Low Level		0	.50	.70	V
OUT High Level		11.0	11.25	12.00	V
Rise Time			25		ns
Fall Time			25		ns

Electrical Characteristics (Cont.)

Unless specified: VCC = 12V; CL = 100pF; T_A = -40°C to 105°C

Parameter	Test Conditions	Min	Typ	Max	Unit
VCC Under Voltage Lockout					
Start Threshold		4.0	4.40	4.5	V
Hysteresis		100	140	200	mV
Line Under Voltage Lockout					
Start Threshold	R23 = 14kΩ, R33 = 10kΩ (see page 11)	-3%	VREF	+3%	V
Hysteresis	R23 = 14kΩ, R33 = 10kΩ (see page 11)		5.6% of VREF		mV
Soft Start					
Internal Soft Start Ramp			200		µs/V
Soft Start Duration	Rcs = 1kΩ (See formula in the application information section on page 18)		12		µs
Soft Start Delay			140		µs
Oscillator					
Oscillator Frequency	R_{osc} = 11kΩ, C_{osc} = 200pF	450	500	550	KHz
Oscillator Ramp			VREF/2 +0.25		V
RC pin to GND capacitance			22		pF
Oscillator Frequency Range		50		1000	KHz
Sync/CLOCK					
Clock SYNC Threshold			1.0		V
Sync Frequency Range				F_{osc}*1.3	KHz
Bandgap					
Reference Voltage		2.970	3.125	3.280	V
Reference Current			5		mA
Overall					
Startup Current	VCC < start threshold			150	µA
Operating Supply Current	FB = 0V, CS = 0V			7	mA
VCC Zener Shunt Voltage	IDD = 10mA	16			V

Pin Configuration



(MSOP-10)

Ordering Information

Part Number	Package	Temp. Range (T_A)
SC4808B-2MSTRT(1)(2)	MSOP-10	-40°C to 105°C

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

FB: The inverting input to the PWM comparator. Stray inductances and parasitic capacitance should be minimized by utilizing ground planes and correct layout guide lines (see page 19).

REF: A 0.1µF or 47nF low ESR capacitor is required and must be placed right at the pin.

CS: Current sense input and internal slope compensation are both provided via the CS pin. The current sense input from a sense resistor is used for the peak current and overcurrent comparators. An internal 1 to 3 feed back voltage divider provides a 3X amplification of the CS signal. This is used for comparison to the external error amplifier signal. If an external resistor is connected from CS to the current sense resistor, the internal current source will provide a programmable slope compensation. The value of the resistor will determine the level of compensation. At higher compensation levels, voltage mode of operation can be achieved.

RC: The oscillator programming pin. The oscillator should be referenced to a stable reference voltage for an accurate and stable frequency. Only two components are required to program the oscillator, a resistor (tied to Vref and RC), and a capacitor (tied to the RC and GND). The following formula can be used for a close approximation of the oscillator frequency.

$$F_{OSC\_A} \cong \frac{1}{R_{OSC} C_{TOT} \times 0.8} \qquad F_{OSC\_B} \cong \frac{1}{R_{OSC} C_{TOT} \times 0.9}$$

where:

$$C_{TOT} = C_{OSC} + C_{SC4808} + C_{Circuit}$$

$$C_{SC4808} \cong 22\,pF$$

Where the frequency is in Hertz, resistance in ohms, and capacitance in farads. The recommended range of timing resistors is between 10 kohm and 200kohm and range of timing capacitors is between 100pF and 1000pF. Timing resistors less than 10 kohm should be avoided.
Refer to layout guide lines on (page 19) to achieve best results.

LUVLO: Line undervoltage lockout pin. An external resistive divider will program the undervoltage lockout level. The external divider should be referenced to the quiet analog ground (see page 19). During the LUVLO, the driver outputs are disabled and the softstart is reset. This pin can also function as an Enable/Disable.

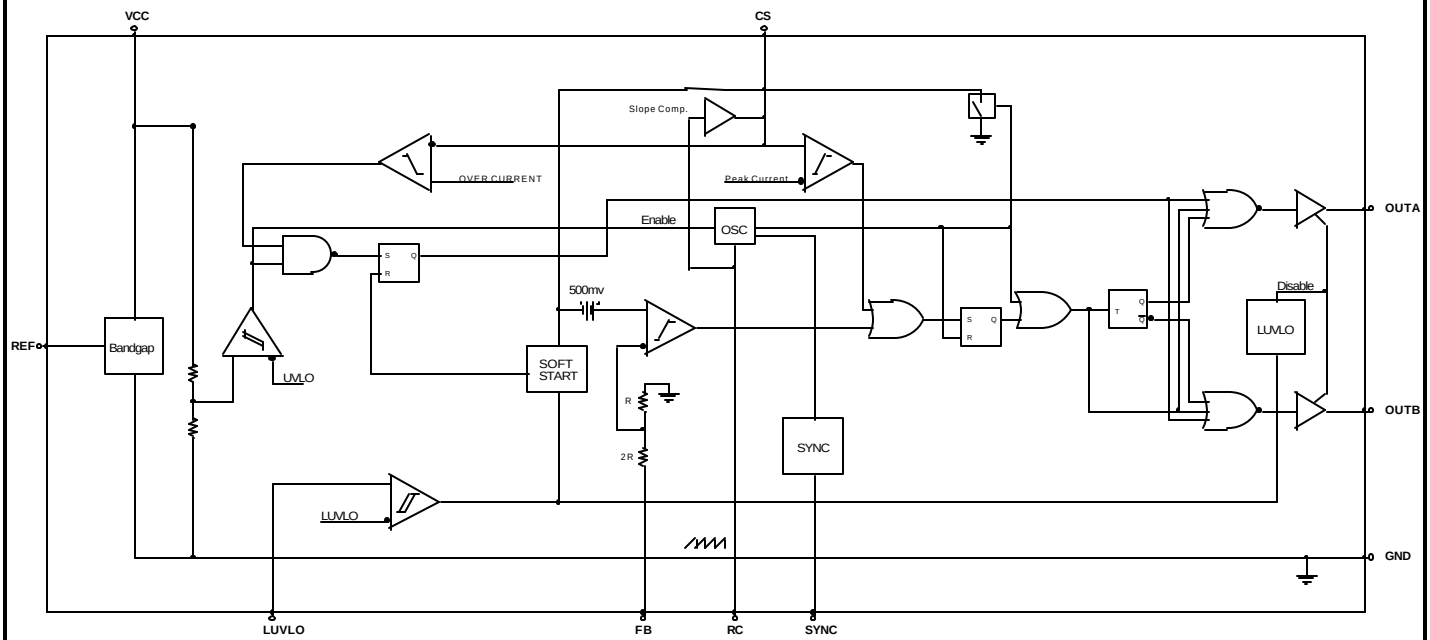
SYNC: SYNC is a positive edge triggered input with a threshold set to 1.0V. In a single controller operation, SYNC could be grounded or connected to an external synchronization clock within the SYNC frequency range (see page 3). In the Bi-Phase operation mode SYNC pins could be connected to the Cosc (Timing Capacitors) of the other controller. This will force an out of phase operation (see page 12).

GND: Device power and analog ground. Careful attention should be paid to the layout of the ground planes (see page 19).

OUTA and OUTB: Out of phase gate drive stages. The driver's peak source and sink current drive capability of 100mA, enables the use of an external MOSFET driver or a NPN/PNP transistor buffer.
The oscillator RC network programs the oscillator frequency, which is twice the OUTA/OUTB frequency. To insure that the outputs do not overlap, a dead time can be generated between the two outputs by sizing the oscillator timing capacitor (see page 11).

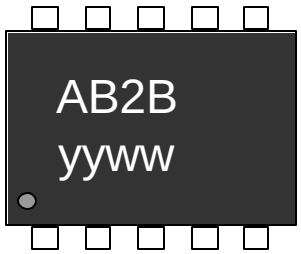
VCC: The supply input for the device. Once VCC has exceeded the UVLO limit, the internal reference, oscillator, drivers and logic are powered up. A low ESR capacitance, should be used for decoupling right at the IC pin to minimize noise problems.

Block Diagram

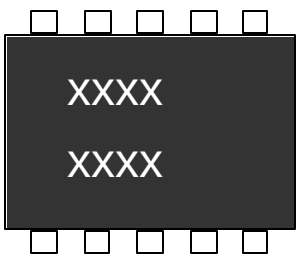


Marking Information

Top Mark

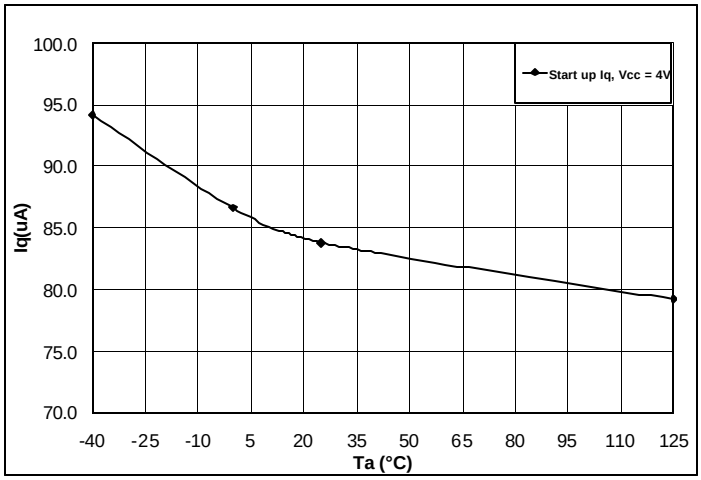


Bottom Mark

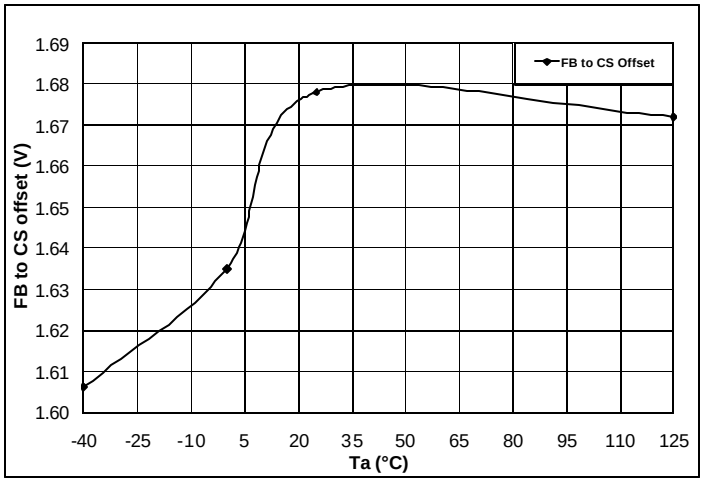


yyww = Datecode (Example: 9912)
xxxx = Semtech Lot # (Example: E901
xxxx 01-1)

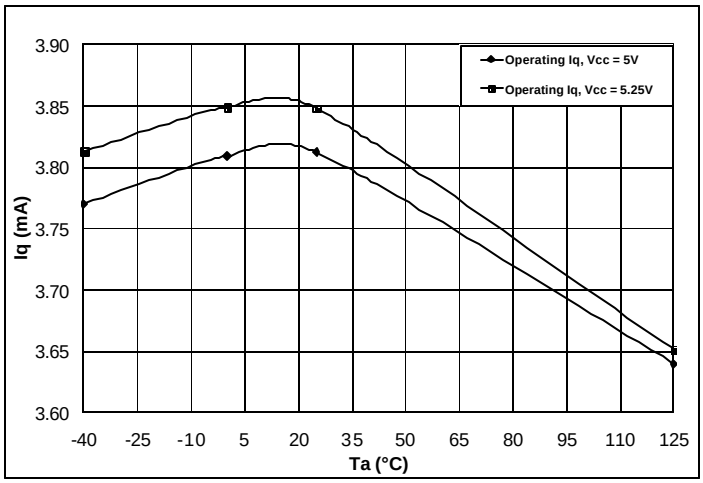
SC4808B-2 Typical Characteristics



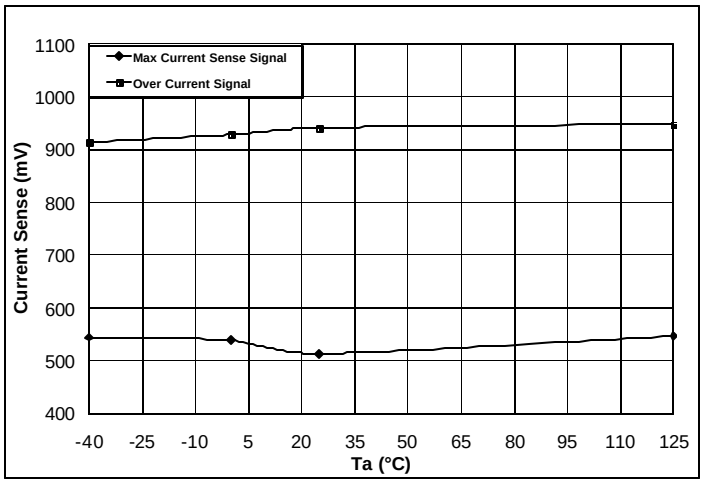
Iq (start up) vs. Temperature



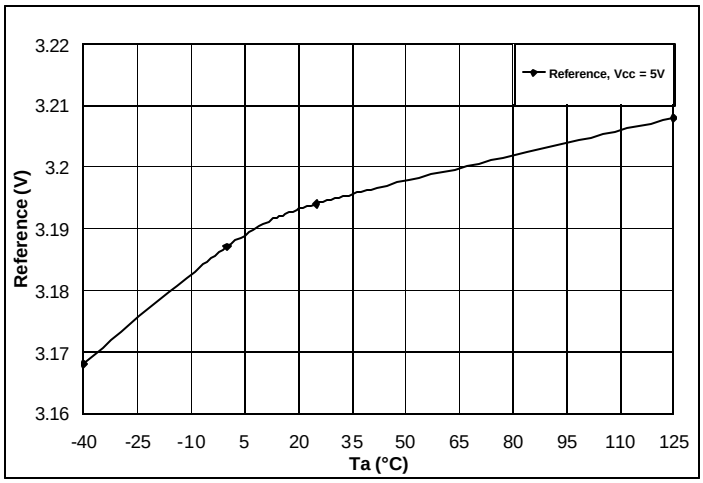
FB to CS Offset vs. Temperature



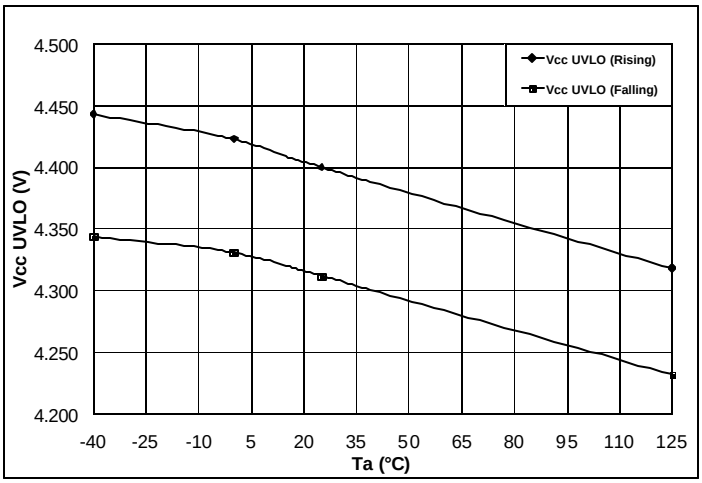
Iq (operating) vs. Temperature



Current sense vs. Temperature

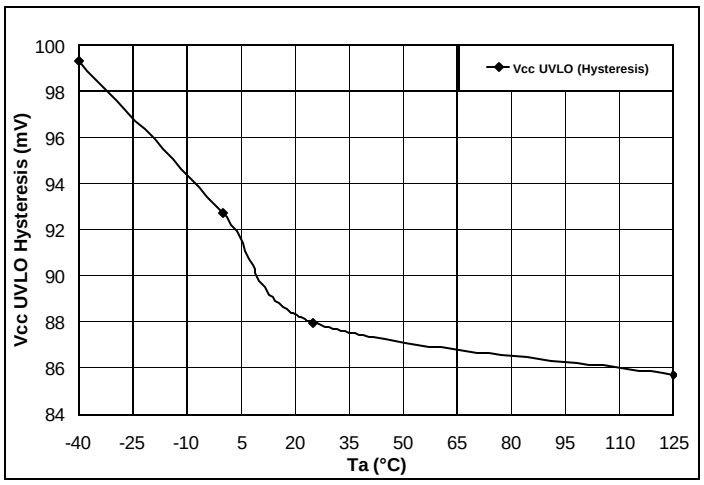


Reference vs. Temperature

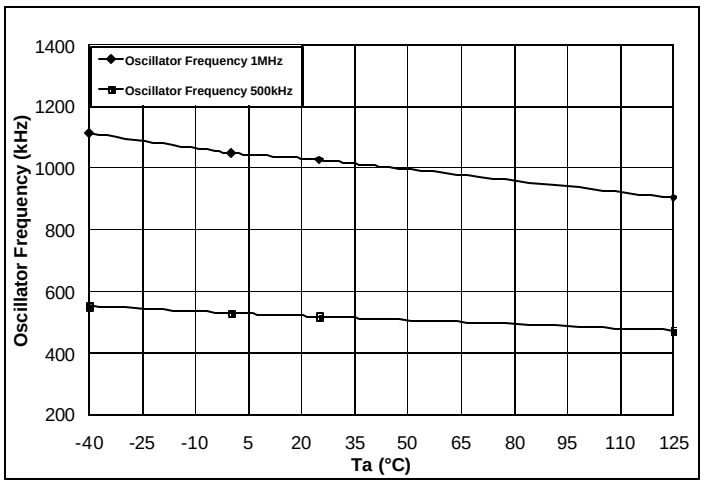


Vcc UVLO vs. Temperature

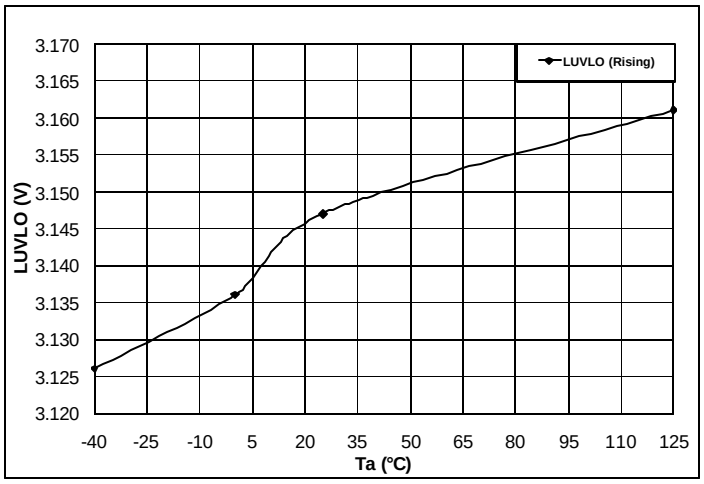
SC4808B-2 Typical Characteristics (Cont.)



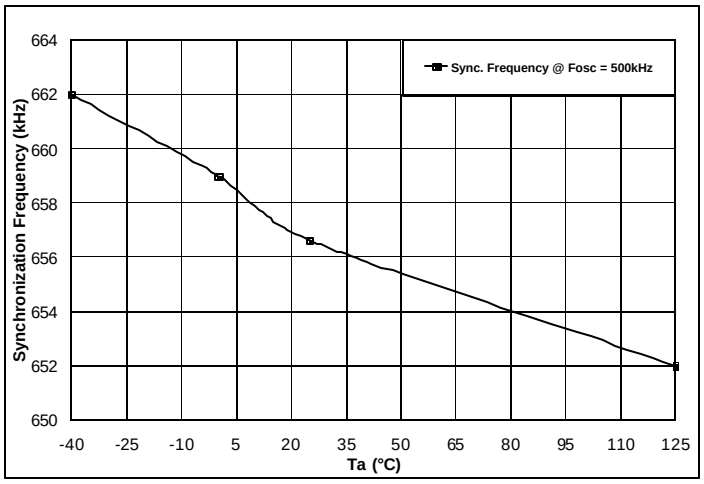
Vcc UVLO Hysteresis vs. Temperature



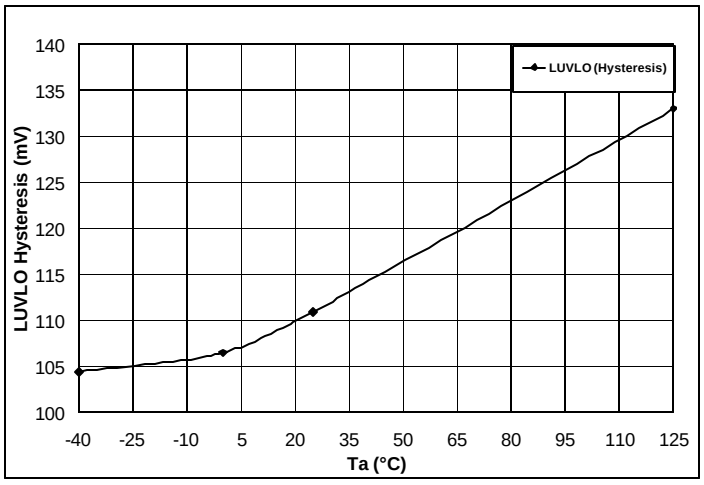
Oscillator Frequency vs. Temperature



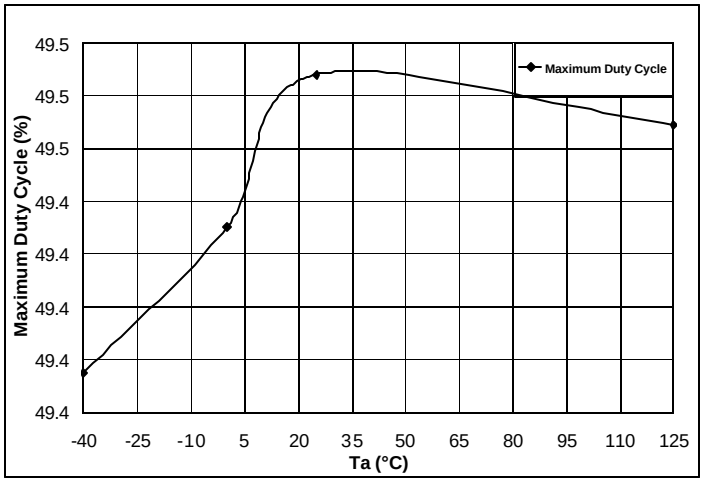
Line UVLO vs. Temperature



Synchronization Frequency vs. Temperature

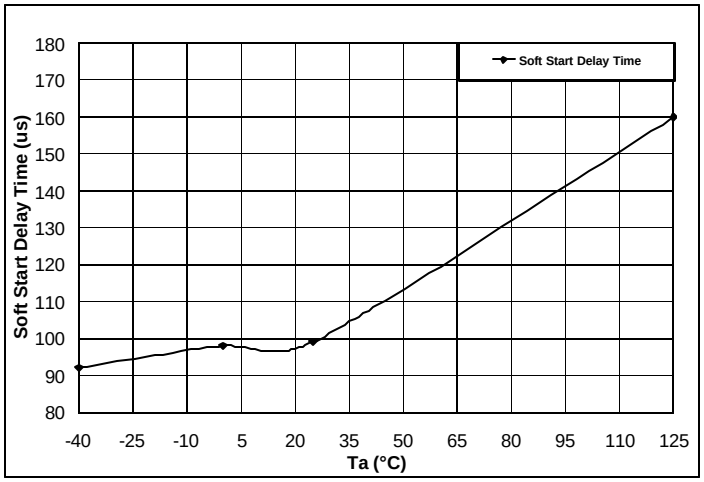


Line UVLO Hysteresis vs. Temperature



Maximum Duty Cycle vs. Temperature

SC4808B-2 Typical Characteristics (Cont.)



Soft Start Delay time vs. Temperature

Application Information

THEORY OF OPERATION

The SC4808B-2 is a versatile double ended, high speed, low power, pulse width modulator that is optimized for applications requiring minimum space.

The device contains all of the control and drive circuitry required for isolated or non isolated power supplies where an external error amplifier is used. A fixed oscillator frequency (up to 1MHz) can be programmed by an external RC network.

The SC4808B-2 is a peak current or voltage mode controller, depending on the amount of slope compensation, programmable with only one external resistor. The cycle by cycle peak current limit prevents core saturation when a transformer is used for isolation while the overcurrent circuitry initiates the softstart cycle.

The SC4808B-2 dual output drive stages are arranged in a push-pull configuration. Both outputs switch at half the oscillator frequency using a toggle flip flop. The dead time between the two outputs is programmable depending on the values of the timing capacitor and resistors, thus limiting each output stage duty cycle to less than 50%.

The SC4808B-2 also provides flexibility with programmable LUVLO thresholds, with built-in hysteresis.

SUPPLY

A single supply, VCC is used to provide the bias for the internal reference, oscillator, drivers, and logic circuitry of SC4808B-2. To ensure proper operation during start up, VCC slew rate of less than 10V/mS is recommended.

PWM CONTROLLER

SC4808B-2 is a double ended PWM controller that can be used in voltage or current mode applications. The SC4808B-2 provides a 4.4V VCC UVLO, and a 3.125V reference. The oscillator frequency is programmed by a resistor and a capacitor network connected to an external reference provided by the SC4808B-2. The two outputs, OUTA and OUTB, are 180 degrees out of phase and run at half of the oscillator frequency.

An external error amplifier will provide the error signal to the FB pin of the SC4808B-2.

The current sense input and internal slope compensation are both provided via the CS pin. The current sense input from a sense resistor is used for the peak current and overcurrent comparators. An internal 1 to 3 feedback voltage divider provides a 3X amplification of the CS signal. This is used for comparison to the external error amplifier signal. If an external resistor is connected from CS to the current sense resistor, the internal current source will provide a programmable slope compensation. The value of the resistor will determine the level of compensation. At higher compensation levels, voltage mode of operation can be achieved. The error amplifier signal at the FB pin will be used in conjunction with the CS signal to achieve regulation.

Two levels of undervoltage lockout are also available. The LUVLO (line under voltage lockout) pin via an external resistive divider will program the undervoltage lockout level. During the LUVLO, the driver outputs are disabled and the softstart is reset.

Once VCC has exceeded the UVLO (VCC under voltage lockout) limit, the internal reference, oscillator, drivers and logic are powered up.

SYNC is a positive edge triggered input with a threshold set to 1.0V.

By connecting an external control signal to the SYNC pin, the internal oscillator frequency will be synchronized to the positive edge of the external control signal. In a single controller operation, SYNC should be grounded or connected to an external synchronization clock within the SYNC frequency range (see page 3).

In the Bi-phase operation mode a very unique oscillator is utilized to allow two SC4808B-2 to be synchronized together and work out of phase. This feature is setup by simple connection of the SYNC input to the RC pin of the other part. The fastest oscillator automatically becomes the master, forcing the two PWMs to operate out of phase. This feature minimizes the input and output ripples, and reduces stress on the capacitors.

Application Information (Cont.)

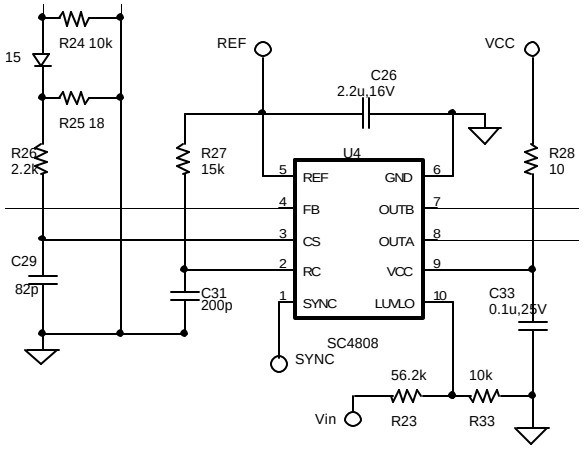
VCC UNDER VOLTAGE LOCK OUT

Depending on the application and the voltages available, the SC4808B-2 (UVLO = 4.4V) can be used to provide the VCC undervoltage lock out function to ensure the converters controlled start up.
Before the VCC UVLO has been reached, the internal reference, oscillator, OUTA/OUTB drivers, and logic are disabled.

LINE UNDER VOLTAGE LOCK OUT

The SC4808B-2 also provides a line undervoltage (LUVLO = Vref) function. The LUVLO pin is programmed via an external resistor divider connected as shown below. The actual start-up voltage can be calculated by using the equation below:

$$V_{Startup} = V_{REF} \times \frac{(R23 + R33)}{R33}$$

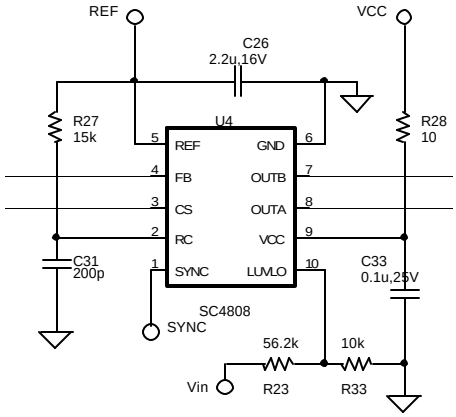


REFERENCE

A 3.125V(SC4808B-2) reference voltage is available that can be used to source a typical current of 5mA to the external circuitry. The Vref can be used to provide the oscillator RC network with a regulated bias.

OSCILLATOR

The oscillator frequency is set by connecting a RC network as shown below.



The oscillator has a ramp voltage of about Vref/2. The oscillator frequency is twice the frequency of the OUTA and OUTB gate drive controls.

The oscillator capacitor C31 is charged by a current sourced from the Vref through R27. Once the RC pin reaches about Vref/2, the capacitor is discharged internally by the SC4808B-2. It should be noted that larger capacitor values will result in a longer dead time during the down slope of the ramp.
The following equation can be used as an approximation of the oscillator frequency and the Dead time:

$$F_{OSC\_A} \cong \frac{1}{R_{OSC} C_{TOT} \times 0.8} \qquad F_{OSC\_B} \cong \frac{1}{R_{OSC} C_{TOT} \times 0.9}$$

where:

$$C_{TOT} = C_{OSC} + C_{SC4808} + C_{Circuit}$$

$$C_{SC4808} \cong 22\,pF$$

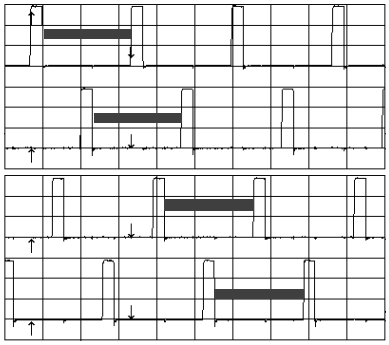
$$T_{deadtime} \cong \frac{C_{OSC} \times V_{REF} \times 0.5}{3 \cdot 10^{-3}}$$

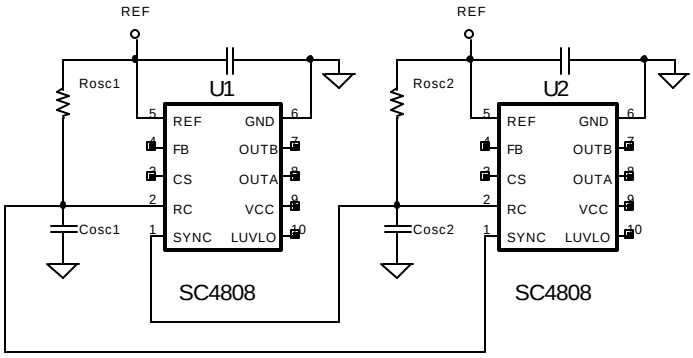
The recommended range of timing resistors is between 10 kohm and 200kohm, range of timing capacitors is between 100pF and 1000pF. Timing resistors less than 10 kohm should be avoided.

Application Information (Cont.)

SYNC/Bi-Phase operation

In noise sensitive applications where synchronization of the oscillator frequency to a reference frequency is required, the SYNC pin can accept the external clock. By connecting an external control signal to the SYNC pin, the internal oscillator frequency will be synchronized to the positive edge of the external control signal. SYNC is a positive edge triggered input with a threshold set to 1.0V (SC4808B-2).
In a single controller operation, SYNC should be grounded or connected to an external synchronization clock within the SYNC frequency range (see page 3).

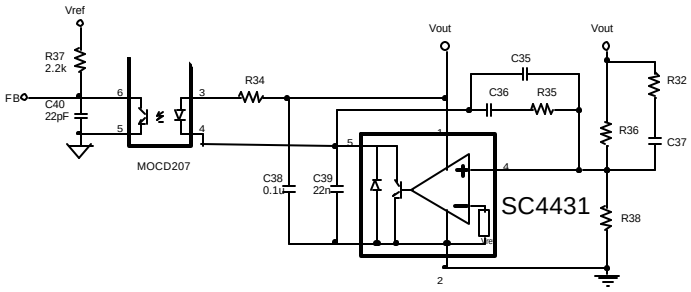




In the Bi-phase operation mode a very unique oscillator is utilized to allow two SC4808B-2's to be synchronized together and work out of phase. This feature is set up by a simple connection of the SYNC input to the RC pin of the other part. The fastest oscillator automatically becomes the master, forcing the two PWMs to operate out of phase. This feature minimizes the input and output ripples, and reduces stress on the capacitors.

FEED BACK

The error signal from the output of an external error amplifier such as SC431 or SC4431 is applied to the inverting input of the PWM comparator at the FB pin either directly or via an opto coupler for the isolated applications. For best stability, keep the FB trace length as short as possible.



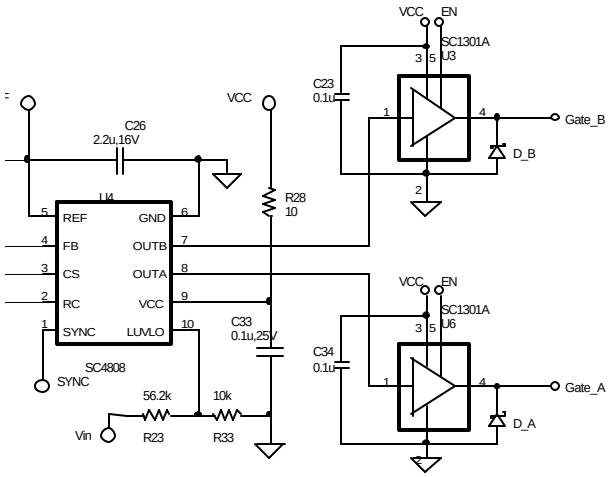
The signal at the FB pin is then compared to the 3X amplified signal from the current sense/ slope compensation CS pin. Matched out of phase signals are generated to control the OUTA and OUTB gate drives of the two phases. A single ramp signal is used to generate the control signals for both phases, hence achieving a tightly matched per phase operation.
Voltages below 1.5V at the FB pin, will produce a 0% duty cycle at the OUTA/OUTB gate drives. This offset is to provide enough head room for the opto coupler used in isolated applications.

GATE DRIVERS

OUTA and OUTB are out of phase bipolar gate drive output stages, that are supplied from VCC and provide a peak source/sink current of about 100mA. Both stages are capable of driving the logic input of external MOSFET drivers or a NPN/PNP transistor buffer. The output stages switch at half the oscillator frequency. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This "dead time" between the two outputs, along with a slower output rise and fall time, insures that the two outputs can not be on at the same time. The dead time is programmable and depends upon the timing capacitor.

Application Information (Cont.)

It should be noted that if high speed/high current drivers such as the SC1301 are used, careful layout guide lines must be followed in order to minimize stray inductance, which might cause negative voltages at the output of the drivers. This negative voltage can be clamped to a reasonable level by placing a small Schottky diode directly at the output of the driver as shown below.



OVER CURRENT

Two levels of over current protection are provided by the SC4808B-2. The current information is sensed at the CS pin and compared to a peak current limit level of 525mV. If the 525mV limit is exceeded, the OUTA and OUTB pulse widths and duty cycle is reduced until the CS pin reaches a second threshold of 950mV. At that point, the OUTA and OUTB are disabled, and after a delay of 140µs, the internal softstart sequence is started. After the softstart duration (see page 21 for calculation of softstart time), normal operation is achieved, unless the over current condition is still present.

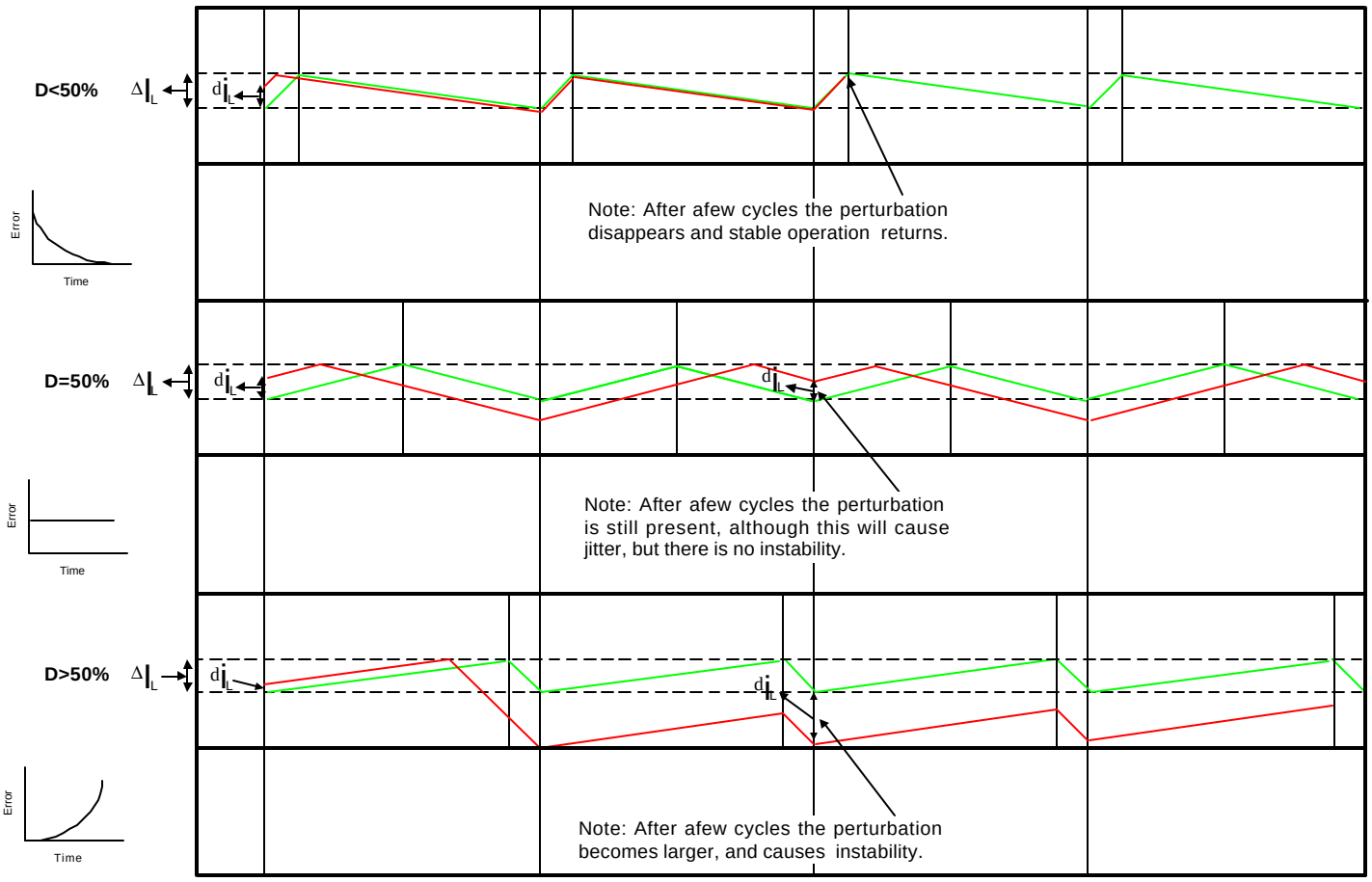
Application Information (Cont.)

SLOPE COMPENSATION (Current or Voltage mode of operation)

In applications where a current mode control is used for regulation, the peak inductor current information is used to produce the average output current. If a small perturbation due to changes in supply voltage or noise pick up is generated, instability may occur if the duty cycle is >50%.
This phenomenon is graphically shown below. The inductor current and disturbed inductor current are shown for three different duty cycles conditions.
The top wave form shows the applications where the duty cycle D is less than 50%. As shown, even if an error is introduced, after only a few cycles the error converges to zero.
The second wave form shows the case where D = 50%. Under this condition, even though the error does not completely disappear, it stays constant and is not getting larger. This will be seen as jitter at the inductor voltage.
The bottom wave form shows D>50%. As shown, a very small error results in a much larger error only after a few cycles. This will cause instability in the converter and the average output inductor current. The output load will not be able to be kept in regulation.

Instability in current mode operation due to Duty cycle >50%

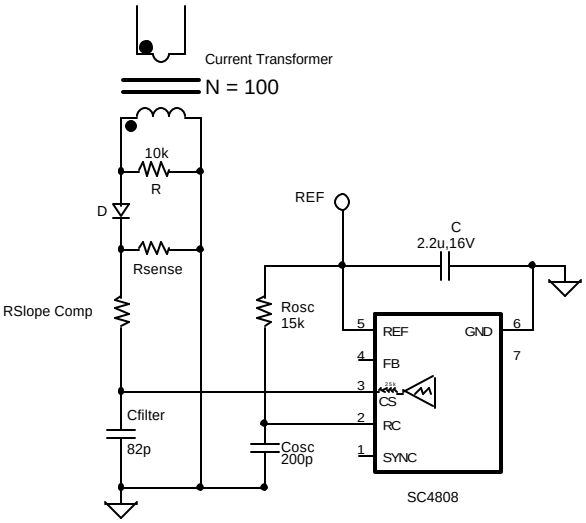
di_L : Small Inductor current perturbation
ΔI_L : Inductor current



Application Information (Cont.)

The instability can be corrected by modification of the peak current information slope. One of the methods to alter the peak current information is to add a positive going ramp to the output of the current sensing circuitry.

The SC4808B-2 achieves this by using an internal slope compensation circuit. The oscillator ramp is internally buffered and an internal 25kOhms resistor in conjunction with an external resistor at the CS pin will program the level of slope compensation.



RSlope Comp value will determine the Mode of operation (Voltage or Current)

The Peak current information is sensed and the result is realistically summed to the buffered oscillator ramp, as shown above. The value of the external resistor $R_{slope\ comp}$ will determine the percentage of the slope compensation. As the value for $R_{slope\ comp}$ is reduced, the current information becomes more dominant and the mode of operation becomes more current mode. At the same time the slope of the current information is modified to provide the slope compensation.

If the $R_{slope\ comp}$ is increased, the internal ramp becomes the dominant signal and more voltage mode of operation is achieved. As it can be calculated from the second formula below, a 100% voltage mode operation can be achieved by choosing $R_{slope\ comp}$ to be greater than 6.25K ohms. Also if a 100% current mode of operation is required, $R_{slope\ comp}$ is reduced to zero and the contribution from the internal ramp is completely eliminated.

$$\%Slope\_Comp = \frac{V_{Ramp} \times \frac{(R_{slope\_Comp} + R_{sense})}{(R_{slope\_Comp} + R_{sense}) + R_{internal}}}{V_{CS}}$$

or

$$R_{external} \cong R_{internal} \bullet \left[\frac{0.2 \times (\%slope\_Comp)}{1 - (0.2 \times \%slope\_Comp)} \right]$$

Next page illustrates how the buffered oscillator ramp is used to modify the sensed inductor current.

It should be noted that in order for the slope compensation to be effective, the current sensed signal slope should be at least 50% less steeper than the oscillator positive ramp slope. The slope will include the magnetizing current of the transformer and the inductor output current in isolated applications. In non-isolated applications, the slope will only include the inductor output current.

$d i_L$: Small Inductor current perturbation

ΔI_L : Inductor current

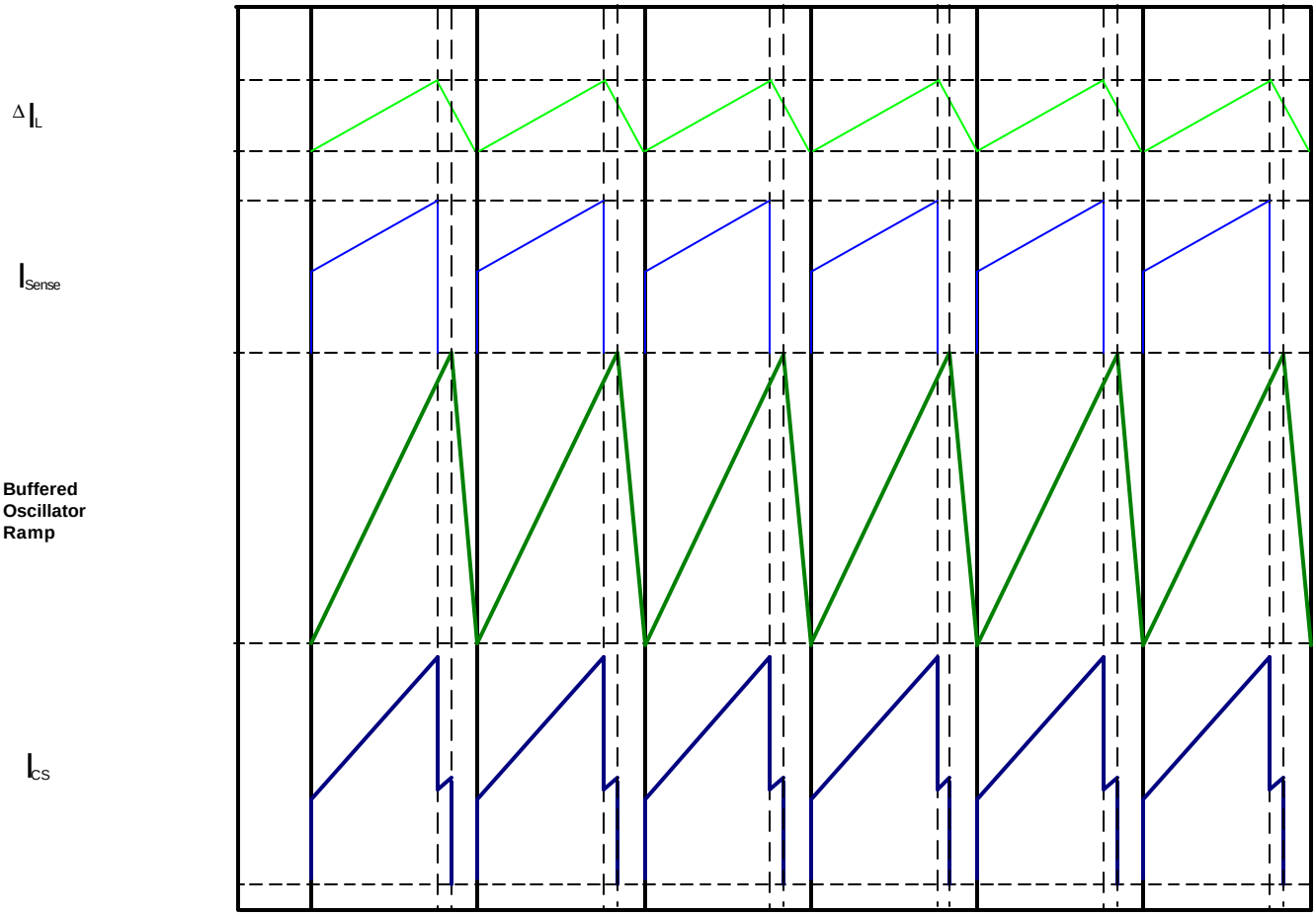
I_{Sense} : Sensed Mosfet current

I_{CS} : Summation of Isense and slope compensation, at the CS pin of the SC4808.

Slope Compensation generation from Buffered Oscillator Ramp

D>50%

Note: Below wave forms are not to scale.



Application Information (Cont.)

Below the benefits from the slope compensation become apparent. The top wave form shows the stable operation before the perturbation. The second wave form shows the perturbation and the instability caused from it if no slope compensation is added to the current information. The last wave form shows the slope compensation and the effect of it. The increase in the slope of the current information results in an early termination of the inductor current, hence a reduction in the amount of error. As the cycle is repeated, the perturbation is reduced and finally eliminated.

$d i_L$: Small Inductor current perturbation

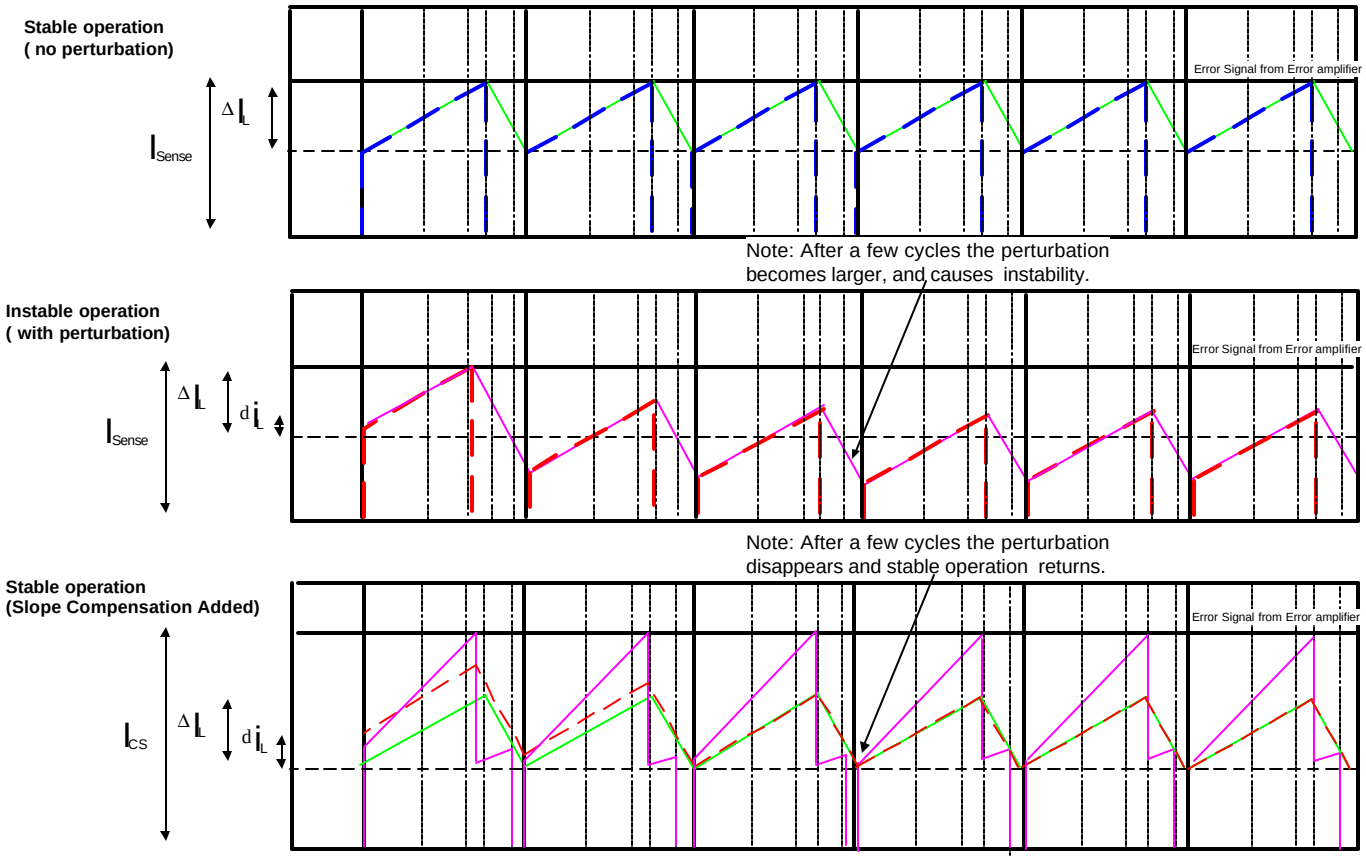
ΔI_L : Inductor current

I_{Sense} : Sensed Mosfet current

I_{CS} : Summation of Isense and slope compensation, at the CS pin of the SC4808.

Stable current mode operation with Slope Compensation

D>50%



Application Information (Cont.)

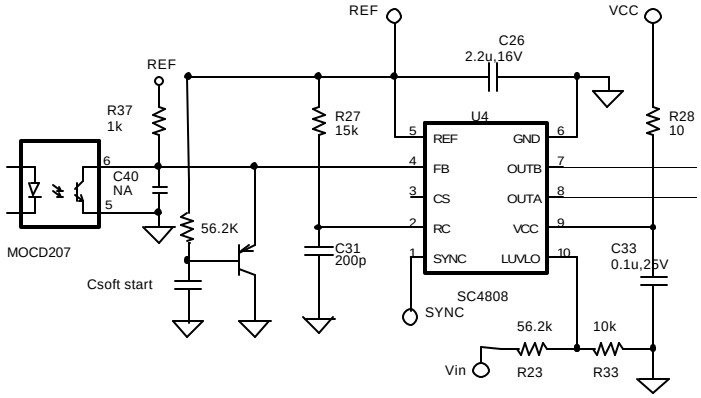
SOFT START

During start up of the converter, the discharged output capacitor and the load current have large supply current requirements. To avoid this a soft start scheme is usually implemented where the duty cycle of the regulator is gradually increased from 0% until the soft start duration is elapsed.

SC4808B-2 has an internal soft start circuit that limits the duty cycle for a duration approximated by the formula below. Also the soft start circuitry is activated if an over current condition occurs. After an over current condition, OUTA and OUTB are disabled and kept low for a duration of about 140µs. After the delay, the OUTA and OUTB are enabled while the soft start limits the duty cycle. If the over current condition persists, the soft start cycle repeats indefinitely. Approximate internal soft start duration can be calculated as below:

$$T_{SoftStart} \cong \frac{(Ramp_{SoftStart}) \times \left(\frac{VREF}{2}\right)}{\left(\frac{R_{Internal\_SlopeComp}}{R_{CS\_to\_GND}} + 1\right)}$$

If longer soft start durations are required, the simple external circuit shown below can be implemented.



Approximate soft start duration can be calculated as below:

$$T_{SoftStart} \cong C_{SoftStart} \times R37$$

START UP SEQUENCE

Initially during the power up, the SC4808B-2 is in under voltage lock out condition. As the Vcc supply exceeds the UVLO limit of the SC4808B-2, the internal reference, oscillator, and logic circuitry are powered up.

The OUTA and OUTB drivers are not enabled until the line under voltage lock out limit is reached. At that point, once the FB pin is above 1.5V, soft start circuitry starts the output drivers, and gradually increases the duty cycle from 0%. The soft start duration is internally set (see formula in Soft Start section).

As the output voltage starts to increase, the error signal from the error amplifier starts to decrease. If isolation is required, the error amplifier output can drive the LED of the opto isolator. The output of the opto is connected in a common emitter configuration with a pull-up resistor to a reference voltage connected to the FB pin of the SC4808B-2. The voltage level at the FB pin provides the duty cycle necessary to achieve regulation.

If an over current condition occurs, the outputs are disabled and after a soft start delay time of about 100µs, the softstart sequence mentioned above is repeated.

Application Information (Cont.)

LAYOUT GUIDELINES

Careful attention to layout requirements are necessary for successful implementation of the SC4808B-2 PWM controller.

High current switching is present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1). The high power parts of the circuit should be laid out first. A ground plane should be used, the number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, such as the input capacitor and FET ground.

2). In the loop formed by the Input Capacitor(s) (Cin), the FET must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically “cleaner” grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.

3). The connection between FETs and the Transformer should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI.

4) The Output Capacitor(s) (Cout) should be located as close to the load as possible. Fast transient load currents are supplied by Cout only, and connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

5) The SC4808B-2 is best placed over a quiet ground plane area. Avoid pulse currents in the Cin FET loop flowing in this area. GND should be returned to the ground plane close to the package and close to the ground side of (one of) the VCC supply capacitor(s). Under no circumstances should GND be returned to a ground inside the Cin, Q1, Q2 loop. Avoid making a star connection between the quiet GND planes that the SC4808B-2 will be connected to and the noisy high current GND planes connected to the FETs.

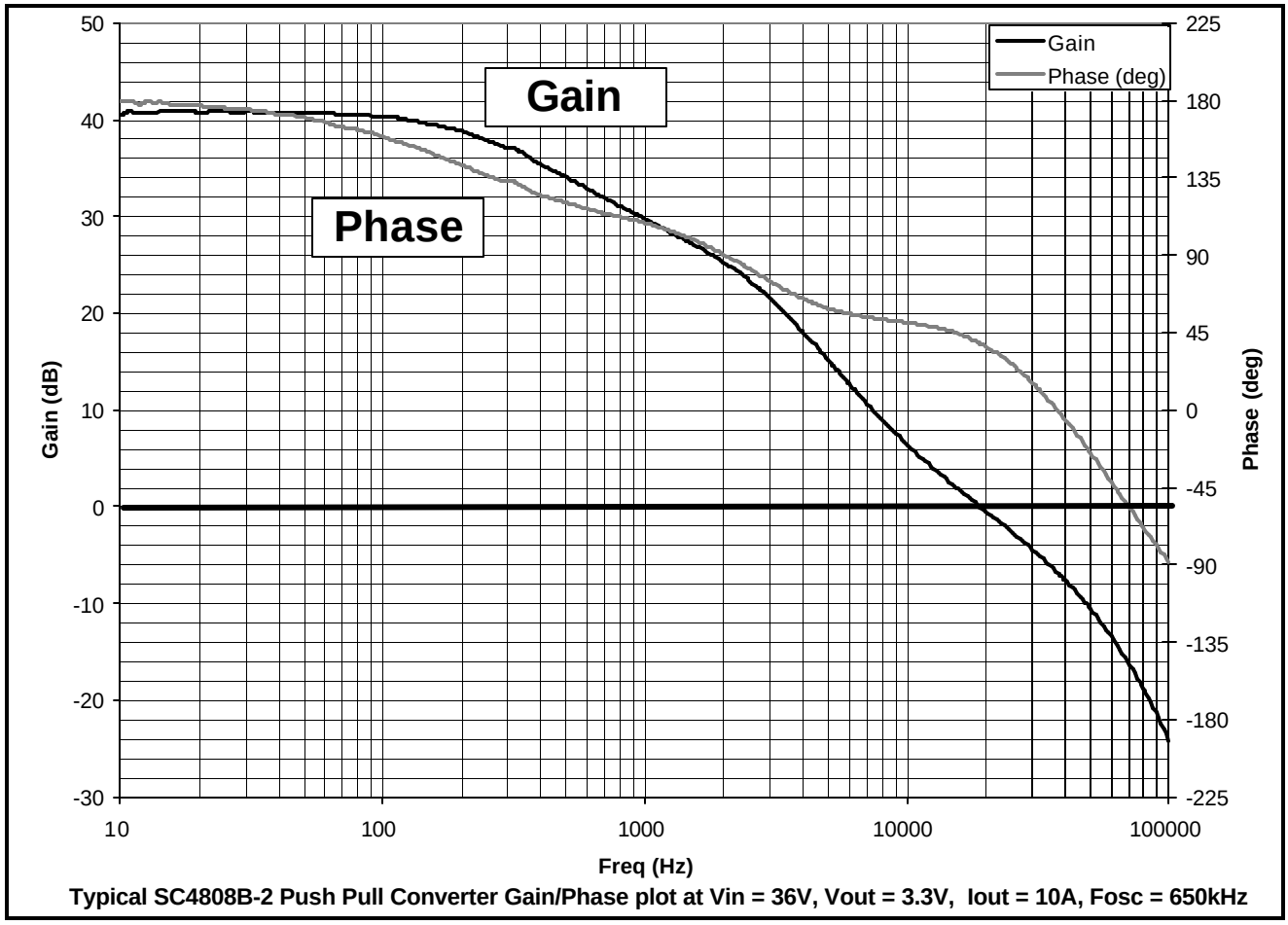
6) The feed back connection between the error amplifier and the FB pin should be kept as short as possible The GND connections should be connected to the quiet GND used for the SC4808B-2.

7) If an Opto isolator is used for isolation, quiet primary and secondary ground planes should be used. The same precautions should be followed for the primary GND plane as mentioned in item 5 mentioned above. For the secondary GND plane, the GND plane method mentioned in item 4 should be followed.

8) All the noise sensitive components such as LUVLO resistive divider, reference by pass capacitor, Vcc bypass capacitor, current sensing circuitry, feedback circuitry, and the oscillator resistor/capacitor network should be connected as close as possible to the SC4808B-2. The GND return should be connected to the quiet SC4808B-2 GND plane.

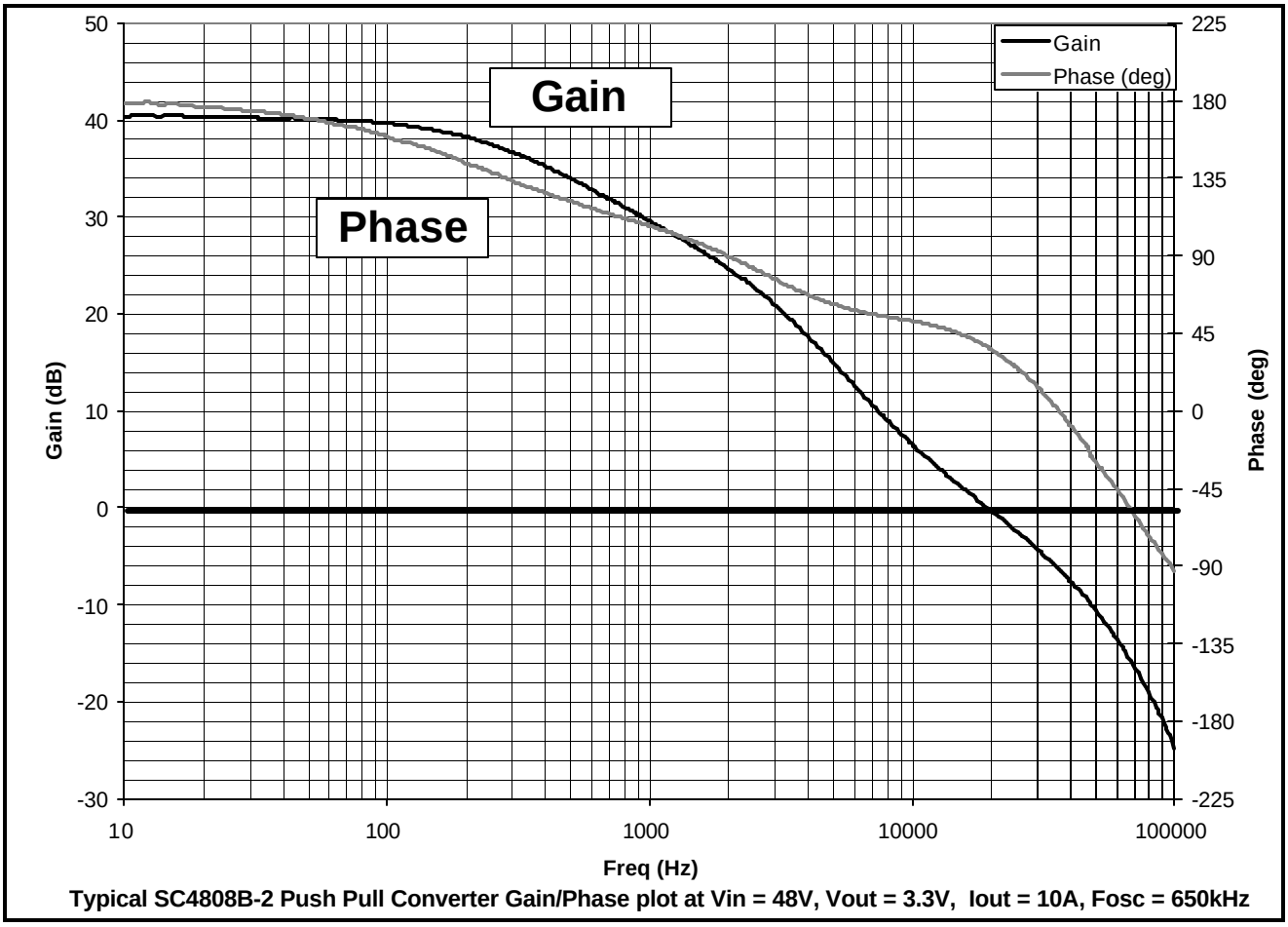
9) The connection from the OUTA and OUTB of the SC4808B-2 should be minimized to avoid any stray inductance. If the layout can not be optimized due to constraints, a small Schottky diode may be connected from the OUTA/B pins to the ground directly at the IC. This will clamp excessive negative voltages at the IC. If drivers are used, the Schottky diodes should be connected directly at the IC from the output of the driver to the driver ground (See page 9).

10) If the SYNC function is not used, the SYNC pin should be grounded at the SC4808B-2 GND to avoid noise pick up.



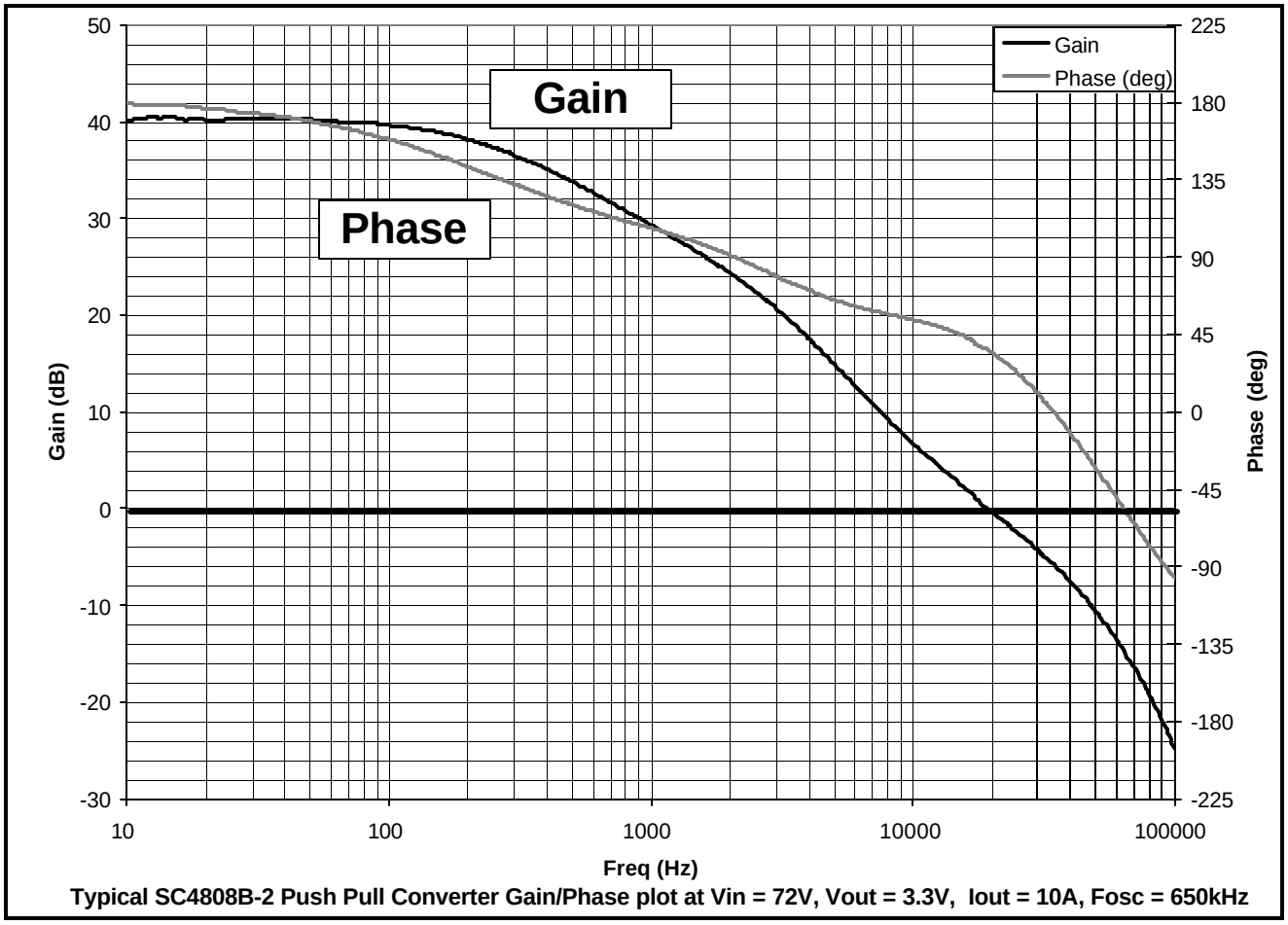
Typical SC4808B-2 Push Pull Converter Gain/Phase plot at Vin = 36V, Vout = 3.3V, Iout = 10A, Fosc = 650kHz

Gain & Phase Margin (Cont.)



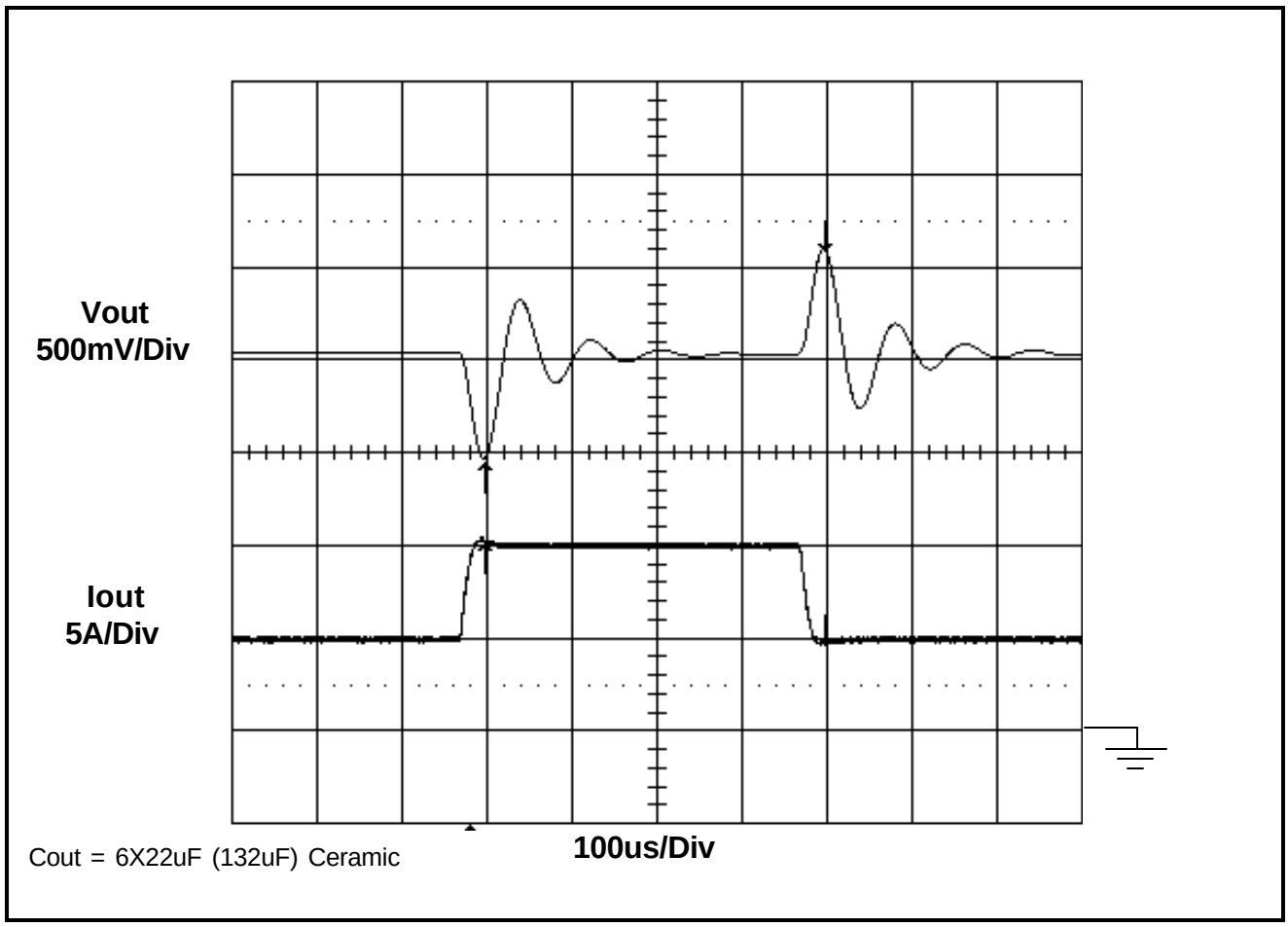
Typical SC4808B-2 Push Pull Converter Gain/Phase plot at Vin = 48V, Vout = 3.3V, Iout = 10A, Fosc = 650kHz

Gain & Phase Margin (Cont.)



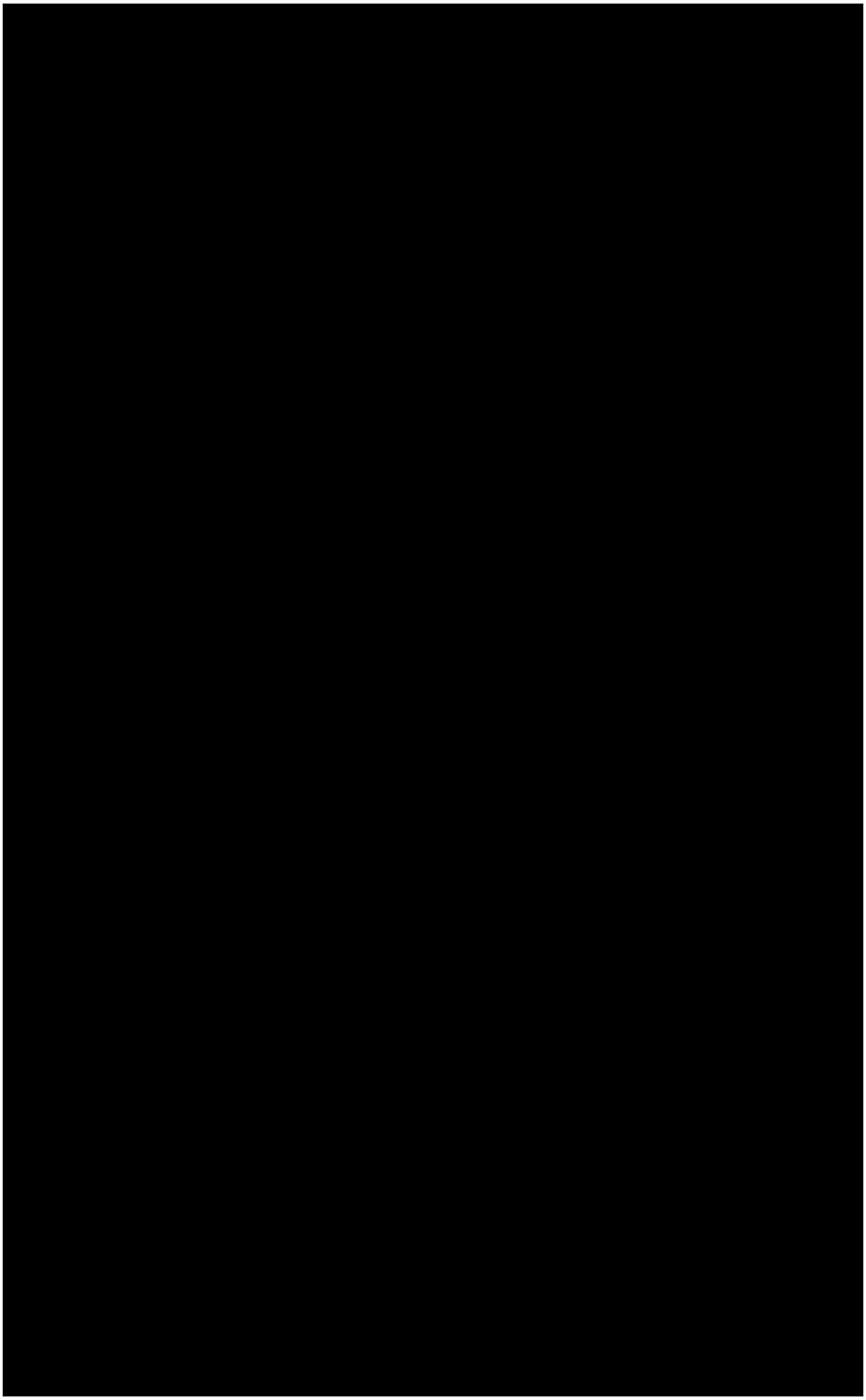
Typical SC4808B-2 Push Pull Converter Gain/Phase plot at Vin = 72V, Vout = 3.3V, Iout = 10A, Fosc = 650kHz

Typical Step Load



Typical SC4808B-2 Push Pull Converter Step Load plot at Vin = 48V, Vout = 3.3V, Step = 37% to 75% Iout, Fosc = 650kHz

Evaluation Board Schematics



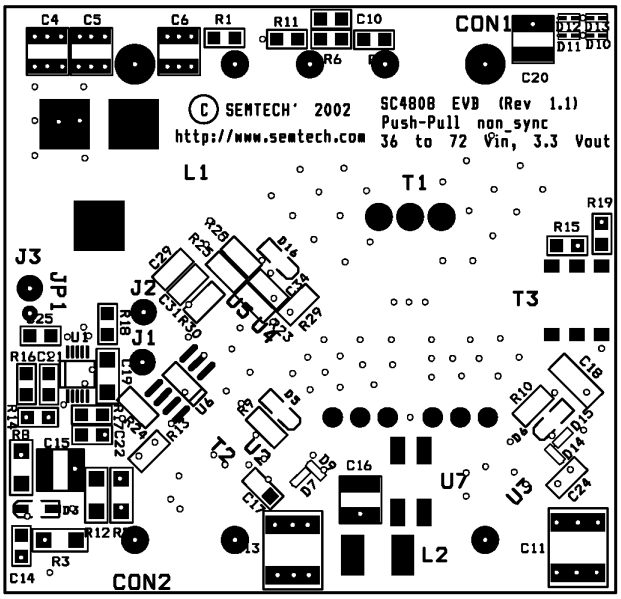
Evaluation Board Bill of Materials

SC4808 Push Pull 3.3V 50W non Synchronous
SC4808EVB__non_sync Revision: 1.1

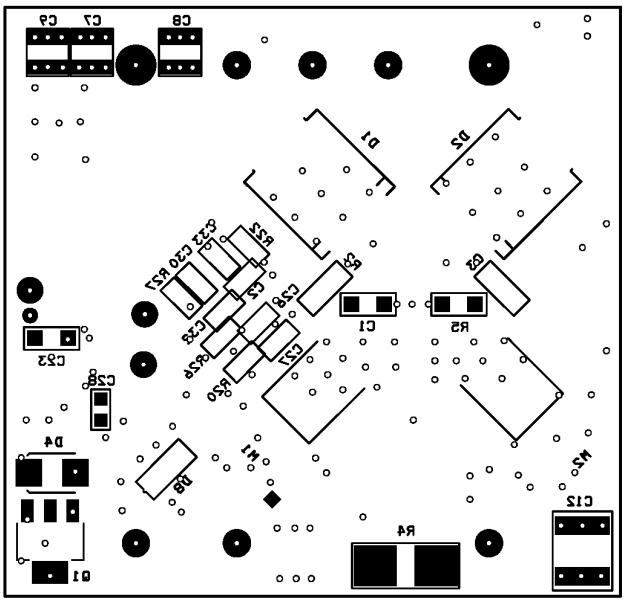
Bill Of Materials October 7,2002 13:35:18

Item	Quantity	Reference	Part	Manufacturer #	Foot Print
1	1	CON1	5output_half_brick		CON\5OUTPUT_HALF_BRICK
2	1	CON2	3input_half_brick		CON\3INPUT_HALF_BRICK
3	2	C3,C1	2.2n		SM/C_1206
4	6	C2,C10,C17,C24,C26,C32	0.1u		SM/C_0805
5	6	C4,C5,C6,C7,C8,C9	22u,6.3V	GRM32DR60J226KA01	SM/C_1210_GRM
6	3	C11,C12,C13	1u,100V	GRM55DR72E105KW01	SM/C_2220
7	1	C14	.1u,16V		SM/C_0805
8	2	C15,C16	10u,16V	GRM32DR61C106KA01	SM/C_1210_GRM
9	1	C18	22nF		SM/C_1206
10	1	C19	2.2u,16V		SM/C_1206
11	1	C20	1u,16V	GRM32RR71H105KA011	SM/C_1210_GRM
12	2	C22,C21	82p		SM/C_0805
13	1	C23	0.1u,25V		SM/C_1206
14	1	C25	10nF		SM/C_0805
15	2	C27,C33	22n		SM/C_0805
16	1	C28	NA		SM/C_0805
17	1	C29	100pF		SM/C_0805
18	1	C30	1nF		SM/C_0805
19	1	C31	470pF		SM/C_0805
20	1	C34	.1uF		SM/C_0805
21	1	C35	2.2uF 16V		SM/C_0805
22	2	D2,D1	MBRB2535CTL		DIODE_D2PAK
23	4	D3,D5,D6,D16	1N5819HW		SOD123
24	1	D4	ZM4743A		SMB/DO214
25	8	D7,D9,D10,D11,D12,D13, D14,D15	CMOSH-3	CMOSH-3 (Central Semiconductor)	SOD523
26	1	D8	LS4448		SM/DO213AC
27	1	JP1	short		VIA\2P
28	1	J1	REF		ED5052
29	1	J2	Vcc		ED5052
30	1	J3	SYNC		ED5052
31	1	L1	0.9uH		PG0006
32	1	L2	LQH43MN102K011	LQH43MN102K01L	SDIP0302
33	2	M1,M2	SUD19N20-90	SUD19N20-90	DPAKFET
34	1	Q1	FZT853		SM/SOT223_BCEC
35	1	Q2	FMMT718		
36	4	R1,R7,R15,R19	0		SM/R_0805
37	2	R5,R2	10		SM/R_1206
38	1	R3	20k		SM/R_1206
39	1	R4	250		SM/R_1210_MCR
40	2	R6,R11	TBD		SM/R_0805
41	1	R8	0		SM/R_1206
42	2	R9,R10	2.2		SM/R_0805
43	1	R12	56.2k		SM/R_1206
44	1	R13	10k		SM/R_0805
45	1	R14	15		SM/R_0805
46	2	R16,R24	1k		SM/R_0805
47	3	R17,R27,R30	15k		SM/R_0805
48	1	R18	10		SM/R_0805
49	2	R26,R20	2.2k		SM/R_0805
50	1	R21	10k		SM/R_1206
51	1	R22	37.4k		SM/R_0805
52	1	R23	18.2k		SM/R_0805
53	1	R25	11.5k		SM/R_0805
54	1	R28	25.5k		SM/R_0805
55	1	R29	100		SM/R_0805
56	1	R31	16.2		SM/R_1206
57	1	R32	56.2k		SM/R_0805
58	1	T1	PA0500		PA0500
59	1	T2	P8208T		P8208T
60	1	T3	PE-68386		PE-68386
61	1	U1	SC4808		MSOP10
62	2	U2,U3	SC1301A		SOT23_5PIN
63	2	U4,U5	SC4431		SOT23_5PIN
64	1	U6	MOCD207		SO-8
65	1	U7	CBRHD-02		CBRHD-02

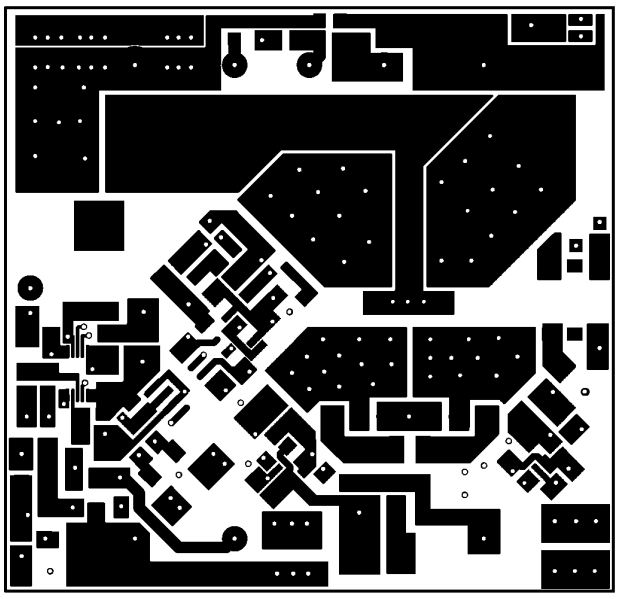
Evaluation Board Gerber Plots



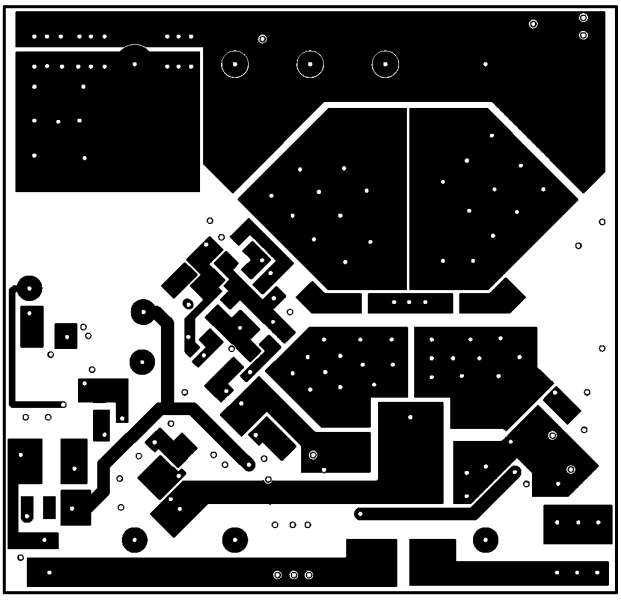
Board Layout Assembly Top



Board Layout Assembly Bottom

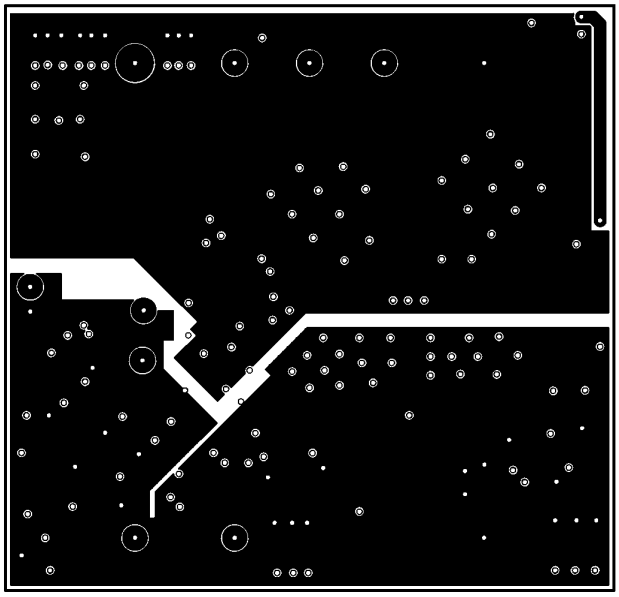


Board Layout Top

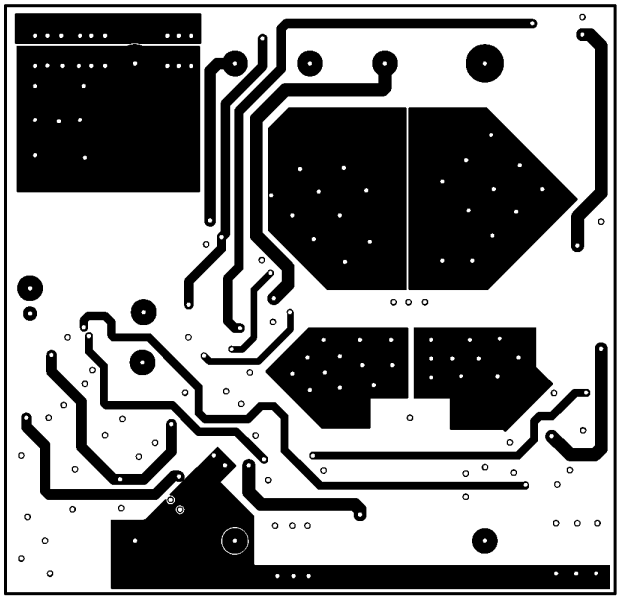


Board Layout Bottom

Evaluation Board Gerber Plots

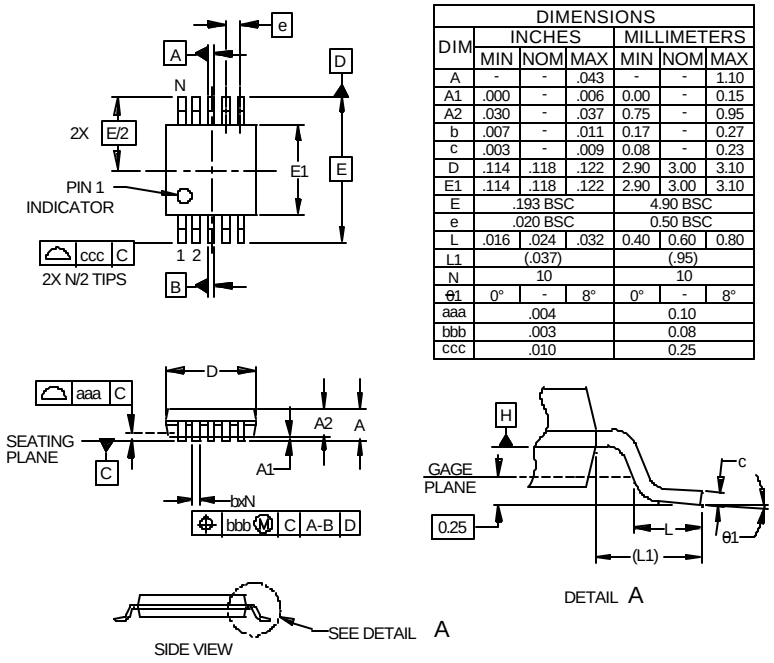


Board Layout INNER1



Board Layout INNER2

Outline Drawing - MSOP-10

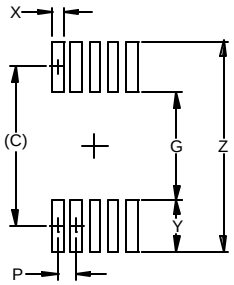


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.007	-	.011	0.17	-	0.27
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.020 BSC			0.50 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	10			10		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.003			0.08		
ccc	.010			0.25		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION BA.

Land Pattern - MSOP-10



DIM	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.020	0.50
X	.011	0.30
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804