Pin Configuration

```
         VEE ☐ 1 ○        20 ☐ CLKA0
      CLK_EN ☐ 2          19 ☐ CLKA0#
     CLK_SEL ☐ 3          18 ☐ VDDO
     REF_IN0+ ☐ 4         17 ☐ CLKA1
     REF_IN0- ☐ 5         16 ☐ CLKA1#
     REF_IN1+ ☐ 6         15 ☐ CLKB0
     REF_IN1- ☐ 7         14 ☐ CLKB0#
          NC ☐ 8          13 ☐ VDDO
     M_RESET ☐ 9          12 ☐ CLKB1
         VDD ☐ 10         11 ☐ CLKB1#
```

Pinout Table

| Pin No.	Pin Name	I/O Type		Description
1	V_{EE}	Power		Negative supply pin
2	CLK_EN	Input	Pull up	Synchronous clock enable. When High, clock outputs follow REF_IN. When low, CLK outputs are forced low, CLK# are forced high
3	CLK_SEL	Input	Pull-down	Clock Select input. When HIGH, selects REF_IN1. When LOW, selects REF_IN0.
4	REF_IN0+	Input	Pull-down	Reference input 0
5	REF_IN0-	Input	Pull Up	Inverted reference input 0
6	REF_IN1+	Input	Pull-down	Reference input 1
7	REF_IN1-	Input	Pull up	Inverted reference input 1
8	NC	-	-	No connect
9	M_RESET	Input	Pull-down	Master Reset pin. Active High. When logic High, CLKAn and CLKBn go low and CLKAn# and CLKBn# go high. When logic Low, outputs are enabled.
10	V_{DD}	Power		Core power supply
11	CLKB1#	Output		Differential output, LVPECL signalling level
12	CLKB1	Output	-	Differential output, LVPECL signalling level
13, 18	V_{DDO}	Power		Output power supply
14	CLKB0#	Output	-	Differential output, LVPECL signalling level
15	CLKB0	Output		Differential output, LVPECL signalling level
16	CLKA1#	Output		Differential output, LVPECL signalling level
17	CLKA1	Output		Differential output, LVPECL signalling level
19	CLKA0#	Output		Differential output, LVPECL signalling level
20	CLKA0	Output		Differential output, LVPECL signalling level

Pin Characteristics

Symbol	Parameter	Min	Typ	Max	Units
C_{IN}	Input Capacitance		4		pF
R_{PULLUP}	Input Pullup Resistor		51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor		51		kΩ

Control Inputs

Inputs				Outputs	
M_RESET	CLK_EN	CLK_SEL	SOURCE	CLKA0, CLKA1, CLKB0, CLKB1	CLKA0#, CLKA1#, CLKB0#, CLKB1#
1	X	X	X	LOW	HIGH
0	0	0	REF_IN0, REF_IN0#	Disabled, LOW,	Disabled, HIGH
0	0	1	REF_IN1, REF_IN1#	Disabled, LOW,	Disabled, HIGH
0	1	0	REF_IN0, REF_IN0#	Enabled	Enabled
0	1	1	REF_IN1, REF_IN1#	Enabled	Enabled

CLK_EN Timing Diagram
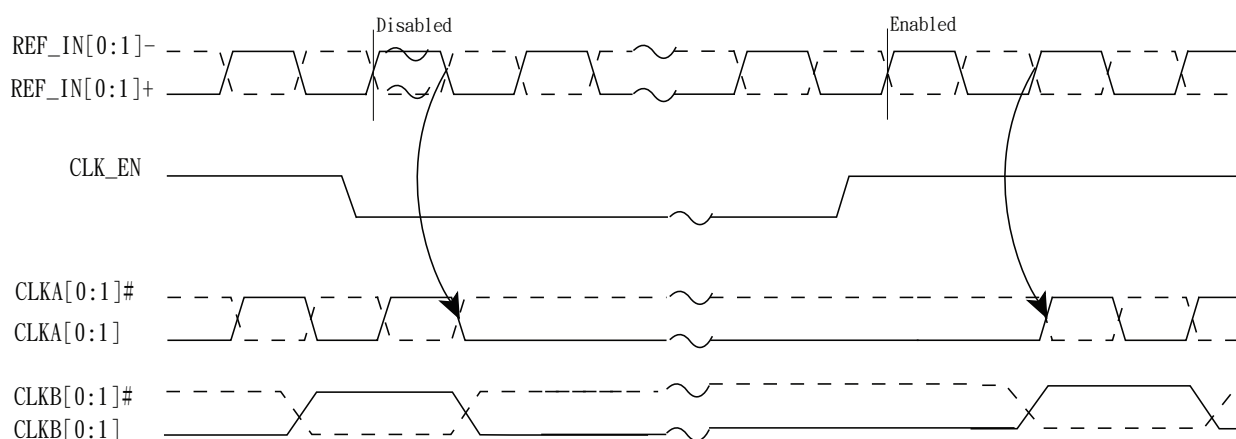
Maximum Ratings (Over operating free-air temperature range)

Storage Temperature... -65°C to+155°C

Ambient Temperature with Power Applied.........-40°C to+85°C

Supply Voltage (relative to VEE)..............................-0.5 to +3.7V

ESD Protection (HBM) 2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

Power Supply DC Characterisitcs, (T_A = -40°C to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Core Supply Voltage		3.0	3.3	3.6	V
			2.375	2.5	2.625	
V_{DDO}	Output Supply Voltage		3.0	3.3	3.6	V
			2.375	2.5	2.625	
I_{EE}	Power Supply Current				115	mA
I_{DD}	Power Supply Current				100	mA

LVCMOS/LVTTL DC Characteristics, (T_A = -40°C to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage	V_{DD} = 3.3 V +/- 10%	2		3.765	V
		V_{DD} = 2.5 V +/- 5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	V_{DD} = 3.3 V +/- 10%	-0.3		0.8	V
		V_{DD} = 2.5 V +/- 5%	-0.3		0.7	V
I_{IH}	Input High Current	CLK_EN V_{DD} = VIN = 3.63V			30	µA
		M_RESET, IN_SEL, Ref_IN V_{DD} = VIN = 3.63V			150	
I_{IL}	Input Low Current	CLK_EN V_{DD} = 3.63V, V_{IN} = 0V	-150			µA
		M_RESET, IN_SEL, Ref_IN V_{DD} = 3.63V, V_{IN} = 0V	-30			

Differential input DC Characteristics (T_A = -40°C to 85°C)

Symbols	Parameters		Test Conditions	Min.	Typ	Max.	Units
I_{IH}	Input High Current	REF_IN-	$V_{DD} = V_{IN}$ =3.465V			5	uA
		REF_IN+	$V_{DD} = V_{IN}$ =3.465V			150	
I_{IL}	Input Low Current	REF_IN-	V_{DD} = 3.465V or 2.625V V_{IN} = 0V	-150			uA
		REF_IN+		-5			uA
V_{PP}	Peak-to-Peak Input Voltage [1]		V_{DD} = 3.3V	0.15		1.3	V
			V_{DD} = 2.5V	0.25		1.3	
V_{CMR}	Common Mode Input Voltage [1,2]		V_{DD} = 3.3V and 2.5V	V_{EE} + 0.5		V_{DD} - 0.85	V

Notes:

1. For single ended applications, $V_{IH} = V_{DD} + 0.3V$.

2. Common mode voltage is defined as V_{IH}.

LVPECL Output DC Characterisitcs, (T_A = -40ºC to 85ºC)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output High Voltage[1]	V_{DDO} = 3.3V	1.9		2.4	V
		V_{DDO} = 2.5V	1.5		1.7	
V_{OL}	Output Low Voltage[1]	V_{DDO} = 3.3V	1.3		1.8	V
		V_{DDO} = 2.5V	0.8		1.1	

Note: 1. LVPECL Termination: Source 150ohm to GND and 100ohm across CLK and CLK#.

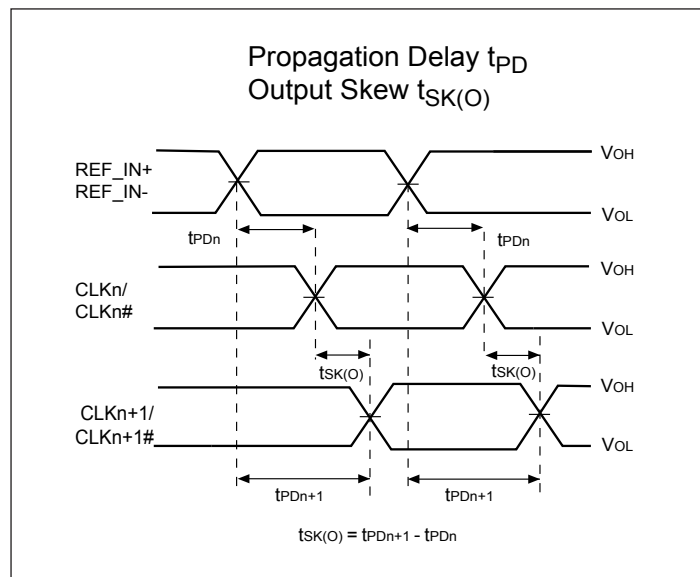## AC Electrical Characteristics, $(T_A = -40^oC \text{ to } 85^oC)$

Under the test configurations shown in figures

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
f_{OUT}	Output Frequency				650	MHz
t_R / t_F	Output Rise/Fall Time	20% to 80%, 3.3V operation, ≤ 312.5MHz	200		700	ps
		20% to 80%, 2.5V operation, ≤ 312.5MHz	160		700	ps
$t_{SK(O)}$	Output Skew	Outputs at the same loading, same bank @ 156.25MHz			65	ps
t_{PD}	Propagation Delay	From differential input to the differential output cross point, CLKA	0.8		2.0	ns
$t_{jit(A\varnothing)}$	Additive Phase Jitter, (Random)[1]	156.25MHz, (12kHz - 20MHz)		30		fs
		312.5MHz, (12kHz - 20MHz)		30		fs
o_{DC}	Output Duty Cycle	Measured at 156.25MHz	48	50	52	%
V_{PP}	Output Swing	LVPECL outputs, Single-ended, 3.3V operation	0.55		1.1	V
		LVPECL outputs, Single-ended, 2.5V operation	0.5		0.75	

Note:
1. Please refer to the Phase Noise Plots.

Propagation Delay and Output Skew

Propagation Delay t_{PD}
Output Skew $t_{SK(O)}$

REF_IN+
REF_IN−

V_{OH}
V_{OL}

t_{PDn} t_{PDn}

CLKn/
CLKn#

V_{OH}
V_{OL}

$t_{SK(O)}$ $t_{SK(O)}$

CLKn+1/
CLKn+1#

V_{OH}
V_{OL}

t_{PDn+1} t_{PDn+1}

$t_{SK(O)} = t_{PDn+1} - t_{PDn}$

Part to Part Skew

Part-to-Part Skew $t_{SK(P)}$

REF_IN+
REF_IN−

V_{OH}
V_{OL}

t_{PD1} t_{PD1}

Part1
CLK/CLK#

V_{OH}
V_{OL}

T_{SK} T_{SK}

Part2
CLK/CLK#

V_{OH}
V_{OL}

T_{PD2} T_{PD2}

$t_{SK(P)} = t_{PD2} - T_{PD1}$

Output Duty Cycle

Duty Cycle o_{DC}

t_{PW}

CLKn/
CLKn#

V_{OH}
V_{OL}

t_{PERIOD}

$o_{DC} = (t_{PW} / t_{PERIOD}) \times 100\%$
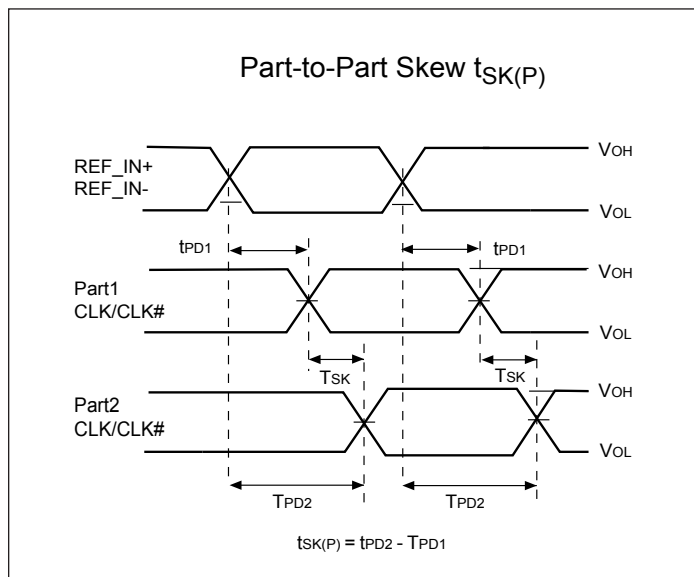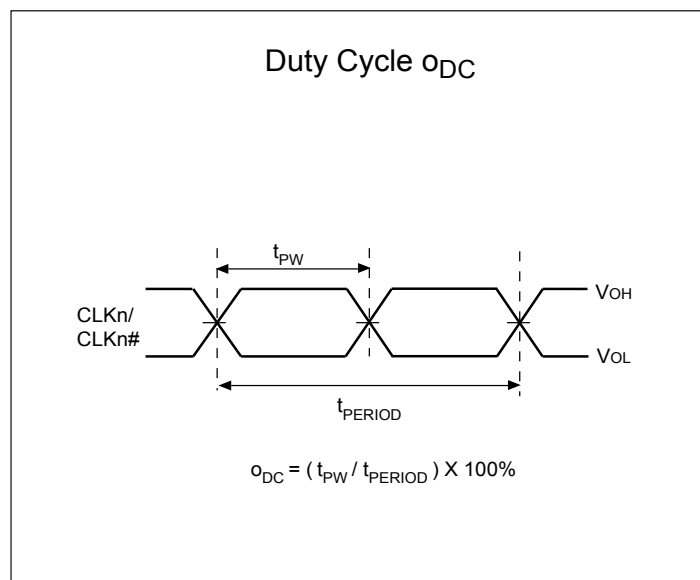
Phase Noise Plots
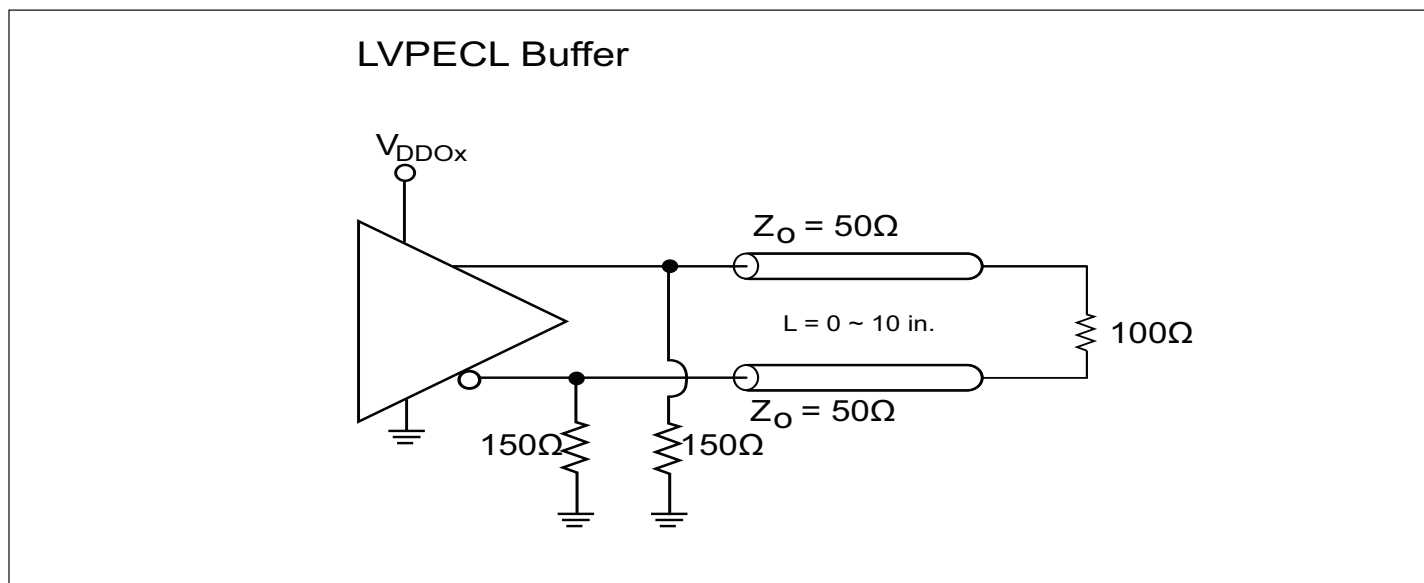
f_{OUT} = 156.25MHz

Output phase noise (Dark Blue) vs Input Phase noise (light blue)

Additive jitter is calculated at 156.25MHz~23fs RMS (12kHz to 20MHz). Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$
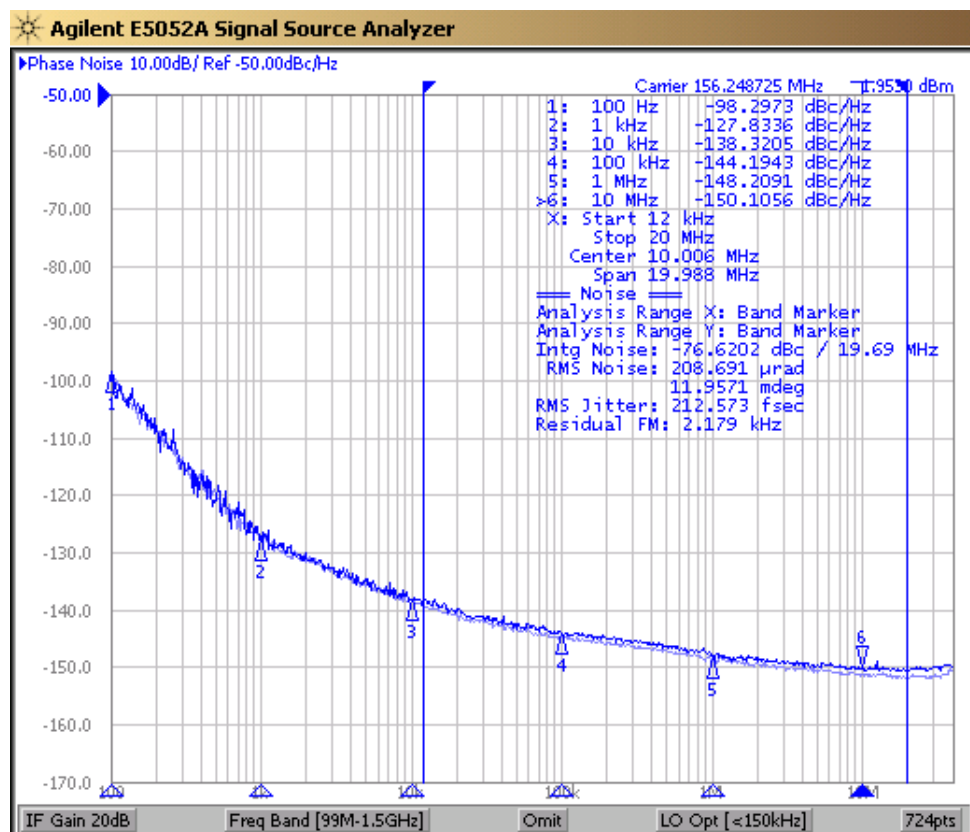
LVPECL Test Circuit

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The PI6C4911504D2 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.1µF bypass capacitors should be used for each pin. Figure below illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.
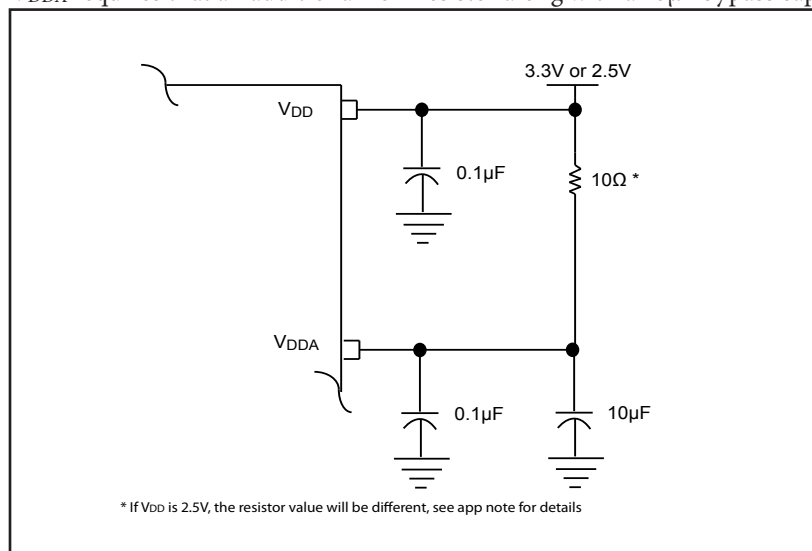
Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage $V\_REF = V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to postion the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R1/R2 = 0.609.
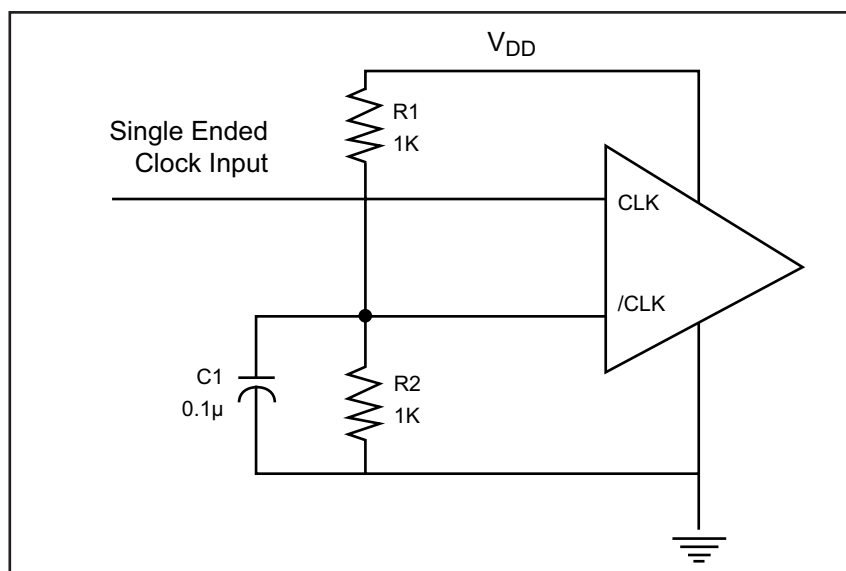

Figure 1. Single-ended input to Differential input device

Recommendations for Unused Input and Output Pins

Inputs:

CRef_IN Input:

For applications not requiring the use of the clock, it can be left floating. A 1kΩ resistor tied from the Ref_IN to ground can provide additional protection.
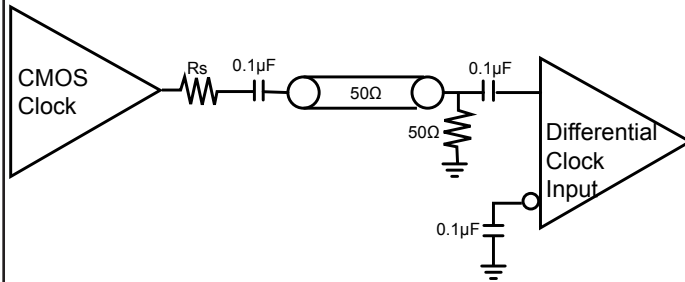
LVCMOS Control Pins:

All control pins have internal pulldowns; A 1kΩ resistor tied from each control pin to ground can provide additional protection.
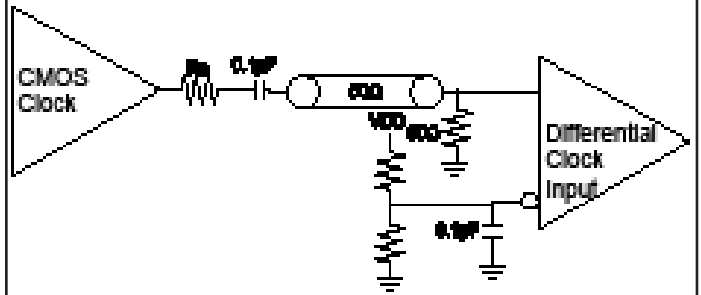
Outputs:

LVPECL Outputs:

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.
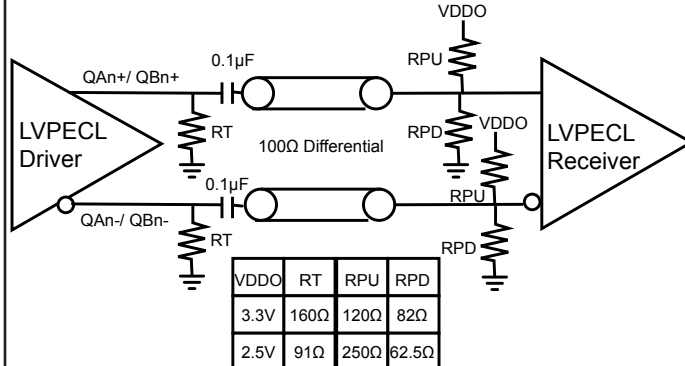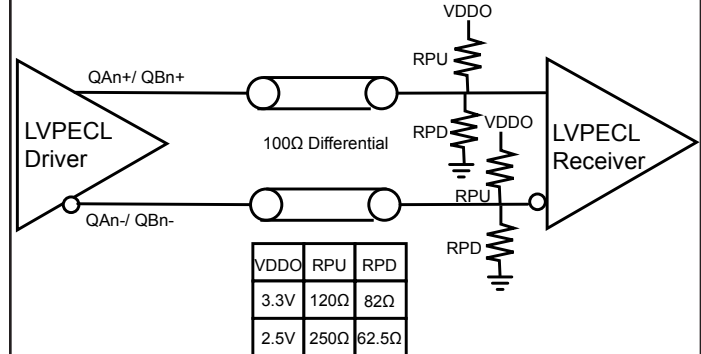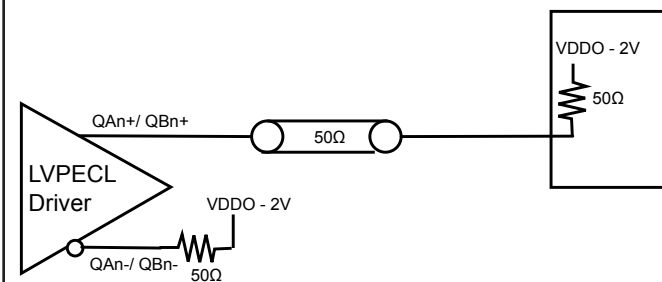
PERICOM®

Single Ended Input, AC couple

CMOS Clock
Rs
0.1µF
50Ω
50Ω
0.1µF
0.1µF
Differential Clock Input

Single Ended Input, DC couple

CMOS Clock
0.1µF
50Ω
VDDO
Differential Clock Input

LVPECL, AC Couple, Thevenin Equivalent

LVPECL Driver
QAn+/ QBn+
0.1µF
RT
100Ω Differential
QAn-/ QBn-
0.1µF
RT
VDDO
RPU
RPD
VDDO
RPU
RPD
LVPECL Receiver

VDDO	RT	RPU	RPD
3.3V	160Ω	120Ω	82Ω
2.5V	91Ω	250Ω	62.5Ω

LVPECL, DC Couple, Thevenin Equivalent

LVPECL Driver
QAn+/ QBn+
100Ω Differential
QAn-/ QBn-
VDDO
RPU
RPD
VDDO
RPU
RPD
LVPECL Receiver

VDDO	RPU	RPD
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

Single Ended LVPECL, DC Couple

LVPECL Driver
QAn+/ QBn+
50Ω
VDDO - 2V
50Ω
QAn-/ QBn-
VDDO - 2V
50Ω

Single Ended LVPECL, DC Couple, Thevenin Equivalent

LVPECL Driver
QAn+/ QBn+
50Ω
VDDO - 2V
RPU
RPD
VDDO
RPU
RPD
QAn-/ QBn-

VDDO	RPU	RPD
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω
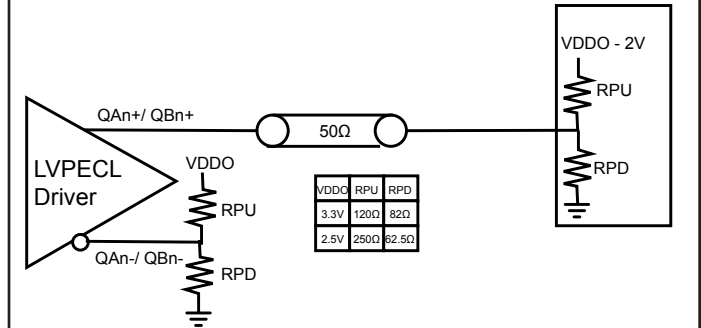
Single Ended LVPECL, AC Couple, Thevenin Equivalent
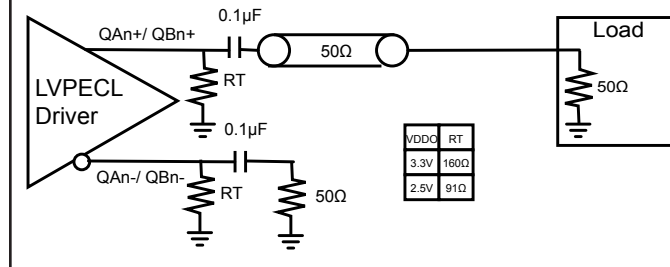
Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	84.0 ^{O}C/W
Θ_{JC}	Junction-to-case thermal resistance		17.0 ^{O}C/W

Packaging Mechanical: 20-Contact TSSOP (L)

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)			
SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	–	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Notes:
1. Refer JEDEC MO-153F/AC
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

PERICOM	DATE: 05/03/12
Enabling Serial Connectivity	

DESCRIPTION: 20-pin, 173mil Wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1311	REVISION: F

12-0373

Ordering Information

Ordering Code	Packaging Type	Package Description	Operating Temperature
PI6C4911504D2LIE	L	Pb-free & Green, 20-pin TSSOP	Industrial
PI6C4911504D2LIEX	L	Pb-free & Green, 20-pin TSSOP, Tape & reel	Industrial

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging