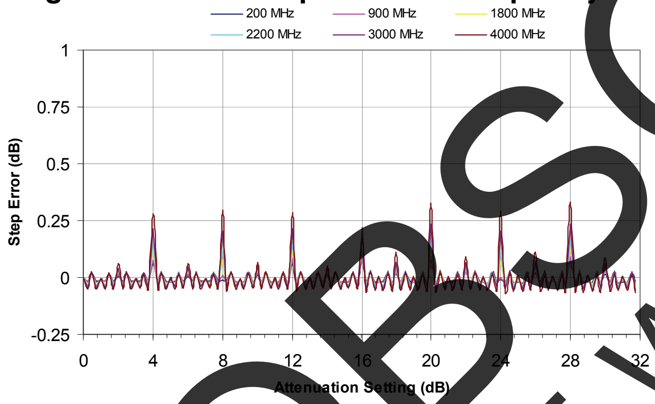
Table 1. Electrical Specifications @ +25°C, V_{DD} = 3.3 V or 5.0 V

Parameter	Test Conditions	Frequency	Min	Typical	Max	Units
Frequency Range			9 kHz		4.0 GHz	
Attenuation Range	0.25 dB Step			0 – 31.75		dB
Insertion Loss		9 kHz - 4 GHz		2.0	2.5	dB
Attenuation Error	0 dB - 7.75 dB Attenuation settings 8 dB - 31.75 dB Attenuation settings	9 kHz - 4 GHz 9 kHz - 4 GHz			±(0.2 + 3%) ±(0.3 + 4%)	dB dB
Return Loss		9 kHz - 4 GHz		18		dB
Relative Phase	All States	9 kHz - 4 GHz		44		deg
P1dB (note 1)	Input	20 MHz - 4 GHz	30	32		dBm
IIP3	Two tones at +18 dBm, 20 MHz spacing	20 MHz - 4 GHz		57		dBm
Typical Spurious Value		1MHz		-110		dBm
Video Feed Through				10		mVpp
Switching Time	50% DC CTRL to 10% / 90% RF			650		ns
RF Trise/Tfall	10% / 90% RF			400		ns
Settling Time	RF settled to within 0.05 dB of final value. RBW = 5 MHz, Averaging ON.			4		µs

Note 1. Please note Maximum Operating Pin (50Ω) of +23dBm as shown in Table 3.

Performance Plots

Figure 3. 0.25dB Step Error vs. Frequency*



*Monotonicity is held so long as Step-Error does not cross below -0.25

Figure 4. 0.25dB Attenuation vs. Attenuation State

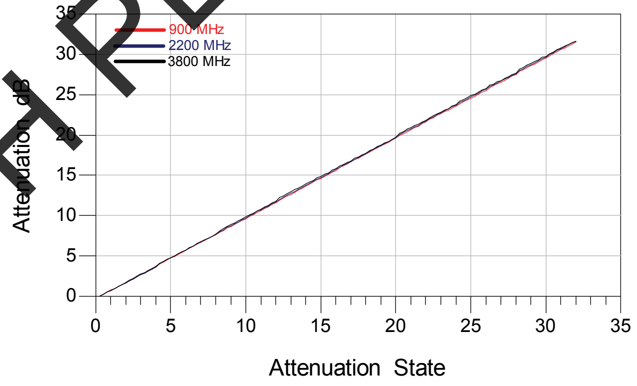


Figure 5. 0.25dB Major State Bit Error

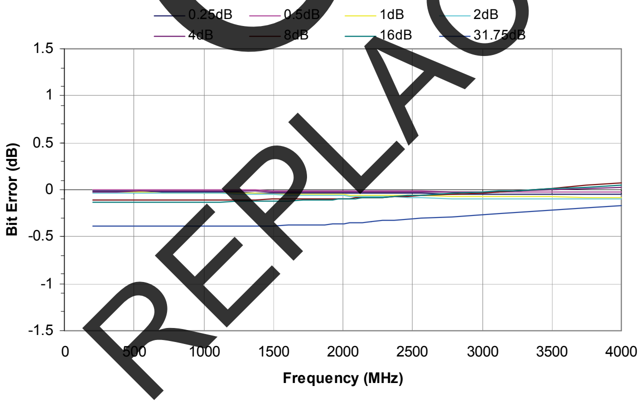


Figure 6. 0.25dB Attenuation Error vs. Frequency

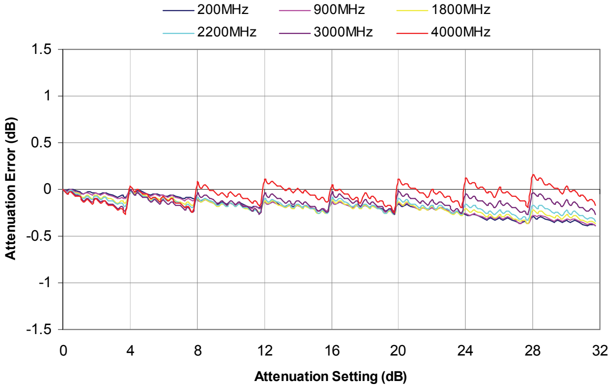


Figure 7. Insertion Loss vs. Temperature

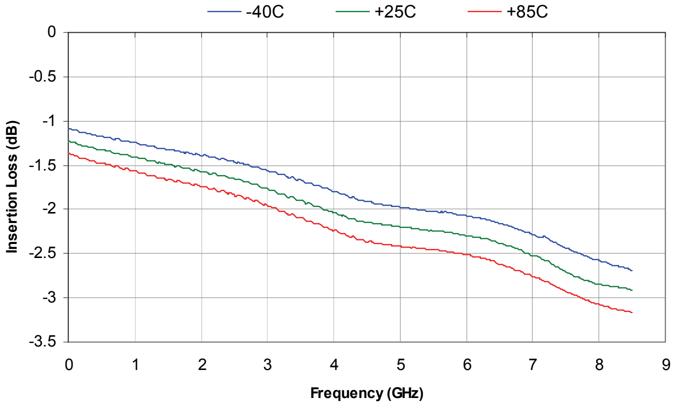


Figure 8. Input Return Loss vs. Attenuation @ T = +25C

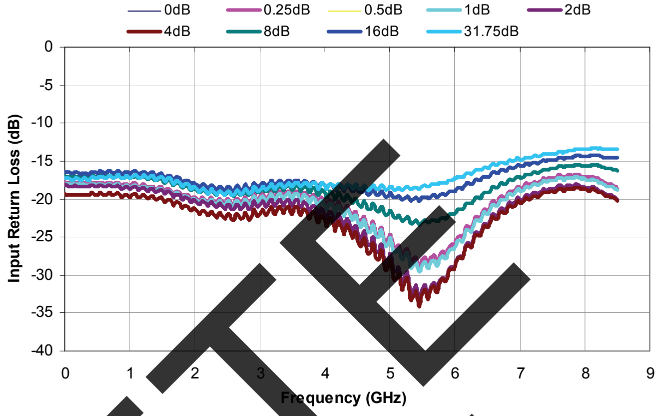


Figure 9. Output Return Loss vs. Attenuation @ T = +25C

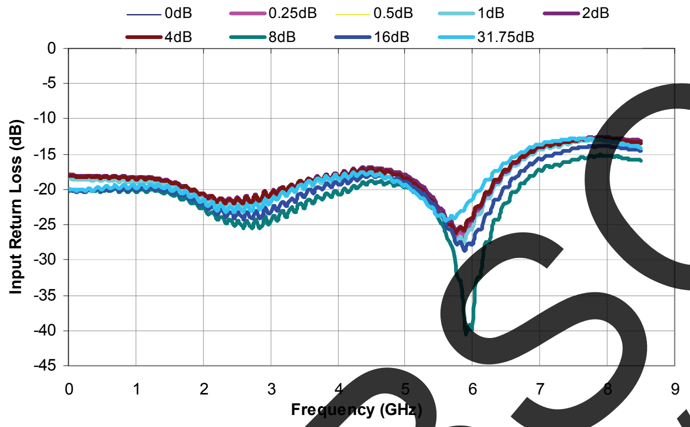


Figure 10. Relative Phase vs. Frequency

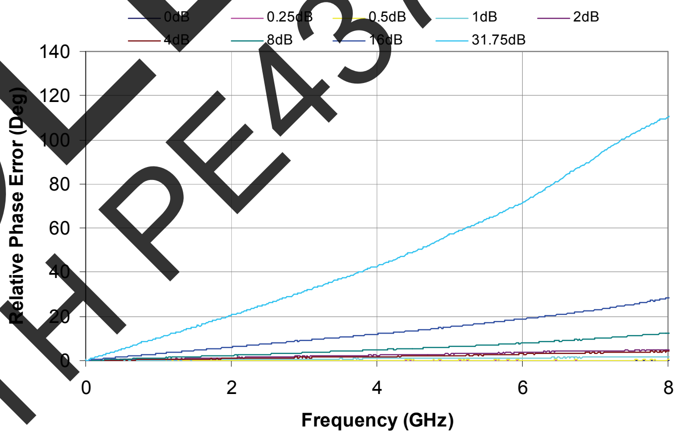


Figure 11. Attenuation Error vs. Temperature @ 4 GHz

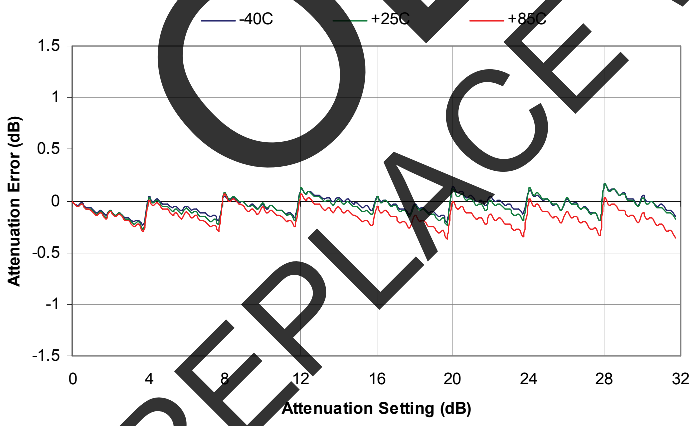


Figure 12. Input IP3 vs. Frequency

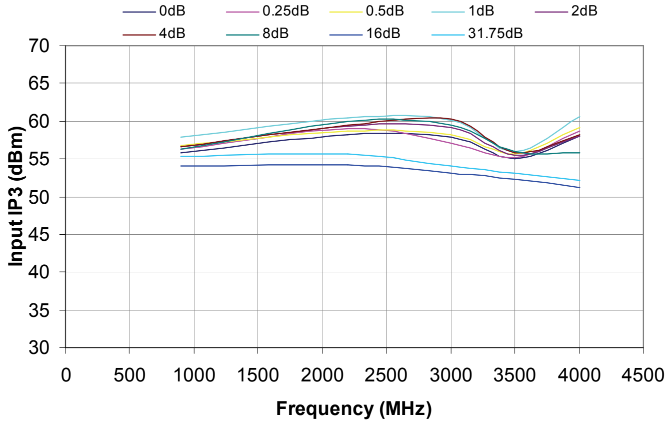


Figure 13. Pin Configuration (Top View)

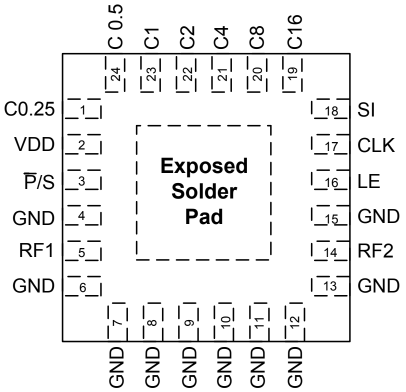


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	C0.25 (D0)	Attenuation control bit, 0.25 dB
2	V_{DD}	Power supply pin
3	$\overline{P}$/S	Serial/Parallel mode select
4	GND	Ground
5	RF1	RF1 port
6 - 13	GND	Ground
14	RF2	RF2 port
15	GND	Ground
16	LE	Serial interface Latch Enable input
17	CLK	Serial interface Clock input
18	SI	Serial interface Data input
19	C16 (D6)	Parallel control bit, 16 dB
20	C8 (D5)	Parallel control bit, 8 dB
21	C4 (D4)	Parallel control bit, 4 dB
22	C2 (D3)	Parallel control bit, 2 dB
23	C1 (D2)	Parallel control bit, 1 dB
24	C0.5 (D1)	Parallel control bit, 0.5 dB
Paddle	GND	Ground for proper operation

Note: Ground C0.25, C0.5, C1, C2, C4, C8, C16 if not in use.

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE43702 in the 24-lead 4x4 QFN package is MSL1.

Switching Frequency

The PE43702 has a maximum 25 kHz switching rate. Switching rate is defined to be the speed at which the DSA can be toggled across attenuation states.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	3.0	3.3		V
V_{DD} Power Supply Voltage		5.0	5.5	V
I_{DD} Power Supply Current		50	350	µA
Digital Input High	2.6		5.5	V
P_{IN} Input power (50Ω): 9 kHz ≤20 MHz 20 MHz ≤4 GHz			*Fig. 14* +23	dBm dBm
T_{OP} Operating temperature range	-40	25	85	°C
Digital Input Low	0		1	V
Digital Input Leakage[1]			15	µA

Note 1. Input leakage current per Control pin

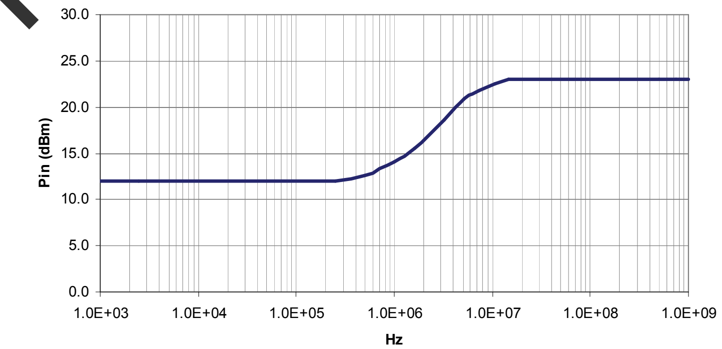
Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	6.0	V
V_I	Voltage on any Digital input	-0.3	5.8	V
T_{ST}	Storage temperature range	-65	150	°C
P_{IN}	Input power (50Ω) 9 kHz ≤20 MHz 20 MHz ≤4 GHz		*Fig. 14* +23	dBm dBm
V_{ESD}	ESD voltage (HBM)[1] ESD voltage (Machine Model)		500 100	V V

Note: 1. Human Body Model (HBM, MIL_STD 883 Method 3015.7)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Figure 14. Maximum Power Handling Capability



Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Table 5. Control Voltage

State	Bias Condition
Low	0 to +1.0 Vdc at 2 μA (typ)
High	+2.6 to +5 Vdc at 10 μA (typ)

Table 6. Latch and Clock Specifications

Latch Enable	Shift Clock	Function
0	↑	Shift Register Clocked
↑	X	Contents of shift register transferred to attenuator core

Table 7. Parallel Truth Table

Parallel Control Setting							Attenuation Setting RF1-RF2
D6	D5	D4	D3	D2	D1	D0	
L	L	L	L	L	L	L	Reference I.L.
L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	H	L	0.5 dB
L	L	L	L	H	L	L	1 dB
L	L	L	H	L	L	L	2 dB
L	L	H	L	L	L	L	4 dB
L	H	L	L	L	L	L	8 dB
H	L	L	L	L	L	L	16 dB
H	H	H	H	H	H	H	31.75 dB

Table 8. Serial Register Map

MSB (last in) ↓

LSB (first in) ↓

Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
D7	D6	D5	D4	D3	D2	D1	D0

Attenuation Word

▨ Bit must be set to logic low

Table 9. Serial Attenuation Word Truth Table

Attenuation Word								Attenuation Setting RF1-RF2
D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	
L	L	L	L	L	L	L	L	Reference I.L.
L	L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	L	H	L	0.5 dB
L	L	L	L	L	H	L	L	1 dB
L	L	L	L	H	L	L	L	2 dB
L	L	L	H	L	L	L	L	4 dB
L	L	H	L	L	L	L	L	8 dB
L	H	L	L	L	L	L	L	16 dB
L	H	H	H	H	H	H	H	31.75 dB

Attenuation Word is derived directly from the attenuation value. For example, to program the 12.5 dB state:

Attenuation Word: Multiply by 4 and convert to binary → 4 * 12.5 dB → 50 → 00110010
Serial Input: 00110010

Programming Options

Parallel/Serial Selection

Either a parallel or serial interface can be used to control the PE43702. The $\overline{P}$/S bit provides this selection, with $\overline{P}$/S=LOW selecting the parallel interface and $\overline{P}$/S=HIGH selecting the serial interface.

Parallel Mode Interface

The parallel interface consists of seven CMOS-compatible control lines that select the desired attenuation state, as shown in *Table 7*.

The parallel interface timing requirements are defined by *Fig. 16* (Parallel Interface Timing Diagram), *Table 11* (Parallel Interface AC Characteristics), and switching speed (*Table 1*).

For *latched*-parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (*per Fig. 16*) to latch new attenuation state into device.

For *direct* parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct Mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Serial Interface

The serial interface is a 8-bit serial-in, parallel-out shift register buffered by a transparent latch. The 8-bits make up the Attenuation Word that controls the DSA. *Fig. 15* illustrates a example timing diagram for programming a state.

The serial-interface is controlled using three CMOS-compatible signals: Serial-In (SI), Clock (CLK), and Latch Enable (LE). The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. Attenuation Word truth table is listed in *Table 9*. A programming example of the serial register is illustrated in *Table 8.* The serial timing diagram is illustrated in *Fig. 15.* It is required that all parallel pins be grounded when the DSA is used in serial mode.

Power-up Control Settings

The PE43702 will always initialize to the maximum attenuation setting (31.5 dB) on power-up for both the serial and latched-parallel modes of operation and will remain in this setting until the user latches in the next programming word. In direct-parallel mode, the DSA can be preset to any state within the 31.5 dB range by pre-setting the parallel control pins prior to power-up. In this mode, there is a 400-μs delay between the time the DSA is powered-up to the time the desired state is set. During this power-up delay, the device attenuates to the maximum attenuation setting (31.5 dB) before defaulting to the user defined state. If the control pins are left floating in this mode during power-up, the device will default to the minimum attenuation setting (insertion loss state).

Dynamic operation between serial and parallel programming modes is possible.

If the DSA powers up in serial mode ($\overline{P}$/S = HIGH), all the parallel control inputs DI[6:0] must be set to logic low. Prior to toggling to parallel mode, the DSA *must* be programmed serially to ensure D[7] is set to logic low.

If the DSA powers up in either latched or direct-parallel mode, all parallel pins DI[6:0] must be set to logic low prior to toggling to serial mode ($\overline{P}$/S = HIGH), and *held* low until the DSA has been programmed serially to ensure bit D[7] is set to logic low.

The sequencing is only required once on power-up. Once completed, the DSA may be toggled between serial and parallel programming modes at will.

Figure 15. Serial Timing Diagram

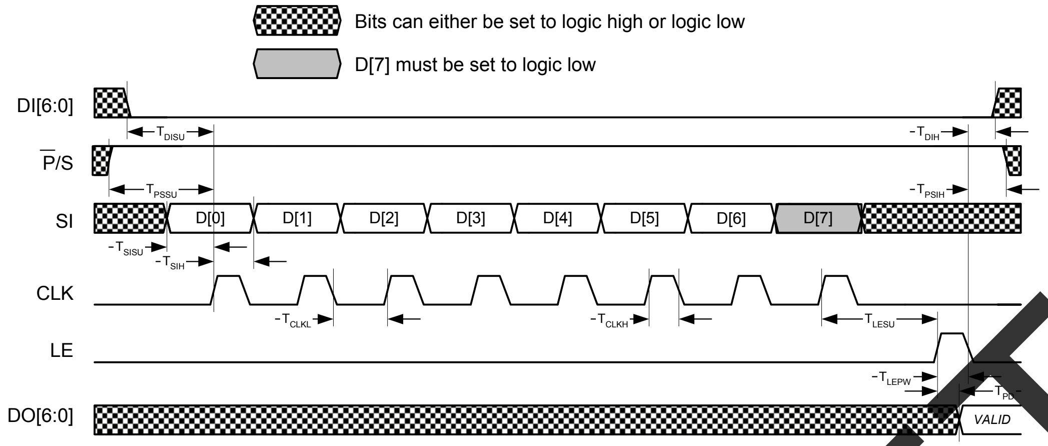


Figure 16. Latched-Parallel/Direct-Parallel Timing Diagram

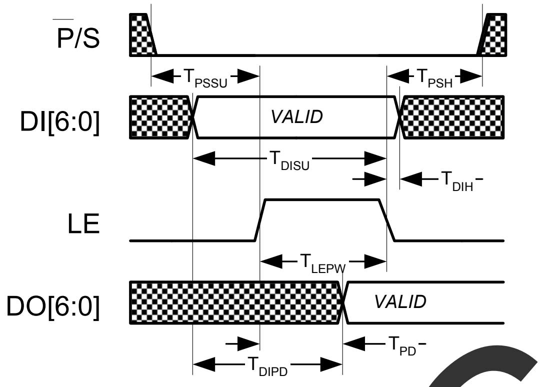


Table 10. Serial Interface AC Characteristics

V_{DD} = 3.3 or 5.0 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
F_{CLK}	Serial clock frequency	-	10	MHz
T_{CLKH}	Serial clock HIGH time	30	-	ns
T_{CLKL}	Serial clock LOW time	30	-	ns
T_{LESU}	Last serial clock rising edge setup time to Latch Enable rising edge	10	-	ns
T_{LEPW}	Latch Enable min. pulse width	30	-	ns
T_{SISU}	Serial data setup time	10	-	ns
T_{SIH}	Serial data hold time	10	-	ns
T_{DISU}	Parallel data setup time	100	-	ns
T_{DIH}	Parallel data hold time	100	-	ns
T_{ASU}	Address setup time	100	-	ns
T_{AH}	Address hold time	100	-	ns
T_{PSSU}	Parallel/Serial setup time	100	-	ns
T_{PSH}	Parallel/Serial hold time	100	-	ns
T_{PD}	Digital register delay (internal)	-	10	ns

Table 11. Parallel and Direct Interface AC Characteristics

V_{DD} = 3.3 or 5.0 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
T_{LEPW}	Latch Enable minimum pulse width	30	-	ns
T_{DISU}	Parallel data setup time	100	-	ns
T_{DIH}	Parallel data hold time	100	-	ns
T_{PSSU}	Parallel/Serial setup time	100	-	ns
T_{PSIH}	Parallel/Serial hold time	100	-	ns
T_{PD}	Digital register delay (internal)	-	10	ns
T_{DIPD}	Digital register delay (internal, direct mode only)	-	5	ns

Evaluation Kit

The Digital Attenuator Evaluation Kit board was designed to ease customer evaluation of the PE43702 Digital Step Attenuator.

Direct-Parallel Programming Procedure
For automated direct-parallel programming, connect the test harness provided with the EVK from the parallel port of the PC to the J1 & Serial header pin and set the D0-D6 SP3T switches to the 'MIDDLE' toggle position. Position the Parallel/Serial ($\overline{\text{P}}$/S) select switch to the Parallel (or left) position. The evaluation software is written to operate the DSA in either Parallel or Serial-Addressable Mode. Ensure that the software is set to program in *Direct-Parallel* mode. Using the software, enable or disable each setting to the desired attenuation state. The software automatically programs the DSA each time an attenuation state is enabled or disabled.

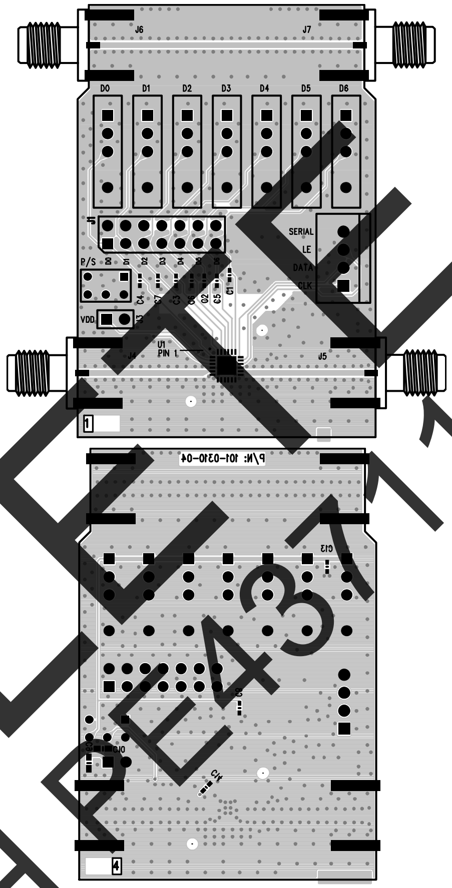
For manual direct-parallel programming, disconnect the test harness provided with the EVK from the J1 and Serial header pins. Position the Parallel/Serial ($\overline{\text{P}}$/S) select switch to the Parallel (or left) position. The LE pin on the Serial header must be tied to V_{DD}. Switches D0-D6 are SP3T switches which enable the user to manually program the parallel bits. When any input D0-D6 is toggled 'UP', logic high is presented to the parallel input. When toggled 'DOWN', logic low is presented to the parallel input. Setting D0-D6 to the 'MIDDLE' toggle position presents an OPEN, which forces an on-chip logic low. *Table 9* depicts the parallel programming truth table and *Fig. 16* illustrates the parallel programming timing diagram.

Latched-Parallel Programming Procedure
For automated latched-parallel programming, the procedure is identical to the direct-parallel method. The user only must ensure that *Latched-Parallel* is selected in the software.

For manual latched-parallel programming, the procedure is identical to direct-parallel except now the LE pin on the Serial header must be logic low as the parallel bits are applied. The user must then pulse LE from 0V to V_{DD} and back to 0V to latch the programming word into the DSA. LE must be logic low prior to programming the next word.

Figure 17. Evaluation Board Layout

Peregrine Specification 101-0310

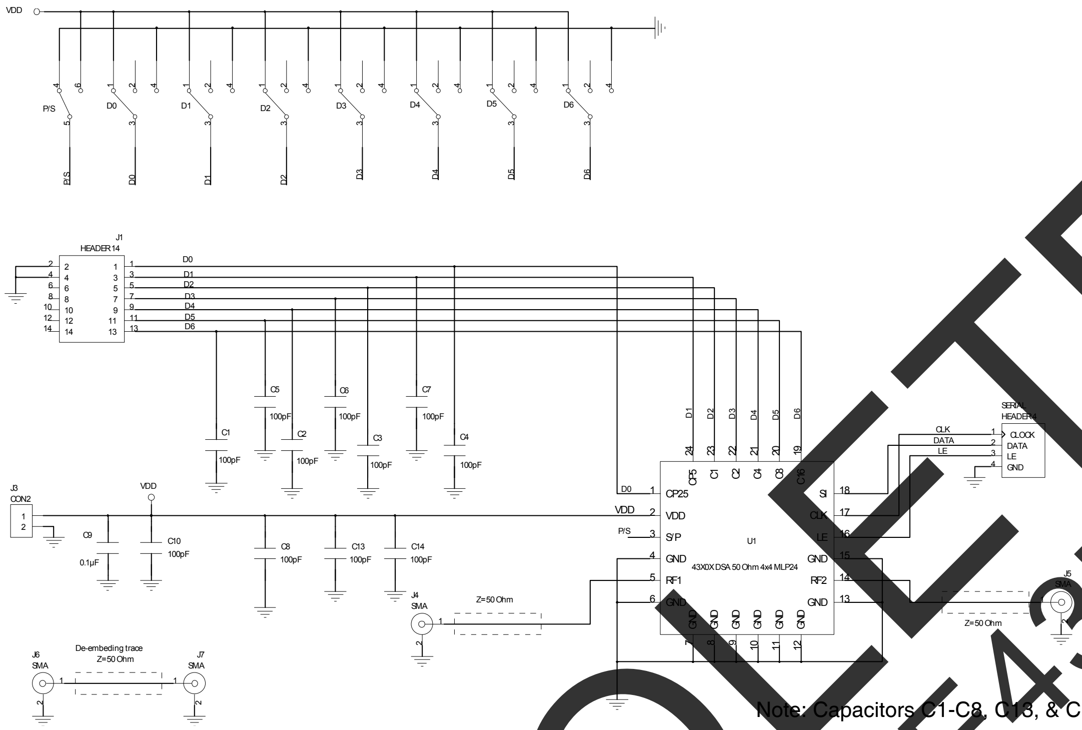


Note: Reference Figure 18 for Evaluation Board Schematic

Serial Programming Procedure
Position the Parallel/Serial ($\overline{\text{P}}$/S) select switch to the Serial (or right) position. The evaluation software is written to operate the DSA in either Parallel or Serial Mode. Ensure that the software is set to program in Serial mode. Using the software, enable or disable each setting to the desired attenuation state. The software automatically programs the DSA each time an attenuation state is enabled or disabled.

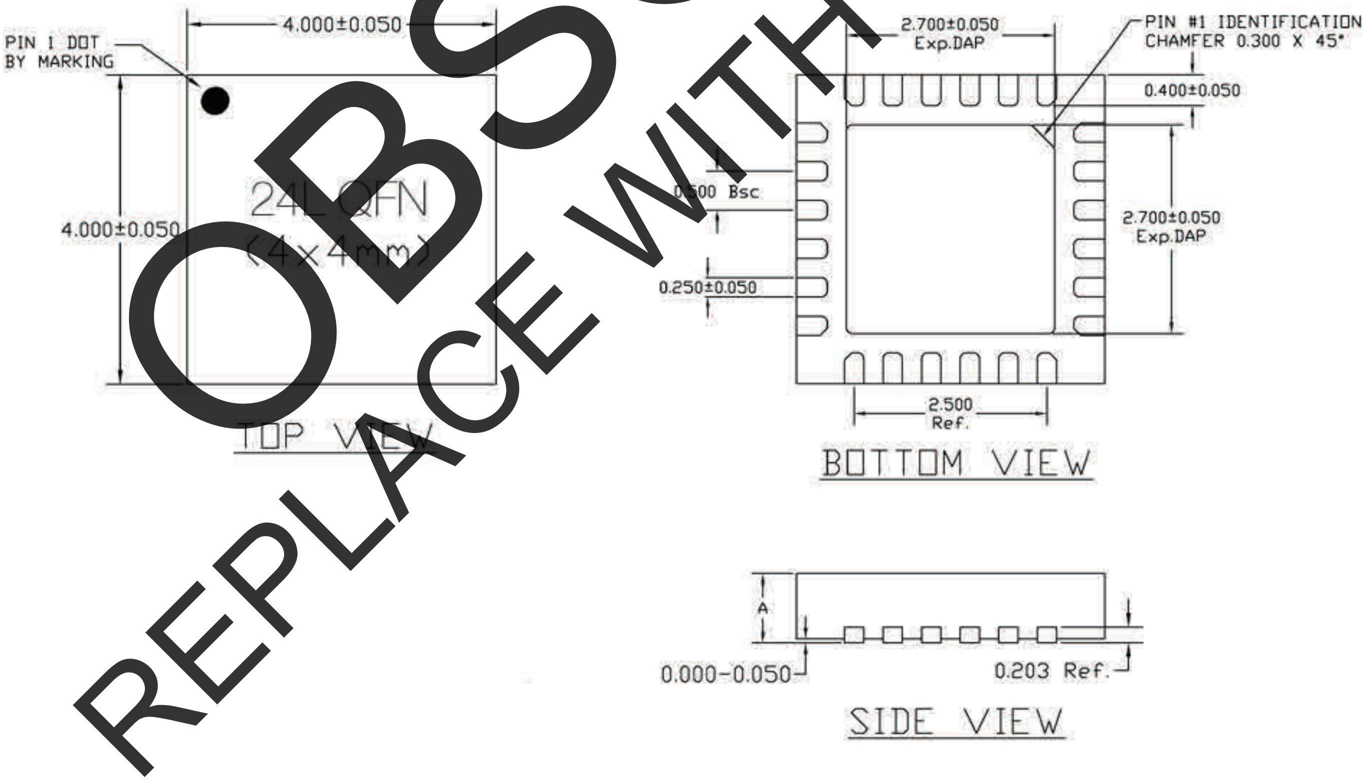
Figure 18. Evaluation Board Schematic

Peregrine Specification 102-0379



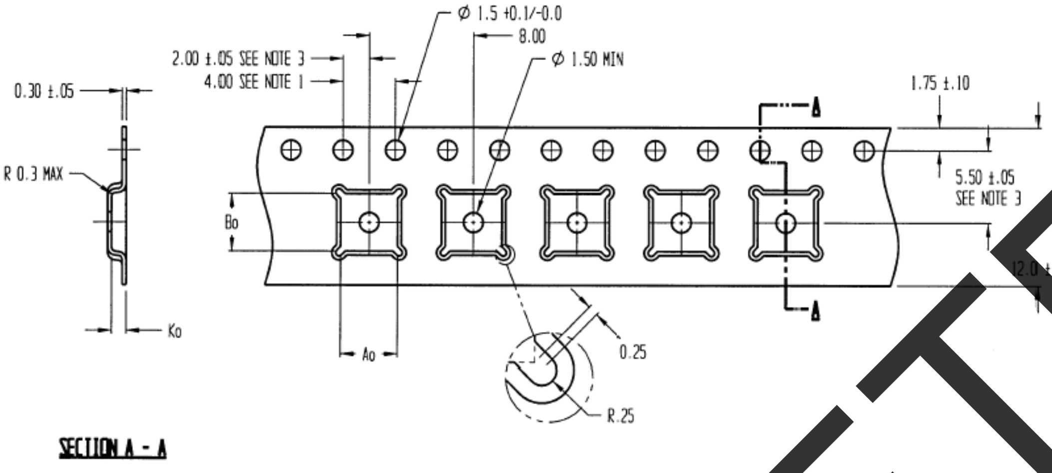
Note: Capacitors C1-C8, C13, & C14 may be omitted.

Figure 19. Package Drawing



Logo updated under non-rev change. Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com

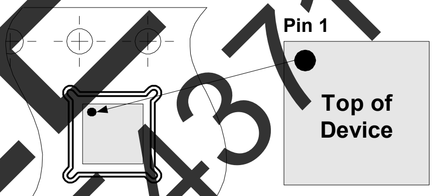
Figure 20. Tape and Reel Drawing



Tape Feed Direction

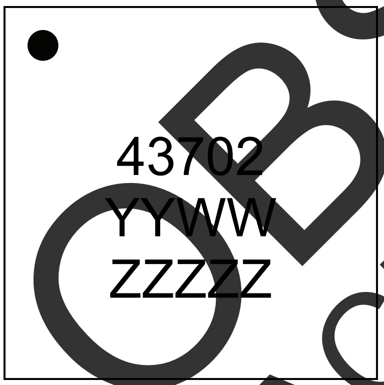
NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

A_0 = 4.35
B_0 = 4.35
K_0 = 1.1



Device Orientation in Tape

Figure 21. Marking Specifications



YYWW = Date Code
ZZZZZ = Last five digits of Lot Number

Table 12. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
PE43702MLI	43702	PE43702 G - 24QFN 4x4mm-75A	Green 24-lead 4x4mm QFN	Bulk or tape cut from reel
PE43702MLI-Z	43702	PE43702 G – 24QFN 4x4mm-3000C	Green 24-lead 4x4mm QFN	3000 units / T&R
EK43702-01	43702	PE43702 G – 24QFN 4x4mm-EK	Evaluation Kit	1 / Box

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For a list of representatives in your area, please refer to our Web site at: ***www.psemi.com***

Data Sheet Identification

Advance Information

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Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

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