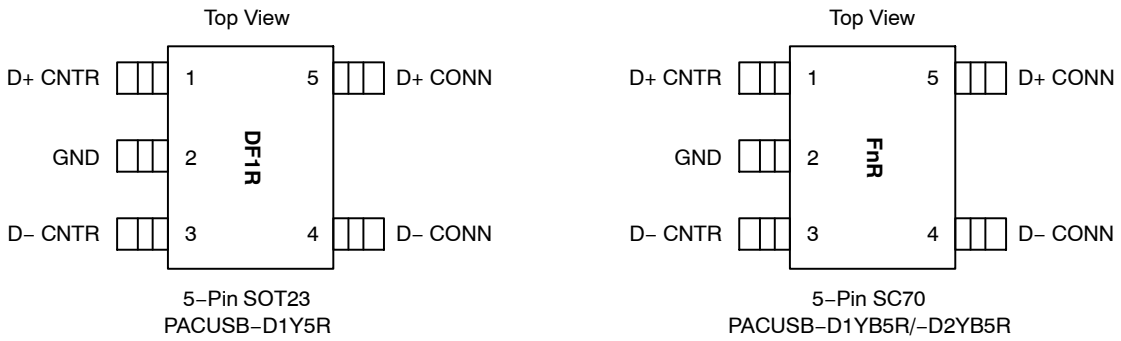
PACKAGE / PINOUT DIAGRAMS



5−Pin SOT23
PACUSB−D1Y5R

5−Pin SC70
PACUSB−D1YB5R/−D2YB5R

Note 1: The “n” shown in part markings above represents either the digit “1” or “2”.
Note 2: SOT23 and SC70 package sizes may differ. These drawing are not in scale.

Table 1. PIN DESCRIPTIONS

Pins	Name	Description
1	D+ CNTR	D+ Data to the USB Controller Circuitry
2	GND	Ground Pin
3	D− CNTR	D− Data to the USB Controller Circuitry
4	D− CONN	D− Data to the USB Connector
5	D+ CONN	D+ Data to the USB Connector

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Storage Temperature Range	−65 to +150	°C
Power Dissipation per Resistor	100	mW
Package Power Dissipation	200	mW
Voltage on any Pin (DC)	6	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature	−40 to +85	°C

SPECIFICATIONS (Cont'd)

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R1	Resistance of R1 Resistor (PACUSB−D2YB5R)	T_A = 25°C	12	15	18	Ω
R1	Resistance of R1 Resistor (PACUSB−D1Y5R, −D1YB5R)	T_A = 25°C	26.4	33.0	39.6	Ω
R2	Resistance of R2 Resistor	T_A = 25°C		15		kΩ
TCR	Temperature Coefficient of Resistance	(Note 1)		±1300		ppm/°C
C1	Capacitance of C1 Capacitor	0 V DC, 30 mV AC, 1 MHz, 25°C	37.6	47.0	56.4	pF
		2.5 V DC, 30 mV AC, 1 MHz, 25°C	25.6	32.0	38.4	pF
TOL_{CM}	Matching Tolerance of C1 Capacitors	1 MHz, 25°C			±2	%
I_{LEAK}	Diode Leakage Current to GND	Measured at 3.3 V DC, 25°C		1	100	nA
V_{RB}	Diode Reverse Bias Voltage	I_{LOAD} = 10 μA, T_A = 25°C	5.5			V
V_{SIG}	Signal Voltage: Positive Clamp Negative Clamp	 I_{LOAD} = 10 mA, T_A = 25°C I_{LOAD} = 10 mA, T_A = 25°C	 5.6 −0.4	 6.8 −0.8	 9.0 −1.5	V
V_{ESD}	In−system ESD Withstand Voltage MIL−STD−883D, Method 3015 (HBM) IEC 61000−4−2 Contact Discharge	 Pins 1, 3 (Notes 2 and 3) Pins 4, 5 (Note 2) Pins 4, 5 (Note 2)	 ±4 ±20 ±15			kV
V_{CL}	Clamping Voltage under ESD Discharge	MIL−STD−883D, Method 3015 +8 kV (Note 4)		12		V
		MIL−STD−883D, Method 3015 −8 kV (Note 4)		−7		V

1. Electrical operating characteristics guaranteed over standard operating conditions unless specified otherwise.
2. ESD voltage applied to pins with respect to GND, one at a time; unused pins are left open.
3. Pins 1 and 3 are not connected to the USB port connector, and therefore are not exposed to external ESD hazards. Thus, they do not require the high ESD protection levels provided for pins 4 and 5.
4. ESD Clamping Voltage is measured at the opposite end of R1 from the pin to which the ESD discharge is applied (e.g., if ESD is applied to pin 6, then the clamping voltage is measured at pin 1).

PERFORMANCE INFORMATION

Capacitance vs. Voltage

The C1 capacitance value as a function of DC voltage across it is presented in Figure 1. The curve is normalized to a capacitance of 1.0 capacitance units at 2.5 V DC.

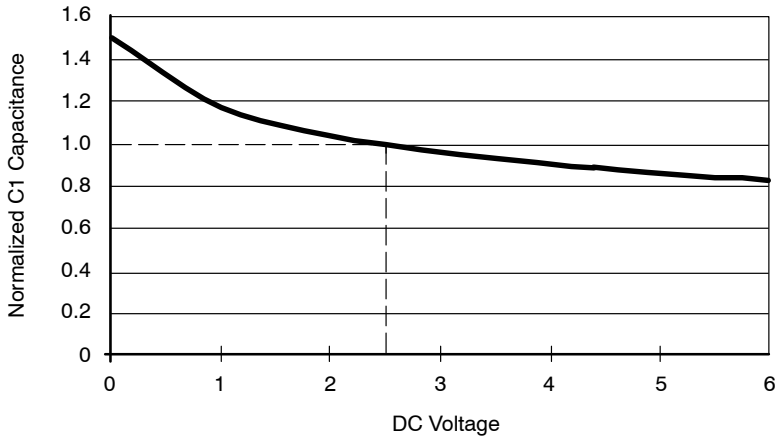


Figure 1. Diode Capacitance vs. DC Voltage (Normalized)

Insertion Loss vs. Frequency Characteristics

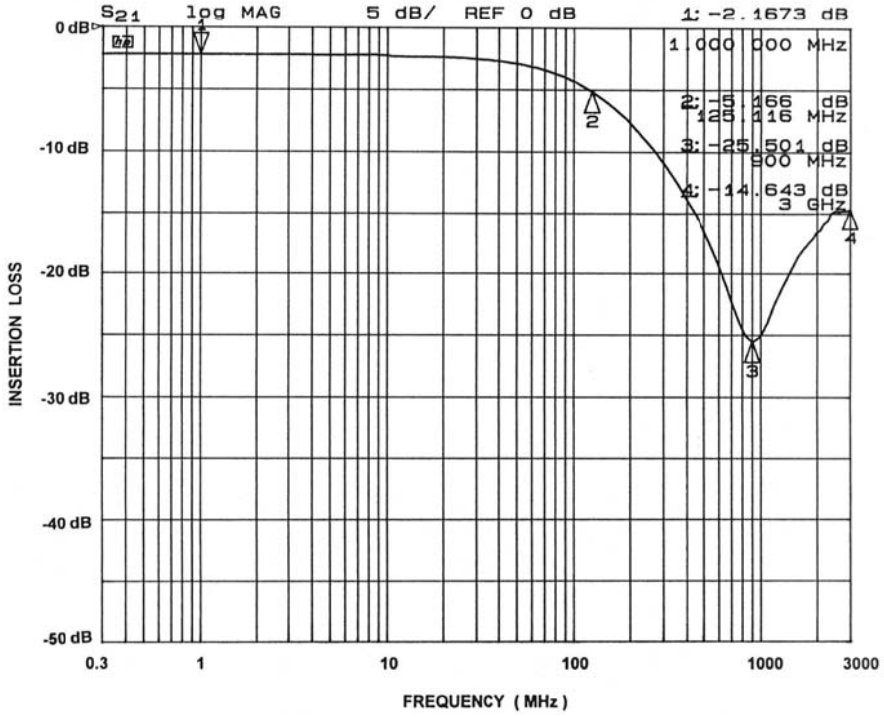


Figure 2. Insertion Loss vs. Frequency Performance Curve, PACUSB−D1 (SOT23−5)

PERFORMANCE INFORMATION (Cont'd)

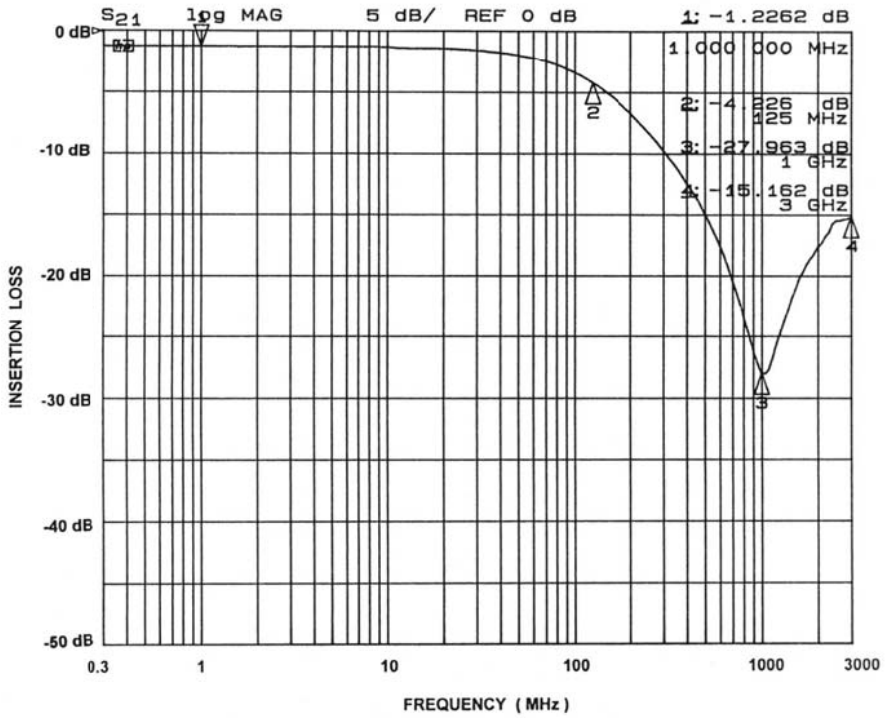


Figure 3. Insertion Loss vs. Frequency Performance Curve, PACUSB−D2 (SOT23−5)

APPLICATION INFORMATION

The PACUSB−D1/D2 provides a complete interface for a single downstream USB port typically found in computers and USB hubs. It integrates the series resistors (R1) and the 15 kΩ pull−down resistors (R2) for both USB data lines (D+ and D−) as well as the capacitors to ground for EMI suppression. Zener diodes provide ESD protection up to 15 kV contact discharge per the IEC 61000−4−2 standard and protect the USB controller on both data lines.

The PACUSB−D1/D2 should be placed on the PCB between the USB controller and the USB connector, as shown on the Connection Diagram, Figure 4.

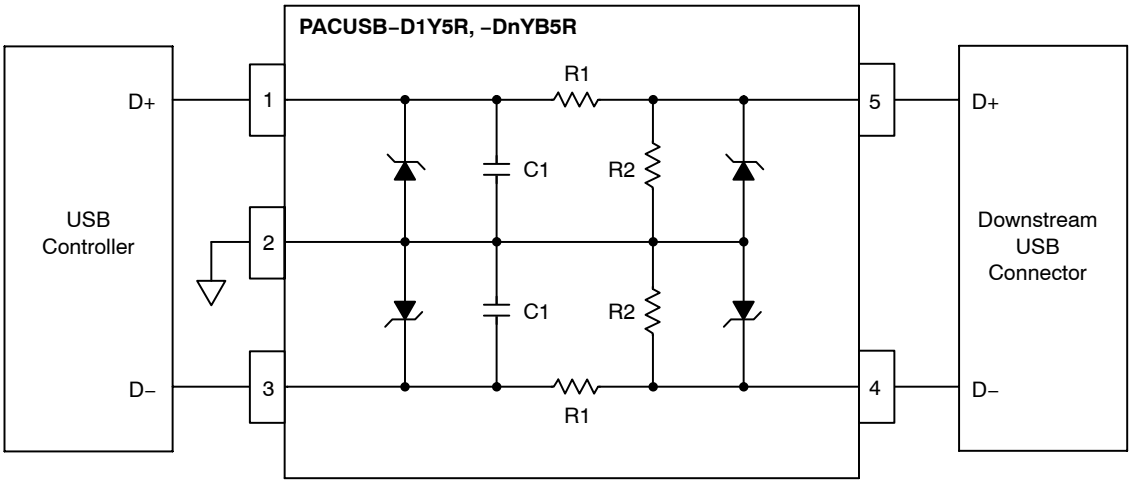
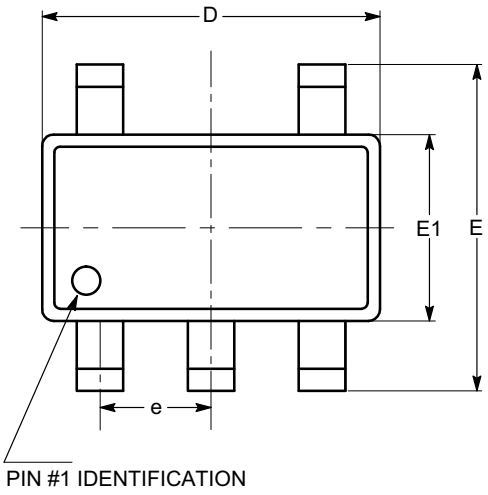


Figure 4. Connection Diagram for PACUSB−D1/D2 Devices

To guarantee the best ESD and filtering performance, it is recommended to physically locate the PACUSB−D1/D2 close to the USB connector. Also, the trace lengths between the PACUSB−D1/D2 and the USB controller should be kept as short as possible.

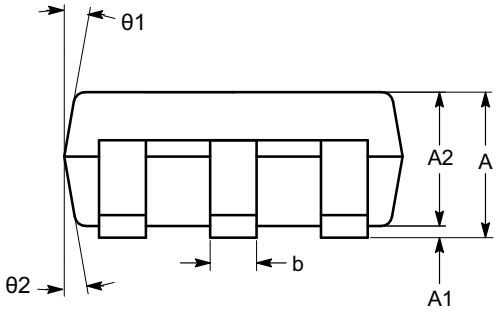
PACKAGE DIMENSIONS

SOT−23, 5 Lead
CASE 527AH−01
ISSUE O

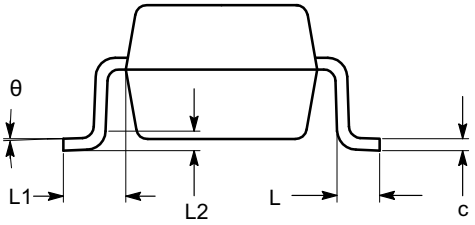


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.90		1.45
A1	0.00		0.15
A2	0.90	1.15	1.30
b	0.30		0.50
c	0.08		0.22
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
e		0.95 BSC	
L	0.30	0.45	0.60
L1		0.60 REF	
L2		0.25 REF	
θ	0°	4°	8°
θ1	5°	10°	15°
θ2	5°	10°	15°



SIDE VIEW



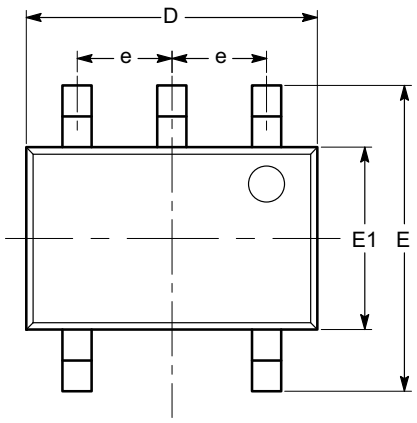
END VIEW

Notes:
(1) All dimensions in millimeters. Angles in degrees.
(2) Complies with JEDEC standard MO-178.

PACUSBD

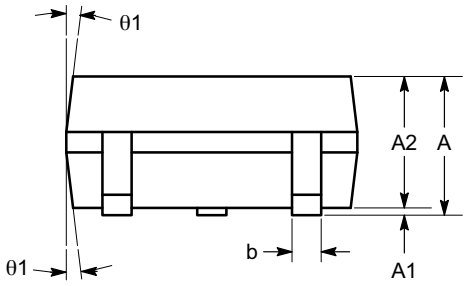
PACKAGE DIMENSIONS

SC−88A (SC−70 5 Lead), 1.25x2
CASE 419AC−01
ISSUE A

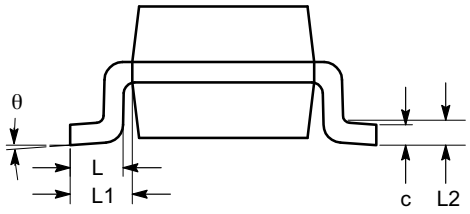


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e		0.65 BSC	
L	0.26	0.36	0.46
L1		0.42 REF	
L2		0.15 BSC	
θ	0°		8°
θ1	4°		10°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-203.

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