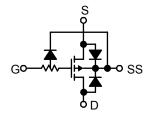
Schematic Symbol

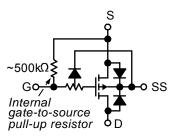
Source Substrate

Schematic Symbol

Functional Diagrams







MIC94031

Absolute Maximum Ratings⁽¹⁾

Voltage and current values are negative. Signs n	ot shown for clarity.
Drain-to-Source Voltage (pulse)	16V
Gate-to-Source Voltage (pulse)	16V
Continuous Drain Current	
$T_A = 25^{\circ}C$	1A
T _A = 100°C	0.5A
Operating Junction Temperature	55°C to +150°C
Storage Temperature	55°C to +150°C

Total Power Dissipation	
T _A = 25°C	568mW
T _A = 100°C	
Thermal Resistance	
θ_{JA}	220°C/W
θ _{JC}	130°C/W
Lead Temperature	
1/16" from case, 10s	+300°C

Electrical Characteristics

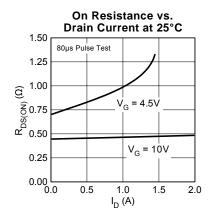
Voltage and current values are negative. Signs not shown for clarity.

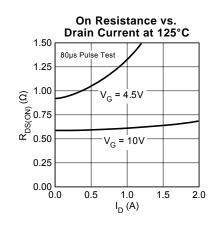
Symbol	Parameter	Condition (Note 1)	Min	Тур	Max	Units
V _{BDSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	13.5			V
V _{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.6	1.0	1.4	V
I _{GSS}	Gate-Body Leakage	V _{DS} = 0V, V _{GS} = 12V, Note 2, Note 3			1	μA
R _{GS}	Gate-Source Resistor	V _{DS} = 0V, V _{GS} = 12V, Note 2, Note 4	500	750	1000	kΩ
C _{ISS}	Input Capacitance	V _{GS} = 0V, V _{DS} = 12V		100		pF
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 12V, V _{GS} = 0V			25	μA
		V _{DS} = 12V, V _{GS} = 0V, T _J = 125°C		0.010	250	μA
I _{D(ON)}	On-State Drain Current	V _{DS} = 10V, V _{GS} = 10V, Note 5		6.3		Α
R _{DS(ON)}	Drain-Source On-State Resist	$V_{GS} = 10V$, $I_D = 100mA$ $V_{GS} = 4.5V$, $I_D = 100mA$ $V_{GS} = 2.7V$, $I_D = 100mA$		0.45 0.75 1.20	1.00	Ω Ω Ω
9 FS	Forward Transconductance	V _{DS} = 10V, I _D = 200mA, Note 5		480		mS

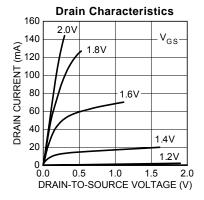
Notes:

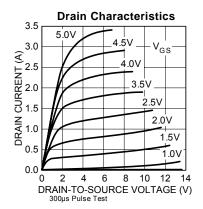
- 1. $T_A = 25$ °C unless noted. Substrate connected to source for all conditions.
- 2. ESD gate protection diode conducts during positive gate-to-source voltage excursions.
- 3. MIC94030 only.
- 4. MIC94031 only.
- 5. Pulse Test: Pulse Width ≤ 80µsec, Duty Cycle ≤ 0.5%.

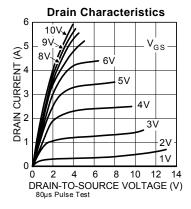
Typical Characteristics











Typical Applications

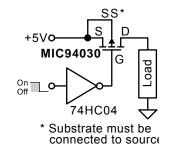


Figure 1. Power Switch Application

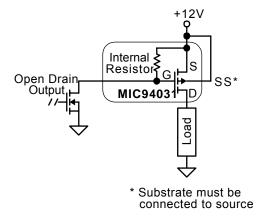


Figure 2. Power Control Application

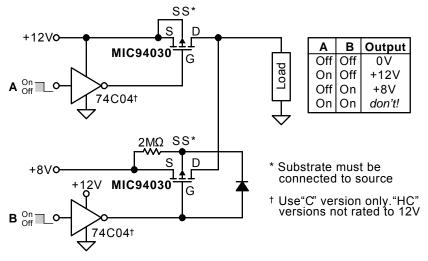
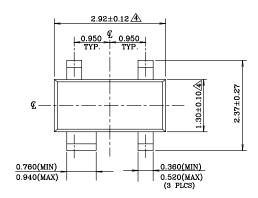
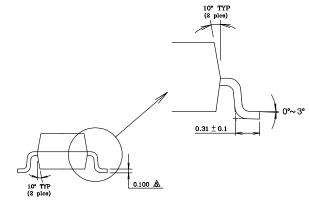


Figure 3. Analog Switch Application

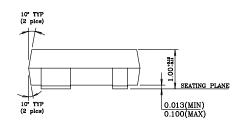
Package Information



TOP VIEW



END VIEW



SIDE VIEW

NOTE:

- 1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
- 2. Package surface to be mirror finish.
- 3. Die is facing up for mold & trim/form.
- Dimension are exclusive of mold flash and gate burr.
- 5 Dimension are exclusive of solder plating.

SOT-143 (M4)

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