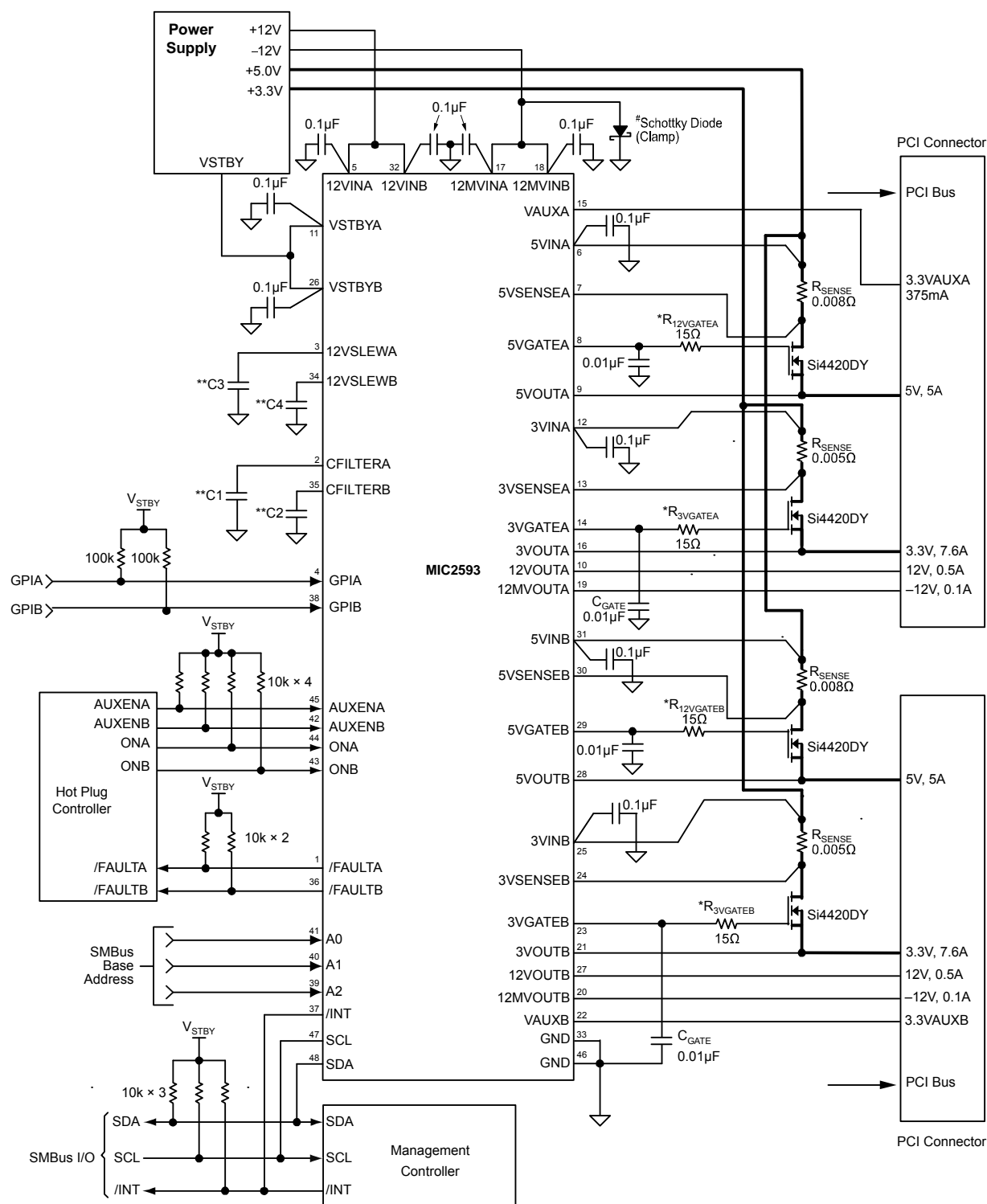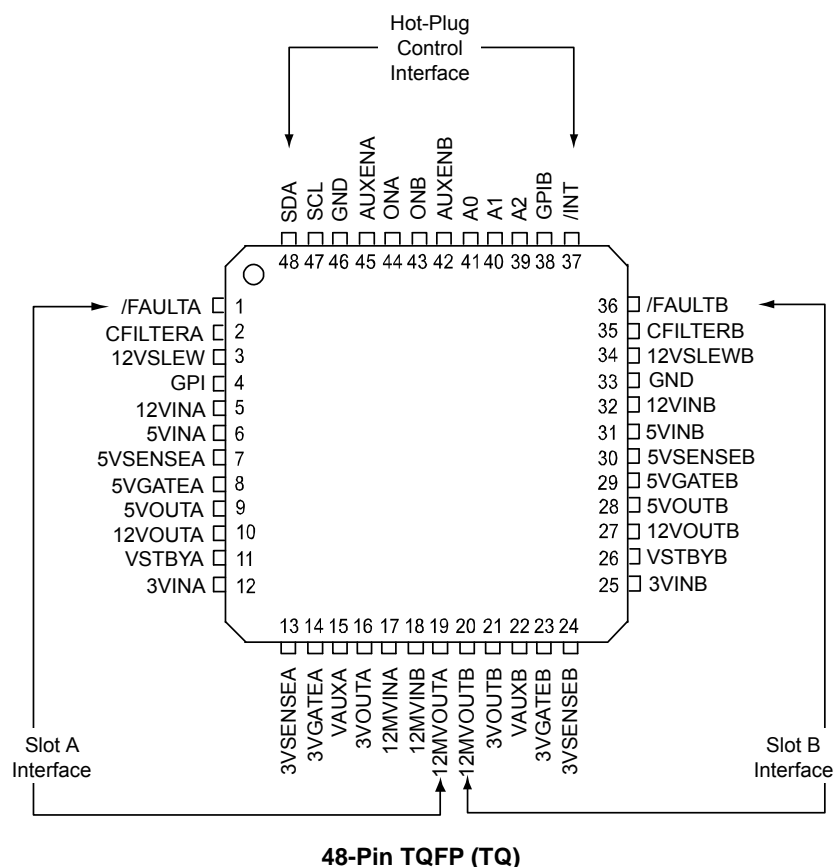# Typical Application

*   Values for $R_{5VGATE[A/B]}$ and $R_{3VGATE[A/B]}$ may vary depending upon the C_{GS} of the external MOSFETs.

** Values determined by design requirements. See "Functional Description" section for detailed information.

\#   MBRS140T3 or equivalent is recommended.

Bold lines indicate high current paths

Pin Configuration

Hot-Plug
Control
Interface

48-Pin TQFP (TQ)

Slot A Interface

Slot B Interface

Top pins (48–37): SDA, SCL, GND, AUXENA, ONA, ONB, AUXENB, A0, A1, A2, GPIB, /INT

Left pins (1–12): /FAULTA (1), CFILTERA (2), 12VSLEW (3), GPI (4), 12VINA (5), 5VINA (6), 5VSENSEA (7), 5VGATEA (8), 5VOUTA (9), 12VOUTA (10), VSTBYA (11), 3VINA (12)

Right pins (36–25): /FAULTB (36), CFILTERB (35), 12VSLEWB (34), GND (33), 12VINB (32), 5VINB (31), 5VSENSEB (30), 5VGATEB (29), 5VOUTB (28), 12VOUTB (27), VSTBYB (26), 3VINB (25)

Bottom pins (13–24): 3VSENSEA, 3VGATEA, VAUXA, 3VOUTA, 12MVINA, 12MVINB, 12MVOUTA, 12MVOUTB, 3VOUTB, VAUXB, 3VGATEB, 3VSENSEB

Pin Description

Pin Number	Pin Name	Pin Function
5, 32	12VINA, 12VINB	+12V Supply Power [A/B]: Pin 5 is the input to the drain side of the internal MOSFET switch for +12V Slot A. Pin 32 is the input to the drain side of the internal MOSFET switch for +12V Slot B. These two pins must ultimately connect to each other within 10cm of the MIC2593. An undervoltage lockout circuit (UVLO) prevents the switches from turning on while this input is less than its lockout threshold.
10, 27	12VOUTA, 12VOUTB	+12V Output [A/B]: Pin 10 is connected to the source terminal of the internal MOSFET switch for +12V Slot A and pin 27 is connected similarly for Slot B.
17, 18	12MVINA, 12MVINB	–12V Supply Power [A/B]: Pin 17 is the input to the drain side of the internal MOSFET switch for +12V Slot A. Pin 18 is the input to the drain side of the internal MOSFET switch for –12V Slot B. These two pins must ultimately connect to each other within 10cm of the MIC2593. An undervoltage lockout circuit (UVLO) prevents the switches from turning on while this input is less than its lockout threshold.
19, 20	12MVOUTA, 12MVOUTB	–12V Output [A/B]: Pin 19 is connected to the source terminal of the internal MOSFET switch for –12V Slot A and pin 20 is connected similarly for Slot B.
3, 34	12VSLEWA, 12VSLEWB	12V Slew Rate Control [A/B]: Connect capacitors between these pins and ground to set the output slew rates of the +12V and –12V supplies. See the "Functional Description" section for more details.

Pin Number	Pin Name	Pin Function
6, 31	5VINA, 5VINB	5V Supply Power and Sense Input [A/B]: Pin 6 is the (+) Kelvin-sense connection to the supply side of the sense resistor for 5V Slot A. Pin 31 is the (+) Kelvin sense connection to the supply side of the sense resistor for 5V Slot B. These two pins must ultimately connect to each other within10cm of the MIC2593. An undervoltage lockout circuit (UVLO) prevents the switches from turning on while this input is less than its lockout threshold.
7, 30	5VSENSEA, 5VSENSEB	5V Circuit Breaker Sense Input [A/B]: The current limit thresholds are set by connecting sense resistors between these pins and 5VIN[A/B]. When the current limit threshold of IR = 50mV is reached, the 5VGATE[A/B] pin is modulated to maintain a constant voltage across the sense resistor and therefore a constant current into the load. If the 50mV threshold is exceeded for t_{FLT} (see CFILTER[A/B] pin description), the circuit breaker is tripped and the GATE pin for the affected supply's external MOSFET is immediately pulled low.
9, 28	5VOUTA, 5VOUTB	5V Power-Good Sense Inputs: Connect to 5V[A/B] outputs. Used to monitor the 5V output voltages for Power-is-Good status.
8, 29	5VGATEA, 5VGATEB	5V Gate Drive Output [A/B]: Each pin connects to the gate of an external N-Channel MOSFET. During power-up, the C_{GATE} and the C_{GS} of the MOSFETs are charged by a 25µA current source. This controls the value of dv/dt seen at the source of the MOSFETs, and hence the current flowing into the load capacitance. During current-limit events, the voltage at the pin is adjusted to maintain constant current through the switch for a period of t_{FLT}. Whenever an overcurrent, thermal shutdown, or input undervoltage fault condition occurs, the GATE pin for the affected slot is immediately brought low. During power-down, these pins are discharged by an internal current source.
12, 25	3VINA, 3VINB	3.3V Supply Power and Sense Input [A/B]: Pin 12 is the (+) Kelvin-sense connection to the supply side of the sense resistor for 3.3V Slot A. Pin 25 is the (+) Kelvin-sense connection to the supply side of the sense resistor for 3.3V Slot B. These two pins must ultimately connect to each other within 10cm of the MIC2593. An undervoltage lockout circuit (UVLO) prevents the switches from turning on while this input is less than its lockout threshold.
13, 24	3VSENSEA, 3VSENSEB	3V Circuit Breaker Sense Input [A/B]: The current limit thresholds are set by connecting sense resistors between these pins and 3VIN[A/B]. When the current limit threshold of IR = 50mV is reached, the 3VGATE[A/B] pin is modulated to maintain a constant voltage across the sense resistor and therefore a constant current into the load. If the 50mV threshold is exceeded for t_{FLT} (see CFILTER[A/B] pin description), the circuit breaker is tripped and the GATE pin for the affected supply's external MOSFET is immediately pulled low.
16, 21	3VOUTA, 3VOUTB	3.3V Power-Good Sense Inputs: Connect to 3.3V[A/B] outputs. Used to monitor the 3.3V output voltages for Power-is-Good status.
14, 23	3VGATEA, 3VGATEB	3V Gate Drive Output [A/B]: Each pin connects to the gate of an external N-channel MOSFET. During power-up, the C_{GATE} and the C_{GS} of the MOSFETs are connected to a 25µA current source. This controls the value of dv/dt seen at the source of the MOSFETs, and hence the current flowing into the load capacitance. During current limit events, the voltage at this pin is adjusted to maintain constant current through the switch for a period of t_{FLT}. Whenever an overcurrent, thermal shutdown, or input undervoltage fault condition occurs, the GATE pin for the affected slot is immediately brought low. During power down, these pins are discharged by an internal current source.
11, 26	VSTBYA, VSTBYB	.3V Standby Input Voltage: Required to support PCI VAUX output. Additionally, the SMBus logic and internal registers run off of VSTBY[A/B] to ensure that the MIC2593 is accessible during standby modes. A UVLO circuit prevents turn-on of this supply until VSTBY[A/B] rises above its UVLO threshold. Both pins must be connected together externally at the IC.

Pin Number	Pin Name	Pin Function
15, 22	VAUXA, VAUXB	3.3VAUX[A/B] Output to PCI Card Slot: These outputs connect the 3.3AUX pin of the PCI connectors to VSTBY[A/B] via internal 400mΩ MOSFETs. These outputs are current limited and protected against short-circuit faults.
44, 43	ONA, ONB	Enable Inputs: Rising-edge triggered. Used to enable or disable the MAINA and MAINB (5V, 3.3V, +12V and –12V) outputs. Taking ON[A/B] low after a fault resets the 5V, 3.3V, +12V and/or –12V fault latches for the affected slot. Tie these pins to GND if using SMI power control. Also, see pin description for /FAULTA and /FAULTB.
45, 42	AUXENA, AUXENB	Enable Inputs: Rising-edge triggered. Used to enable or disable VAUXA and VAUXB outputs. Taking AUXEN[A/B] low after a fault resets the respective slot's Aux Output Fault Latch. Tie these pins to GND if using SMI power control. Also, see pin description for /FAULTA and /FAULTB.
2, 35	CFILTERA, CFILTERB	Overcurrent Timer (Filter) Capacitor [A/B]: Capacitors connected between these pins and GND set the duration of t_{FLT}. t_{FLT} is the amount of time for which a slot remains in current limit before its circuit breaker is tripped.
1, 36	/FAULTA, /FAULTB	/FAULT[A/B] Outputs: Open-drain, active-low. Asserted whenever the circuit breaker trips due to a fault condition (overcurrent, input undervoltage, overtemperature). Each pin requires an external pull-up resistor to VSTBY. Bringing the slot's ON[A/B] pin low resets /FAULT[A/B] if /FAULT[A/B] was asserted in response to a fault condition on one of the slot's MAIN outputs (5V, 3.3V, +12V, or –12V). /FAULT[A/B] is reset by bringing the slot's AUXEN[A/B] pin low if /FAULT[A/B] was asserted in response to a fault condition on the slot's VAUX output. If a fault condition occurred on both the MAIN and VAUX[A/B] outputs of the same slot, then both ON[A/B] and AUXEN[A/B] must be brought low to de-assert the /FAULT[A/B] output.
4, 38	GPIA, GPIB	General Purpose Inputs: The states of these two inputs are available by reading the Common Status Register, Bits [4:5]. If not used, connect each pin to GND.
40, 41	A1, A0	SMBus Address Select Pins: Connect to ground or leave open in order to 41 A0 program device SMBus base address. These inputs have internal pull-up resistors to VSTBY[A/B].
48	SDA	SMBus Data: Bidirectional SMBus data line.
47	SCL	SMBus Clock: Input.
37	/INT	Interrupt Output: Open-drain, active-low. Asserted whenever a power fault is detected if the INTMSK bit (CS Register Bit D[3]) is a logical "0". This output is de-asserted by performing an "echo reset" to the appropriate fault bit(s) in the STAT[A/B] and/or CS registers. This pin requires an external pull-up resistor to V_{STBY}.
33, 46	GND	IC Ground Connections: Tie directly to the system's analog ground plane directly at the device.

Absolute Maximum Ratings[1]

Supply Voltage
(12V$_{IN}$) ....+14V
(12MV$_{IN}$) ....–14V
(5V$_{IN}$) ....+7V
(3V$_{IN}$), (V$_{STBY}$) ....+7V
Any Logic Pin ....–0.5 to 3.6V
Output Current (FAILT[A/B], /INT, SDA). 10mA
Lead Temperature
IR Reflow, Peak Temperature.......................240 0°C/–5°C
Storage Temperature (T$_s$) ....–65°C to +150°C
ESD Rating[3]
Human Body Model..2kV
Machine Model 200V

Operating Ratings[2]

Supply Voltage
(12V$_{IN}$) .... +11.65V to +12.6V
(12MV$_{IN}$) .... –11.0V to –13.2V
(5V$_{IN}$) .... +4.85V to 5.25V
(3V$_{IN}$) .... +3.1V to +3.6V
(V$_{STBY}$) .... +3.15V to 3.6V
Ambient Temperature (T$_A$) ....0°C to +70°C
Junction Temperature (T$_J$) .... 125°C
Thermal Resistance
    TQFP (θ$_{JA}$) ....56.5°C/W

Electrical Characteristics[4]

12V$_{IN[A/B]}$ = 12V; 12MV$_{IN[A/B]}$ = –12V; 5V$_{IN[A/B]}$ = 5V; 3V$_{IN[A/B]}$ = 3.3V; V$_{STBY[A/B]}$ = 3.3V; T$_A$ = 25°C; unless otherwise noted.
Bold indicates specification applies over the full operating rating temperature range from 0°C to 70°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I$_{CC12V}$	Supply Current			0.6	**2.0**	mA
I$_{CC5V}$				1.2	**2.0**	mA
I$_{CC3.3V}$				0.5	**0.7**	mA
I$_{CC12MV}$				–1.0	**–2.0**	mA
I$_{CCVSBY}$				2.5	**5.0**	mA
	Under Voltage Lockout Thresholds					
V$_{UVLO(12V)}$	12V$_{IN}$[A/B]	12V$_{IN}$ increasing	**8**	9	**10**	V
V$_{UVLO(3V)}$	3V$_{IN}$[A/B]	3V$_{IN}$ increasing	**2.2**	2.5	**2.75**	V
V$_{UVLO(5V)}$	5V$_{IN}$[A/B]	5V$_{IN}$ increasing	**3.7**	4.0	**4.3**	V
V$_{UVLO(12MV)}$	12MV$_{IN}$[A/B]	12MV$_{IN}$ increasing	**–10**	–9	**–8**	V
V$_{UVLO(STBY)}$	V$_{STBY}$[A/B]	V$_{STBY}$ increasing	**2.8**	2.9	**3.0**	V
V$_{HYSUV}$	Under Voltage Lockout Hysteresis - 12V$_{IN}$, 12MV$_{IN}$, 5V$_{IN}$, 3V$_{IN}$			180		mV
V$_{HYSSTBY}$	Under-voltage Lockout Hysteresis - V$_{STBY}$			50		mV
	Power Good Under-Voltage Thresholds					
V$_{UVTH(12V)}$	12V$_{OUT}$[A/B]	12V$_{OUT}$[A/B] decreasing	**10.2**	10.5	**10.8**	V
V$_{UVTH(12MV)}$	12MV$_{OUT}$ [A/B]	12MV$_{OUT}$[A/B] decreasing	**–10.8**	–10.6	**–10.2**	V
V$_{UVTH(3V)}$	3V$_{OUT}$ [A/B]	3V$_{OUT}$[A/B] decreasing	**2.7**	2.8	**2.9**	V
V$_{UVTH(5V)}$	5V$_{OUT}$ [A/B]	5V$_{OUT}$[A/B] decreasing	**4.4**	4.5	**4.7**	V
V$_{UVTH(VAUX)}$	V$_{AUX}$[A/B]	V$_{AUX}$[A/B] decreasing	**2.7**	2.8	**2.9**	V
V$_{HYSPG}$	Power-Good Detect Hysteresis			30		mV
V$_{GATE}$	5V$_{GATE}$/3V$_{GATE}$ Voltage		**12V$_{IN}$–15**		**12V$_{IN}$**	V
I$_{GATE(SOURCE)}$	5V$_{GATE}$/3V$_{GATE}$ Charge Current	start cycle	**15**	25	**35**	µA
I$_{GATE(SINK)}$	5V$_{GATE}$/3V$_{GATE}$ Sink Current (Fault Off)	any fault condition, V$_{GATE}$ = 5V		70		mA

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{FILTER}	C_{FILTER} Threshold Voltage		**1.20**	1.25	**1.30**	V
I_{FILTER}	C_{FILTER} [A/B] Charge Current	$V_{5VIN[A/B]} - V_{5SENSE[A/B]} > V_{THILIMIT}$ and/or $V_{3VIN[A/B]} - V_{3SENSE[A/B]} > V_{THILIMIT}$	**1.80**	2.5	**5.0**	µA
I_{SLEW}	$12V_{SLEW}$[A/B] Charge Current	During turn-on only	**13**	22	**35**	µA
$V_{THILIMIT}$	Current Limit Threshold Voltages 5V[A/B] Supplies	$V_{5VIN[A/B]} - V_{5VSENSE[A/B]}$	**35**	50	**65**	mV
	3.3V[A/B] Supplies	$V_{3VIN[A/B]} - V_{3VSENSE[A/B]}$	**35**	50	**65**	mV
V_{THFAST}	Fast-Trip Current Limit Thresholds 5V[A/B] and 3V[A/B]	MIC2593-2xTQ	**90**	113	**135**	mV
$I_{5VSENSE[A/B]}$	$5V_{SENSE}$[A/B] Input Current	$V_{5VIN[A/B]} - V_{5VSENSE[A/B]} = 50mV$[5]		0.5		µA
$I_{3VSENSE[A/B]}$	$3V_{SENSE}$[A/B] Input Current	$V_{3VIN[A/B]} - V_{3VSENSE[A/B]} = 50mV$[5]		0.5		µA
V_{IL}	LOW-Level Input Voltage ON[A/B], AUXEN[A/B], GPI[A/B], SCL, SDA, A[0-2]				**0.8**	V
V_{OL}	Output LOW Voltage /FAULT[A/B], /INT, SDA	$I_{OL} = 3mA$			**0.4**	V
V_{IH}	HIGH-Level Input Voltage ON[A/B], AUXEN[A/B], GPI[A/B], SCL, SDA, A[0-2]		**2.1**			V
$R_{PULL-UP}$	Internal Pullups from A[0-2] to V_{STBY}			40		kΩ
$I_{LKG,OFF(12VIN[A/B])}$	$12V_{IN}$[A/B] Input Leakage Current	$V_{STBY[A/B]} = +3.3V$ $12V_{IN[A/B]} = OFF$[5]		1		µA
$I_{LKG,OFF(12MVIN[A/B])}$	$12MV_{IN}$[A/B] Input Leakage Current	$V_{STBY[A/B]} = +3.3V$ $12MV_{IN[A/B]} = OFF$[5]		60		µA
$I_{LKG,OFF(5VIN[A/B])}$	$5V_{IN}$[A/B] Input Leakage Current	$V_{STBY[A/B]} = +3.3V$ $5V_{IN[A/B]} = OFF$[5]		200		µA
$I_{LKG,OFF(3VIN[A/B])}$	$3V_{IN}$[A/B] Input Leakage Current	$V_{STBY[A/B]} = +3.3V$ $3V_{IN[A/B]} = OFF$[5]		1		µA
I_{IL}	Input Leakage Current SCL, ON[A/B], AUXEN[A/B], GP[A/B])				**±5**	µA
$I_{LKG(OFF)}$	Off-State Leakage Current SDA, /FAULT[A/B], /INT				**±5**	µA
T_{OV}	Overtemperature Shutdown & Reset Thresholds, with overcurrent on slot	T_J Increasing, each slot [6]		140		°C
		T_J Decreasing, each slot [6]		130		°C
	Overtemperature Shutdown & Reset Thresholds, all other conditions (all outputs will latch OFF)	T_J Increasing, both slots [6]		160		°C
		T_J Decreasing, both slots [6]		150		°C
	Output MOSFET Resistance					
$R_{OUT(12V)}$	+12V MOSFET	$I_{DS} = 500mA$, $T_J = 125°C$			**500**	mΩ
$R_{OUT(12MV)}$	–12V MOSFET	$I_{DS} = 100mA$, $T_J = 125°C$			**2**	Ω
$R_{OUT(AUX)}$	V_{AUX} MOSFET	$I_{DS} = 375mA$, $T_J = 125°C$			**400**	mΩ

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Off-State Output Offset Voltage					
$V_{OFF(+12V)}$	$12V_{OUT}[A/B]$	$12V_{OUT}[A/B]$ = Off, T_J = 125°C			**50**	mV
$V_{OFF(12MV)}$	$12MV_{OUT}[A/B]$	$12MV_{OUT}[A/B]$ = Off, T_J = 125°C	**–50**			mV
$V_{OFF(AUX)}$	$V_{AUX}[A/B]$	$V_{AUX}[A/B]$ = Off, T_J = 125°C			**50**	mV
	Current Limit Slow-Trip Threshold					
$I_{LIM(12V)}$	+12V MOSFET	$12V_{OUT}[A/B]$ = 0V	**0.52**	1.0	**1.5**	A
$I_{LIM(12MV)}$	–12V MOSFET	$12MV_{OUT}[A/B]$ = 0V	**–0.11**	–0.2	**–0.3**	A
	Current Limit Fast-Trip Thresholds	MIC2593-2BTQ	**1.0**	2.15	**3.0**	A
$I_{FASTLIM(12V)}$	+12V MOSFET	$12V_{OUT}[A/B]$	**–0.20**	–0.45	**–0.6**	A
$I_{FASTLIM(12MV)}$	–12V MOSFET	$12MV_{OUT}[A/B]$				
$I_{AUX(THRESH)}$	Auxiliary Output Current Limit Threshold **Figure 4**	Current which must be drawn from V_{AUX} to register as a fault		0.84		A
$I_{SC(TRAN)}$	Maximum Transient Short Circuit Current	V_{AUX} Enabled, then Grounded	I_{MAX} = V_{STBY} / $R_{DS(AUX)}$			A
$I_{LIM(AUX)}$	Regulated Current after Transient	From end of $I_{SC(TRAN)}$ to C_{FILTER} Time Out	**0.375**	0.7	**1.35**	A
R_{DISCH}	Output Discharge Resistance					
$R_{DISCH(12V)}$	$12V_{OUT}[A/B]$	$12V_{OUT}[A/B]$ = 6.0V		1600		Ω
$R_{DISCH(12MV)}$	$12MV_{OUT}[A/B]$	$12MV_{OUT}[A/B]$ = –6.0V		600		Ω
$R_{DISCH(3V)}$	$3V_{OUT}[A/B]$	$3V_{OUT}[A/B]$ = 1.65V		150		Ω
$R_{DISCH(5V)}$	$5V_{OUT}[A/B]$	$5MV_{OUT}[A/B]$ = 2.5V		150		Ω
$R_{DISCH(VAUX)}$	$V_{AUX}[A/B]$	$5V_{OUT}[A/B]$ = 1.65V		430		Ω
$t_{OFF(3V)}$ $t_{OFF(5V)}$	Current Limit Response Time for 3.3V and 5V Outputs, **Figure 2**	MIC2593-2 C_{GATE} = 10nF V_{IN} – V_{SENSE} = 200mV		1		µs
$T_{SC(TRAN)}$	V_{AUX} Current Limiter Response Time, **Figure 5**	$V_{AUX}[A/B]$ = 0V [6]		33		µs
$t_{OFF(12V)}$	12V Current Limit Response Time, **Figure 3**	$12V_{OUT}[A/B]$ = 0V [6]		1		µs
$t_{OFF(12MV)}$	–12V Current Limit Response Time, **Figure 3**	$12MV_{OUT}[A/B]$ = 0V [6]		1		µs
$t_{PROP(3VFAULT)}$	Delay from 3V[A/B] overcurrent-limit to FAULT Output	MIC2593-2 V_{SENSE} – $V_{THLIMIT}$ = 200mV C_{FILTER} = open		1		µs
$t_{PROP(5VFAULT)}$	Delay from 5V[A/B] overcurrent-limit to FAULT Output	MIC2593-2 V_{SENSE} – $V_{THLIMIT}$ = 200mV C_{FILTER} = open		1		µs
t_W	ON[A/B], AUXEN[A/B] Pulse Width	**Note 5**		100		ns
t_{POR}	MIC2593 Power-On Reset Time after V_{STBY} becomes valid	**Note 5**		500		µs
SMBus Timing, Note 5						
t_1	SCL (Clock) Period	**Figure 1**	**2.5**			µs
t_2	Data In Set-Up Time to SCL HIGH	**Figure 1**	**100**			ns

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_3	Data Out Stable after SCL LOW	**Figure 1**	300			ns
t_4	Data LOW Set-Up Time to SCL LOW	Start Condition, **Figure 1**	100			ns
t_5	Data HIGH Hold Time after SCL HIGH	Start Condition, **Figure 1**	100			ns

Notes:

1. Exceeding the absolute maximum rating may damage the device.

2. The device is not guaranteed to function outside its operating rating.

3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.

4. Specification for packaged product only.

5. Schottky diode clamp used for –12VIN[A/B] power bus. See the typical applications circuit.

6. Parameters guaranteed by design. Not 100% production tested.

Test Circuit
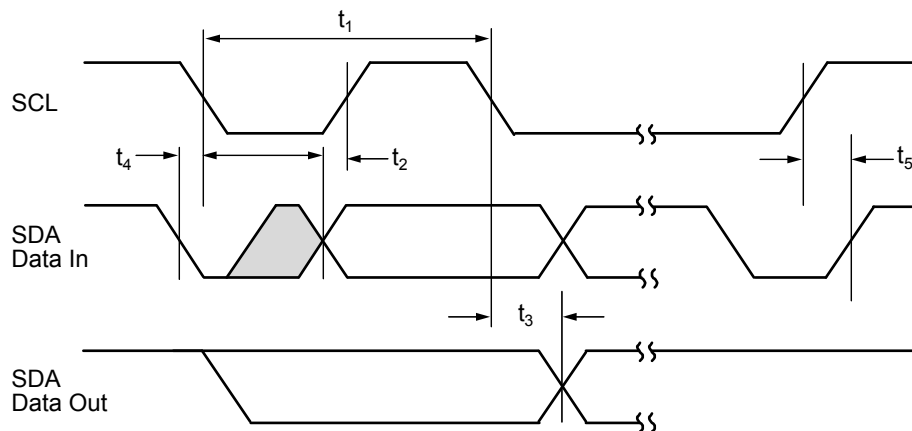
Figure 1. SMBus Timing
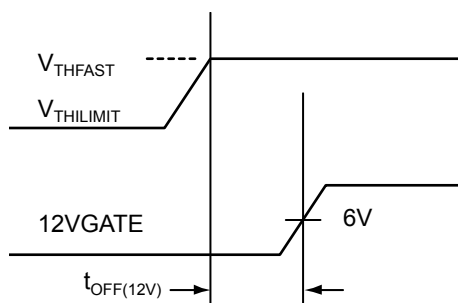
Figure 2. 12V Current Limit Response Timing
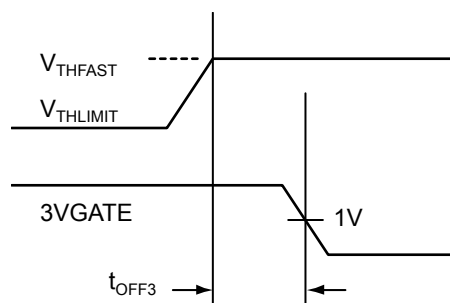
Figure 3. 3V Current Limit Response Timing
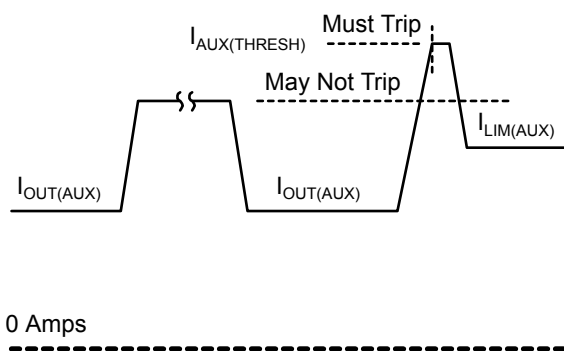
Figure 4. VAUX Current Limit Threshold
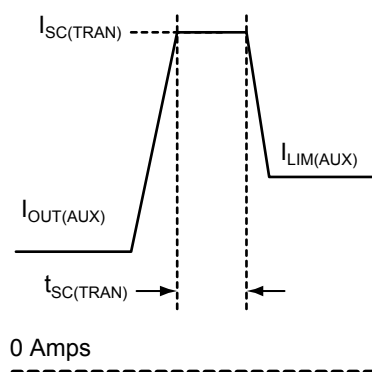
Figure 5. VAUX Current Limit Response Timing

Functional Description

Hot Swap Insertion

When circuit boards are inserted into systems carrying live supply voltages ("hot-plugged"), high inrush currents often result due to the charging of bulk capacitance that resides across the circuit board's supply pins. This transient inrush current can cause the system's supply voltages to temporarily go out of regulation, causing data loss or system lock-up. In more extreme cases, the transients occurring during a hot plug event may cause permanent damage to connectors or on-board components.

The MIC2593 addresses these issues by limiting the inrush currents to the load (PCI Board), and thereby controlling the rate at which the load's circuits turn-on. In addition to this inrush current control, the MIC2593 offers input and output voltage supervisory functions and current limiting to provide robust protection for both the system and circuit board.

System Interfaces

The MIC2593 employs two system interfaces: the hardware Hot Plug Interface (HPI) and the System Management Interface (SMI). The HPI includes ON[A/B], AUXEN[A/B], as well as /FAULT[A/B]; the SMI consists of SDA, SCL, and /INT, whose signals conform to the levels and timing of the SMBus specification. The MIC2593 can be operated exclusively from the SMI, or can employ the HPI for power control while continuing to use the SMI for access to all but the power control registers.

In addition to the basic power control features of the MIC2593 accessible by the HPI, the SMI also gives the host access to the following information from the part:

1. Fault conditions occurring on each supply.

2. GPI[A/B] pin status.

When using the System Management Interface for power control, do not use the Hot Plug Interface. Conversely, when using the Hot Plug Interface for power control, do not execute power control commands over the System Management Interface bus (all other register accesses via the SMI bus remain permissible while in the HPI control mode). When utilizing the SMI exclusively, the HPI input pins ON[A/B] and AUXEN[A/B] should be tied to ground as shown below in Figure 6 (Disabling HPI when SMI control is used). This configuration safeguards the power slots in the event that the SMBus communication link is disconnected for any reason.

Additionally, when utilizing the HPI exclusively, the SMBus (or SMI) will be inactive if the input pins (SDA, SCL, A0, A1, and A2) are configured as shown in Figure 6 below (disabling SMI when HPI Control is used).

Power-On Reset and Power Cycling

The MIC2593 utilizes VSTBY[A/B] as the main supply input source. VTSBY[A/B] is required for proper operation of the MIC2593 SMBus interface and registers and must be applied at all times. A Power-On Reset (POR) cycle is initiated after VSTBY[A/B] rises above its UVLO threshold and remains valid at that voltage for 500µs. All internal registers are cleared after POR. If VSTBY[A/B] is recycled, the MIC2593 enters a new power-on reset cycle. VSTBY[A/B] must be the first supply input applied followed by the MAIN supply inputs of $12V_{IN}$, $12MV_{IN}$, $5V_{IN}$, and $3V_{IN}$. The MAIN supply inputs may be applied in any order. The SMBus is ready for access at the end of the POR interval (500µs after VSTBY[A/B] is valid). All outputs remain off during t_{POR}.
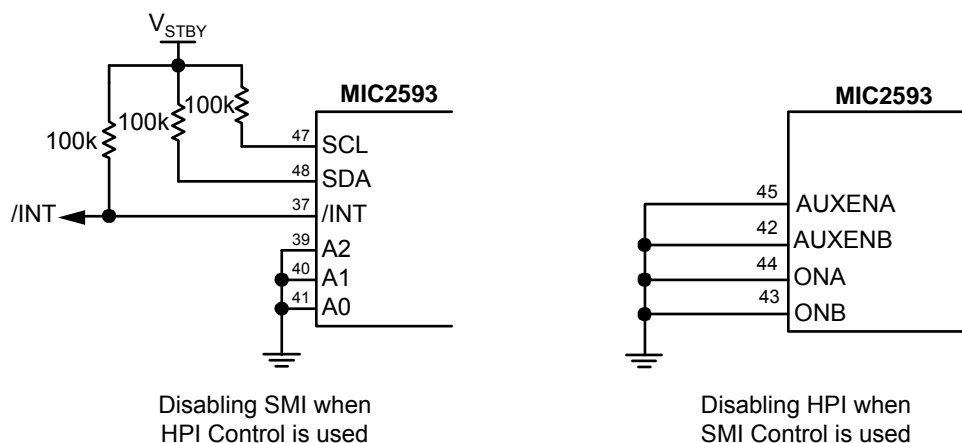

Disabling SMI when
HPI Control is used

Disabling HPI when
SMI Control is used

**Figure 6. Input Pin Configuration for
Disabling HPI/SMI Control**

Power-Up Cycle

When a slot is off, the 5VGATE and 3VGATE pins are held low with an internal pull-down current source. When a slot's MAIN outputs are enabled by applying a rising-edge signal at the ON[A/B] control input and all input voltages are above their respective undervoltage lockout thresholds, all four main supplies will then execute a controlled turn on. The 5VGATE and 3VGATE pins are each connected to a constant current source of 25µA, nominal. Both the 5V and 3.3V outputs act as source followers, where:

$$V_{SOURCE} = \left[V_{GATE} - V_{TH(ON)}\right]$$

until the associated output is equal to its input. The voltages on the gates of the external MOSFETs for the 5V and 3.3V MAIN supplies will continue to rise to approximately 11.5V, ensuring minimum $R_{DS(ON)}$ of the MOSFET. Note that a delay exists between the ON command to a slot and the appearance of voltage at the slot's 3.3V or 5V MAIN output. This delay is the time required to charge the 3V or 5V GATE output up to the threshold voltage of the external MOSFET (typically about 4V). For the 5V and 3.3V MAIN supplies, the source (output) side of the external MOSFET will reach the drain (input) voltage in a time given by:

$$t_{DELAY} = \frac{\left(C_{GATE} \times V_{DRAIN}\right)}{I_{GATE(SOURCE)}}$$

Table 1 provides a reference list of the expected GATE output slew rate for the 3.3V and 5V supplies using several (decade-scale) standard capacitors.

I_{SLEW} = 25µA	
C_{GATE}	dv/dt (load)
0.001µF	25000V/s
0.01µF	2500V/s
0.1µF	250V/s
1µF	25V/s

Table 1. 3.3V/5V Output Slew Rate Selection

For the +12V and –12V supplies, the output slew rate is controlled by capacitors connected to the 12VSLEWA and 12VSLEWB pins. To determine the minimum value of the slew rate capacitor, (C_{SLEW}), and to ensure the device does not enter into current limit during start-up, the following equation is used:

$$C_{SLEW}(min) = \frac{I_{SLEW}}{I_{LIM[12V/12MV]}} \times C_{LOAD}$$

where C_{LOAD} is the load capacitance connected to the +12V and –12V outputs, $I_{LIM[12V/12MV]}$ are the current limit slow-trip thresholds and I_{SLEW} is the slew rate charge current found in the "Electrical Characteristics" table. The slew rate dv/dt is computed by:

$$dv/dt \text{ (at load)} = \frac{I_{SLEW}}{C_{SLEW} \times 10^6}$$

By appropriately selecting the value of C_{SLEW}, the magnitude of the inrush current will not exceed the current limit for a given load capacitance. Since one capacitor fixes the slew rate for both +12V and –12V, the capacitor value should be chosen to provide the slower slew rate of the two. Table 2 depicts the ±12V output slew rate for various values of C_{SLEW}.

I_{SLEW} = 22µA	
C_{GATE}	dv/dt (load)
0.001µF	22V/ms
0.01µF	2.2V/ms
0.1µF	0.22V/ms
1µF	0.022V/ms

Table 2. ±12V Output Slew Rate Selection

Power Down Cycle

When a slot is turned off, internal switches are connected to each of the outputs to discharge the PCI board's bypass capacitors to ground.

Standby Mode

Standby mode is entered when any (one or more) enabled MAIN supply input (12V$_{IN}$, 12MV$_{IN}$, 5V$_{IN}$ and/or 3V$_{IN}$) drops below its respective UVLO threshold. The MIC2593 supplies two 3.3V auxiliary outputs, VAUX[A/B], satisfying PCI 2.x specifications. These outputs are fed via the VSTBY[A/B] input and controlled by the AUXEN[A/B] inputs or via their SMI bus Control Registers. These outputs are independent of the MAIN outputs: should one or more of the MAIN supply inputs move below its UVLO thresholds, VAUX[A/B] will still function as long as VSTBY[A/B] is present. Prior to entering standby mode, ONA and ONB (or the MAINA and MAINB bits in the Control Registers) inputs should be de-asserted. If this is not done, the MIC2593 will assert /FAULT and also /INT if interrupts are enabled, when the MIC2593 detects an undervoltage condition on a supply input.

Circuit Breaker Functions

The MIC2593 provides an electronic circuit breaker function that protects against excessive loads, such as short circuits, at each supply. When the current from one or more of a slot's MAIN outputs exceeds the current limit threshold (50mV/R$_{SENSE}$ for 3.3V and 5V, 1.0A for +12V, and/or 0.2A for –12V) for a duration greater than the overcurrent timer, t$_{FLT}$, the circuit breaker is tripped and all MAIN supplies (all outputs except VAUX[A/B]) are shut off. Should the load current exceed I$_{THFAST}$ (+12V and –12V), or cause a MAIN output's V$_{SENSE}$ to exceed V$_{THFAST}$ (+3.3V and +5V), the outputs are shut off with no delay. Undervoltage conditions on the MAIN supply inputs also

trip the circuit breaker, but only when the MAIN outputs are enabled (to signal a supply input brown-out condition).

The VAUX[A/B] outputs have their own separate circuit breaker functions. VAUX[A/B] do not incorporate a fast-trip threshold, but instead regulate the output current into a fault to avoid exceeding their operating current limit. The circuit breaker will trip due to overcurrents on VAUX[A/B] when the overcurrent fault timer (t_{FLT}) expires. This use of the overcurrent timer prevents the circuit breaker from tripping prematurely due to brief current transients.

Following a fault condition, the outputs can be turned on again via the ON inputs (if the fault occurred on one of the MAIN outputs), via the AUXEN inputs (if the fault occurred on the AUX outputs), or by cycling both ON and AUXEN (if faults occurred on both the MAIN and AUX outputs). A fault condition can alternatively be cleared under SMI control of the ENABLE bits in the CNTRL[A/B] registers (See Register Bits D[1:0]). When the circuit breaker trips, /FAULT[A/B] will be asserted if the outputs were enabled through the Hot Plug Interface inputs. At the same time, /INT will be asserted (unless interrupts are masked). Note that /INT is de-asserted by writing a Logic 1 back into the respective fault bit position(s) in the STAT[A/B] register or the Common Status Register. The response time (t_{FLT}) of the MIC2593's primary overcurrent detector is set by external capacitors at the CFILTER[A/B] pins to GND. For Slot A, CFILTER[A] is located at Pin 2; for Slot B, CFILTER[B] is located at Pin 35. For a given response time, the value for CFILTER[A/B] is given by.

$$CFILTER[A/B](\mu F) = \frac{t_{FLT[A/B]}(ms) \times I_{FILTER}(\mu A)}{V_{FILTER}(V) \times 10^3}$$

where $t_{FLT[A/B]}$ is the selected overcurrent response time and I_{FILTER} and V_{FILTER} are specified in the "Electrical Characteristics" table.

Thermal Shutdown

The internal +12V, –12V, and V_{AUX} MOSFETs are protected against damage not only by current limiting, but by dual-mode overtemperature protection as well. Each slot controller on the MIC2593 is thermally isolated from the other. Should an overcurrent condition raise the junction temperature of one slot's controller and internal pass elements to 140°C, all of the outputs for that slot (including V_{AUX}) will be shut off, and the slot's /FAULT output will be asserted. The other slot's operation will remain unaffected. However, should the MIC2593's overall die temperature exceed 160°C, both slots (all outputs, including V_{AUXA} and V_{AUXB}) will be shut off, whether or not a current limit condition exists. A 160°C overtemperature condition additionally sets the overtemperature bit (OT_INT) in the Common Status Register.

Output Power-Good Status

For the MIC2593, "Power-is-Good" is valid on a slot when the outputs of the four MAIN supplies (12V, –12V, 5V, and 3.3V) and the auxiliary supply output are all above their respective power-good thresholds specified in the "Electrical Characteristics" table. The power-good status of either slot is verified by polling the CNTRL[A/B] Register Bits D[7:6]. CNTRL[A/B] Register Bits D[7] and D[6] indicate output power-good status for the AUX supply and MAIN supplies, respectively. Figure7 below illustrates an equivalent logic circuit that determines the output power-good status for the MAIN and AUX supplies.
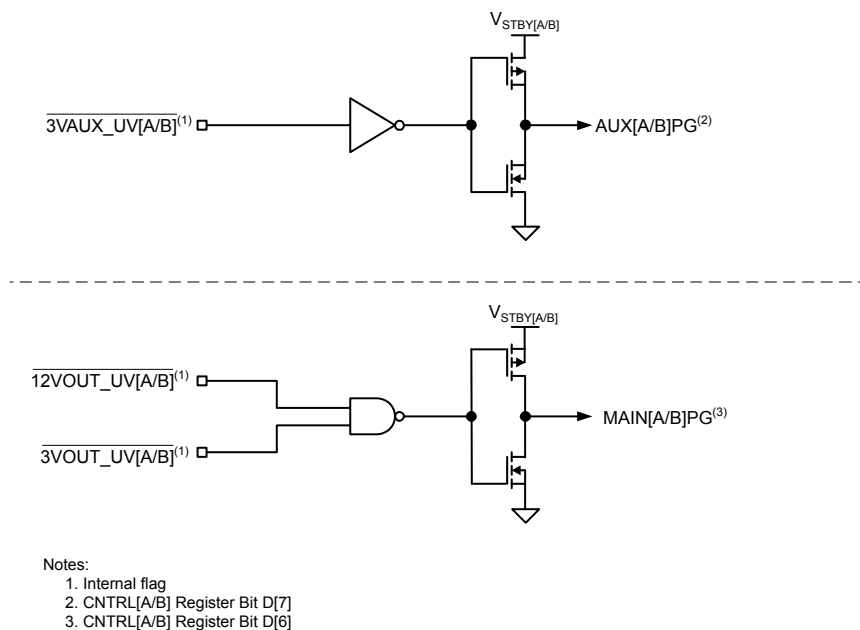

Notes:
1. Internal flag
2. CNTRL[A/B] Register Bit D[7]
3. CNTRL[A/B] Register Bit D[6]

Figure 7. Power-Good Status Logic Diagram

General Purpose Input (GPI) Pins

Two pins on the MIC2593 are available for use as GPI pins. The logic state of each of these pins can be determined by polling Bits [4:5] of Common Status Register. Both of these inputs are compliant to 3.3V. If unused, connect the GPI[A/B] pins to GND.

Fault Reporting and /INT Interrupt Generation

SMI-only Control Applications

In applications where the MIC2593 is controlled only by the SMI, the ON[A/B] and AUXEN[A/B] should be connected to GND as shown in Figure 6. In this case, the MIC2593's /FAULT[A/B] outputs and STAT[A/B] Register Bit D[7] (FAULT[A/B]) are not activated, as fault status is determined by polling STAT[A/B] Register Bits D[4:0] and CS (Common Status) Register Bits D[2:1]. Individual fault bits in STAT[A/B] and CS are asserted after power-on-reset when

Either or both CNTRL[A/B] Register Bits D[1:0] are asserted,

AND

- 12VIN[A/B], 12MVIN[A/B], 5VIN[A/B], 3VIN[A/B], or VSTBY[A/B] input voltage is lower than its respective ULVO threshold, OR
- The fast OC circuit breaker[A/B] has tripped, OR
- The slow OC circuit breaker[A/B] has tripped AND its filter timeout has expired, OR

- The slow OC circuit breaker[A/B] has tripped AND Slot[A/B] die temperature exceeds 140°C, OR
- The MIC2593's global die temperature exceeds 160°C

To clear any one or all STAT[A/B] Register Bits D[4:0] and/or CS Register Bits D[2:1] once asserted, a software subroutine can perform an "echo reset" where a Logical "1" is written back to those register bit locations that have indicated a fault.

The open-drain, active-LOW /INT output signal is activated after power-on-reset when the INTMSK bit (CS Register Bit D[3]) has been reset to Logical "0". Once activated, the /INT output is asserted by any one of the fault conditions listed above and de-asserted when one or all STAT[A/B] Register Bits D[4:0] and/or CS Register Bits D[2:1] are reset upon the execution of an SMBus "echo reset" WRITE_BYTE cycle.

HPI-only Control Applications

In applications where the MIC2593 is controlled only by the HPI, SMBus signals SCL, SDA, and /INT signals are connected to VSTBY as shown in Figure 6. In this configuration, the MIC2593's /FAULT[A/B] outputs are activated after power-on-reset and become asserted when:
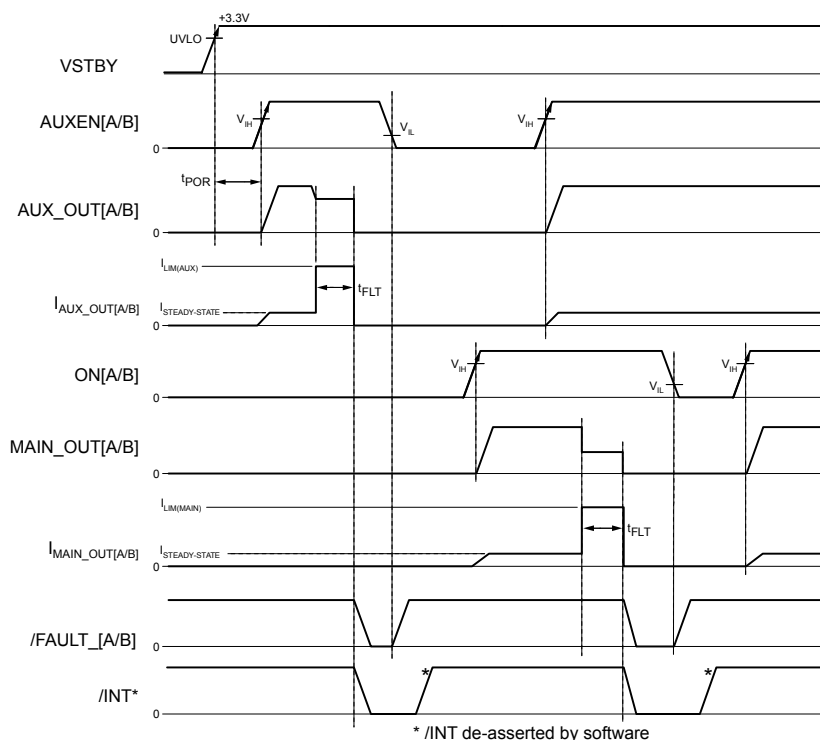

Figure 8. Hot Plug Interface Mode Operation

Either or both external ON[A/B] and AUXEN[A/B] input signals are asserted, AND

- 12VIN[A/B], 12MVIN[A/B], 5VIN[A/B], 3VIN[A/B], or VSTBY[A/B] input voltage is lower than its respective ULVO threshold, OR
- The fast OC circuit breaker[A/B] has tripped, OR
- The slow OC circuit breaker[A/B] has tripped AND its filter timeout[A/B] has expired, OR
- The slow OC circuit breaker[A/B] has tripped AND Slot[A/B] die temperature exceeds 140°C, OR
- The MIC2593's global die temperature exceeds160°C

In order to clear /FAULT[A/B] outputs once asserted, ON[A/B] and/or AUXEN[A/B] input signals must be de-asserted. Please see the /FAULT[A/B] pin description for additional information.

Hot Plug Interface (HPI) Operation

Once the input supplies are above their respective UVLO thresholds, the Hot Plug Interface can be utilized for power control by enabling the control input pins (AUXEN[A/B] and ON[A/B]) for each slot. In order for the MIC2593 to switch on the VAUX supply for either slot, the AUXEN[A/B] control must be enabled after the power-on-reset delay, t_{POR} (typically 500µs), has elapsed. The MAIN output supplies can also be enabled after t_{POR}. The timing response diagram of Figure 8 illustrates a Hot Plug Interface operation where an overcurrent fault is detected by the MIC2593 controller after initiating a power-up sequence. The figure illustrates the output response of /FAULT, /INT, VAUX[A/B] supplies, and an external MOSFET control MAIN[A/B] output supply, either 3.3V or 5V.

MIC2593 SMBus Address Configuration

The MIC2593 responds to its own unique address which is assigned using A2, A1, and A0. These represent the 3 LSBs of its 7-bit address, as shown in Table 3. These address bits are assigned only during power up of the VSTBY[A/B] supply input. These three bits allow up to eight MIC2593 devices in a single system. These pins are either grounded or left unconnected to specify a logical 0 or 1, respectively. A pin designated as a logical 1 may also be pulled up to V_{STBY}.

Serial Port Operation

The MIC2593 uses standard SMBus Write_Byte and Read_Byte operations for communication with its host. The SMBus Write_Byte operation involves sending the device's slave address, with the R/W bit (LSB) set to the low (write) state, followed by a command byte and a data byte. The SMBus Read_Byte operation is similar, but is a composite write and read operation: the host first sends the device's slave address followed by the command byte, as in a write operation. A new "Start" bit must then be sent to the MIC2593, followed by a repeat of the slave address with the R/W bit set to the high (read) state. The data to be read from the part may then be clocked out. There is one exception to this rule: If the location latched in the pointer register from the last write operation is known to be correct (i.e., points to the desired register within the MIC2593), then the "Receive_Byte" procedure may be used. To perform a Receive_Byte operation, the host sends an address byte to select the slave MIC2593, with the R/W bit set to the high (read) state, and then retrieves the data byte. Figures 9 through 11 show the formats for these data read and data write procedures.

The Command Register is eight bits (one byte) wide. This byte carries the address of the MIC2593's register to be operated upon. The command byte values corresponding to the various MIC2593 register addresses are shown in Table 4. Command byte values other than 0000 0XXXb = 00h - 07hare reserved and should not be used.

Inputs			MIC2593 Slave Addresses	
A2	A1	A0	Binary	Hex
0	0	0	1000 000$_b$	80$_h$
0	0	1	1000 001$_b$	82$_h$
0	1	0	1000 010$_b$	84$_h$
0	1	1	1000 011$_b$	86$_h$
1	0	0	1000 100$_b$	88$_h$
1	0	1	1000 101$_b$	8A$_h$
1	1	0	1000 110$_b$	8C$_h$
1	1	1	1000 111$_b$	8E$_h$

Table 3. MIC2593 SMBus Addressing

Register Set and Programmer's Model

Target Register		Common Byte Value		Power-On Default
Label	Description	Read	Write	
RESERVED	Do not Use	00_h	n/a	n/a
RESERVED	Do not Use	01_h	n/a	n/a
CNTRLA	Control Register Slot A	02_h	02_h	00_h
CNTRLB	Control Register Slot B	03_h	03_h	00_h
STATA	Slot A Status	04_h	04_h	00_h
STATB	Slot B Status	05_h	05_h	00_h
CS	Common Status Register	06_h	06_h	$Xxxx\ 0000_b$
RESERVED	Reserved / Do not Use	$07_h\ 0FF_h$	$07_h\ 0FF_h$	Undifined

Table 4. MIC2593 Register Addresses
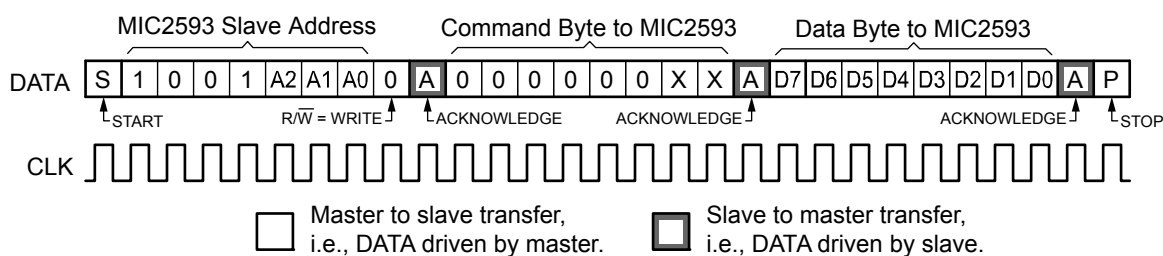
Figure 9.WRITE_BYTE Protocol
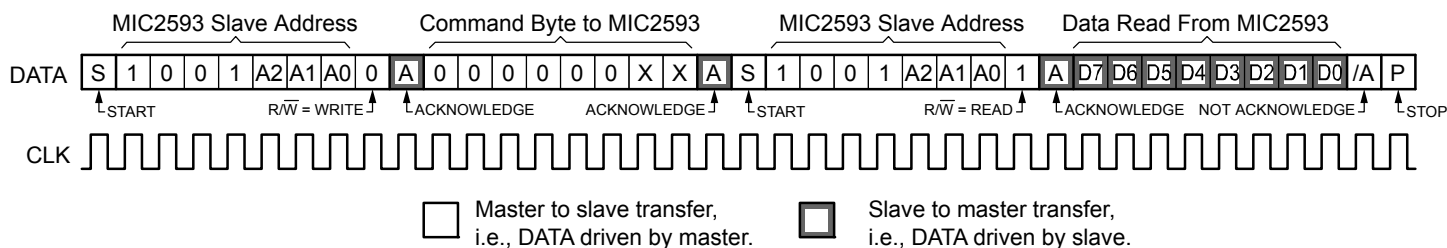
Figure 10.READ_BYTE Protocol
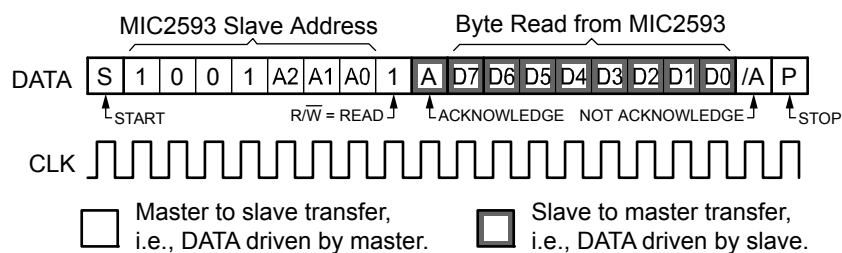
Figure 11.RECEIVE_BYTE Protocol

Detailed Register Descriptions below:

Control Register, Slot A (CNTRLA)

8-Bits, Read/Write

Control Register, Slot A (CNTRLA)							
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read-only	read-only	read-only	read-only	read-only	read-only	read/write	read/write
AUXAPG	MAINAPG	Reserved	Reserved	Reserved	Reserved	MAINA	AUXA

Bit(s)	Function	Operation
AUXAPG	AUX output power-good status, Slot A	1 = Power-is-Good (VAUXA Output is above its UVLO threshold)
MAINAPG	MAIN output power-good status, Slot A	1 = Power-is-Good (MAINA Outputs are above their UVLO thresholds)
D[5]	Reserved	Always read as zero
D[4]	Reserved	Always read as zero
D[3]	Reserved	Always read as zero
D[2]	Reserved	Always read as zero
MAINA	MAIN enable control, Slot A	0 = Off, 1 = On
AUXA	VAUX enable control, Slot A	0 = Off, 1 = On

Power-Up Default Value: $0000\ 0000_b = 00_h$

Read Command_Byte Value (R/W): $0000\ 0010_b = 02_h$

The power-up default value is 00_h. Slot is disabled upon power-up, i.e., all supply outputs are off.

Control Register, Slot A (CNTRLB)

8-Bits, Read/Write

Control Register, Slot B (CNTRLB)							
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read-only	read-only	read-only	read-only	read-only	read-only	read/write	read/write
AUXBPG	MAINBPG	Reserved	Reserved	Reserved	Reserved	MAINB	AUXB

Bit(s)	Function	Operation
AUXBPG	AUX output power-good status, Slot B	1 = Power-is-Good (VAUXB Output is above its UVLO threshold)
MAINBPG	MAIN output power-good status, Slot B	1 = Power-is-Good (MAINB Outputs are above their UVLO thresholds)
D[5]	Reserved	Always read as zero
D[4]	Reserved	Always read as zero
D[3]	Reserved	Always read as zero
D[2]	Reserved	Always read as zero
MAINB	MAIN enable control, Slot B	0 = Off, 1 = On
AUXB	VAUX enable control, Slot B	0 = Off, 1 = On

Power-Up Default Value: $0000\ 0000_b = 00_h$

Command_Byte Value (R/W): $0000\ 0011_b = 03_h$

The power-up default value is 00_h. Slot is disabled upon power-up, i.e., all supply outputs are off.

Status Register, Slot A (STATA)
8-Bits, Read-Only

Status Register, Slot A (STATA)							
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read-only	read-only	read-only	read/write	read/write	read/write	read/write	read/write
FAULTA	MAINA	VAUXA	VAUXAF	12MVAF	12VAF	5VAF	3VAF

Bit(s)	Function	Operation
FAULTA	FAULT Status, Slot A	1 = /FAULTA pin asserted (/FAULTA pin is LOW) 0 = /FAULTA pin de-asserted (/FAULTA pin is HIGH) See Notes 1 and 2
MAINA	MAIN Enable Status, Slot A	Represents the actual state (on/off) of the four Main Power outputs for Slot A (+12V, –12V, +5V and +3.3V) 1 = Main Power ON 0 = Main Power OFF
VAUXA	VAUX Enable Status, Slot A	Represents the actual state (on/off) of the Auxiliary Power output for Slot A 1 = AUX Power ON 0 = Main Power OFF
VAUXAF	Overcurrent Fault: VAUXA supply A	1 = Fault, 0 = No fault
12MVAF	Overcurrent Fault: –12V supply A	1 = Fault, 0 = No fault
12VAF	Overcurrent Fault: +12V supply A	1 = Fault, 0 = No fault
5VAF	Overcurrent Fault: 5V supply A	1 = Fault, 0 = No fault
3VAF	Overcurrent Fault: 3V supply A	1 = Fault, 0 = No fault

Power-Up Default Value: $0000\ 0000_b = 00_h$

Command_Byte Value (R/W): $0000\ 0100_b = 04_h$

The power-up default value is 00_h. Both slots are disabled upon power-up, i.e., all supply outputs are off. In response to anovercurrent fault condition, writing a logical 1 back into the active (or set) bit position will clear the bit and de-assert /INT. Thestatus of the /FAULTA pin is not affected by reading the Status Register or by clearing active status bits.

Note 1.   If FAULTA has been set by an overcurrent condition on one or more of the MAIN outputs, the ONA input must go LOW to reset FAULTA.

If FAULTA has been set by a VAUXA overcurrent event, the AUXENA input must go LOW to reset FAULTA.

If an overcurrent has occurred on both a MAIN output and the VAUX output of slot A, both ONA and AUXENA of the slot must go low to reset FAULTA.

Note 2.   Neither the FAULTA bit nor the /FAULTA pin is active when the MIC2593 power paths are controlled by the System Management Interface. When using SMI power path control, AUXENA and ONA pins for that slot must be tied to GND.

Status Register, Slot B (STATB)

8-Bits, Read-Only

Status Register, Slot B (STATB)							
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read-only	read-only	read-only	read/write	read/write	read/write	read/write	read/write
FAULTB	MAINB	VAUXB	VAUXBF	12MVBF	12VBF	5VBF	3VBF

Bit(s)	Function	Operation
FAULTB	FAULT Status, Slot B	1 = /FAULTB pin asserted (/FAULTB pin is LOW) 0 = /FAULTB pin de-asserted (/FAULTB pin is HIGH) See Notes 1 and 2
MAINB	MAIN Enable Status, Slot B	Represents the actual state (on/off) of the four Main Power outputs for Slot B (+12V, –12V, +5V and +3.3V) 1 = Main Power ON 0 = Main Power OFF
VAUXB	VAUX Enable Status, Slot B	Represents the actual state (on/off) of the Auxiliary Power output for Slot B 1 = AUX Power ON 0 = Main Power OFF
VAUXBF	Overcurrent Fault: VAUXB supply B	1 = Fault, 0 = No fault
12MVBF	Overcurrent Fault: –12V supply B	1 = Fault, 0 = No fault
12VBF	Overcurrent Fault: +12V supply B	1 = Fault, 0 = No fault
5VBF	Overcurrent Fault: 5V supply B	1 = Fault, 0 = No fault
3VBF	Overcurrent Fault: 3V supply B	1 = Fault, 0 = No fault

Power-Up Default Value: $0000\ 0000_b = 00_h$

Command_Byte Value (R/W): $0000\ 0101_b = 05_h$

The power-up default value is 00_h. Both slots are disabled upon power-up, i.e., all supply outputs are off. In response to an overcurrent fault condition, writing a logical 1 back into the active (or set) bit position will clear the bit and de-assert /INT. The status of the /FAULTB pin is not affected by reading the Status Register or by clearing active status bits.

Note 1. If FAULTB has been set by an overcurrent condition on one or more of the MAIN outputs, the ONB input must go LOW to reset FAULTB.

If FAULTB has been set by a VAUXB overcurrent event, the AUXENB input must go LOW to reset FAULTB.

If an overcurrent has occurred on both a MAIN output and the VAUX output of slot B, both ONB and AUXENB of the slot must go low to reset FAULTB.

Note 2. Neither the FAULTB bit nor the /FAULTB pin is active when the MIC2593 power paths are controlled by the System Management Interface. When using SMI power path control, AUXENB and ONB pins for that slot must be tied to GND.

Common Status Register (CS)

8-Bits, Read/Write

Common Status Register (CS)							
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read/write	read/write	read-only	read-only	read/write	read/write	read/write	read-only
Reserved	Reserved	GPI_B	GPI_A	INTMSK	UV_INT	OV_INT	Reserved

Bit(s)	Function	Operation
D[7]	Reserved	Always read as zero
D[6]	Reserved	Always read as zero
GPI_B	General Purpose Input 0, Slot B	State of GPIB pin
GPI_A	General Purpose Input 0, Slot A	State of GPIA pin
INTMSK	Interrupt Mask	0 = /INT generation is enabled 1 = /INT generation is disabled The MIC2593 does not participate in the SMBus Alert Response Address (ARA) protocol.
UV_INT	Undervoltage Interrupt	0 = No UVLO fault 1 = UVLO fault Set whenever a circuit breaker fault condition occurs as a result of an undervoltage lockout condition on one of the main supply inputs. This bit is only set if a UVLO condition occurs while the ON[A/B] pin is asserted or the MAIN[A/B] control bits are set.
OV_INT	Overtemperature Interrupt	0 = Die Temp < 160°C 1 = Fault: Die Temp > 160°C Set if a fault occurs as a result of theMIC2593's die temperature exceeding160°C.
D[0]	Reserved	Undefined

Power-Up Default Value: 0000 0000$_b$ = 00$_h$

Command_Byte Value (R/W):   0000 0110$_b$ = 06$_h$

To reset the OT_INT and UV_INT fault bits, a logical 1 must be written back to these bits.

Application Information

Current Sensing

For the three power supplies switched with internal MOS-FETs (+12V, –12V, and VAUX), the MIC2593 provides all necessary current sensing functions to protect the IC, the load, and the power supply. For the remaining four supplies which the part is designed to control, the high currents at which these supplies typically operate make sensing the current inside the MIC2593 impractical. Therefore, each of these supplies, 3V[A/B] and 5V[A/B], requires an external current sensing resistor. The VIN connection to the IC from each supply (e.g., 5VINA) is connected to the positive terminal of the slot's current sense amplifier, and the corresponding SENSE input (in this case, 5VSENSEA) is connected to the negative terminal of the current sense amplifier.

Sense Resistor Selection

The MIC2593 uses low-value sense resistors to measure the current flowing through the MOSFET switches to the loads. These sense resistors are nominally valued at $50mV/I_{LOAD(CONT)}$. To accommodate worst-case tolerances for the sense resistor (allow ±3% over time and temperature for a resistor with ±1% initial tolerance) and still supply the maximum required steady-state load current, a slightly more detailed calculation must be used.

The current limit threshold voltage (i.e., the "trip point") for the MIC2593 may be as low as 35mV, which would equate to a sense resistor value of $35mV/I_{LOAD(CONT)}$. Carrying the numbers through for the case where the value of the sense resistor is 3% high yields this:

$$R_{SENSE} = \frac{35mV}{(1.03)\left(I_{LOAD(CONT)}\right)} = \frac{34mV}{I_{LOAD(CONT)}}$$

Once the value of R_{SENSE} has been chosen in this manner, it is good practice to check the maximum $I_{LOAD(CONT)}$ which the circuit may let through in the case of tolerance build-up in the opposite direction. Here, the worst-case maximum current is found using a 65mV trip voltage and a sense resistor which is 3% low in value. The resulting current is:

$$I_{LOAD(CONT, MAX)} = \frac{65mV}{(0.97)\left(R_{SENSE(NOM)}\right)} = \frac{67mV}{R_{SENSE(NOM)}}$$

As an example, if an output must carry a continuous 4.5A without nuisance trips occurring, R_{SENSE} for that output should be 34mΩ/4.5A = 7.55mΩ. The nearest standard value is 7.5mΩ, so a 7.5mΩ ±1% resistor would be a good choice. At the other set of tolerance extremes for the output in question, $I_{LOAD(CONT,max)}$ = 67mV/7.5mΩ = 8.93A. Knowing this final datum, we can determine the necessary wattage of the sense resistor, using $P = I^2R$, where I is $I_{LOAD(CONT, MAX)}$, and R is $(0.97)(R_{SENSE(NOM)})$. These numbers yield the following:

$$P_{MAX} = (8.93A)^2 (7.28m\Omega) = 0.581W$$

A 1W sense resistor would work well in this application.

Kelvin Sensing

Because of the low values of the sense resistors, special attention to the layout must be used in order for the MIC2593's circuit breaker function to operate properly. Specifically, the use of a 4-wire Kelvin connection to measure the voltage across R_{SENSE} is highly recommended. Kelvin sensing is simply a means of making sure that any voltage drops in the power traces connecting to the resistors does not get picked up by the traces themselves. The Kelvin connections should be isolated from all other signal traces to avoid introducing noise onto these sensitive nodes. Additionally, a high-frequency noise filter across the sense inputs is highly recommended to avoid nuisance tripping of the (overcurrent) circuit breaker on the opposite slot to the slot that incurred an overcurrent event. Due to the variation of each system's susceptibility to noise, the exact value of this filter is experimentally determined. A value between 10pF to 100pF is a good starting point.

Figure 12 illustrates how Kelvin sensing is performed. All the high current in the circuit (from the 5V supply through R_{SENSE} and then to the drain of the 5V (Slot A) output MOSFET) flows directly through the power PCB traces and R_{SENSE}. The voltage drop resulting across R_{SENSE} is sampled in such away that the high currents through the power traces will not introduce any extraneous IR drops.
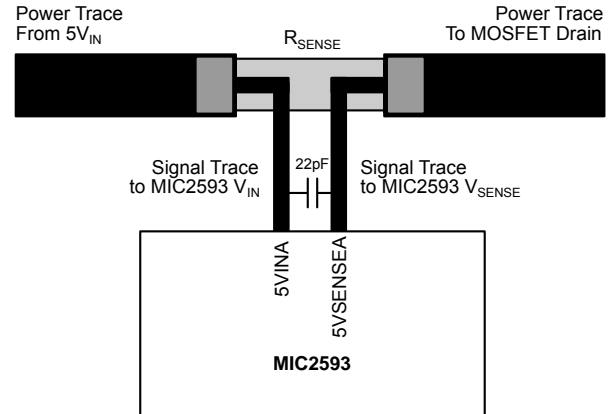

Figure 12. Kelvin Sensing Connections for R_SENSE (Applicable to 5V[A/B] and 3V[A/B])

MOSFET Selection

Selecting the proper MOSFET for use as a current pass and switching element for each of the 3V and 5V slots of the MIC2593 primarily involves three straightforward tasks:

1. Choice of a MOSFET which meets the minimum voltage requirements.

2. Selection of a device to handle the maximum continuous current (steady-state thermal issues).

3. Verification that the selected part can withstand any current peaks (transient thermal issues).

MOSFET Voltage Requirements

The first voltage requirement for each MOSFET is easily stated: the drain-source breakdown voltage of the MOSFET must be greater than $V_{IN(MAX)}$ for the slot in question. For instance, the 5V input may reasonably be expected to see high-frequency transients as high as 6.5V. Therefore, the drain-source breakdown voltage of the MOSFET must be at least 7V.

The second breakdown voltage criteria which must be met is a bit subtler than simple drain-source breakdown voltage, but is not hard to meet. Low-voltage MOSFETs generally have low breakdown voltage ratings from gate to source as well. In MIC2593 applications, the gates of the external MOSFETs are driven from the +12V input to the MIC2593 controller. That supply may well be at 12V + (5% x 12V) = 12.6V. At the same time, if the output of the MOSFET (its source) is suddenly shorted to ground, the gate-source voltage will go to (12.6V – 0V) = 12.6V. This means that the external MOSFETs must be chosen to have a gate-source breakdown voltage in excess of 13V; after 12V absolute maximum, the next commonly available voltage class has a 20V maximum gate-source voltage. At the present time, most power MOSFETs with a 20V gate-source voltage rating have a 30V drain-source breakdown rating or higher. As a general tip, look to surface mount devices with a drain-source rating of 30V as a starting point.

MOSFET Steady-State Thermal Issues

The selection of a MOSFET to meet the maximum continuous current is a fairly straightforward exercise. First, arm yourself with the following data:

- The value of $I_{LOAD(CONT, MAX)}$ for the output in question (see Sense Resistor Selection).
- The manufacturer's data sheet for the candidate MOSFET.
- The maximum ambient temperature in which the device will be required to operate.
- Any knowledge you can get about the heat sinking available to the device (e.g., Can heat be dissipated into the ground plane or power plane, if using a surface mount part? Is any airflow available?).

The data sheet will almost always give a value of on resistance given for the MOSFET at a gate-source voltage of 4.5V, and another value at a gate-source voltage of 10V. As a first approximation, add the two values together and divide by two to get the on-resistance of the part with 7V to 8V of enhancement (11.5V nominal V_{GATE} minus the 3.5V to 4.5V gate threshold of the MOSFET). Call this value R_{ON}. Since a heavily enhanced MOSFET acts as an ohmic (resistive) device, almost all that's required to determine steady-state power dissipation is to calculate I^2R. The one addendum to this is that MOSFETs have a slight increase in R_{ON} with increasing die temperature. A good approximation for this

value is 0.5% increase in R_{ON} per °C rise in junction temperature above the point at which R_{ON} was initially specified by the manufacturer. For instance, if the selected MOSFET has a calculated R_{ON} of 10mΩ at T_J = 25°C and the actual junction temperature ends up at 110°C, a good first cut at the operating value for R_{ON} would be:

$$R_{ON} \cong 10m\Omega[1 + (110 - 25)(0.05)] \cong 14.3m\Omega$$

Next, approximate the steady-state power dissipation (I^2R) using $I_{LOAD(CONT,max)}$ and the approximated R_{ON}.

$$R_{ON} \cong [I_{LOAD(CONT,MAX)}]^2 \times R_{ON} \cong (8.93A)^2 \times 14.3m\Omega \cong 1.14W$$

The final step is to make sure that the heat sinking available to the MOSFET is capable of dissipating at least as much power (rated in °C/W) as that with which the MOSFET's performance was specified by the manufacturer. Here are a few practical tips:

1. The heat from a surface-mount device such as an SO-8 MOSFET flows almost entirely out of the drain leads. If the drain leads can be soldered down to one square inch or more, the copper trace will act as the heat sink for the part. This copper trace must be on the same layer of the board as the MOSFET drain.

2. Airflow works. Even a few LFM (linear feet per minute) of air will cool a MOSFET down substantially. If you can, position the MOSFET(s) near the inlet of a power supply's fan, or the outlet of a processor's cooling fan.

3. The best test of a surface-mount MOSFET for an application (assuming the above tips show it to be a likely fit) is an empirical one. Check the MOSFET's temperature in the actual layout of the expected final circuit, at full operating current. The use of a thermocouple on the drain leads, or infrared pyrometer on the package, will then give a reasonable idea of the device's junction temperature.

MOSFET Transient Thermal Issues

Having chosen a MOSFET that will, a) withstand both the applied voltage stresses, and b) handle the worst-case continuous I^2R power dissipation that it will endure; verifying the MOSFET's ability to handle short-term overload power dissipation without overheating is the lone item to be determined. A MOSFET can handle a much higher pulsed power without damage than its continuous dissipation ratings would imply. The reason for this is that thermal devices (silicon die, lead frames, etc.) have thermal inertia.

In terms related directly to the specification and use of power MOSFETs, this is known as "transient thermal impedance. "Almost all power MOSFET data sheets give a Transient Thermal Impedance Curve. For example, take the case where t_{FLT} for the 5V supply has been set to

50ms, $I_{LOAD(CONT, MAX)}$ is 5.0A, the slow-trip threshold is 50Mv nominal, and the fast-trip threshold is 100mV. If the output is connected to a 0.60Ω load, the output current from the MOSFET for the slot in question will be regulated to 5.0A for 50ms before the MIC2593 circuit breaker trips. During that time, the dissipation in the MOSFET is given by:

$$P = E \times I \quad E_{MOSFET} = \left[5V - 5A(0.6\Omega)\right] = 2V$$

$$P_{MOSFET} = \left(2V \times 5A\right) = 10W \text{ for 50ms}$$

At first glance, it would appear that a really hefty MOSFET is required to withstand this sort of fault condition. This is where the transient thermal impedance curves become very useful. Figure 13 shows the curve for the Vishay (Siliconix) Si4430DY, a commonly used SO-8 power MOSFET.

Taking the simplest case first, we'll assume that once a fault event such as the one in question occurs, it will be a long time, several seconds, before the fault is isolated and the channel is reset. In such a case, we can approximate this as a "single pulse" event, that is to say, there's no significant duty cycle. Then, reading up from the X-axis at the point where "Square Wave Pulse Duration" is equal to 0.1sec (=100msec), we see that the $Z_{\theta(JA)}$ of this MOSFET to a highly infrequent event of this duration is only 7% of its continuous $R_{\theta(JA)}$.

This particular part is specified as having an $R_{\theta(JA)}$ of 35°C/W for intervals of 10 seconds or less. Thus:

Assume T_A = 55°C maximum, 1 square inch of copper at the drain leads, no airflow.

Recalling from our previous approximation hint, the part has an R_{ON} of (0.014/2) = 7mΩ at 25°C.

Assume it has been carrying just about 5A for some time.

When performing this calculation, be sure to use the highest anticipated ambient temperature ($T_{A(MAX)}$) in which the MOSFET will be operating as the starting

temperature, and find the operating junction temperature increase (ΔT_J) from that point. Then, as shown next, the final junction temperature is found by adding $T_{A(MAX)}$ and ΔT_J. Since this is not a closed-form equation, getting a close approximation may take one or two iterations, but it's not a hard calculation to perform and tends to converge quickly.

Then the starting (steady-state) T_J is:

$$T_J \cong T_{A(MAX)} + \Delta T_J$$

$$\cong T_{A(MAX)} + \left[R_{ON} + (T_{A(MAX)} - T_A)(0.005°C)(R_{ON})\right]$$

$$\times I^2 \times R_{\theta(JA)}$$

$$T_J \cong 55°C + \left[7m\Omega + (55°C - 25°C)(0.005)(7m\Omega)\right]$$

$$\times (5A)^2 \times (35°C/W)$$

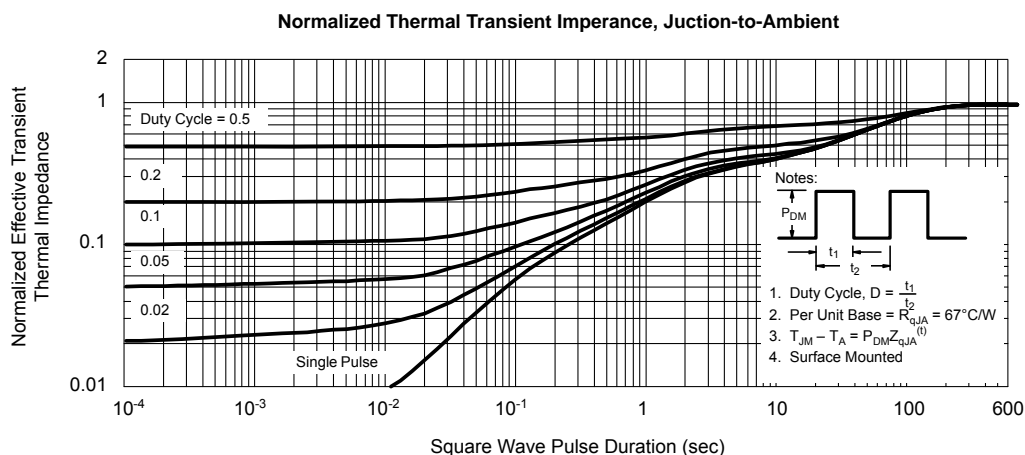$$T_J \cong 55°C + (0.20125W)(35°C)$$

$$\cong 62.0°C$$

Iterate the calculation once to see if this value is within a few percent of the expected final value. For this iteration we will start with T_J equal to the already calculated value of 62.0°C:

$$T_J \cong T_A + \left[7m\Omega + (62.0°C - 25°C)(0.005)(7m\Omega)\right]$$

$$\times (5A)^2 \times (35°C/W)$$

$$T_J \cong 55°C + (0.20125W)(35°C) \cong 62.35°C$$

So our original approximation of 62.0°C was very close to the correct value. We will use T_J = 62°C.

Finally, add (10W)(35°C/W)(0.07) = 24.5°C to the steady-state T_J to get $T_{J(TRANSIENT \ MAX.)}$ = 86.5°C. This is an acceptable maximum junction temperature for this part.

Normalized Thermal Transient Imperance, Juction-to-Ambient

Figure 13. Si4430DY MOSFET Transient Thermal Impedance Curve

MOSFET and Sense Resistor Selection Guide

Listed in Table 5 below, by Manufacturer and Type Number, are some of the more popular MOSFET and resistor types used in PCI hot plug applications. Although far from comprehensive, this information will constitute a good starting point for most designs.

Power Supply Decoupling

In general, prudent system design requires that power supplies used for logic functions should have less than 100mV of noise at frequencies of 100kHz and above. In particular, the –12V supply should have less than 100mV of peak-to-peak noise at frequencies of 1MHz or higher. This is because the –12V supply is the most negative potential applied to the IC, and is therefore connected to the device's substrate. All of the subcircuits integrated onto the silicon chip are hence subjected by capacitive coupling to any HF noise on the –12V supply. While individual capacitances are quite low, the amount of injected energy required to cause a "glitch" can also be quite low at the internal nodes of high speed logic circuits.

Less obviously, but equally important, is the fact that the internal charge pump for the $3.3V_{AUX}$ supplies is somewhat susceptible to noise on the +12V input when that input is at or near zero volts. The +12V supply should not carry HF noise in excess of 200mV peak-to-peak with respect to chip ground when it is in the "off" state.

If either the –12V input, the +12V input, of both supplies do carry significant HF noise (as can happen when they are locally derived by a switching converter), the solution is both small and inexpensive. An LC filter made of a ferrite bead between the noisy power supply input and the MIC2593, followed by a "composite capacitor" from the affected MIC2593 input pin to ground, will suffice for almost any situation. A good composite capacitor for this purpose is the parallel combination of a 47µF tantalum bulk decoupling capacitor, and one 1µF and one 0.01µF ceramic capacitor for high-frequency bypass. A suggested ferrite bead for such use is Fair-Rite Products Corporation part number 2743019447 (this is a surface-mountable part). Similar parts from other vendors or a 0.27µH air-core coil can also be used.
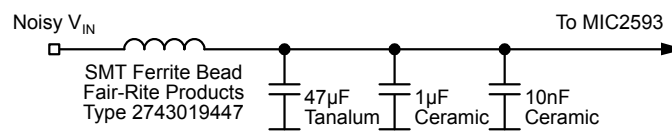

Figure 14. Filter Circuit for Noisy Supplies
(+3.3V and/or –12V)

It is theoretically possible that high-amplitude, HF noise reflected back into one or both of the MIC2593's –12V outputs could interfere with proper device operation, although such noisy loads are unlikely to occur in the real world. If this becomes an application-specific concern, a pair of filters similar to that in Figure 14 will provide the required HF bypassing. The capacitors would be connected to the MIC2593's –12V output pins, and the ferrite beads would be placed between the –12V output pins and the loads.

MOSFET Vendors	Key MOSFET Type(s)	Web Address
Vishay (Siliconix)	Si4430DY ("LittleFoot®" Series)	www.siliconix.com
	Si4420DY ("LittleFoot®" Series)	
International Rectifier	IRF7413A (SO-8 package part)	www.irf.com
	Si4420DY (second source to Vishay)	
Fairchild Semiconductor	FDS6644 (SO-8 package part)	www.fairchildsemi.com
	FDS6670A (SO-8 package part)	
	FDS6688 (SO-8 package part)	

Resistor Vendors	Sense Resistors	Web Address
Vishay (Dale)	WSL Series	
	WSL 3637 Series	www.vishay.com/docs/wsl_30100.pdf
IRC	OARS Series	irctt.com/pdf_files/OARS.pdf
	LR Series	irctt.com/pdf_files/LRC.pdf
	(second source to WSL)	

−12V Input Clamp Diode

The −12V input to the MIC2593 is the most negative potential on the part and is therefore connected to the chip's substrate (as described in "Power Supply Decoupling," above). Although no particular sequencing of the −12V supply relative to the other MIC2593 supplies is required for normal operation, this substrate connection does mean that the −12V input must never exceed the voltage on the GROUND pin of the IC by more than 0.3 volts. Small amounts of internal leakage current can cause this to happen when the VSTBY pins are energized and the 12MVIN pins are not energized. In addition, power supply output ringing or L(di/dt) effects in the wiring and on the PCB itself will cause brief transient voltages in excess of +0.3V to appear at the −12V input. For this reason, it is required to clamp the −12V input to ground with a Schottky diode. A diode rated at 1 amp and 20V to 40V as shown in our application schematic diagram is suggested. The diode's anode should be physically placed directly at the −12V input to the MIC2593, and its cathode should have as short a path as possible back to the part's ground. A good SMT part for this application is a type MBRS140T3 (1A, 40V).

Gate Resistor Guidelines

The MIC2593 controls four external power MOSFETs, that handle the high currents for each of the two 3.3V and 5V outputs. A capacitor is connected in the application circuit from each GATE pin of the MIC2593 to ground. However, an external capacitor, C_{GATE}, is not required for operation of the MIC2593. Each C_{GATE} controls the ramp-up rate of its respective power output (e.g., 5VOUTB). These capacitors, which are typically in the 10nF range, cause the GATE outputs of the MIC2593 to have very low AC impedances to ground at any significant frequency. It is therefore necessary to place a modest value of gate damping resistance (R_{GATE}) between each C_{GATE} and the gate of its associated MOSFET as shown in Figure 15. These resistances prevent high-frequency MOSFET source-follower oscillations from occurring. The exact value of the resistors used is not critical; 10Ω to 33Ω is usually a sufficient choice. Each R_{GATE} should be physically located directly adjacent to the MOSFET gate lead to which it connects.
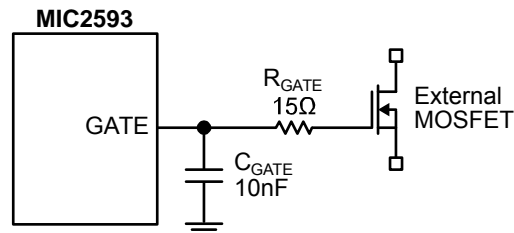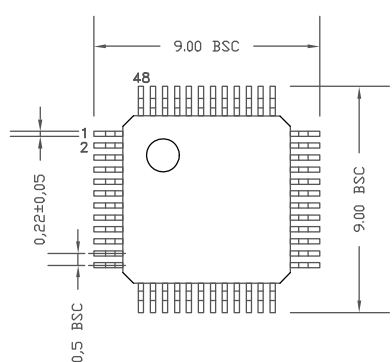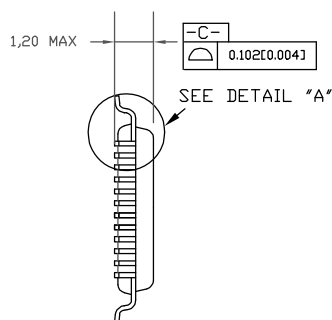

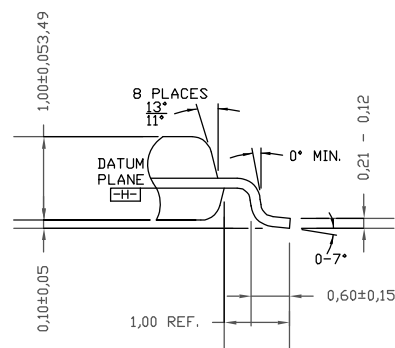**Figure 15.** C_{GATE} and R_{GATE} Connection
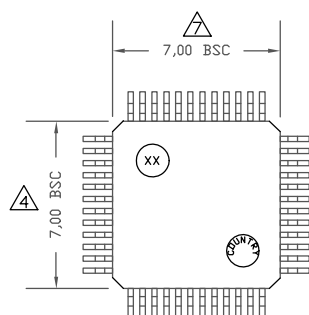
Package Information

TOP VIEW   SIDE VIEW   DETAIL "A"

BOTTOM VIEW

NOTES:

1. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS,
   EITHER OF WHICH SHALL NOT EXCEED 0.254MM.
2. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
3. PACKAGE TOP MOLD DIMENSIONS ARE SMALLER THAN BOTTOM
   MOLD DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG
   BOTTOM OF PACKAGE.

48-Pin TQFP (TQ)

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