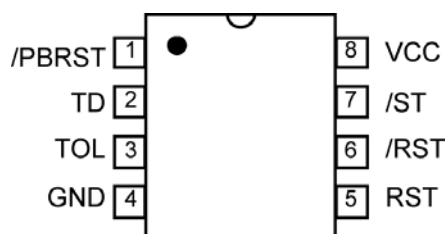


## Ordering Information

Part Number	Temperature Range	Package	Lead Finish
MIC1832NY	−40° to +85°C	8-Pin PDIP	Pb-Free
MIC1832MY	−40° to +85°C	8-Pin SOIC	Pb-Free

## Pin Configuration



8-Pin PDIP  
8-Pin SOIC

## Pin Description

Pin Number	Pin Name	Pin Function
1	/PBRST	Pushbutton Reset input: This input is debounced and can be driven with external logic signals or by using a mechanical pushbutton to actively force a reset. All pulses less than 1ms in duration on the /PBRST pin are ignored; any pulse with a duration of 20ms or greater is guaranteed to cause a reset.
2	TD	Time Delay input: This input selects the timebase used by the watchdog timer. When TD = 0V, the watchdog timeout period is set to a normal value of 150ms. When TD = open, the watchdog timeout period is set to a nominal value of 600ms. When TD = V <sub>CC</sub> , the watchdog period is 1.2s nominally.
3	TOL	Tolerance Select input: This input selects whether 10% or 20% of V <sub>CC</sub> is used as the reset threshold voltage. When TOL = 0V, the 10% tolerance level is selected and when TOL = V <sub>CC</sub> , a 20% tolerance level is selected.
4	GND	IC ground pin, 0V reference
5	RST	RST is asserted high if either V <sub>CC</sub> goes below the reset threshold, the watchdog times out, or /PBRST is pulled low for a minimum of 20ms. RST remains asserted for one reset timeout period after V <sub>CC</sub> exceeds the reset threshold, after the watch times out, or after /PBRST goes high.
6	/RST	/RST is asserted low if either V <sub>CC</sub> goes below the reset threshold, the watchdog times out, or /PBRST is pulled low for a minimum of 20ms. /RST remains asserted for one reset timeout period after V <sub>CC</sub> exceeds the reset threshold, after the watch times out, or after /PBRST goes high. Open-drain output
7	/ST	Input to watchdog timer. If /ST does not see a transition from high to low within the watchdog timeout period, RST and /RST are asserted.
8	VCC	Primary supply input.

**Absolute Maximum Ratings<sup>(1)</sup>**

## Terminal Voltage

 $V_{CC}$  ..... -0.3V to 7VAll other inputs ..... -0.3V to ( $V_{CC} + 0.3V$ )

## Input Current

 $V_{CC}$  ..... 250mA

GND, all other inputs ..... 25mA

Lead Temperature (soldering, 10 sec.) ..... 300°C

Storage Temperature ..... -65°C to 150°C

**Operating Ratings<sup>(2)</sup>**

## Operating Temperature Range

MIC1832M/N ..... -40°C to 85°C

Power Dissipation ..... 700mW

**Electrical Characteristics** $V_{CC} = 1.4V$  to  $5.5V$ ;  $T_A$  = Operating Temperature Range; **bold** values indicate  $-40^\circ C \leq T_A \leq +85^\circ C$ , unless noted.

Parameter	Condition	Min	Typ	Max	Units
Supply Voltage Range	$V_{CC}$	1.4		5.5	V
Supply Current	$I_{CC}$ @ $V_{CC} = 5V^{(3)}$		18	<b>30</b>	$\mu A$
	$I_{CC}$ @ $V_{CC} = 3.3V^{(3)}$		15	<b>25</b>	$\mu A$
/ST and /PBRST Input Levels	$V_{IH}^{(4)}$	<b>2</b>		$V_{CC} + 0.3$	V
	$V_{IH}^{(5)}$	$V_{CC} - 0.4$		$V_{CC} + 0.3$	V
	$V_{IL}$	<b>-0.3</b>		<b>0.5</b>	V
Input Leakage, /ST <sup>(6)</sup>	$I_{IL}$			<b><math>\pm 1</math></b>	$\mu A$
Output Voltage, /RST, RST	$I_{SOURCE} = 350\mu A$ , $V_{CC} = 3.3V$	2.4			V
Output Voltage, /RST, RST	$I_{SINK} = 10mA$ , $V_{CC} = 3.3V$			<b>0.4</b>	V
Output Voltage	$V_{CC} = 1.4V$ , $I_{SINK} = 50\mu A$			0.3	V
$V_{CC}$ 10% Trip Point (Reset Threshold Voltage)	TOL = Gnd	<b>2.80</b>	2.88	<b>2.97</b>	V
$V_{CC}$ 20% Trip Point (Reset Threshold Voltage)	TOL = $V_{CC}$	<b>2.47</b>	2.55	<b>2.64</b>	V
Input Capacitance, /ST, TOL	$C_{IN}^{(7)}$			5	pF
Output Capacitance, /RST, RST	$C_{OUT}^{(7)}$			7	pF

**Notes:**

- Exceeding the absolute maximum rating may damage the device.
- The device is not guaranteed to function outside its operating rating.
- $I_{CC}$  is measured with /PBRST and all outputs open and inputs within 0.5V of supply rails.
- Measured with  $V_{CC} \geq 2.7V$ .
- Measured with  $V_{CC} < 2.7V$ .
- /PBRST has an internal pull-up resistor to  $V_{CC}$  (typ. 40k $\Omega$ ).
- Guaranteed by design at  $T_A = 25^\circ C$ .

## AC Electrical Characteristics

$V_{CC} = 1.4V$  to  $5.5V$   $T_A$  = Operating Temperature Range; **bold** values indicate  $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ , unless noted.

Parameter	Condition	Min	Typ	Max	Units
/PBRST Min. Pulse Width, $t_{PB}$	/PBRST = $V_{IL}$ <sup>(1)</sup>	<b>20</b>			ms
/PBRST Delay, $t_{PBD}$		<b>1</b>	4	<b>20</b>	ms
Reset Active Time, $t_{RST}$		<b>250</b>	610	<b>1000</b>	ms
/ST Pulse Width, $t_{ST}$		<b>20</b>			ns
/ST Timeout Period, $t_{TD}$	TD = 0V	<b>62.5</b>	150	<b>250</b>	ms
	TD = Open	<b>250</b>	600	<b>1000</b>	ms
	TD = $V_{CC}$	<b>500</b>	1200	<b>2000</b>	ms
$V_{CC}$ Fall Time, $t_F$		<b>40</b>			$\mu s$
$V_{CC}$ Rise Time, $t_R$		<b>0</b>			ns
$V_{CC}$ Detect to /RST Low and RST High, $t_{RPD}$	$V_{CC}$ Falling <sup>(2)</sup>		5	<b>8</b>	$\mu s$
$V_{CC}$ Detect to /RST Low and RST Low, $t_{RPD}$	$V_{CC}$ Falling <sup>(1)</sup>	<b>250</b>	610	<b>1000</b>	$\mu s$

### Notes:

1. /PBRST must be held low for a minimum of 20ms to guarantee a reset.
2.  $V_{CC}$  falling at 8.5mV/ $\mu s$ .

## Timing Diagrams

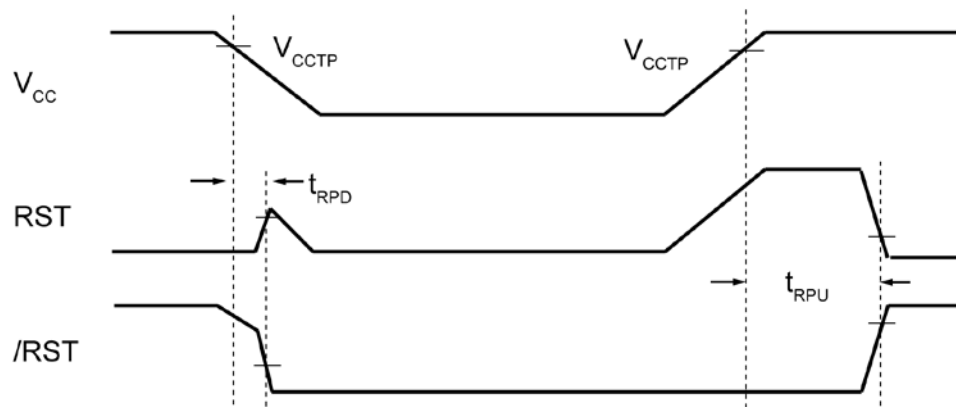


Figure 1. Power-Up/Power-Down Sequence

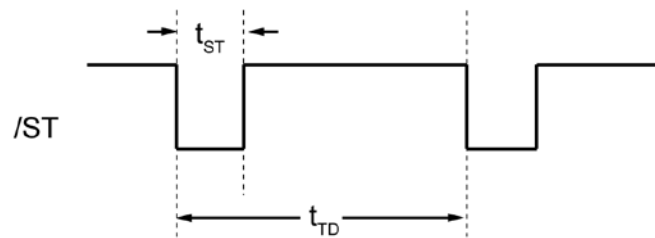


Figure 2. Watchdog Input

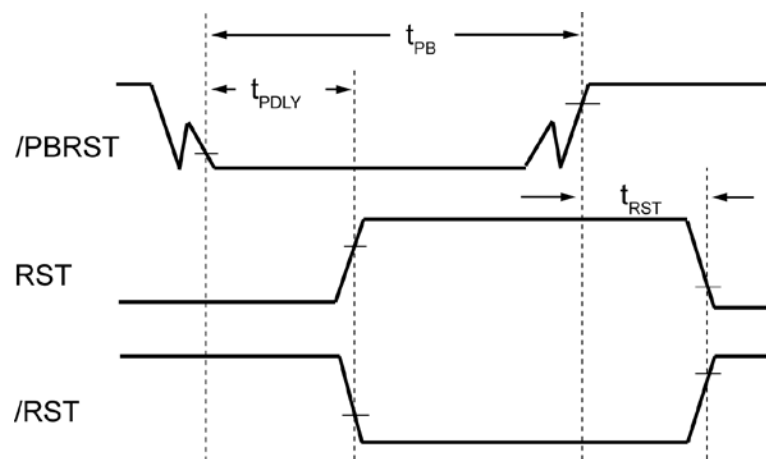


Figure 3. Pushbutton Reset

## Application Information

### Power Monitor

The /RST and RST pins are asserted whenever  $V_{CC}$  falls below the reset threshold voltage determined by the TOL pin. A 10% of 3.3V tolerance level (2.97V reset threshold voltage) can be selected by connecting the TOL pin to ground. A 20% of 3.3V tolerance level (2.64V reset threshold voltage) can be selected by connecting the TOL pin to  $V_{CC}$ . The reset pins will remain asserted for a period of 250ms after  $V_{CC}$  has risen above the reset threshold voltage. The reset function ensures that the microprocessor is properly reset and powers up into a known condition after a power failure. /RST will remain valid with  $V_{CC}$  as low as 1.4V.

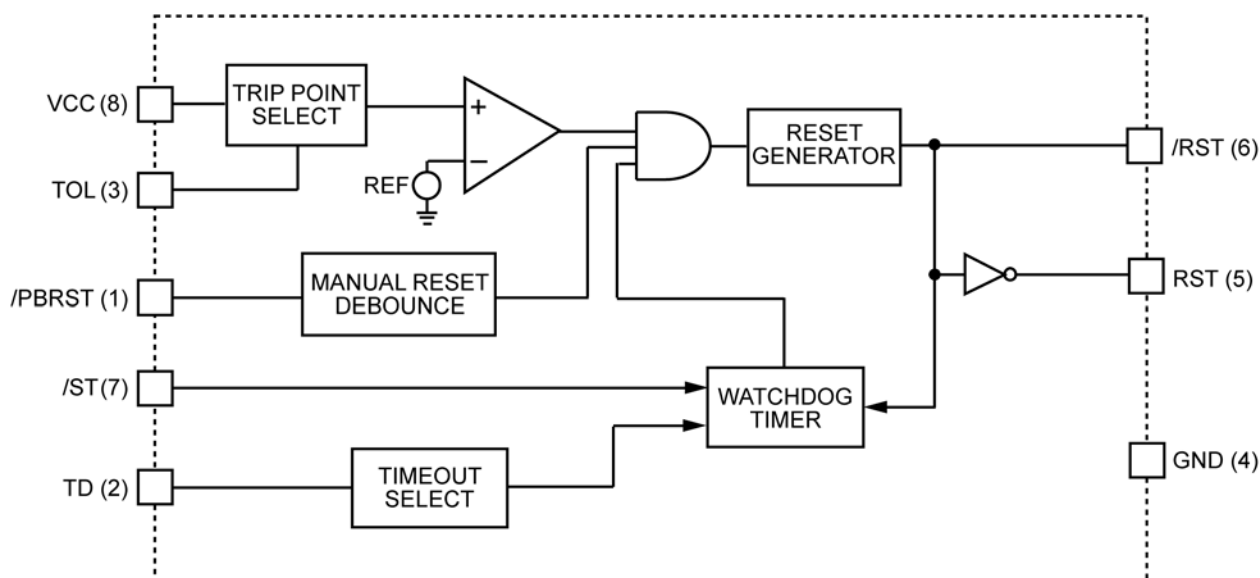
### Watchdog Timer

The microprocessor can be mounted by connecting the /ST pin (watchdog input) to a bus line or I/O line. If a high-to-low does not occur on the /ST pin within the watchdog timeout period determined by the TD pin (see the Electrical Characteristics Table), the /RST and the RST will remain asserted for 250ms. A minimum pulse of 20ns or any transition high-to-low on the /ST pin resets the watchdog timer. The watchdog timer is reset if /ST sees a valid transition within the watchdog timeout period.

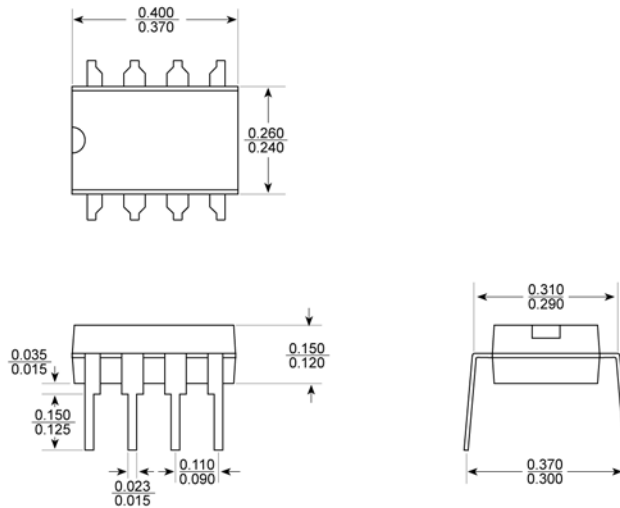
### Pushbutton Reset Input

The /PBRST input can be driven with a manual pushbutton switch or with external logic signals. The input is internally debounced and requires an active low signal to force the reset outputs into their active states. The /PBRST input recognizes any pulse that is 20ms or longer in duration and ignores all pulses that are less than 1ms in duration.

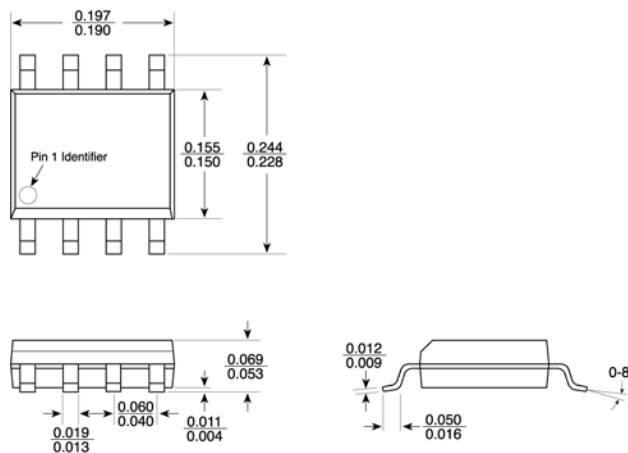
## Block Diagram



## Package Information<sup>(1)</sup>



**8-Pin DIP (N)**



**8-Pin SOIC (M)**

**Note:**

- Package information is correct as of the publication date. For updates and most current information, go to [www.micrel.com](http://www.micrel.com).

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