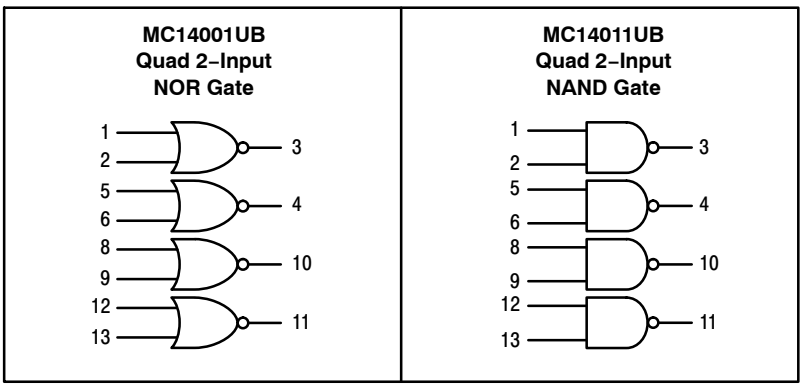
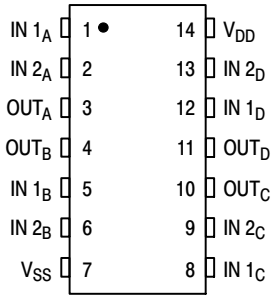
LOGIC DIAGRAMS



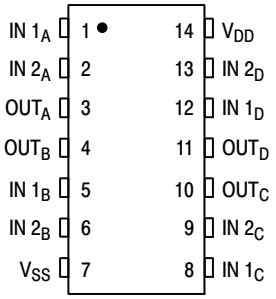
V_{DD} = PIN 14
V_{SS} = PIN 7
FOR ALL DEVICES

PIN ASSIGNMENTS

MC14001UB
Quad 2−Input NOR Gate



MC14011UB
Quad 2−Input NAND Gate



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD} "1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
Input Voltage "0" Level (V_O = 4.5 Vdc) (V_O = 9.0 Vdc) (V_O = 13.5 Vdc)	V_{IL}	5.0 10 15	– – –	1.0 2.0 2.5	– – –	2.25 4.50 6.75	1.0 2.0 2.5	– – –	1.0 2.0 2.5	Vdc
(V_O = 0.5 Vdc) "1" Level (V_O = 1.0 Vdc) (V_O = 1.5 Vdc)	V_{IH}	5.0 10 15	4.0 8.0 12.5	– – –	4.0 8.0 12.5	2.75 5.50 8.25	– – –	4.0 8.0 12.5	– – –	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 1.0 – 0.25 – 0.62 – 1.8	– – – –	– 0.75 – 0.2 – 0.4 – 1.5	– 1.7 – 0.36 – 0.9 – 3.5	– – – –	– 0.55 – 0.14 – 0.15 – 1.0	– – – –	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.1 3.4	0.88 2.25 8.8	– – –	0.36 0.7 2.4	– – –	mAdc
Input Current	I_{in}	15	–	± 0.1	–	±0.00001	± 0.1	–	± 1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	– – –	0.25 0.5 1.0	– – –	0.0005 0.0010 0.0015	0.25 0.5 1.0	– – –	7.5 15 30	μAdc
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Gate C_L = 50 pF)	I_T	5.0 10 15	I_T = (0.3 μA/kHz) f + I_{DD}/N I_T = (0.6 μA/kHz) f + I_{DD}/N I_T = (0.8 μA/kHz) f + I_{DD}/N							μAdc

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μH (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 x the number of exercised gates per package.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise Time t_{TLH} = (3.0 ns/pF) C_L + 30 ns t_{TLH} = (1.5 ns/pF) C_L + 15 ns t_{TLH} = (1.1 ns/pF) C_L + 10 ns	t_{TLH}	5.0 10 15	– – –	180 90 65	360 180 130	ns
Output Fall Time t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 15 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	90 50 40	180 100 80	ns

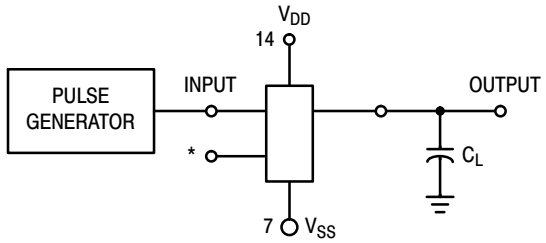
5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

ORDERING INFORMATION

Device	Package	Shipping†
MC14001UBCPG	PDIP−14 (Pb−Free)	25 Units / Rail
MC14001UBDG	SOIC−14 (Pb−Free)	55 Units / Rail
NLV14001UBDG*		
MC14001UBDR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
NLV14001UBDR2G*		
MC14011UBCPG	PDIP−14 (Pb−Free)	25 Units / Rail
NLV14011UBCPG*		
MC14011UBDG	SOIC−14 (Pb−Free)	55 Units / Rail
NLV14011UBDG*		
MC14011UBDR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
NLV14011UBDR2G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.



*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.

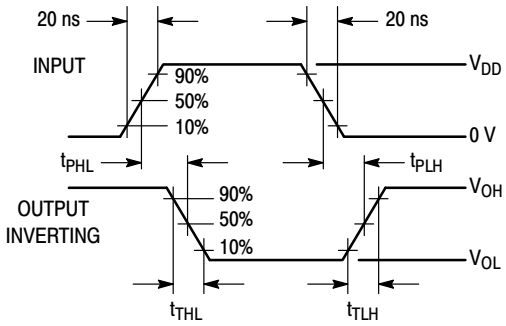
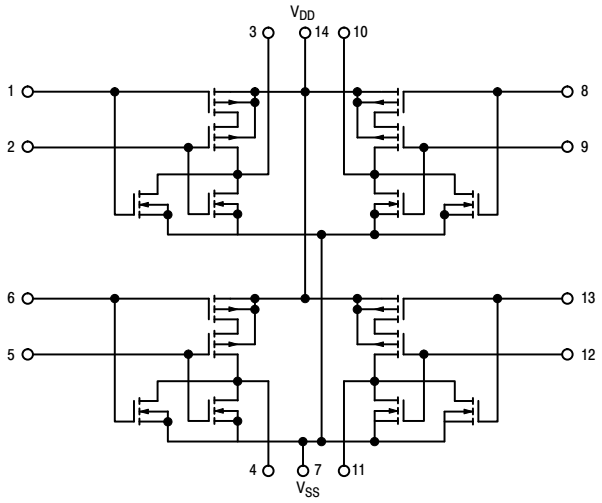
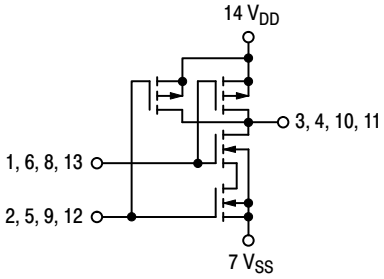


Figure 1. Switching Time Test Circuit and Waveforms

MC14001UB CIRCUIT SCHEMATIC



MC14011UB CIRCUIT SCHEMATIC
(1/4 of Device Shown)



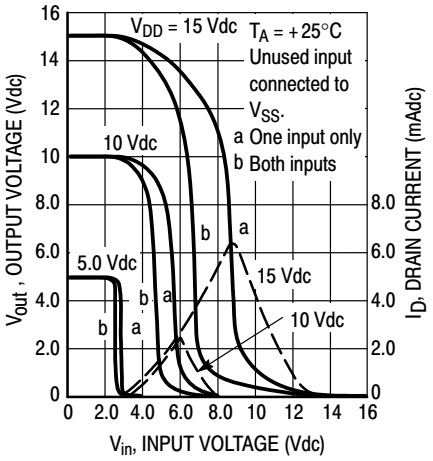


Figure 2. Typical Voltage and Current Transfer Characteristics

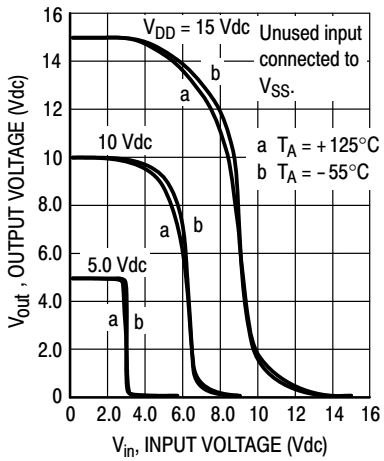


Figure 3. Typical Voltage Transfer Characteristics versus Temperature

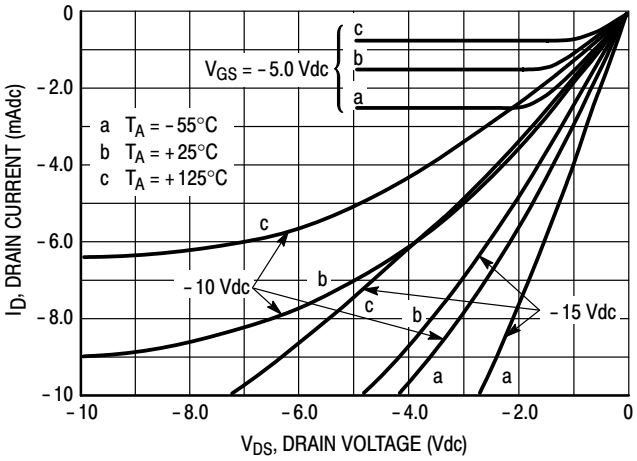


Figure 4. Typical Output Source Characteristics

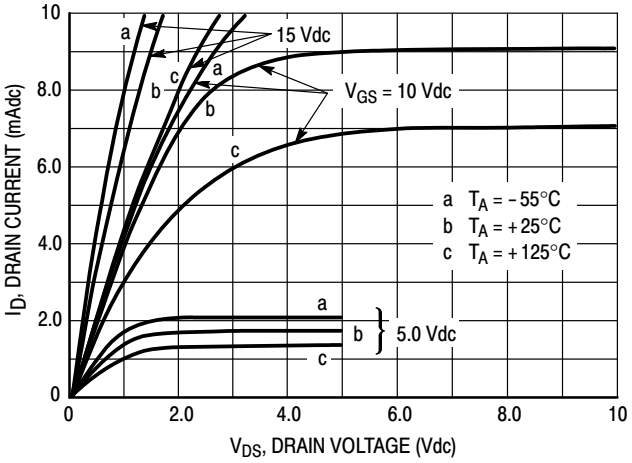
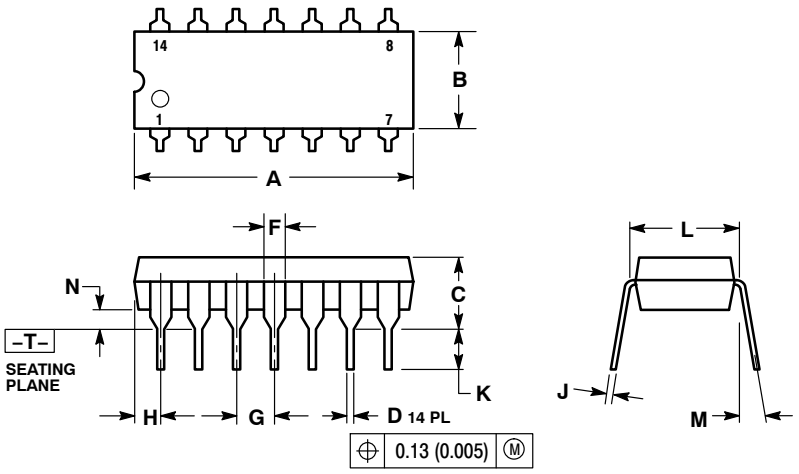


Figure 5. Typical Output Sink Characteristics

PACKAGE DIMENSIONS

PDIP−14
CASE 646−06
ISSUE P

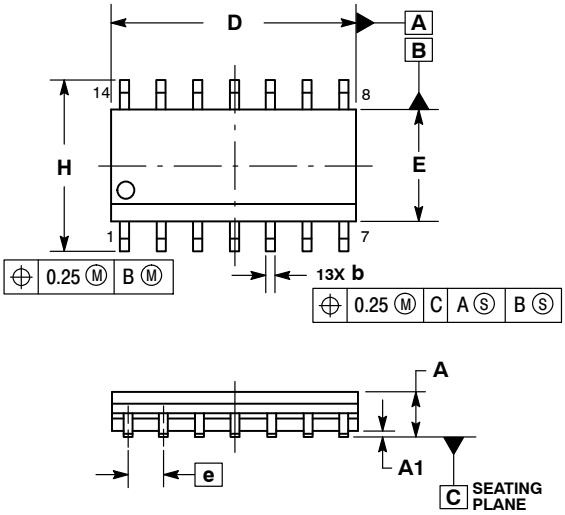


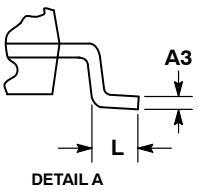
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

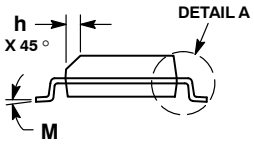
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	−−−	10 °	−−−	10 °
N	0.015	0.039	0.38	1.01

PACKAGE DIMENSIONS

SOIC−14 NB
CASE 751A−03
ISSUE K



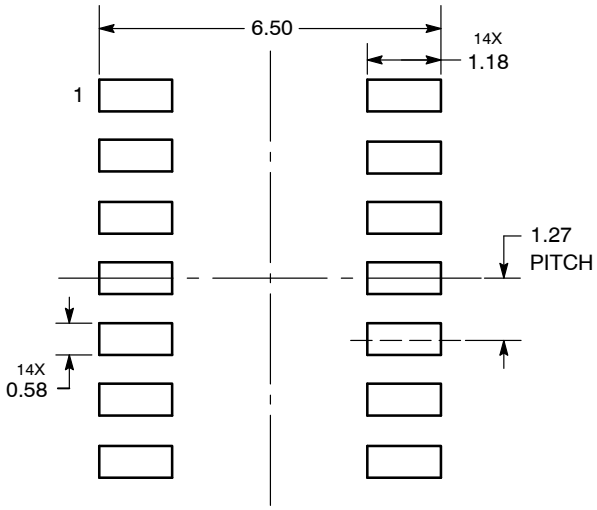




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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