200kHz, 4µA, Rail-to-Rail I/O Op Amps with Shutdown

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{DD} to V_{SS}) ....-0.3V to +6.0V
IN_+, IN_-, OUT_, $\overline{SHDN}$_............... (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Current into IN_+, IN_- ....±20mA
Output Short-Circuit Duration to V_{DD} or V_{SS} ....Continuous
Continuous Power Dissipation (T_A = +70°C)
5-Pin SC70 (derate 3.1mW/°C above +70°C)............. 247mW
6-Bump WLP (derate 10.5mW/°C above +70°C).........840mW
6-Pin SC70 (derate 3.1mW/°C above +70°C)............. 245mW
8-Pin SOT23 (derate 9.1mW/°C above +70°C)........... 727mW
10-Pin µMAX (derate 5.6mW/°C above +70°C)...........444mW
Operating Temperature Range .... -40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (excluding WLP, soldering 10s)........+300°C
Soldering Temperature (reflow)
Lead(Pb)-Free Packages...+260°C
Packages Containing Lead(Pb)...................................+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.8V to 5.5V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD} / 2, R_L = ∞ connected to V_{DD} / 2, $\overline{SHDN}$_ = V_{DD}, **T_A = +25°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSRR test		1.8		5.5	V
Supply Current	I_{DD}	MAX9910/MAX9911	V_{DD} = 1.8V		4		µA
			V_{DD} = 5.5V		4	5.0	
		MAX9912/MAX9913	V_{DD} = 1.8V		7		
			V_{DD} = 5.5V		7	9	
Shutdown Supply Current	$I_{DD(\overline{SHDN}\_)}$	$\overline{SHDN}$_ = GND, MAX9911/MAX9913			0.001	0.5	µA
Input Offset Voltage	V_{OS}				±0.2	±1	mV
Input-Offset-Voltage Matching		MAX9912/MAX9913			±250		µV
Input Bias Current	I_B	(Note 2)			±1	±10	pA
Input Offset Current	I_{OS}	(Note 2)			±1	±10	pA
Input Resistance	R_{IN}	Common mode			1		GΩ
		Differential mode, -1mV < V_{IN} < +1mV			10		
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR test		V_{SS} - 0.1		V_{DD} + 0.1	V
Common-Mode Rejection Ratio	CMRR	-0.1V < V_{CM} < V_{DD} + 0.1V, V_{DD} = 5.5V		70	80		dB
Power-Supply Rejection Ratio	PSRR	1.8V < V_{DD} < 5.5V		65	95		dB
Open-Loop Gain	A_{VOL}	25mV < V_{OUT} < V_{DD} - 25mV, R_L = 100kΩ, V_{DD} = 5.5V		95	120		dB
		100mV < V_{OUT} < V_{DD} - 100mV, R_L = 5kΩ, V_{DD} = 5.5V		95	110		
Output-Voltage-Swing High	V_{OH}	V_{DD} - V_{OUT}	R_L = 100kΩ		2.5	5	mV
			R_L = 5kΩ		50	70	
			R_L = 1kΩ		250		
Output-Voltage-Swing Low	V_{OL}	V_{OUT} - V_{SS}	R_L = 100kΩ		2.5	5	mV
			R_L = 5kΩ		50	70	
			R_L = 1kΩ		250		
Channel-to-Channel Isolation	CH_{ISO}	Specified at DC, MAX9912/MAX9913			100		dB
Output Short-Circuit Current	$I_{OUT(SC)}$				±15		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 1.8V to 5.5V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD} / 2, R_L = ∞ connected to V_{DD} / 2, $\overline{SHDN}$_ = V_{DD}, **T_A = +25°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SHDN}$_ Logic Low	V_{IL}	V_{DD} = 1.8V to 3.6V, MAX9911/MAX9913			0.4	V
		V_{DD} = 3.6V to 5.5V, MAX9911/MAX9913			0.8	
$\overline{SHDN}$_ Logic High	V_{IH}	V_{DD} = 1.8V to 3.6V, MAX9911/MAX9913	1.4			V
		V_{DD} = 3.6V to 5.5V, MAX9911/MAX9913	2			
$\overline{SHDN}$_ Input Bias Current	I_{IL}	$\overline{SHDN}$_ = V_{SS}, MAX9911/MAX9913 (Note 2)			1	nA
	I_{IH}	$\overline{SHDN}$_ = V_{DD} , MAX9911/MAX9913			500	
Output Leakage in Shutdown	$I_{OUT(\overline{SHDN}\_)}$	$\overline{SHDN}$_ = V_{SS}, V_{OUT} = 0V to V_{DD}, MAX9911/MAX9913		1	500	nA
Gain-Bandwidth Product				200		kHz
Slew Rate				0.1		V/µs
Capacitive-Load Stability (See the *Driving Capacitive Loads* Section)	C_{LOAD}	No sustained oscillations, A_V = 1V/V		30		pF
		No sustained oscillations, A_V = 10V/V		250		
		No sustained oscillations, R_L = 5kΩ, A_V = 1V/V		200		
		No sustained oscillations, R_{ISO} = 1kΩ, A_V = 1V/V		100		
Input Voltage-Noise Density		f = 1kHz		400		nV/√Hz
Input Current-Noise Density		f = 1kHz		0.001		pA/√Hz
Settling Time		To 0.1%, V_{OUT} = 2V step, A_V = -1V/V		18		µs
Delay Time to Shutdown	t_{SH}	I_{DD} = 5% of normal operation, V_{DD} = 5.5V, $V_{\overline{SHDN}\_}$ = 5.5V to 0 step		2		µs
Delay Time to Enable	t_{EN}	V_{OUT} = 2.7V, V_{OUT} settles to 0.1%, V_{DD} = 5.5V, $V_{\overline{SHDN}\_}$ = 0 to 5.5V step		30		µs
Power-Up Time		V_{DD} = 0 to 5.5V step		5		µs

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.8V to 5.5V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD} / 2, R_L = ∞ connected to V_{DD} / 2, $\overline{SHDN}$_ = V_{DD}, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSRR test	1.8		5.5	V
Supply Current	I_{DD}	MAX9910/MAX9911, V_{DD} = 5.5V			5.5	µA
		MAX9912/MAX9913, V_{DD} = 5.5V			11	
Shutdown Supply Current	$I_{DD(\overline{SHDN}\_)}$	$\overline{SHDN}$_ = GND, MAX9911/MAX9913			1	µA
Input Offset Voltage	V_{OS}				±5	mV
Input-Offset-Voltage Temperature Coefficient	TC_{VOS}			±5		µV/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 1.8V to 5.5V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD} / 2, R_L = ∞ connected to V_{DD} / 2, $\overline{SHDN\_}$ = V_{DD}, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

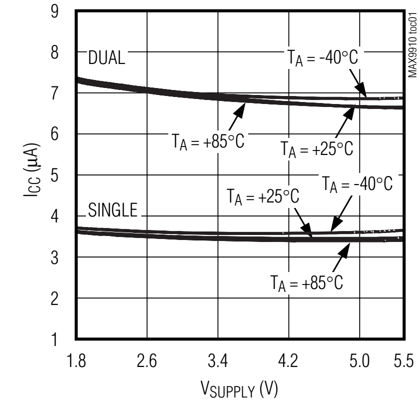
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Bias Current	I_B					±30	pA
Input Offset Current	I_{OS}					±20	pA
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR test		V_{SS} - 0.05		V_{DD} + 0.05	V
Common-Mode Rejection Ratio	CMRR	-0.05V < V_{CM} < V_{DD} + 0.05V, V_{DD} = 5.5V		60			dB
Power-Supply Rejection Ratio	PSRR	1.8V < V_{DD} < 5.5V		59			dB
Open-Loop Gain	A_{VOL}	25mV < V_{OUT} < V_{DD} - 25mV, R_L = 100kΩ, V_{DD} = 5.5V		85			dB
		150mV < V_{OUT} < V_{DD} - 150mV, R_L = 5kΩ, V_{DD} = 5.5V		80			
Output-Voltage-Swing High	V_{OH}	V_{DD} - V_{OUT}	R_L = 100kΩ			5	mV
			R_L = 5kΩ			90	
Output-Voltage-Swing Low	V_{OL}	V_{OUT} - V_{SS}	R_L = 100kΩ			5	mV
			R_L = 5kΩ			90	
$\overline{SHDN\_}$ Logic Low	V_{IL}	V_{DD} = 1.8V to 3.6V				0.4	V
		V_{DD} = 3.6V to 5.5V				0.8	
$\overline{SHDN\_}$ Logic High	V_{IH}	V_{DD} = 1.8V to 3.6V, MAX9911/MAX9913		1.4			V
		V_{DD} = 3.6V to 5.5V, MAX9911/MAX9913		2			
$\overline{SHDN\_}$ Input-Bias Current	I_{IL}	$\overline{SHDN\_}$ = V_{SS}, MAX9911/MAX9913				5	nA
	I_{IH}	$\overline{SHDN\_}$ = V_{DD}, MAX9911/MAX9913				1000	nA
Output Leakage in Shutdown	$I_{OUT(\overline{SHDN\_})}$	$\overline{SHDN\_}$ = V_{SS}, V_{OUT} = 0V to V_{DD}, MAX9911/MAX9913				1000	nA

Note 1: Specifications are 100% tested at T_A = +25°C (exceptions noted). All temperature limits are guaranteed by design.
Note 2: Guaranteed by design, not production tested.

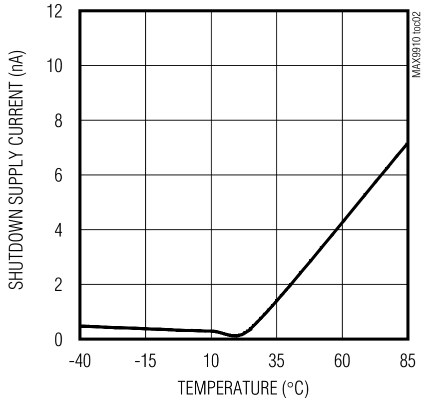
Typical Operating Characteristics

(V_{DD} = 3V, V_{SS} = V_{CM} = 0V, R_L to V_{DD} / 2, T_A = +25°C, unless otherwise noted.)

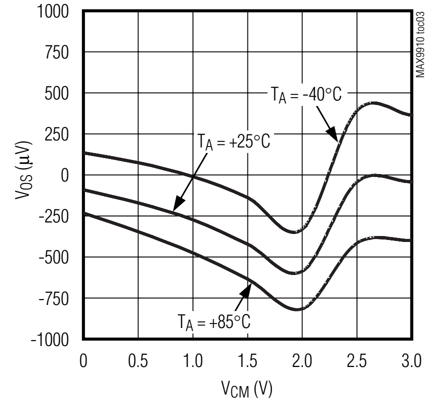
SUPPLY CURRENT vs. SUPPLY VOLTAGE



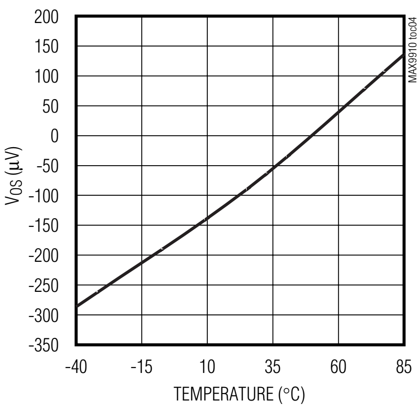
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



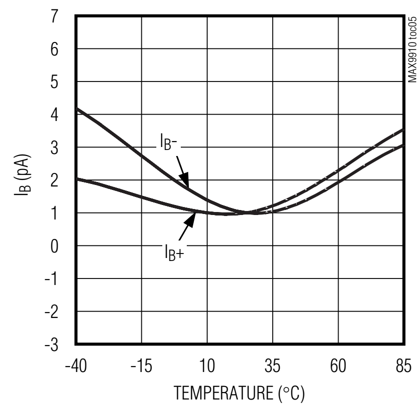
INPUT OFFSET VOLTAGE vs. INPUT COMMON-MODE VOLTAGE



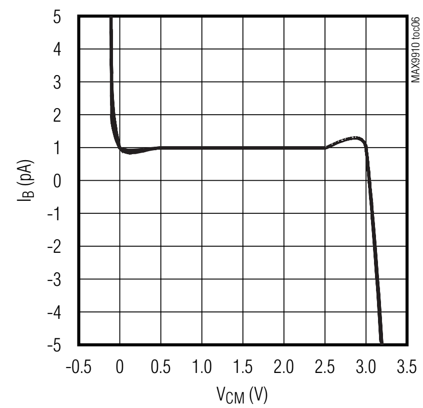
INPUT OFFSET VOLTAGE vs. TEMPERATURE



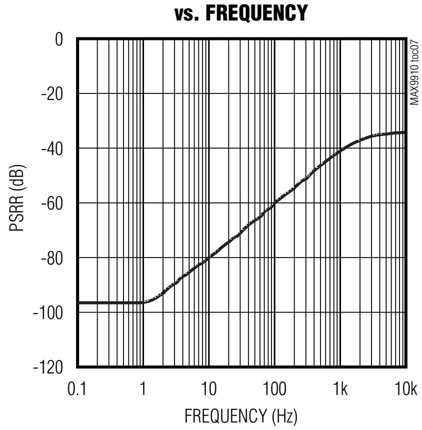
INPUT BIAS CURRENT vs. TEMPERATURE



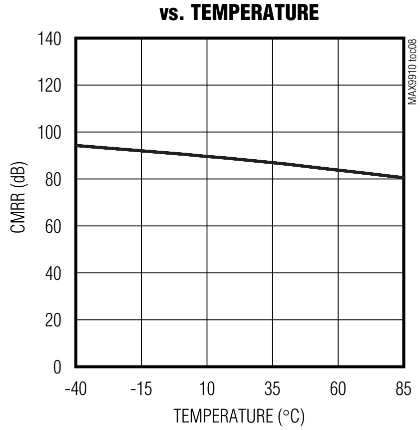
INPUT BIAS CURRENT vs. INPUT COMMON-MODE VOLTAGE



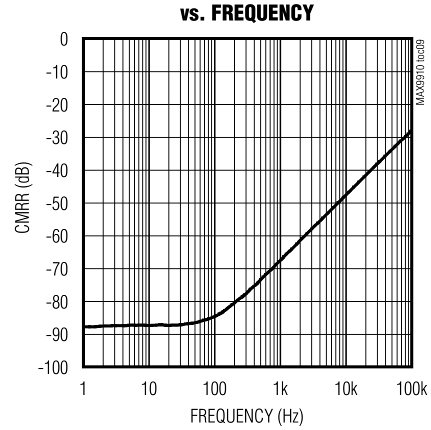
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



COMMON-MODE REJECTION RATIO vs. TEMPERATURE



COMMON-MODE REJECTION RATIO vs. FREQUENCY

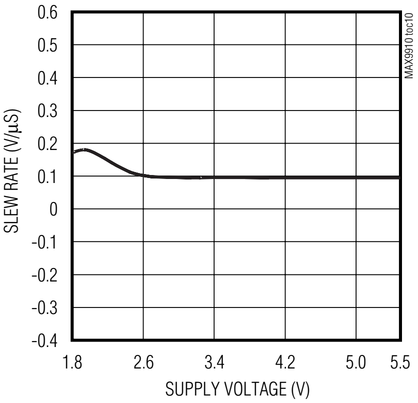


200kHz, 4µA, Rail-to-Rail I/O Op Amps with Shutdown

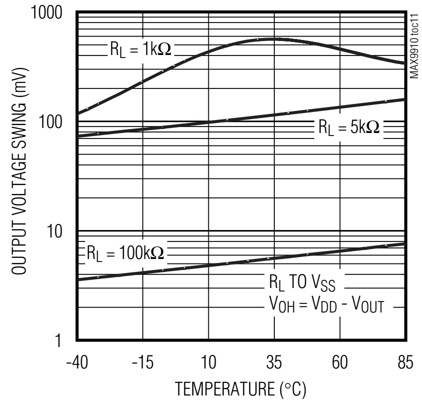
Typical Operating Characteristics (continued)

(V_{DD} = 3V, V_{SS} = V_{CM} = 0V, R_L to V_{DD} / 2, T_A = +25°C, unless otherwise noted.)

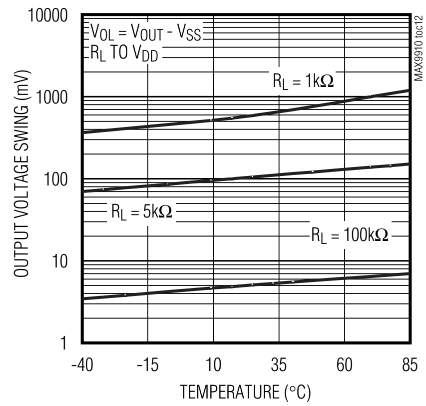
SLEW RATE vs. SUPPLY VOLTAGE



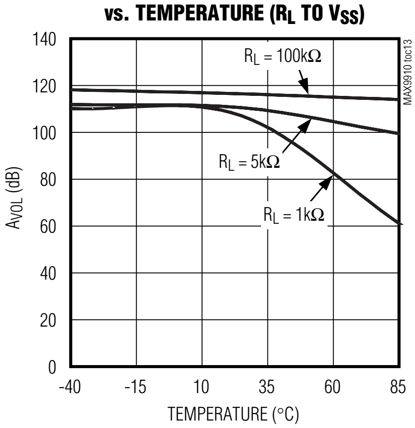
OUTPUT-SWING HIGH vs. TEMPERATURE



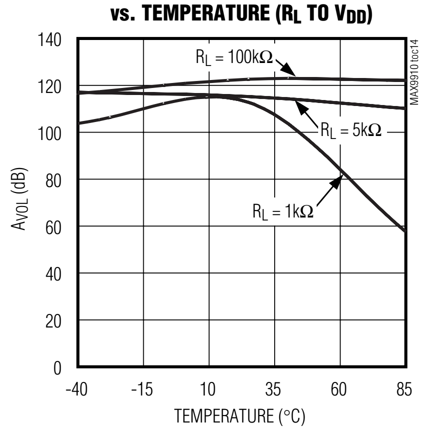
OUTPUT-SWING LOW vs. TEMPERATURE



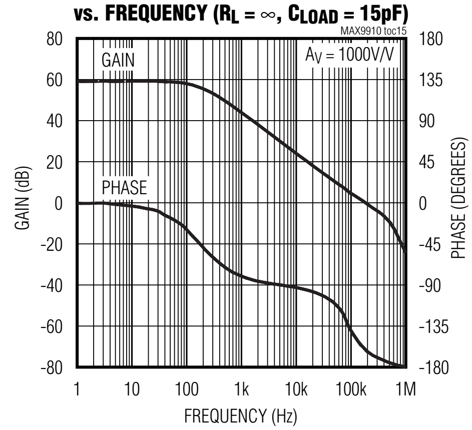
OPEN-LOOP GAIN vs. TEMPERATURE (R_L TO V_{SS})



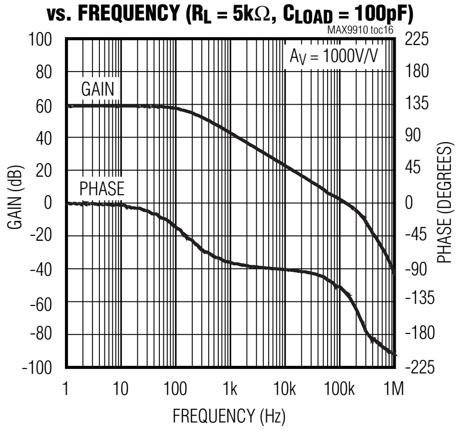
OPEN-LOOP GAIN vs. TEMPERATURE (R_L TO V_{DD})



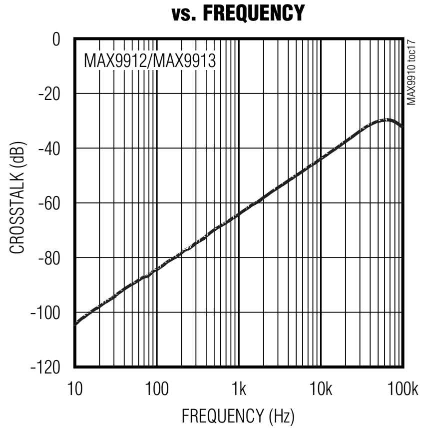
GAIN AND PHASE vs. FREQUENCY (R_L = ∞, C_{LOAD} = 15pF)



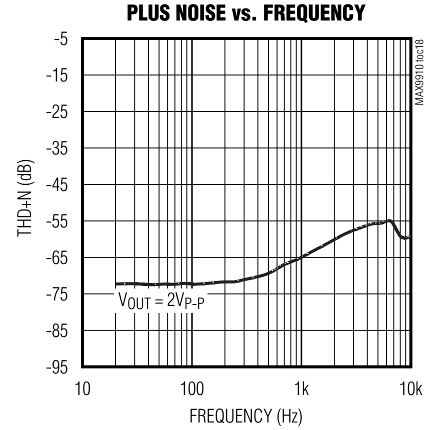
GAIN AND PHASE vs. FREQUENCY (R_L = 5kΩ, C_{LOAD} = 100pF)



CROSSTALK vs. FREQUENCY



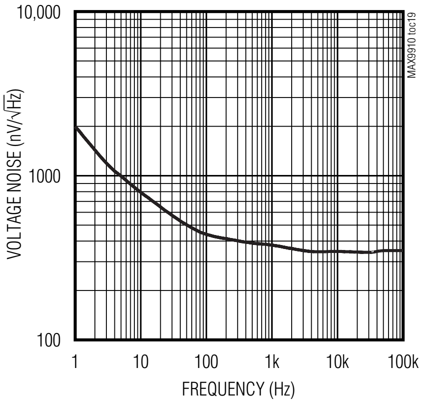
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



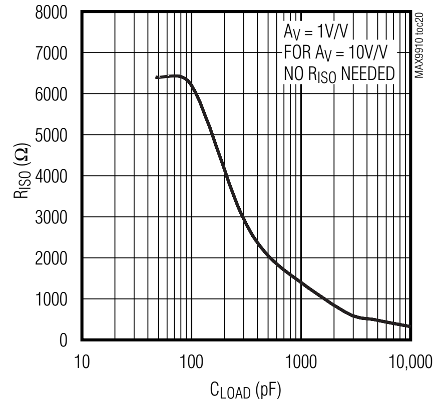
Typical Operating Characteristics (continued)

(V_{DD} = 3V, V_{SS} = V_{CM} = 0V, R_L to V_{DD} / 2, T_A = +25°C, unless otherwise noted.)

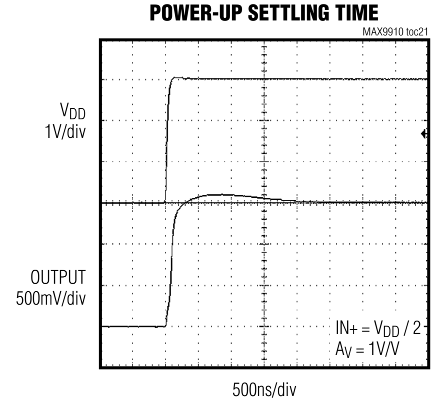
VOLTAGE-NOISE DENSITY vs. FREQUENCY



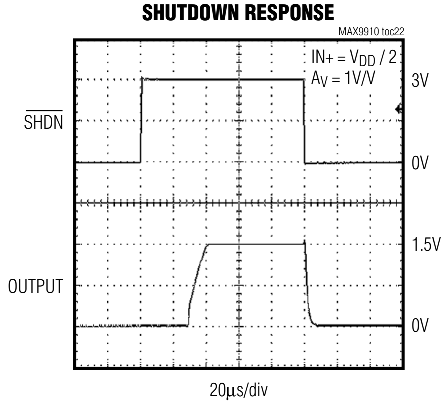
RESISTOR ISOLATION vs. CAPACITIVE LOAD



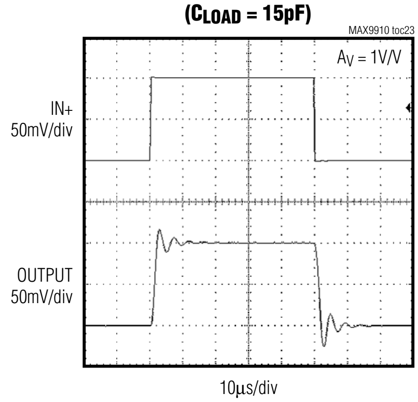
POWER-UP SETTLING TIME



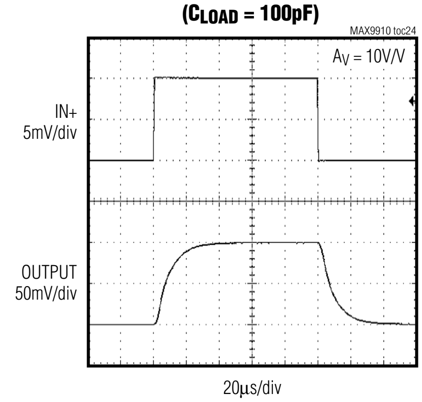
SHUTDOWN RESPONSE



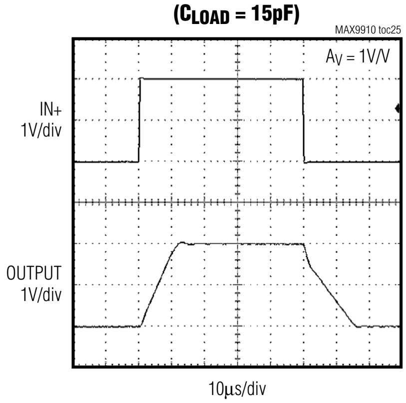
SMALL-SIGNAL PULSE RESPONSE (C_{LOAD} = 15pF)



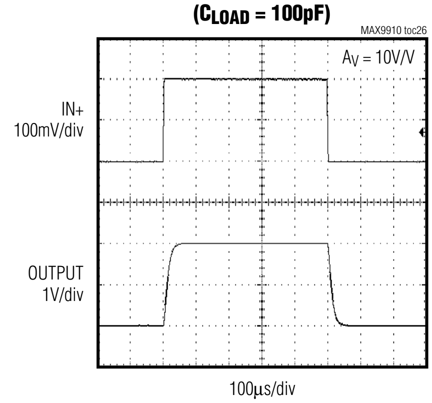
SMALL-SIGNAL PULSE RESPONSE (C_{LOAD} = 100pF)



LARGE-SIGNAL PULSE RESPONSE (C_{LOAD} = 15pF)



LARGE-SIGNAL PULSE RESPONSE (C_{LOAD} = 100pF)

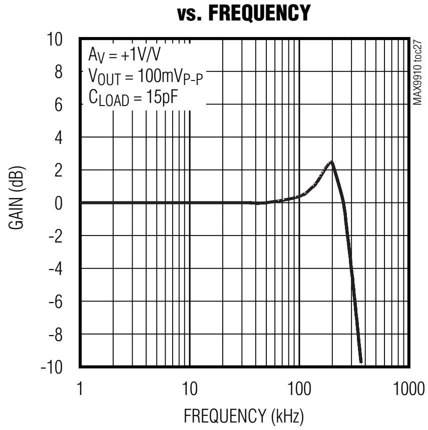


200kHz, 4µA, Rail-to-Rail I/O Op Amps with Shutdown

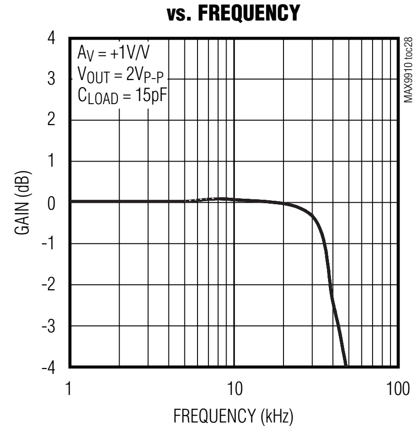
Typical Operating Characteristics (continued)

(V_{DD} = 3V, V_{SS} = V_{CM} = 0V, R_L to V_{DD} / 2, T_A = +25°C, unless otherwise noted.)

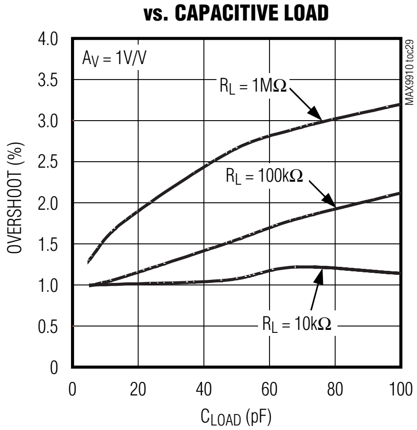
SMALL-SIGNAL GAIN vs. FREQUENCY



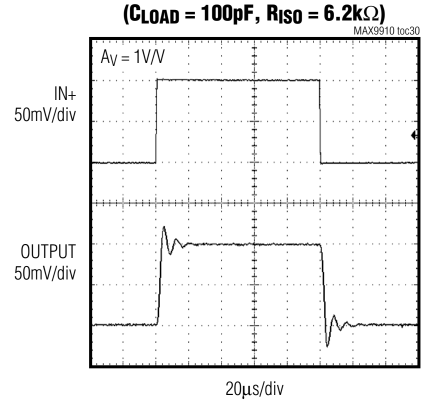
LARGE-SIGNAL GAIN vs. FREQUENCY



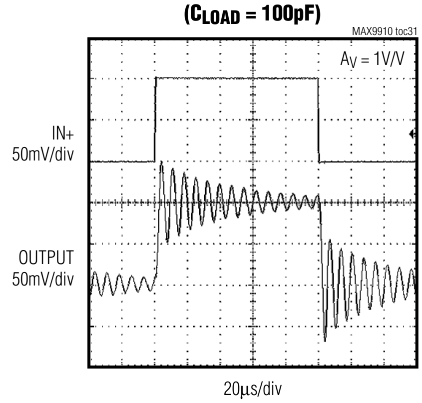
PERCENT OVERSHOOT vs. CAPACITIVE LOAD



OUTPUT WAVEFORM WITH R_{ISO} (C_{LOAD} = 100pF, R_{ISO} = 6.2kΩ)



OUTPUT WAVEFORM WITHOUT R_{ISO} (C_{LOAD} = 100pF)



Pin Description

PIN					NAME	FUNCTION
MAX9911 (WLP)	MAX9910	MAX9911 (SC70)	MAX9912	MAX9913		
A1	1	1	—	—	IN+	Noninverting Amplifier Input
A2	2	2	4	4	V_{SS}	Negative Supply Voltage
B1	3	3	—	—	IN-	Inverting Amplifier Input
C1	4	4	—	—	OUT	Amplifier Output
B2	5	6	8	10	V_{DD}	Positive Supply Voltage
C2	—	5	—	—	$\overline{SHDN}$	Shutdown
—	—	—	1	1	OUTA	Amplifier Output Channel A
—	—	—	2	2	INA-	Inverting Amplifier Input Channel A
—	—	—	3	3	INA+	Noninverting Amplifier Input Channel A
—	—	—	—	5	$\overline{SHDNA}$	Shutdown Channel A
—	—	—	—	6	$\overline{SHDNB}$	Shutdown Channel B
—	—	—	5	7	INB+	Noninverting Amplifier Input Channel B
—	—	—	6	8	INB-	Inverting Amplifier Input Channel B
—	—	—	7	9	OUTB	Amplifier Output Channel B

Detailed Description

Featuring a maximized ratio of GBW to supply current, low operating supply voltage, low input bias current, and rail-to-rail inputs and outputs, the MAX9910–MAX9913 are an excellent choice for precision or general-purpose, low-current, low-voltage, battery-powered applications. These CMOS devices consume an ultra-low 4µA (typ) supply current and a 200µV (typ) offset voltage. For additional power conservation, the MAX9911/MAX9913 feature a low-power shutdown mode that reduces supply current to 1nA (typ), and puts the amplifiers' output in a high-impedance state. These devices are unity-gain stable with a 200kHz GBW product, driving capacitive loads up to 30pF. The capacitive load can be increased to 250pF when the amplifier is configured for a 10V/V gain.

Rail-to-Rail Inputs and Outputs

All of the MAX9910–MAX9913 amplifiers have a parallel-connected n- and p-channel differential input stage that allows an input common-mode voltage range that extends 100mV beyond the positive and negative supply rails, with excellent common-mode rejection.

The MAX9910–MAX9913 are capable of driving the output to within 5mV of both supply rails with a 100kΩ load. These devices can drive a 5kΩ load with swings to within 60mV of the rails. Figure 1 shows the output voltage swing of the MAX9910–MAX9913 configured as a unity-gain buffer powered from a single 3V supply.

Low Input Bias Current

The MAX9910–MAX9913 feature ultra-low 1pA (typ) input bias current. The variation in the input bias current is minimal with changes in the input voltage due to very high input impedance (in the order of 1GΩ).

Applications Information

Driving Capacitive Loads

The MAX9910–MAX9913 amplifiers are unity-gain stable for loads up to 30pF. However, the capacitive load can be increased to 250pF when the amplifier is configured for a minimum gain of 10V/V. Applications that require greater capacitive-drive capability should use an isolation resistor between the output and the capacitive load (Figure 2). Also, in unity-gain applications with relatively small R_L (approximately 5kΩ), the capacitive load can be increased up to 200pF.

Power-Supply Considerations

The MAX9910–MAX9913 are optimized for single 1.8V to 5.5V supply operation. A high amplifier power-supply rejection ratio of 95dB (typ) allows the devices to be powered directly from a battery, simplifying design and extending battery life.

Power-Up Settling Time

The MAX9910–MAX9913 typically require 5µs after power-up. Supply settling time depends on the supply voltage, the value of the bypass capacitor, the output impedance of the incoming supply, and any lead resistance or inductance between components. Op-amp settling time depends primarily on the output voltage and is slew-rate limited. Figure 3 shows the MAX991_ in a noninverting voltage follower configuration with the input held at midsupply. The output settles in approximately 18µs for V_{DD} = 3V (see the *Typical Operating Characteristics* for power-up settling time).

Shutdown Mode

The MAX9911/MAX9913 feature active-low shutdown inputs. The MAX9911/MAX9913 enter shutdown in 2µs (typ) and exit in 30µs (typ). The amplifiers' outputs are in a high-impedance state in shutdown mode. Drive $\overline{SHDN}$ low to enter shutdown. Drive $\overline{SHDN}$ high to enable the amplifier. The MAX9913 dual-amplifier features separate shutdown inputs. Shut down both amplifiers for the lowest quiescent current.

Power-Supply Bypassing and Layout

To minimize noise, bypass V_{DD} with a 0.1µF capacitor to ground, as close to the pin as possible.

Good layout techniques optimize performance by decreasing the amount of stray capacitance and inductance to the op amps' inputs and outputs. Minimize stray capacitance and inductance by placing external components close to the IC.

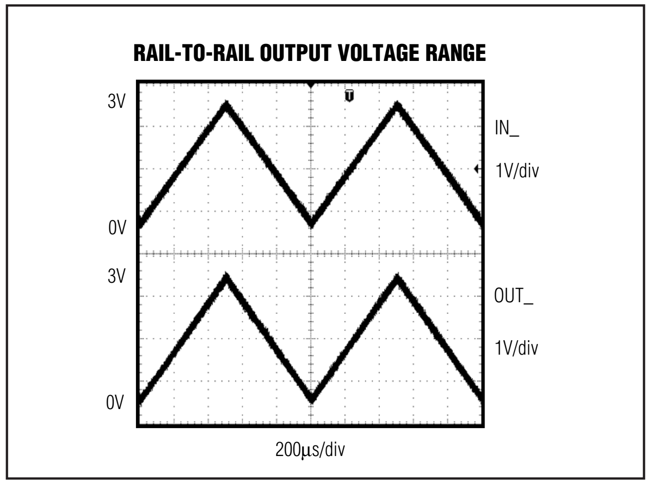


Figure 1. Rail-to-Rail Output Voltage Range

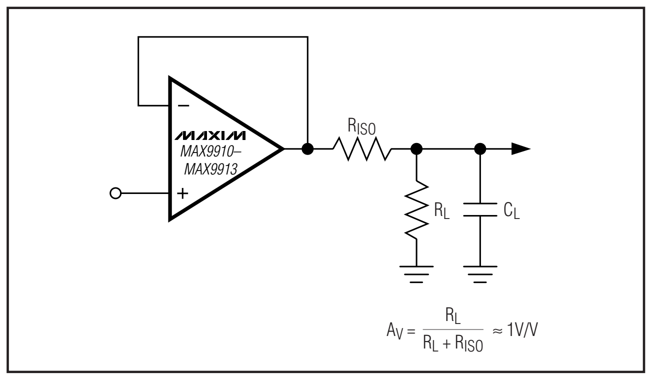


Figure 2. Using a Resistor to Isolate a Capacitive Load from the Op Amp

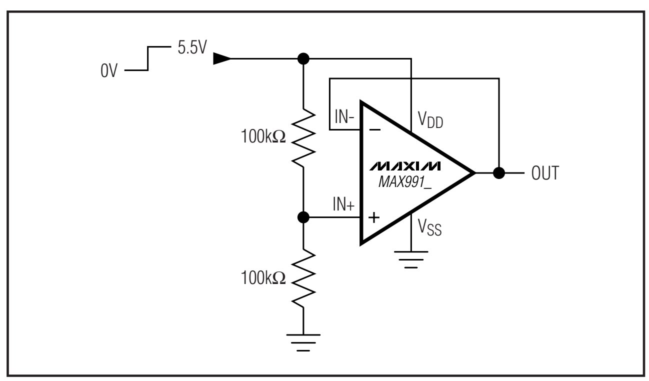
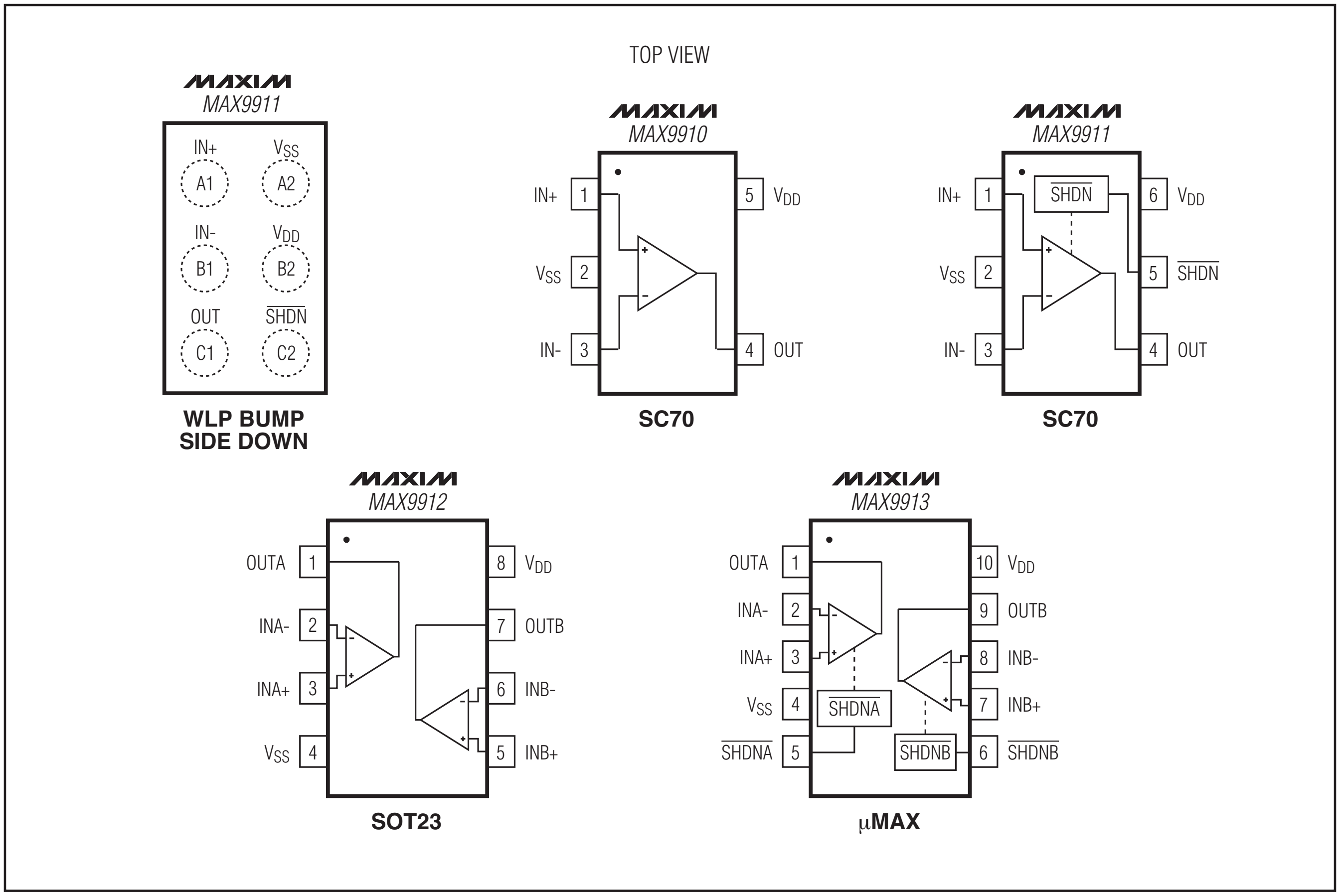


Figure 3. Power-Up Test Configuration

Pin Configurations



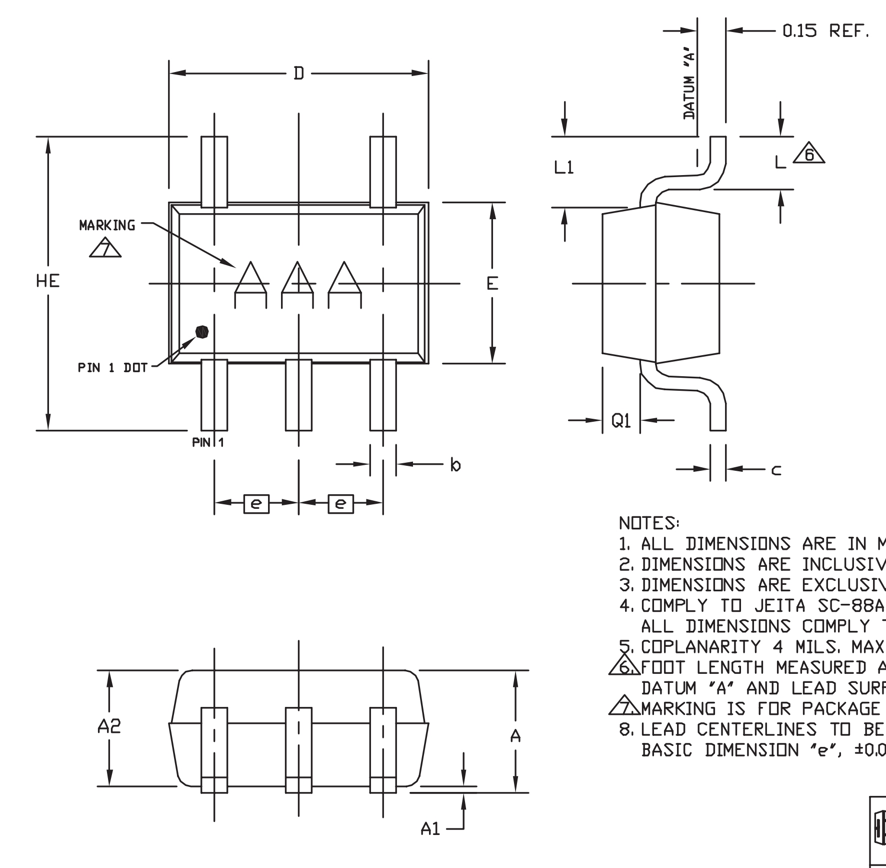
Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
5 SC70	X5+1	21-0076	90-0188
6 SC70	X6SN+1	21-0077	90-0189
6 WLP	W61B1+1	21-0217	—
8 SOT23	K8+5	21-0078	90-0176
10 µMAX	U10+2	21-0061	90-0330



COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.80	2.00	2.20
e	0.65 BSC.		
E	1.15	1.25	1.35
HE	1.80	2.20	2.40
L	0.26	0.34	0.46
L1	0.425 TYP.		
Q1	0.10	0.25	0.40
PKG. CODE	X5-1		

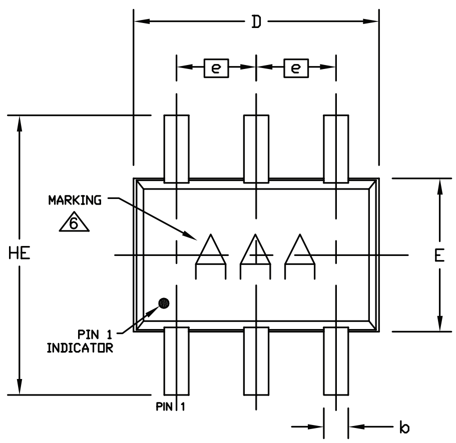
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COMPLY TO JEITA SC-88A EXCEPT FOR DIMENSION "L". ALL DIMENSIONS COMPLY TO JEDEC MO-203.
5. COPLANARITY 4 MILS. MAX.
6. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
8. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

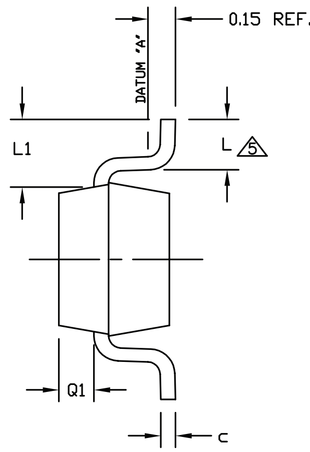
DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 5L SC70			
APPROVAL	DOCUMENT CONTROL NO. 21-0076	REV. E	1/1

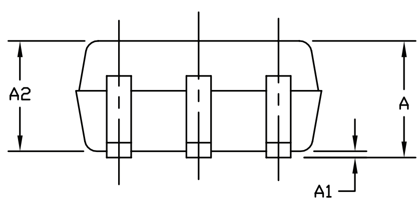
Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.





COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.85	2.00	2.15
e	0.65 BSC.		
E	1.15	1.25	1.35
HE	2.00	2.20	2.35
L	0.26	0.34	0.46
L1	0.425 TYP.		
Q1	0.10	0.25	0.40
PKG. CODES	X6SN-1		



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COPLANARITY 4 MILS. MAX.
5. (Δ) FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM 'A' AND LEAD SURFACE.
6. (Δ) MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
8. ALL DIMENSIONS COMPLY TO JEDEC MO-203.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

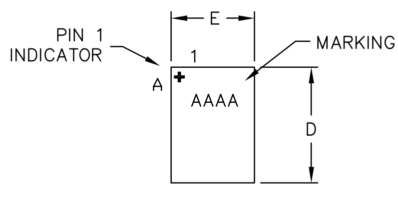
MAXIM

TITLE: PACKAGE OUTLINE, 6L SC70

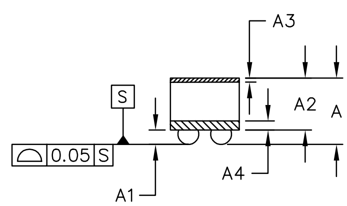
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0077	H	1/1

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



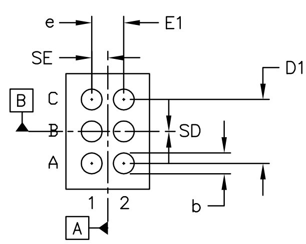
TOP VIEW



SIDE VIEW

COMMON DIMENSIONS	
A	0.64±0.05
A1	0.19±0.03
A2	0.45 REF
A3	0.025 BASIC
A4	0.07 BASIC
b	ø0.27±0.03
D1	0.80 BASIC
E1	0.40 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.20 BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W61B1+1	0.76	0.97	1.17	1.37	NONE
W61D1+1	0.95	1.02	1.36	1.42	NONE



BOTTOM VIEW

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.

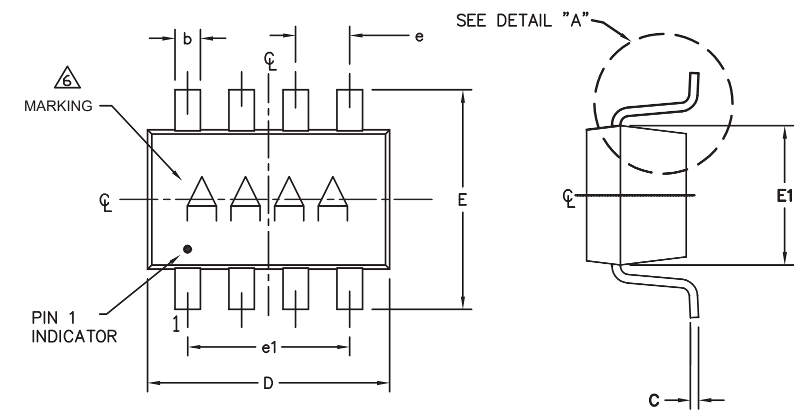
-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE
6 BUMPS, WLP PKG. 0.4mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0217	B	1/1

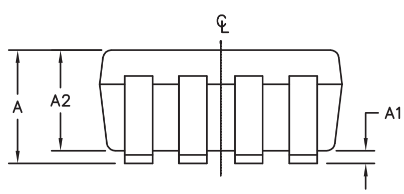
Package Information (continued)

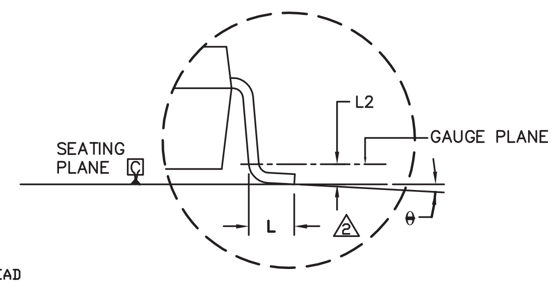
For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.06	0.15
A2	0.90	1.10	1.30
b	0.22	0.30	0.38
C	0.08	0.15	0.22
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.30	0.45	0.60
L2	0.25 BSC.		
e	0.65 BSC.		
e1	1.95 REF.		
θ	0°	3°	8°

PKG CODES:
K8-1, K8-2, K8F-4, K8FH-4, K8-5, K8SN-1; K8CN-2





DETAIL "A"

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178 VARIATION BA.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

MAXIM

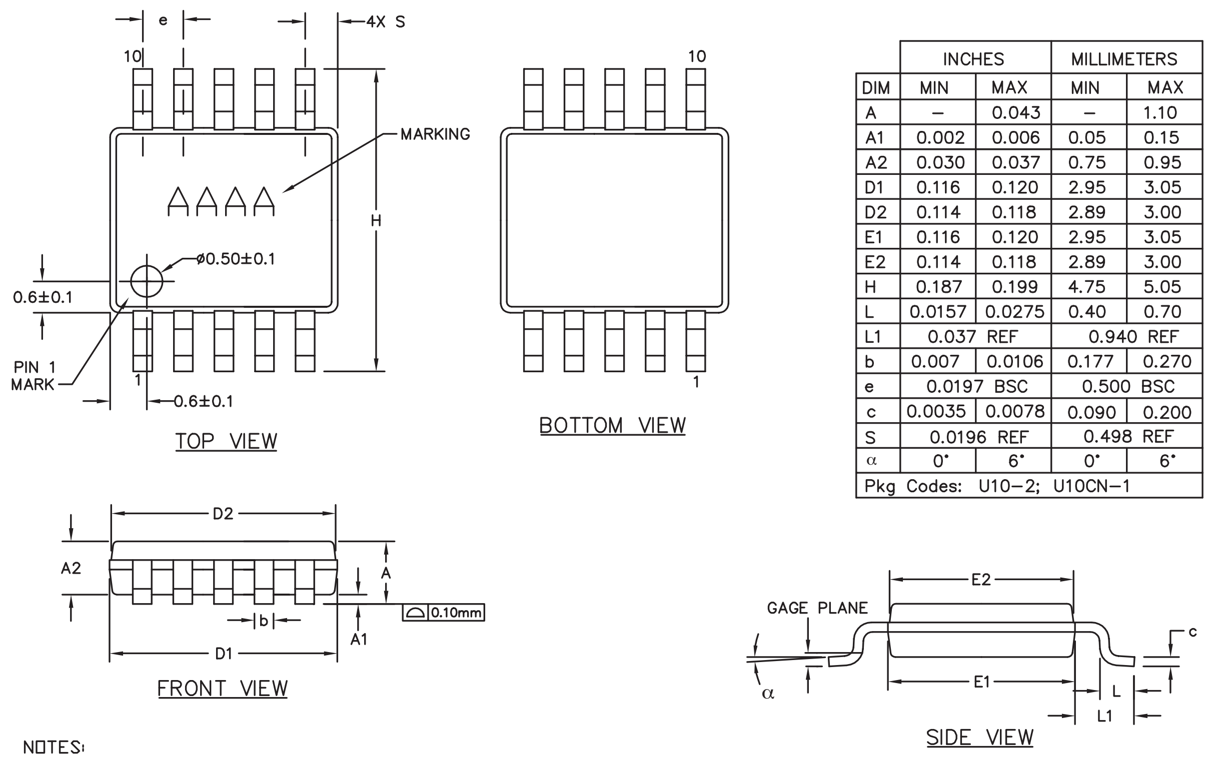
TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0078	J	1/1

200kHz, 4µA, Rail-to-Rail I/O Op Amps with Shutdown

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



10LUMAX.EPS

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°
Pkg Codes: U10–2; U10CN–1				

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COMPLIES TO JEDEC MO-187, LATEST REVISION, VARIATION BA.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

MAXIM

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21–0061	L	1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	10/10	Added WLP package	1, 2, 9, 11