Programmable DC-Balanced 21-Bit Serializers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.5V to +4.0V
LVDS Outputs (TxOUT_, TxCLK OUT_) to GND ...-0.5V to +4.0V
5V Tolerant LVTTL/LVCMOS Inputs
(TxIN_, TxCLK IN, $\overline{PWRDWN}$) to GND .....-0.5V to +6.0V
(DCB/NC) to GND .....-0.5V to (V_{CC} + 0.5V)
LVDS Outputs (TxOUT_, TxCLK OUT_)
Short to GND and Differential Short .....Continuous
Continuous Power Dissipation (multilayer board, T_A = +70°C)
48-Pin TSSOP (derate 16mW/°C above +70°C) 1282mW
48-Pin TQFN (derate 40mW/°C above +70°C) 3200mW
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C

ESD Protection
Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
All Pins to GND .....±2kV
IEC 61000-4-2 (R_D = 330Ω, C_S = 150pF)
Contact Discharge (TxOUT_, TxCLK OUT_) to GND ....±8kV
Air Gap Discharge (TxOUT_, TxCLK OUT_) to GND ..±15kV
ISO 10605 (R_D = 2kΩ, C_S = 330pF)
Contact Discharge (TxOUT_, TxCLK OUT_) to GND ....±8kV
Air Gap Discharge (TxOUT_, TxCLK OUT_) to GND ..±25kV
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, $\overline{PWRDWN}$ = high, DCB/NC = high or low, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (TxIN_, TxCLK IN, $\overline{PWRDWN}$, DCB/NC)							
High-Level Input Voltage	V_{IH}	TxIN_, TxCLK IN, $\overline{PWRDWN}$		2.0		5.5	V
		DCB/NC		2.0		V_{CC} + 0.3	
Low-Level Input Voltage	V_{IL}			-0.3		+0.8	V
Input Current	I_{IN}	V_{IN} = high or low, $\overline{PWRDWN}$ = high or low		-20		+20	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA			-0.9	-1.5	V
LVDS OUTPUTS (TxOUT_, TxCLK OUT)							
Differential Output Voltage	V_{OD}	Figure 1		250	350	450	mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 1			2	25	mV
Output Offset Voltage	V_{OS}	Figure 1		1.125	1.25	1.375	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 1			10	30	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V or V_{CC}, non-DC-balanced mode		-10	±5.7	+10	mA
		V_{OUT+} or V_{OUT-} = 0V or V_{CC}, DC-balanced mode		-15	±8.2	+15	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V, non-DC-balanced mode (Note 3)			5.7	10	mA
		V_{OD} = 0V, DC-balanced mode (Note 3)			8.2	15	
Differential Output Resistance	R_O	DC-balanced mode		78	110	147	Ω
			-40°C to +105°C	78	110	150	
		Non-DC-balanced mode		292	410	547	
			-40°C to +105°C	292	410	564	

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DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, $\overline{PWRDWN}$ = high, DCB/NC = high or low, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output High-Impedance Current	I_{OZ}	$\overline{PWRDWN}$ = low or V_{CC} = 0V, V_{OUT+} = 0V or 3.6V, V_{OUT-} = 0V or 3.6V		-0.5	±0.1	+0.5	µA
Worst-Case Supply Current	I_{CCW}	DC-balanced mode, worst-case pattern, C_L = 5pF, Figure 2	8MHz MAX9209		40	54	mA
			16MHz MAX9209		48	68	
			34MHz MAX9209		71	90	
			16MHz MAX9213		46	64	
			34MHz MAX9213		59	87	
			66MHz MAX9213		94	108	
		Non-DC-balanced mode, worst-case pattern, C_L = 5pF, Figure 2	10MHz MAX9209		30	39	
			20MHz MAX9209		37	53	
			33MHz MAX9209		49	70	
			40MHz MAX9209		56	75	
			20MHz MAX9213		36	49	
			33MHz MAX9213		45	62	
			40MHz MAX9213		49	70	
			66MHz MAX9213		68	89	
			85MHz MAX9213		83	100	
Power-Down Supply Current	I_{CCZ}	$\overline{PWRDWN}$ = low			17	50	µA

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Programmable DC-Balanced 21-Bit Serializers

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, C_L = 5pF, $\overline{PWRDWN}$ = high, DCB/NC = high or low, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS Low-to-High Transition Time	LLHT	Figure 3	MAX9209	150	280	400	ps
			MAX9213	150	260	350	
LVDS High-to-Low Transition Time	LHLT	Figure 3	MAX9209	150	280	400	ps
			MAX9213	150	260	350	
TxCLK IN Transition Time	TCIT	Figure 4				4	ns
Output Pulse Position	TPPosN	N = 0, 1, 2, 3, 4, 5, 6 non-DC-balanced mode, Figure 5 (Note 6)	10MHz MAX9209	N/7 x TCIP - 0.25	N/7 x TCIP	N/7 x TCIP + 0.25	ns
			20MHz MAX9209	N/7 x TCIP - 0.15	N/7 x TCIP	N/7 x TCIP + 0.15	
			40MHz MAX9209	N/7 x TCIP - 0.1	N/7 x TCIP	N/7 x TCIP + 0.1	
			20MHz MAX9213	N/7 x TCIP - 0.25	N/7 x TCIP	N/7 x TCIP + 0.25	
			40MHz MAX9213	N/7 x TCIP - 0.15	N/7 x TCIP	N/7 x TCIP + 0.15	
			85MHz MAX9213	N/7 x TCIP - 0.1	N/7 x TCIP	N/7 x TCIP + 0.1	
		N = 0, 1, 2, 3, 4, 5, 6, 7, 8 DC-balanced mode, Figure 6 (Note 6)	8MHz MAX9209	N/9 x TCIP - 0.25	N/9 x TCIP	N/9 x TCIP + 0.25	
			16MHz MAX9209	N/9 x TCIP - 0.15	N/9 x TCIP	N/9 x TCIP + 0.15	
			34MHz MAX9209	N/9 x TCIP - 0.1	N/9 x TCIP	N/9 x TCIP + 0.1	
			16MHz MAX9213	N/9 x TCIP - 0.25	N/9 x TCIP	N/9 x TCIP + 0.25	
			34MHz MAX9213	N/9 x TCIP - 0.15	N/9 x TCIP	N/9 x TCIP + 0.15	
			66MHz MAX9213	N/9 x TCIP - 0.1	N/9 x TCIP	N/9 x TCIP + 0.1	

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AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, C_L = 5pF, $\overline{PWRDWN}$ = high, DCB/NC = high or low, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TxCLK IN High Time	TCIH	Figure 7	0.3 x TCIP		0.7 x TCIP	ns
TxCLK IN Low Time	TCIL	Figure 7	0.3 x TCIP		0.7 x TCIP	ns
TxIN to TxCLK IN Setup	TSTC	Figure 7	2.2			ns
TxIN to TxCLK IN Hold	THTC	Figure 7	0			ns
TxCLK IN to TxCLK OUT Delay	TCCD	Non-DC-balanced mode, Figure 8	3.5	4.5	6.0	ns
		DC-balanced mode, Figure 8	4.7	5.9	7.2	
Serializer Phase-Locked Loop Set	TPLLS	Figure 9			32800 x TCIP	ns
Serializer Power-Down Delay	TPDD	Figure 10		14	50	ns
TxCLK IN Cycle-to-Cycle Jitter (Input Clock Requirement)	TJIT				2	ns
Magnitude of Differential Output Voltage	V_{OD}	595Mbps data rate, worst-case pattern	250			mV

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{OD}, ΔV_{OD}, and ΔV_{OS}.

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +25°C.

Note 3: Guaranteed by design.

Note 4: TCIP is the period of TxCLK IN.

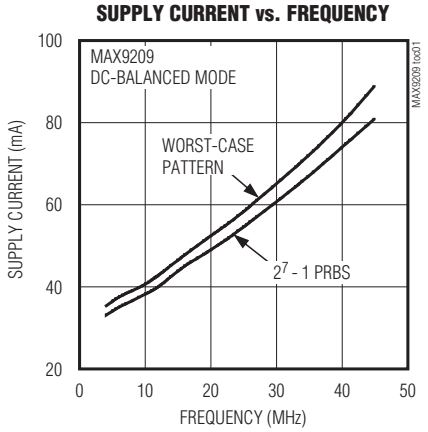
Note 5: AC parameters are guaranteed by design and characterization, and are not production tested. Limits are set at ±6 sigma.

Note 6: Pulse position TPPosN is characterized using 2^7 - 1 PRBS data.

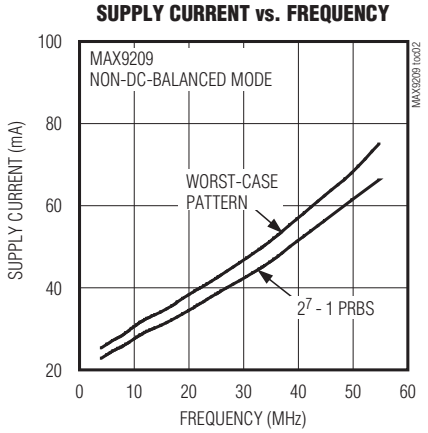
Typical Operating Characteristics

(V_{CC} = +3.3V, R_L = 100Ω ±1%, C_L = 5pF, $\overline{PWRDWN}$ = high, T_A = +25°C, unless otherwise noted.)

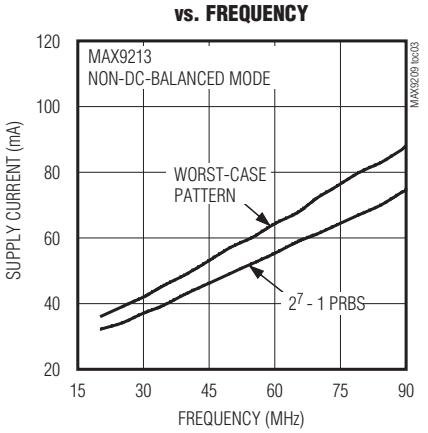
WORST-CASE PATTERN AND PRBS SUPPLY CURRENT vs. FREQUENCY



WORST-CASE PATTERN AND PRBS SUPPLY CURRENT vs. FREQUENCY



WORST-CASE AND PRBS SUPPLY CURRENT vs. FREQUENCY



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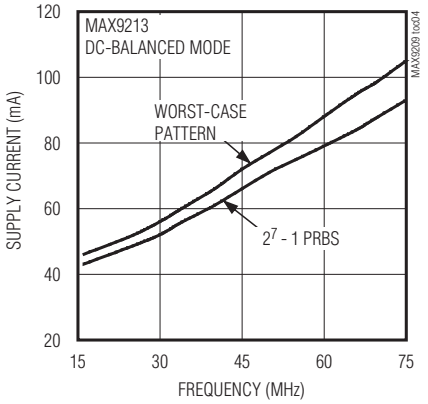
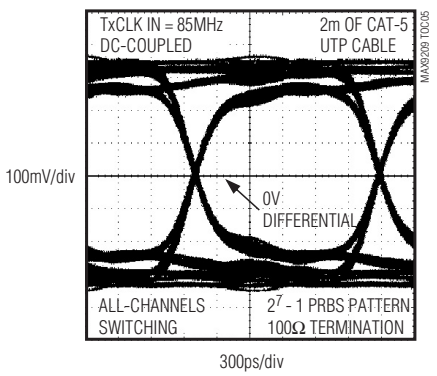
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, R_L = 100Ω ±1%, C_L = 5pF, $\overline{PWRDWN}$ = high, T_A = +25°C, unless otherwise noted.)

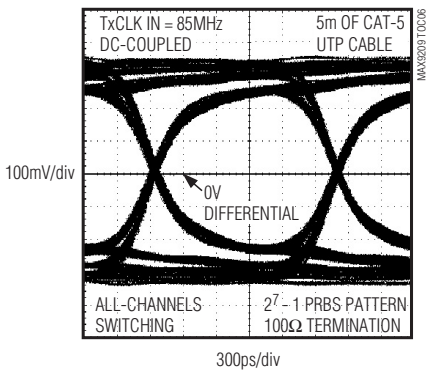
WORST-CASE PATTERN AND PRBS SUPPLY CURRENT vs. FREQUENCY



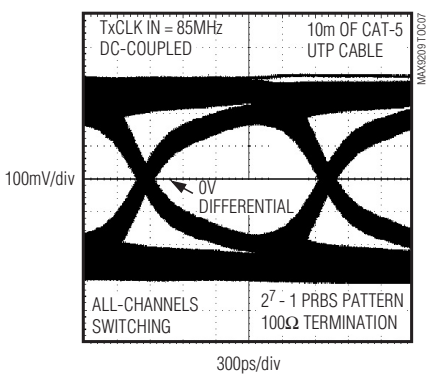
MAX9213 EYE DIAGRAM—NON-DC-BALANCED MODE



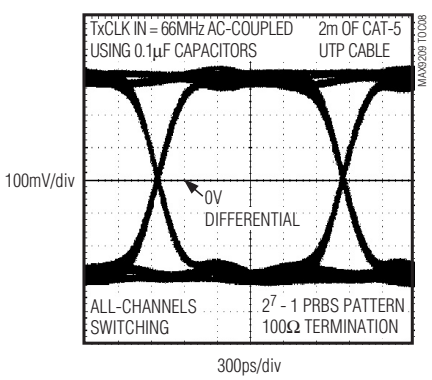
MAX9213 EYE DIAGRAM—NON-DC-BALANCED MODE



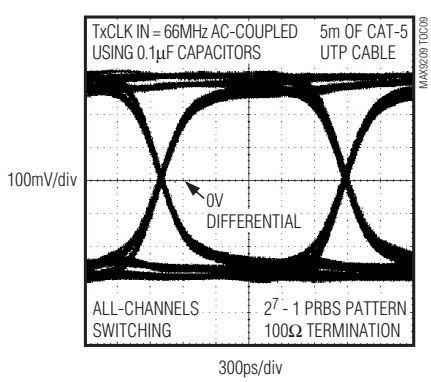
MAX9213 EYE DIAGRAM—NON-DC-BALANCED MODE



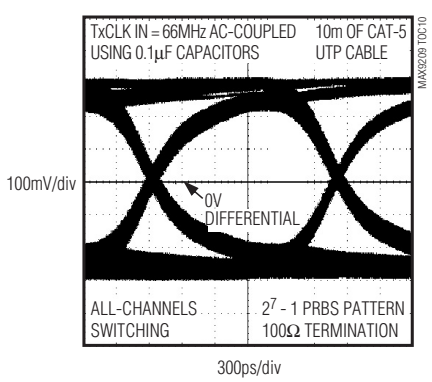
MAX9213 EYE DIAGRAM—DC-BALANCED MODE



MAX9213 EYE DIAGRAM—DC-BALANCED MODE



MAX9213 EYE DIAGRAM—DC-BALANCED MODE



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Pin Description

PIN		NAME	FUNCTION
TSSOP	TQFN		
1, 3, 4, 44, 45, 47, 48,	38, 39, 41, 42, 43, 45, 46	TxIN0–TxIN6	5V Tolerant LVTTL/LVCMOS Channel 0 Data Inputs. Internally pulled down to GND.
2, 8, 14, 21	2, 8, 15, 44	V_{CC}	Digital Supply Voltage
5, 11, 17, 24, 46	5, 11, 18, 40, 47	GND	Ground
6, 7, 9, 10, 12, 13, 15	1, 3, 4, 6, 7, 9, 48	TxIN7–TxIN13	5V Tolerant LVTTL/LVCMOS Channel 1 Data Inputs. Internally pulled down to GND.
16, 18, 19, 20, 22, 23, 25	10, 12, 13, 14, 16, 17, 19	TxIN14–TxIN20	5V Tolerant LVTTL/LVCMOS Channel 2 Data Inputs. Internally pulled down to GND.
26	20	TxCLK IN	5V Tolerant LVTTL/LVCMOS Parallel Rate Clock Input. Internally pulled down to GND.
27	21	$\overline{PWRDWN}$	5V Tolerant LVTTL/LVCMOS Power-Down Input. Internally pulled down to GND. Outputs are high impedance when $\overline{PWRDWN}$ = low or open.
28, 30	22, 24	PLL GND	PLL Ground
29	23	PLL V_{CC}	PLL Supply Voltage
31, 36, 42	25, 30, 36	LVDS GND	LVDS Ground
32	26	TxCLK OUT+	Noninverting LVDS Parallel Rate Clock Output
33	27	TxCLK OUT-	Inverting LVDS Parallel Rate Clock Output
34	28	TxOUT2+	Noninverting Channel 2 LVDS Serial Data Output
35	29	TxOUT2-	Inverting Channel 2 LVDS Serial Data Output
37	31	LVDS V_{CC}	LVDS Supply Voltage
38	32	TxOUT1+	Noninverting Channel 1 LVDS Serial Data Output
39	33	TxOUT1-	Inverting Channel 1 LVDS Serial Data Output
40	34	TxOUT0+	Noninverting Channel 0 LVDS Serial Data Output
41	35	TxOUT0-	Inverting Channel 0 LVDS Serial Data Output
43	37	DCB/NC	LVTTL/LVCMOS DC-Balance Programming Input: MAX9209: pulled up to V_{CC} MAX9213: pulled up to V_{CC} See Table 1.
—	—	EP	Exposed Paddle (TQFN Only). Solder to ground.

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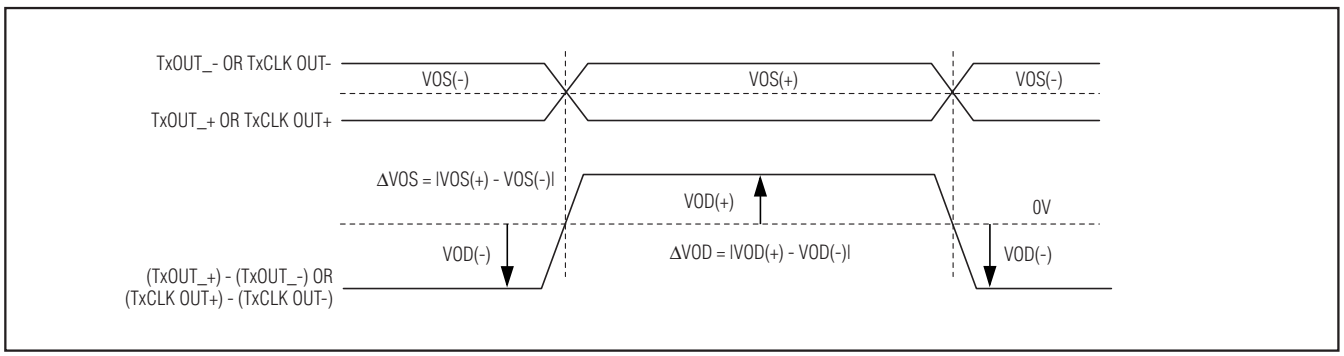

Figure 1. LVDS Output DC Parameters

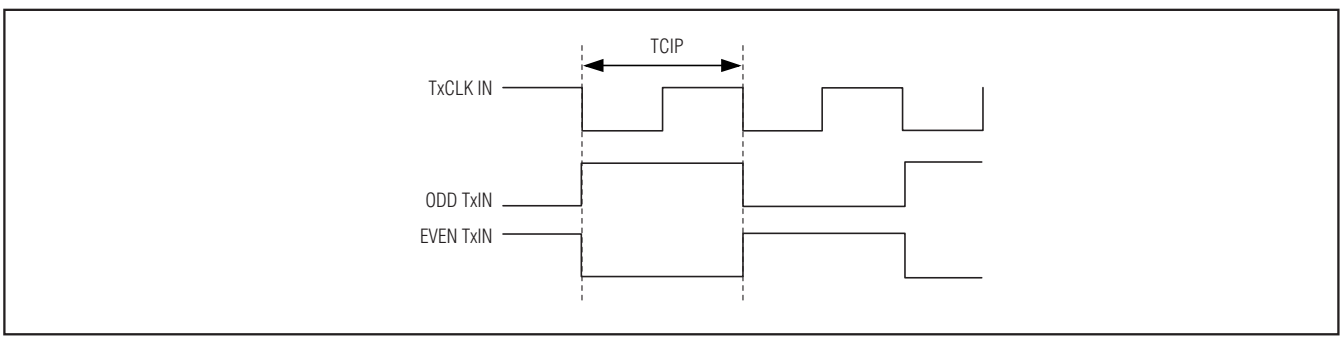

Figure 2. Worst-Case Test Pattern

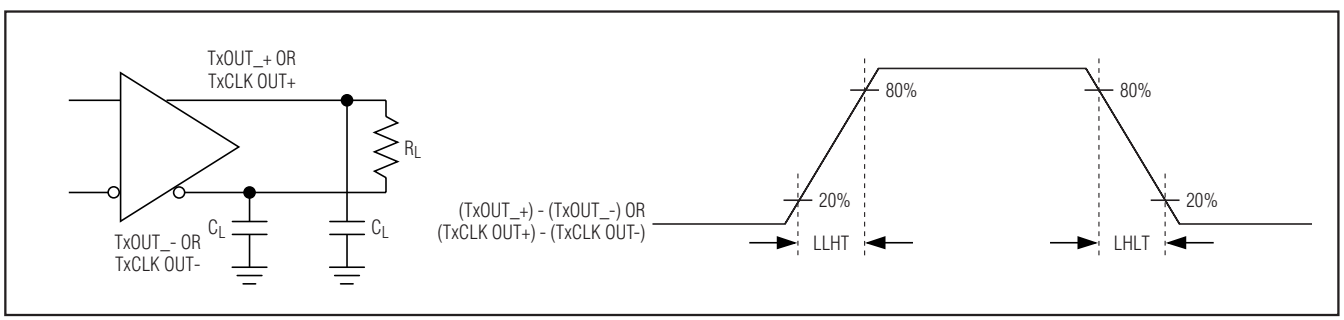

Figure 3. LVDS Output Load and Transition Times

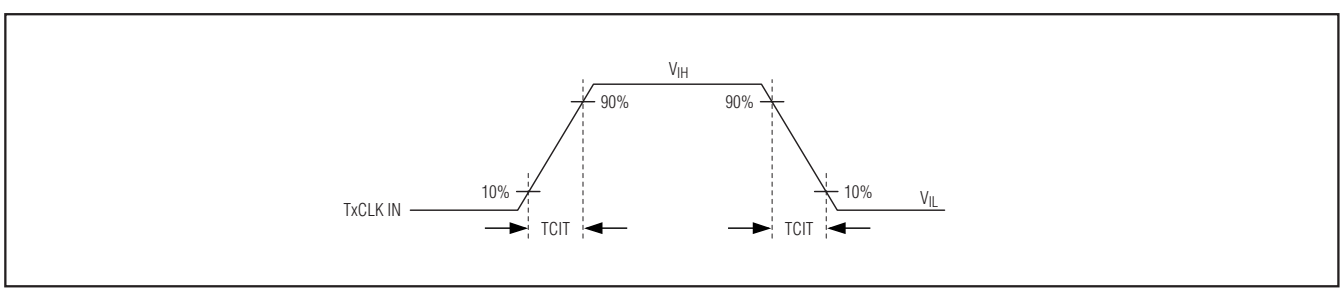

Figure 4. Clock Transition Time Waveform

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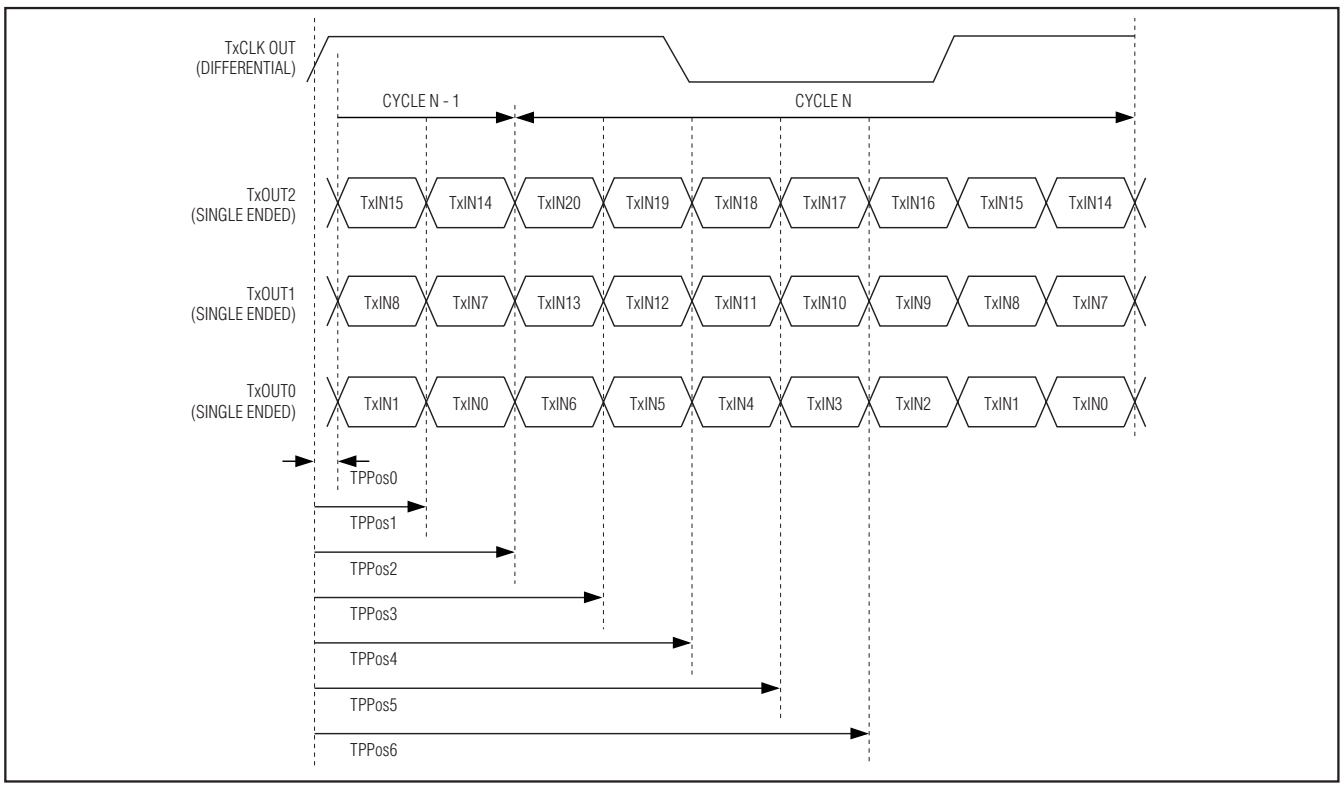

Figure 5. Non-DC-Balanced Mode LVDS Output Pulse Position Measurement

Detailed Description

The MAX9209 operates at a parallel clock frequency of 8MHz to 34MHz in DC-balanced mode and 10MHz to 40MHz in non-DC-balanced mode. The MAX9213 operates at a parallel clock frequency of 16MHz to 66MHz in DC-balanced mode and 20MHz to 85MHz in non-DC-balanced mode.

DC-balanced or non-DC-balanced operation is controlled by the DCB/NC pin (see Table 1). In non-DC-balanced mode, each channel serializes 7 bits every cycle of the parallel clock. In DC-balanced mode, 9 bits are serialized every clock cycle (7 data bits + 2 DC-balance bits). The highest data rate in DC-balanced mode for the MAX9213 is 66MHz x 9 = 594Mbps. In non-DC-balanced mode, the maximum data rate is 85MHz x 7 = 595Mbps. A bit time is 1 divided by the data rate, for example, 1 / 595Mbps = 1.68ns.

DC Balance

Through data coding, the DC-balance circuits limit the imbalance of ones and zeros transmitted on each channel. If +1 is assigned to each binary one transmitted and -1 is assigned to each binary zero transmitted, the variation in the running sum of assigned values is called the digital sum variation (DSV). The maximum DSV for the MAX9209/MAX9213 data channels is 10. At most, 10 more zeros than ones, or 10 more ones than zeros, are transmitted. The maximum DSV for the clock channel is 5. Limiting the DSV and choosing the correct coupling capacitors maintain differential signal amplitude and reduce jitter due to droop on AC-coupled links.

Table 1. DC-Balance Programming

DEVICE	DCB/NC	OPERATING MODE	OPERATING FREQUENCY (MHz)
MAX9209	High or open	DC balanced	8 to 34
	Low	Non-DC balanced	10 to 40
MAX9213	High or open	DC balanced	16 to 66
	Low	Non-DC balanced	20 to 85

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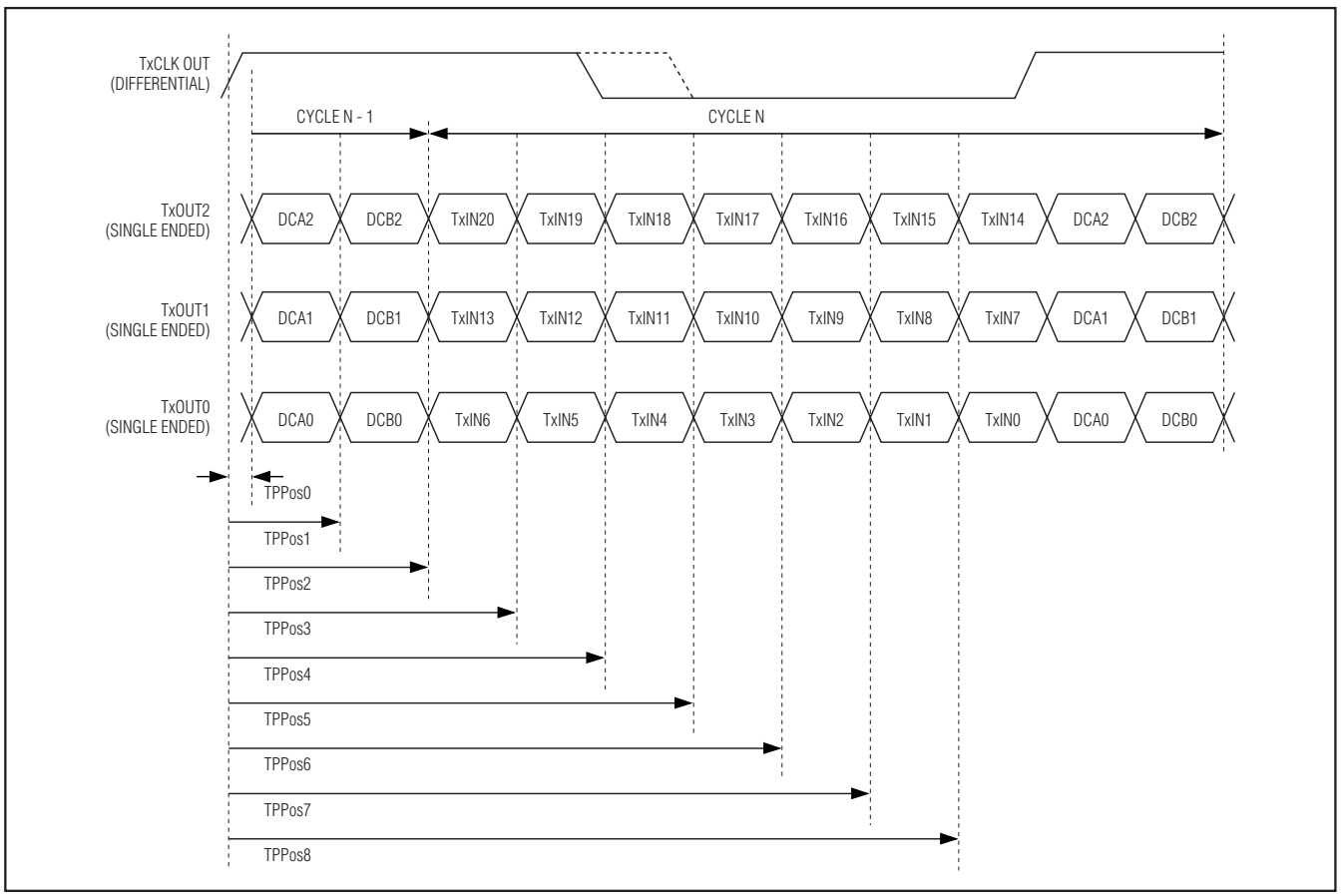

Figure 6. DC-Balanced Mode LVDS Output Pulse Position Measurement

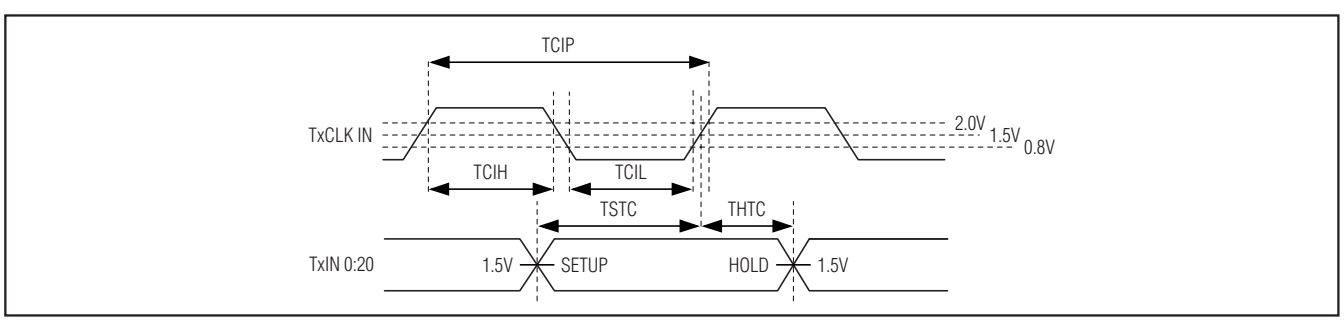

Figure 7. Setup and Hold, High and Low Times

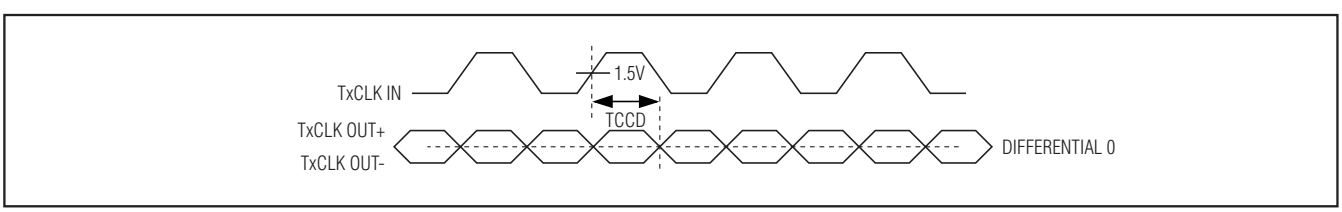

Figure 8. Clock-In to Clock-Out Delay

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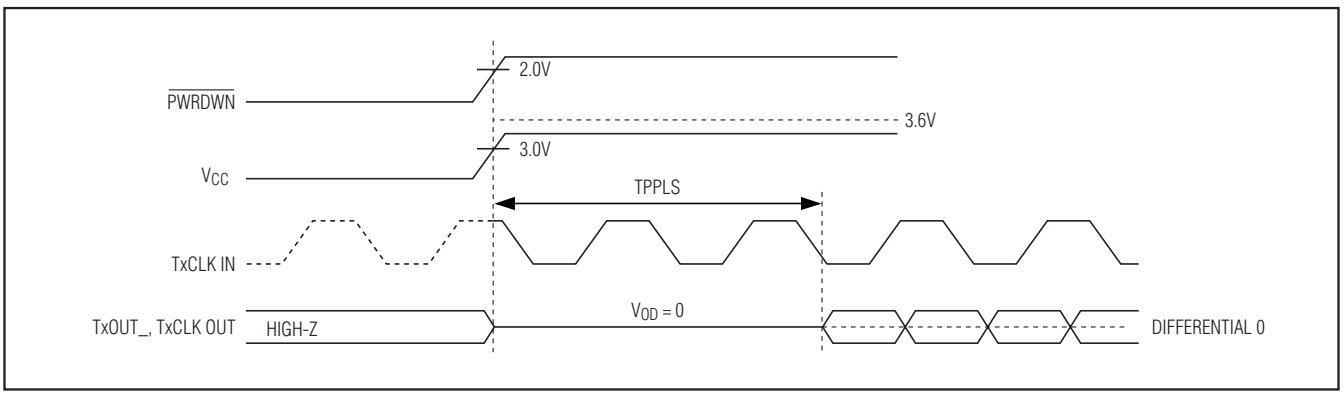

Figure 9. PLL Set Time

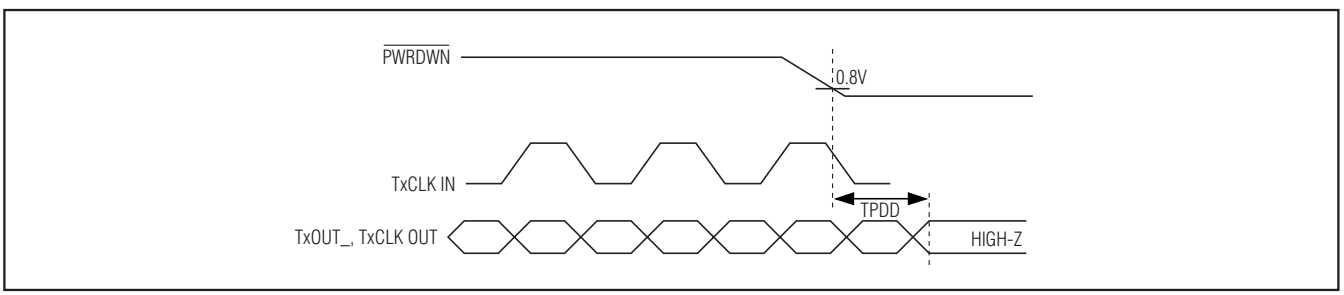

Figure 10. Power-Down Delay

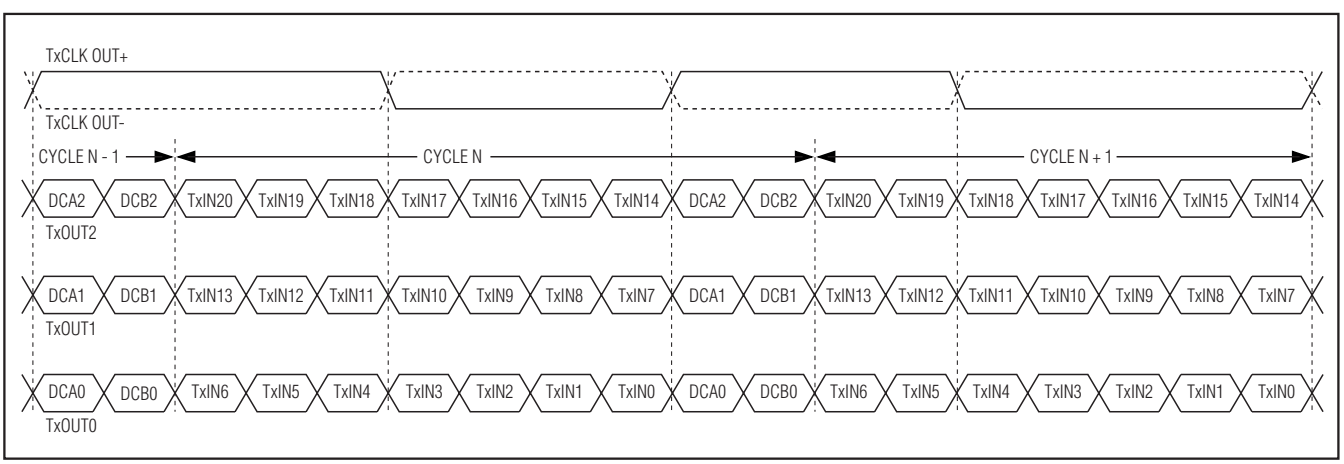

Figure 11. DC-Balanced Mode Inputs Mapped to LVDS Outputs

To obtain DC balance on the data channels, the parallel input data is inverted or not inverted, depending on the sign of the digital sum at the word boundary. Two complementary bits are appended to each group of 7 parallel input data bits to indicate to the MAX9210/MAX9214 deserializers whether the data bits are inverted (Figure 11). The deserializer restores the original state of the parallel data. The LVDS clock signal alternates duty cycles of 4/9 and 5/9, which maintains DC balance. Figure 12 shows the non-DC-balanced mode inputs mapped to LVDS outputs.

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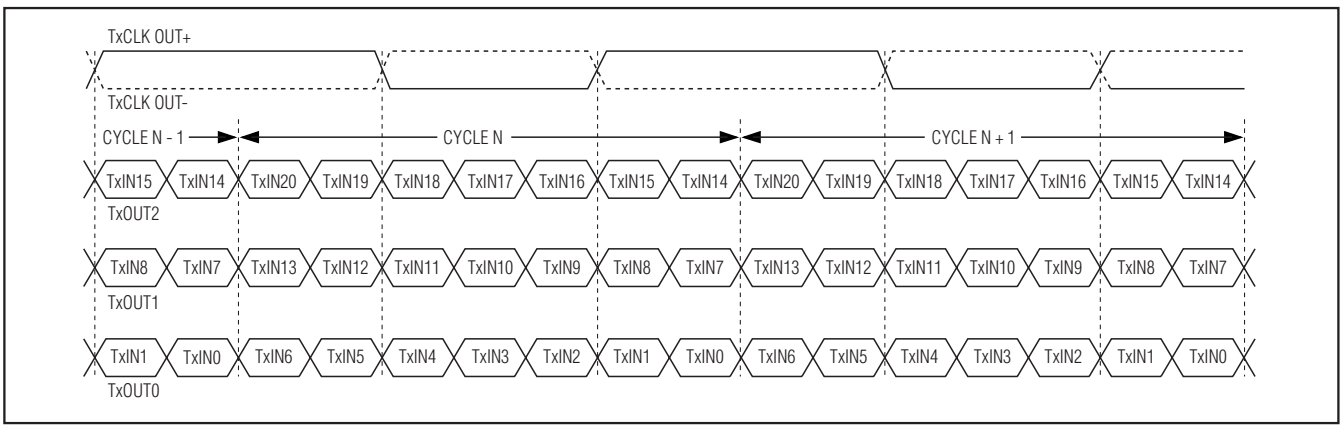

Figure 12. Non-DC-Balanced Mode Inputs Mapped to LVDS Outputs

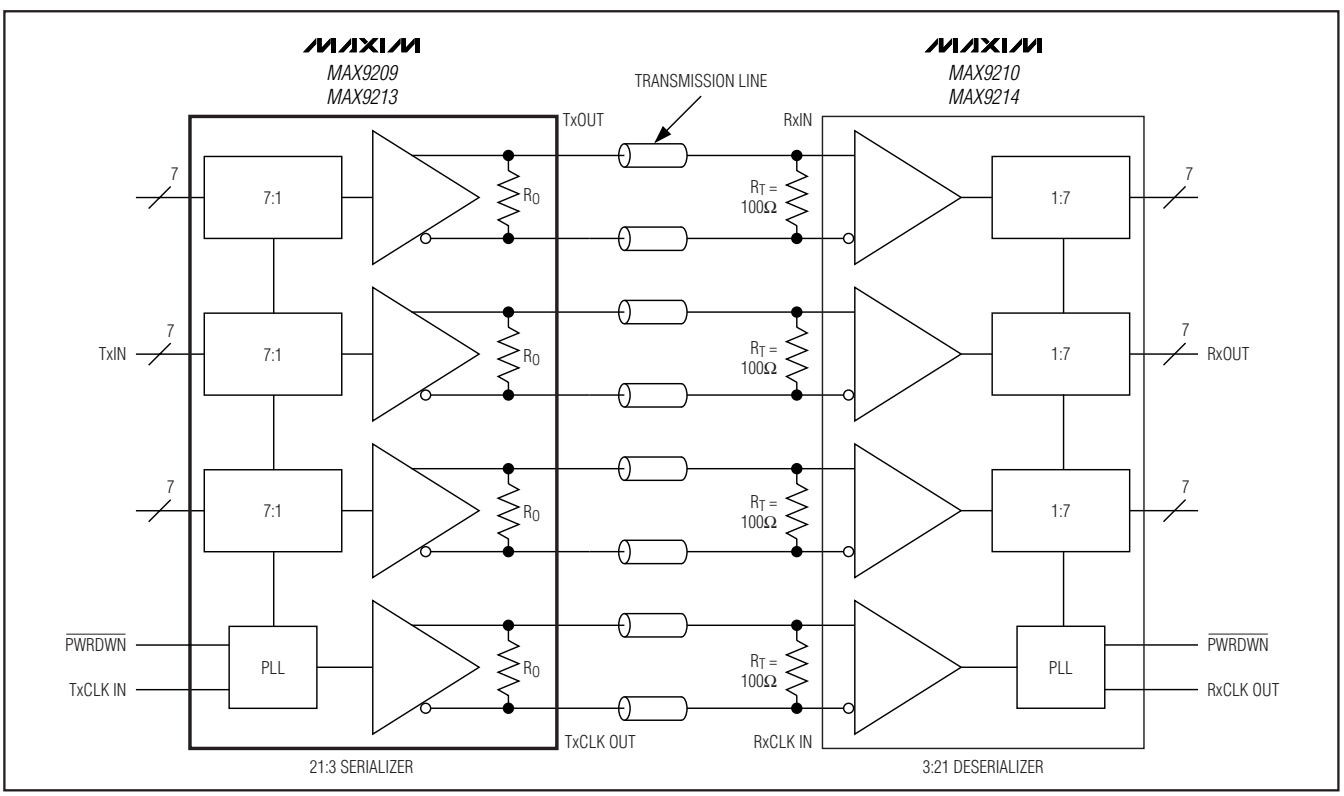

Figure 13. DC-Coupled Link, Non-DC-Balanced Mode

AC-Coupling Benefits

Bit errors experienced with DC-coupling can be eliminated by increasing the receiver common-mode voltage range by AC-coupling. AC-coupling increases the common-mode voltage range of an LVDS receiver to nearly the voltage rating of the capacitor. The typical LVDS driver output is 350mV centered on an offset voltage of 1.25V, making single-ended output voltages of 1.425V and 1.075V. An LVDS receiver accepts signals from 0V to 2.4V, allowing approximately ±1V common-mode difference between the driver and receiver on a DC-coupled link (2.4V - 1.425V = 0.975V and 1.075V - 0V = 1.075V). Figure 13 shows the DC-coupled link, non-DC-balanced mode.

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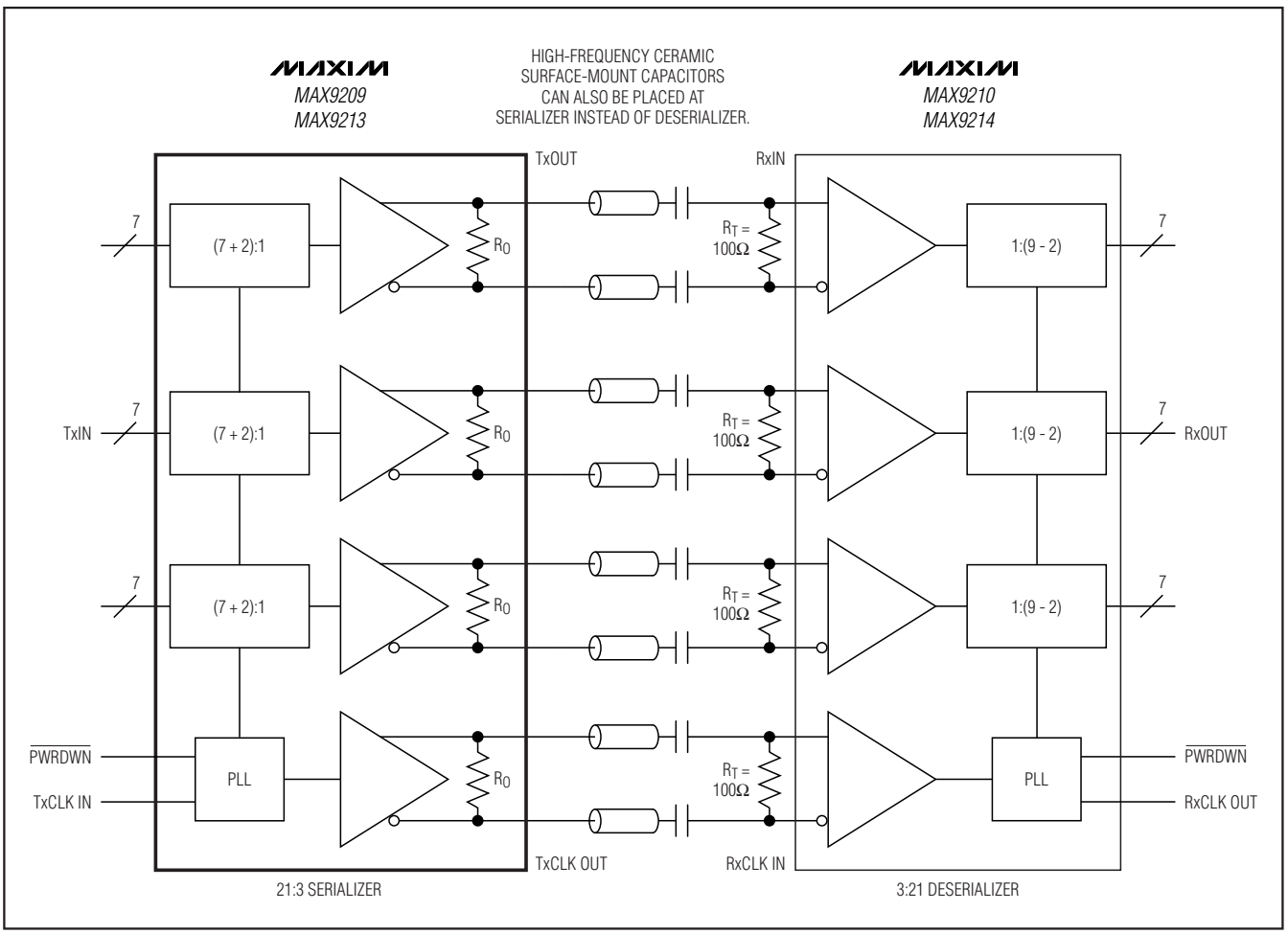

Figure 14. Two Capacitors per Link, AC-Coupled, DC-Balanced Mode

Common-mode voltage differences may be due to ground potential variation or common-mode noise. If there is more than ±1V of difference, the receiver is not guaranteed to read the input signal correctly and may cause bit errors. AC-coupling filters low-frequency ground shifts and common-mode noise and passes high-frequency data. A common-mode voltage difference up to the voltage rating of the coupling capacitor (minus half the differential swing) is tolerated. DC-balanced coding of the data is required to maintain the differential signal amplitude and limit jitter on an AC-coupled link. A capacitor in series with each output of the LVDS driver is sufficient for AC-coupling. However, two capacitors—one at the serializer output and one at the deserializer input—provide protection in case either end of the cable is shorted to a high voltage.

5V Tolerant Inputs

All signal and control inputs except DCB/NC are 5V tolerant and are internally pulled down to GND. The DCB/NC pin has a pullup on the MAX9209/MAX9213.

DCB/NC Pin Default Conditions

The MAX9209/MAX9213 have programmable DC balance/non-DC balance. See Table 1 for DCB/NC default settings and operating modes.

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Programmable DC-Balanced 21-Bit Serializers

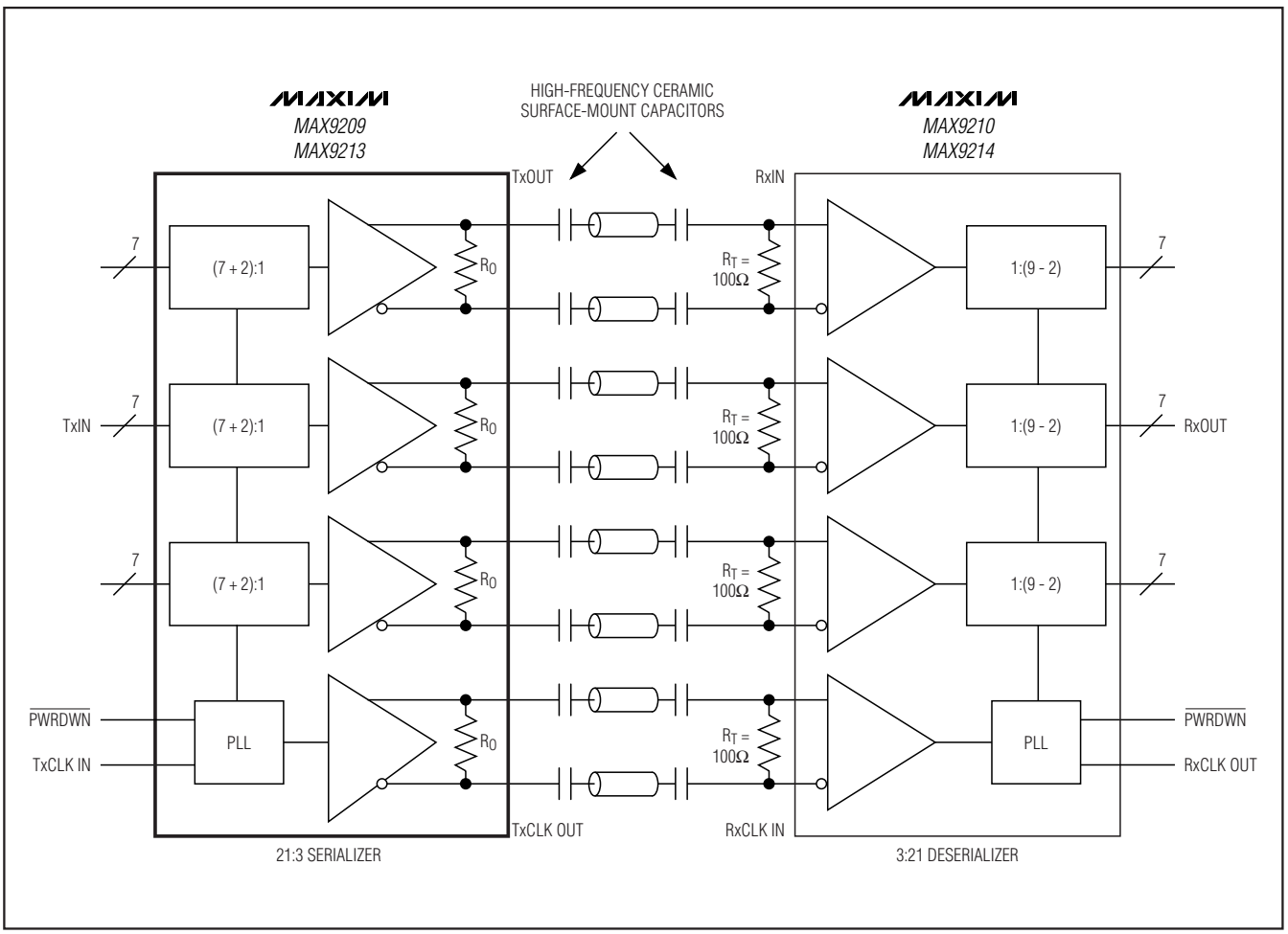

Figure 15. Four Capacitors per Link, AC-Coupled, DC-Balanced Mode

Applications Information

Selection of AC-Coupling Capacitors

Voltage droop and the DSV of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is finite, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level.

The RC network for an AC-coupled link consists of the LVDS receiver termination resistor (R_T), the LVDS driver output resistor (R_O), and the series AC-coupling capacitors (C). The RC time constant for two equal-value series capacitors is (C x (R_T + R_O)) / 2 (Figure 14). The RC time constant for four equal-value series capacitors is (C x (R_T + R_O)) / 4 (Figure 15).

R_T is required to match the transmission line impedance (usually 100Ω) and R_O is determined by the LVDS driver design, with a minimum value of 78Ω (see the *DC Electrical Characteristics* table). This leaves the capacitor selection to change the system time constant.

In the following example, the capacitor value for a droop of 2% is calculated. Jitter due to this droop is then calculated assuming a 1ns transition time:

$$C = -(2 \times t_B \times DSV) / (\ln (1 - D) \times (R_T + R_O)) \quad \text{(Eq 1)}$$

where:
C = AC-coupling capacitor (F)
t_B = bit time (s)
DSV = digital sum variation (integer)
ln = natural log
D = droop (% of signal amplitude)
R_T = termination resistor (Ω)

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R_O = output resistance (Ω)

Equation 1 is for two series capacitors (Figure 14). The bit time (t_B) is the period of the parallel clock divided by 9. The DSV is 10. See equation 3 for four series capacitors (Figure 15).

The capacitor for 2% maximum droop at 8MHz parallel rate clock is:

$$C = -(2 \times t_B \times DSV) / (\ln (1 - D) \times (R_T + R_O))$$
$$C = -(2 \times 13.9ns \times 10) / (\ln (1 - .02) \times (100\Omega + 78\Omega))$$
$$C = 0.0773\mu F$$

Jitter due to droop is proportional to the droop and transition time:

$$t_J = t_T \times D \text{ (Eq 2)}$$

where:
t_J = jitter (s)
t_T = transition time (s) (0% to 100%)
D = droop (% of signal amplitude)

Jitter due to 2% droop and assumed 1ns transition time is:

$$t_J = 1ns \times 0.02$$
$$t_J = 20ps$$

The transition time in a real system depends on the frequency response of the cable driven by the serializer. The capacitor value decreases for a higher frequency parallel clock and for higher levels of droop and jitter. Use high-frequency, surface-mount ceramic capacitors.

Equation 1 altered for four series capacitors (Figure 15) is:

$$C = -(4 \times t_B \times DSV) / (\ln (1 - D) \times (R_T + R_O)) \text{ (Eq 3)}$$

Integrated Termination

The MAX9209/MAX9213 have an integrated output termination resistor across each of the four LVDS outputs. These resistors damp reflections from induced noise and mismatches between the transmission line impedance and termination resistor at the deserializer input. In DC-balanced mode, the differential output resistance is part of the RC time constant. In non-DC-balanced mode, the output termination is increased to 410Ω (typ) to reduce power. In power-down mode ($\overline{PWRDWN}$ = low) or when the power supply is off, the output resistor is switched out and the LVDS outputs are high impedance.

$\overline{PWRDWN}$ and Power-Off

Driving $\overline{PWRDWN}$ low stops the PLL, switches out the integrated output termination resistors, puts the LVDS outputs in high impedance, and reduces supply current to 50µA or less. Driving $\overline{PWRDWN}$ high starts the PLL lock to the input clock and switches in the output termination resistors. The LVDS outputs are not driven until the PLL locks. The differential output resistance pulls the outputs together and the LVDS outputs are high impedance to ground. If the power supply is turned off, the output resistors are switched out and the LVDS outputs are high impedance.

PLL Lock Time

The PLL lock time is set by an internal counter. The maximum time to lock is 32,800 clock periods. Power and clock should be stable to meet the lock-time specification. When the PLL is locking, the LVDS outputs are not active and have a differential output resistance of R_O.

Power-Supply Bypassing

There are separate power domains for LVDS, PLL, and digital circuits. Bypass each LVDS V_{CC}, PLL V_{CC}, and V_{CC} pin with high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.

LVDS Outputs

The LVDS outputs are current sources. The voltage swing is proportional to the load impedance. The outputs are rated for a differential load of 100Ω ±1%.

Cables and Connectors

Interconnect for LVDS typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

Board Layout

Keep the LVTTL/LVCMOS input and LVDS output signals separated to prevent crosstalk. A four-layer PCB with separate layers for power, ground, LVDS outputs, and digital signals is recommended.

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ESD Protection

The MAX9209/MAX9213 ESD tolerance is rated for IEC 61000-4-2, Human Body Model and ISO 10605 standards. IEC 61000-4-2 and ISO 10605 specify ESD tolerance for electronic systems. The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 16). For IEC 61000-4-2, the LVDS outputs are rated for ±8kV contact and ±15kV air discharge. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 17). For the Human Body Model, all pins are rated for ±2kV contact discharge. The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 18). For ISO 10605, the LVDS outputs are rated for ±8kV contact and ±25kV air discharge.

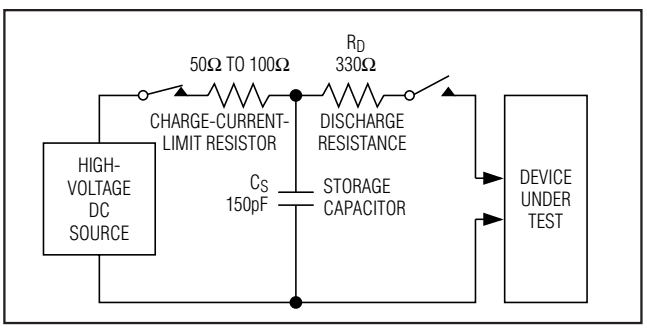

Figure 16. IEC 61000-4-2 Contact Discharge ESD Test Circuit

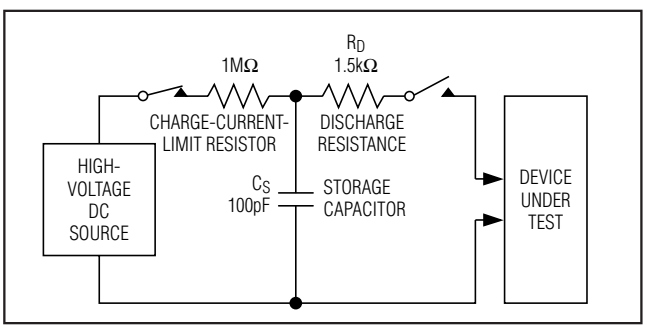

Figure 17. Human Body ESD Test Circuit

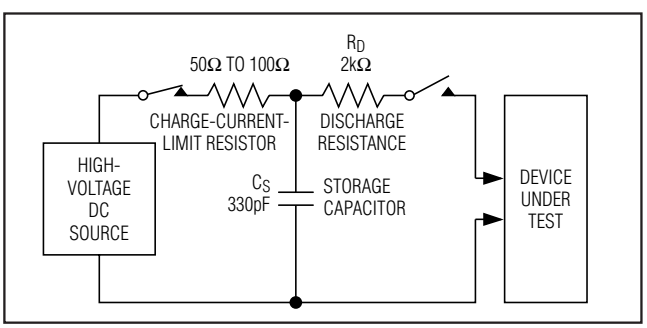

Figure 18. ISO 10605 Contact Discharge ESD Test Circuit

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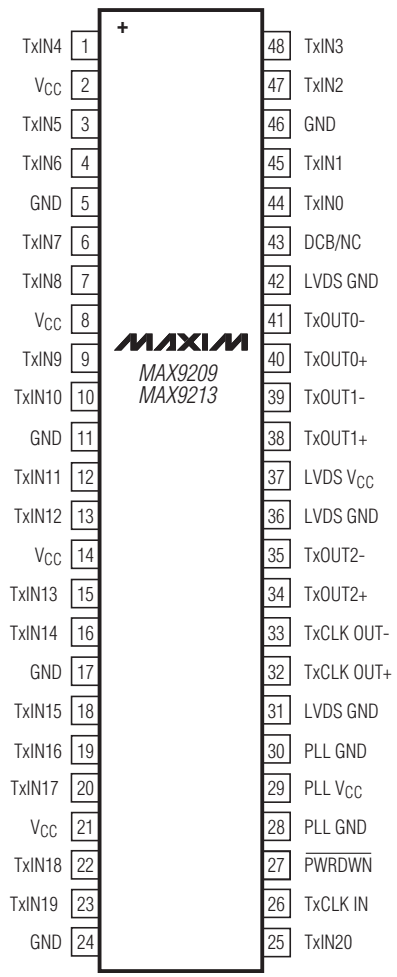
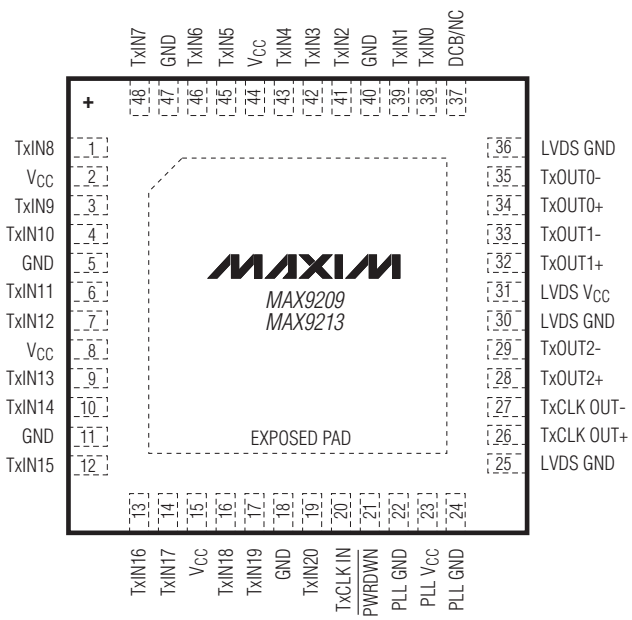
Pin Configurations

TOP VIEW



TSSOP



TQFN

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TSSOP	A48+1	21-0155	90-0124
48 TQFN	T4877+6	21-0144	90-0132

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	6/07	—	1–5, 9, 14, 15, 18, 19, 20
4	10/07	Removed all references to MAX9211 and MAX9215.	1–20
5	3/12	Updated *Ordering Information*	1

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