±15V Digitally Programmable Precision Voltage-Dividers for PGAs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +17V
V_{SS} to GND.....-17V to +0.3V
D0, D1 to GND .....-0.3V to +6V
H, L, W, MATCH_ to GND.....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Current Into Any Signal Pin.....±50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 8.9mW/°C above +70°C).....714mW
10-Pin µMAX (derate 10.3mW/°C above +70°C) 825mW

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +15V, V_{SS} = -15V, GND = 0, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

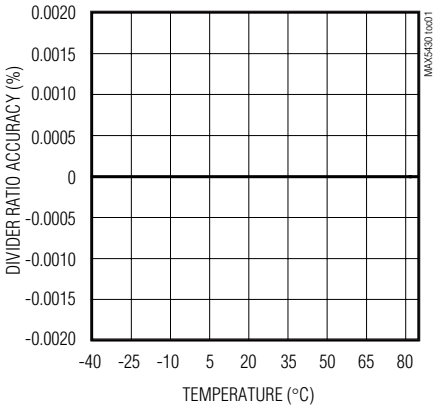
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PERFORMANCE							
Divider Ratio Accuracy (Note 2)		V_H = +5V, V_L = -5V	MAX543_A			0.025	%
			MAX543_B			0.09	
			MAX543_C			0.5	
Resistance between H and L (Figure 1)	R_{HL}				57		kΩ
Capacitance at Analog Pins	C_{ANALOG}				2		pF
Matching Resistor		Ratio = 1			0.5		kΩ
		Ratio = 2, 4, 8			14		
Wiper Resistance	R_W	Ratio = 1			0.5		kΩ
		Ratio = 2, 4, 8			14		
W, H, L, MATCH_H, MATCH _L Voltage Range	V_{ANALOG}			V_{SS}		V_{DD}	V
DIGITAL INPUTS							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Leakage Current		D0, D1 = 5V or GND				±1	µA
Input Capacitance	C_{IN}				5		pF
POWER REQUIREMENTS							
Negative Supply Current	I_{SS}				1	25	µA
Positive Supply Current	I_{DD}				35	60	µA
Positive Power-Supply Voltage	V_{DD}			10.8		15.75	V
Negative Power-Supply Voltage	V_{SS}			-15.75		0	V
DYNAMIC PERFORMANCE							
Switching Time	t_{D2W}, t_{H2W}				0.3		µs

Note 1: All devices are 100% production tested at T_A = +25°C. SOT23 packages are guaranteed by design from T_A = T_{MIN} to T_{MAX}.
Note 2: Gain accuracy is measured without load at pin W.

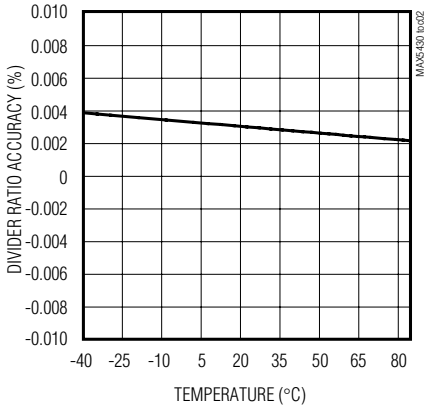
Typical Operating Characteristics

(V_{DD} = +15V, V_{SS} = -15V or V_{SS} = GND, V_H = 5V, V_L =-5V, T_A = 25°C, unless otherwise noted.) (Note 3)

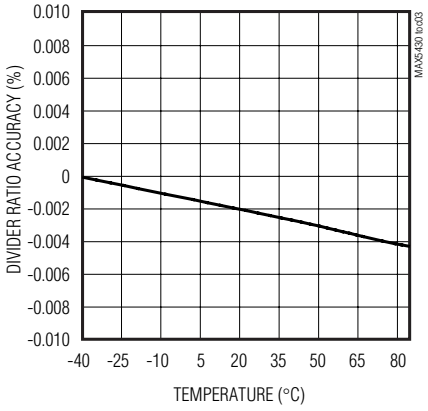
MAX543_A DIVIDER RATIO ACCURACY vs. TEMPERATURE (RATIO = 1)



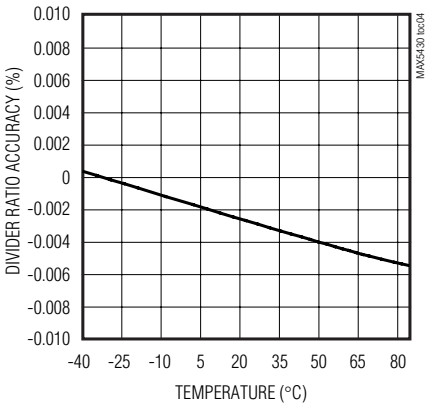
MAX543_A DIVIDER RATIO ACCURACY vs. TEMPERATURE (RATIO = 2)



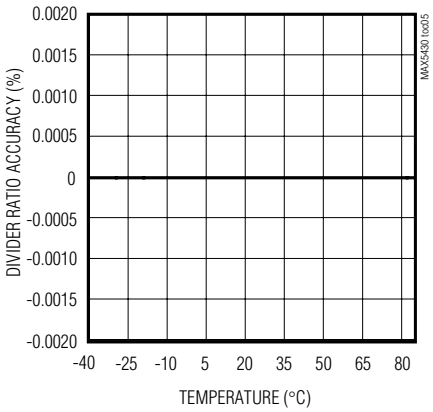
MAX543_A DIVIDER RATIO ACCURACY vs. TEMPERATURE (RATIO = 4)



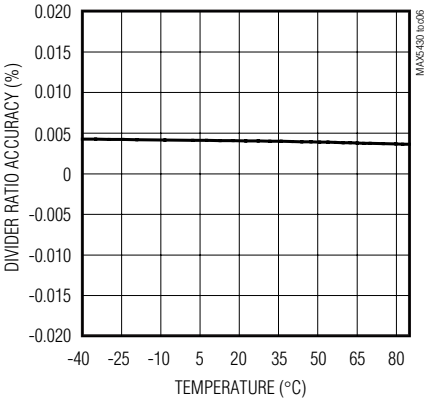
MAX543_A DIVIDER RATIO ACCURACY vs. TEMPERATURE (RATIO = 8)



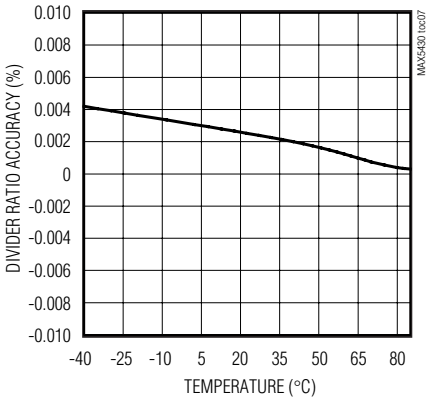
MAX543_B DIVIDER RATIO ACCURACY vs. TEMPERATURE (RATIO = 1)



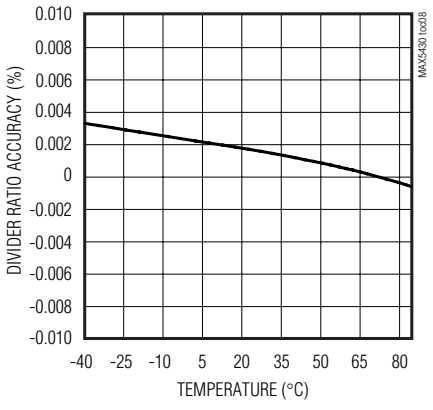
MAX543_B DIVIDER RATIO ACCURACY vs. TEMPERATURE (RATIO = 2)



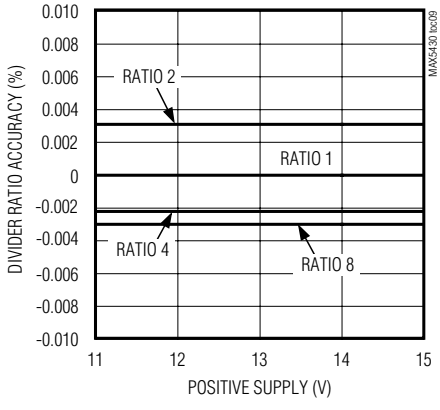
MAX543_B DIVIDER RATIO ACCURACY vs.TEMPERATURE (RATIO = 4)



MAX543_B DIVIDER RATIO ACCURACY vs. TEMPERATURE (RATIO = 8)



MAX543_A DIVIDER RATIO ACCURACY vs. POSITIVE SUPPLY (V_{SS} = -15V)

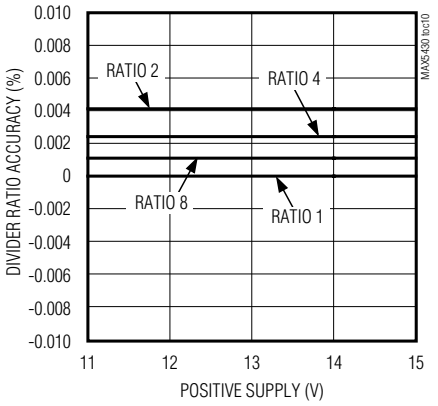


±15V Digitally Programmable Precision Voltage-Dividers for PGAs

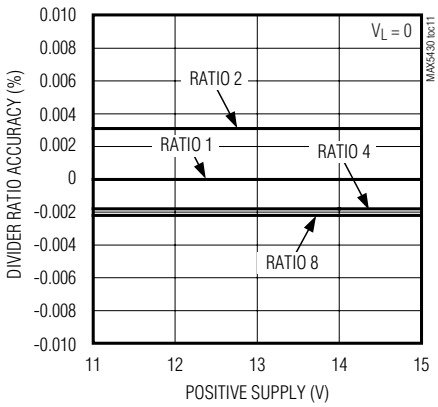
Typical Operating Characteristics (continued)

(V_{DD} = +15V, V_{SS} = -15V or V_{SS} = GND, V_H = 5V, V_L =-5V, T_A = 25°C, unless otherwise noted.) (Note 3)

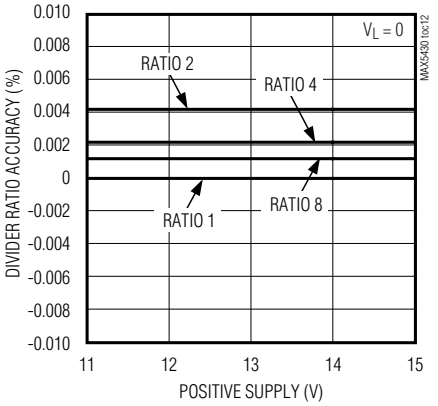
MAX543_B DIVIDER RATIO ACCURACY vs. POSITIVE SUPPLY (V_{SS} = -15V)



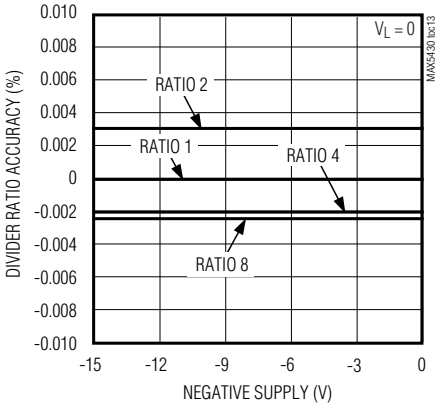
MAX543_A DIVIDER RATIO ACCURACY vs. POSITIVE SUPPLY (V_{SS} = 0V)



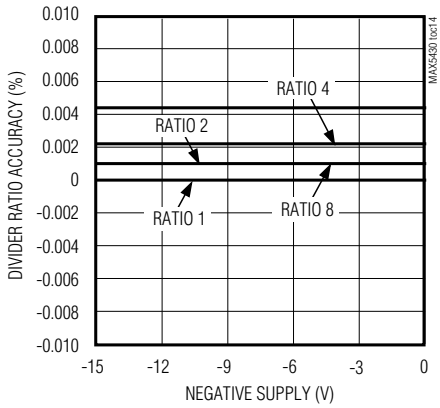
MAX543_B DIVIDER RATIO ACCURACY vs. POSITIVE SUPPLY (V_{SS} = 0V)



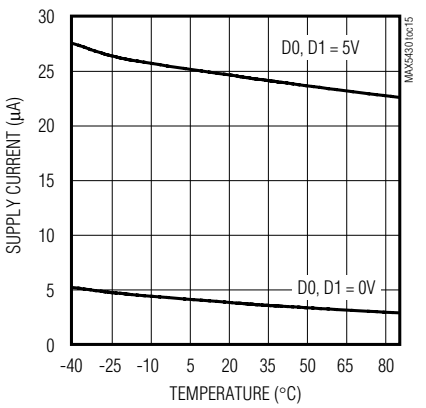
MAX543_A DIVIDER RATIO ACCURACY vs. NEGATIVE SUPPLY



MAX543_B DIVIDER RATIO ACCURACY vs. NEGATIVE SUPPLY



SUPPLY CURRENT vs. TEMPERATURE



Note 3: For MAX543_C accuracy *Typical Operating Characteristics*, refer to MAX543_B accuracy *Typical Operating Characteristics*.

Pin Description

PIN		NAME	FUNCTION
MAX5431	MAX5430		
1	8	V_{DD}	Positive Power Supply
2	—	MATCH_H	Matching Resistor High Terminal
3	7	GND	Ground
4	6	H	High Terminal of Resistive-Divider
5	5	L	Low Terminal of Resistive-Divider
6	—	MATCH_L	Matching Resistor Low Terminal
7	4	V_{SS}	Negative Power Supply
8	3	W	Wiper Terminal of Resistive-Divider
9	2	D1	Second Bit Digital Input (MSB) (Table 1)
10	1	D0	First Bit Digital Input (LSB) (Table 1)

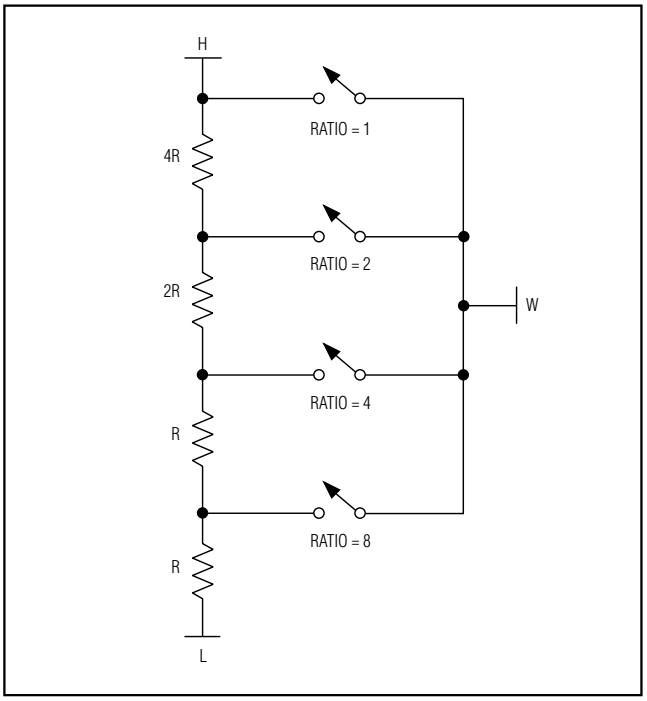


Figure 1. Simplified Functional Diagram

Detailed Description

The MAX5430/MAX5431 are digitally programmable precision resistor arrays. These devices have fixed resistor-dividers with digitally controlled contacts, providing four precision noninverting gains of 1, 2, 4, and 8 for PGA applications (see *Functional Diagram* and Figure 1). The MAX5430/MAX5431 achieve ratio accuracies of 0.025% (MAX5430A/MAX5431A), 0.09% (MAX5430B/MAX5431B), or 0.5% (MAX5430C/MAX5431C).

The end-to-end resistance from H to L is 57kΩ. The impedance seen at W is designed to be the same 14kΩ for gain settings 2, 4, and 8, ensuring excellent op amp input-resistance balance, regardless of gain setting. In a gain of 1 configuration, H is internally connected to W with a typical resistance of 500Ω.

Matching Resistor (MAX5431)

The MAX5431 includes a matching resistor to compensate the offset voltage due to the input bias current of the op amp. The resistance from MATCH_H to MATCH_L is a fixed matching resistor, equal to the resistance seen at W for gains of 2, 4, and 8. In the gain of 1, an internal switch short circuits MATCH_H and MATCH_L. This internal switch matches the impedance of the switch between H and W.

Table 1. Logic-Control Truth Table

DIGITAL INPUTS		GAIN
D1	D0	
0	0	1
0	1	2
1	0	4
1	1	8

±15V Digitally Programmable Precision Voltage-Dividers for PGAs

Digital Interface Operation

The MAX5430/MAX5431 feature a simple two-bit parallel programming interface. D1 and D0 program the gain setting according to the *Logic-Control Truth Table* (see Table 1). The digital interface is CMOS/TTL logic compatible.

Applications Information

Programmable-Gain Amplifier

The MAX5430/MAX5431 are ideally suited for high-precision PGA applications. The typical application circuit of Figure 2 uses the MAX5431 with matching resistor to compensate for voltage offset due to op amp input bias currents. Use the MAX5430 with an ultra-low input bias current op amp (see Figure 3).

Power Supplies and Bypassing

The MAX5430/MAX5431 operate from dual ±15V supplies or a single 15V supply. For dual supplies, bypass V_{DD} and V_{SS} with 0.1µF ceramic capacitors to GND. For single supply, connect V_{SS} to GND and bypass V_{DD} with a 0.1µF ceramic capacitor to GND.

Switching Time and Layout Concerns

The switching time of the MAX5430/MAX5431 depends on the capacitive loading at W. For best performance, reduce parasitic board capacitance by minimizing the circuit board trace from W to the op amp inverting input, and choose an op amp with low input capacitance.

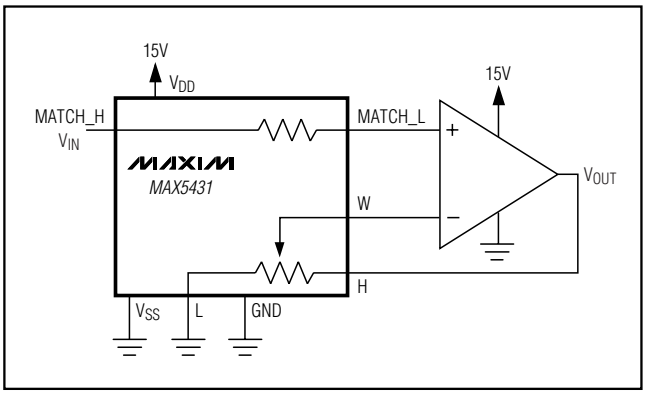


Figure 2. MAX5431 Typical Application Circuit PGA with Input I_{BIAS} Matching

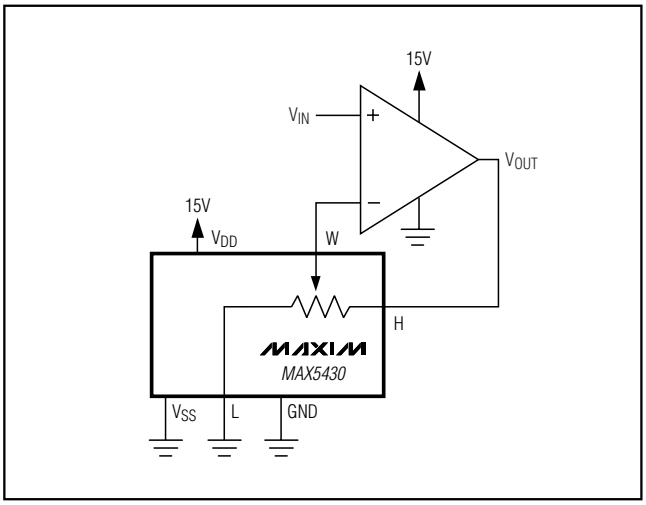
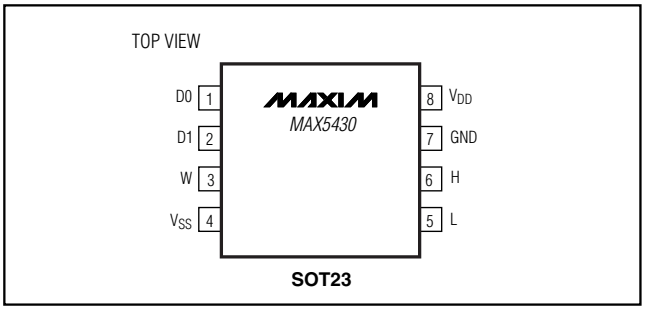


Figure 3. Programmable-Gain Amplifier Using the MAX5430

Pin Configurations (continued)



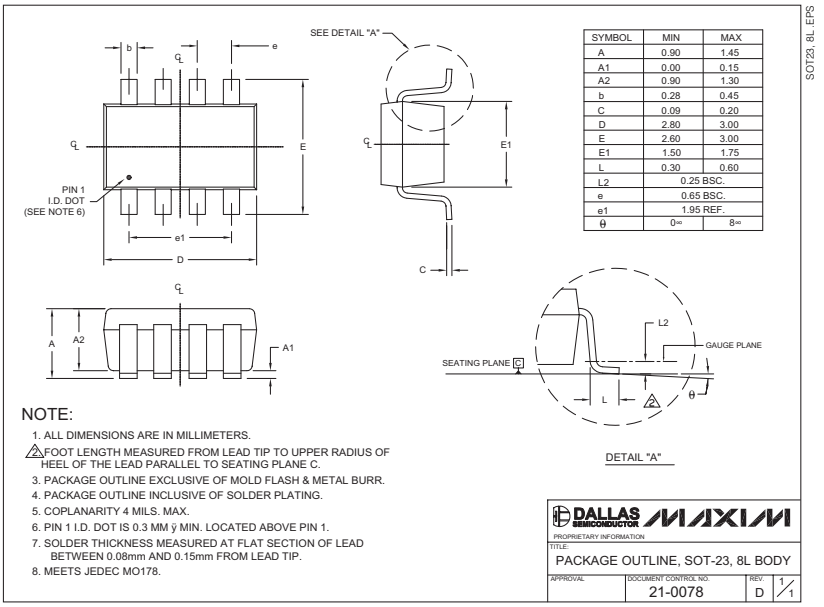
Chip Information

TRANSISTOR COUNT: 121

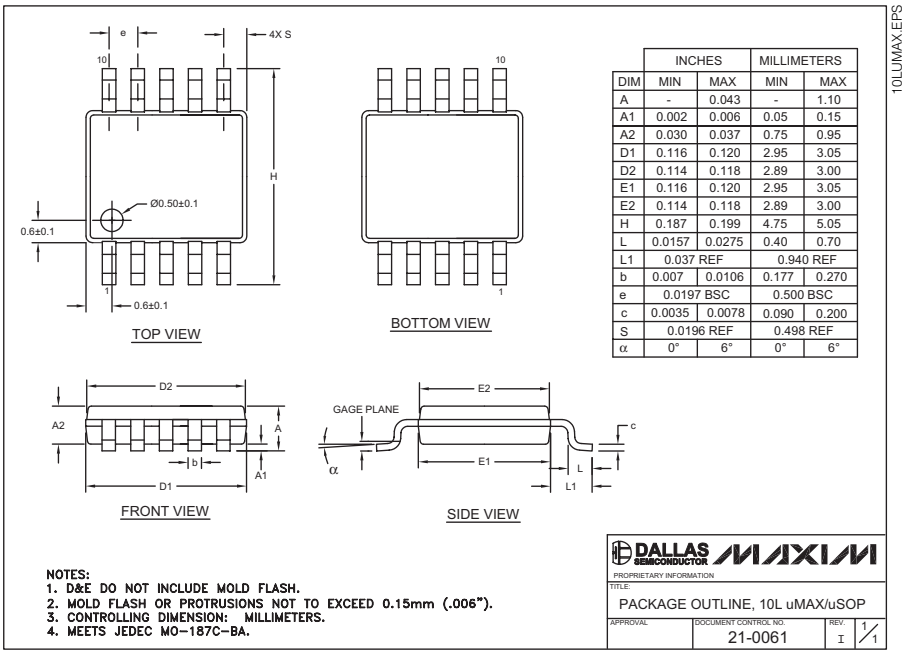
PROCESS: CMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.30	0.60
L2	0.25 BSC.	
e	0.65 BSC.	
e1	1.95 REF.	
θ	0∞	8∞



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°