High-Performance, Single-Ended, Current-Mode PWM Controllers

ABSOLUTE MAXIMUM RATINGS

V_{CC} (Low-Impedance Source) to GND .....-0.3V to +30V
V_{CC} (I_{CC} < 30mA).....Self Limiting
OUT to GND .....-0.3V to (V_{CC} + 0.3V)
OUT Current.....±1A for 10µs
FB, SYNC, COMP, CS, R_T/C_T, REF to GND .....-0.3V to +6V
COMP Sink Current (MAX5094).....10mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 4.5mW/°C above +70°C) 362mW
8-Pin SO (derate 5.9mW/°C above +70°C).....470.6mW
Operating Temperature Range .....-40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, R_T = 10kΩ, C_T = 3.3nF, REF = open, C_{REF} = 0.1µF, COMP = open, V_{FB} = 2V, CS = GND, **$T_A = T_J$ = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
Output Voltage	V_{REF}	T_A = +25°C, I_{REF} = 1mA	4.950	5.000	5.050	V
Line Regulation	ΔV_{LINE}	12V ≤ V_{CC} ≤ 25V, I_{REF} = 1mA		0.4	4	mV
Load Regulation	ΔV_{LOAD}	1mA ≤ I_{REF} ≤ 20mA		6	25	mV
Total Output Variation	V_{REFT}	1mA ≤ I_{REF} ≤ 20mA, 12V ≤ V_{CC} ≤ 25V	4.9		5.1	V
Reference Output-Noise Voltage	V_{NOISE}	10Hz ≤ f ≤ 10kHz, T_A = +25°C		50		µV
Reference Output Short Circuit	I_{S_SC}	V_{REF} = 0V	-30	-100	-180	mA
OSCILLATOR						
Initial Accuracy		T_A = +25°C	51	54	57	kHz
Voltage Stability		12V ≤ V_{CC} ≤ 25V		0.2	0.5	%
Temp Stability		-40°C ≤ T_A ≤ +85°C		0.5		%
R_T/C_T Voltage Ramp (P-P)	V_{RAMP}			1.7		V
R_T/C_T Voltage Ramp Valley	V_{RAMP_VALLEY}			1.1		V
Discharge Current	I_{DIS}	$V_{RT/CT}$ = 2V, T_A = +25°C	7.9	8.3	8.7	mA
		$V_{RT/CT}$ = 2V, -40°C ≤ T_A ≤ +85°C	7.5	8.3	9.0	
Frequency Range	f_{OSC}		20		1000	kHz
ERROR AMPLIFIER (MAX5094)						
FB Input Voltage	V_{FB}	FB shorted to COMP	2.465	2.5	2.535	V
FB Input Bias Current	$I_{B(FB)}$			-0.01	-0.1	µA
Open-Loop Voltage Gain	A_{VOL}	2V ≤ V_{COMP} ≤ 4V		100		dB
Unity-Gain Bandwidth	f_{GBW}			1		MHz
Power-Supply Rejection Ratio	PSRR	12V ≤ V_{CC} ≤ 25V (Note 2)	60	80		dB
COMP Sink Current	I_{SINK}	V_{FB} = 2.7V, V_{COMP} = 1.1V	2	6		mA
COMP Source Current	I_{SOURCE}	V_{FB} = 2.3V, V_{COMP} = 5V	-0.5	-1.2	-1.8	mA
COMP Output High Voltage	V_{COMPH}	V_{FB} = 2.3V, R_{COMP} = 15kΩ to GND	5	5.8		V
COMP Output Low Voltage	V_{COMPL}	V_{FB} = 2.7V, R_{COMP} = 15kΩ to REF		0.1	1.1	V
CURRENT-SENSE AMPLIFIER						
Gain (Notes 3, 4)	A_{CS}	(MAX5094A/MAX5094B)	2.85	3	3.26	V/V
		(MAX5094C/D, MAX5095_)	2.85	3	3.40	V/V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +15V, R_T = 10kΩ, C_T = 3.3nF, REF = open, C_{REF} = 0.1µF, COMP = open, V_{FB} = 2V, CS = GND, **$T_A = T_J$ = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Current-Sense Signal	V_{CS_MAX}	MAX5094A/B (Note 3)	0.95	1	1.05	V
		MAX5094C/MAX5094D (Note 3)	0.275	0.3	0.325	
		V_{COMP} = 5V, MAX5095	0.275	0.3	0.325	
Power-Supply Rejection Ratio	PSRR	12V ≤ V_{CC} ≤ 25V		70		dB
Input Bias Current	I_{CS}	V_{COMP} = 0V		-1	-2.5	µA
Delay From CS to OUT	t_{CS_DELAY}	50mV overdrive		60		ns
MOSFET DRIVER						
OUT Low-Side On-Resistance	V_{RDS_ONL}	I_{SINK} = 200mA		4.5	10	Ω
OUT High-Side On-Resistance	V_{RDS_ONH}	I_{SOURCE} = 100mA		3.5	7	Ω
I_{SOURCE} (Peak)	I_{SOURCE}	C_{OUT} = 10nF		2		A
I_{SINK} (Peak)	I_{SINK}	C_{OUT} = 10nF		1		A
Rise Time	t_R	C_{OUT} = 1nF		15		ns
Fall Time	t_F	C_{OUT} = 1nF		22		ns
UNDERVOLTAGE LOCKOUT/STARTUP						
Startup Voltage Threshold	V_{CC_START}		7.98	8.40	8.82	V
Minimum Operating Voltage After Turn-On	V_{CC_MIN}		7.1	7.6	8.0	V
Undervoltage-Lockout Hysteresis	$UVLO_{HYST}$			0.8		V
PWM						
Maximum Duty Cycle	D_{MAX}	MAX5094A/MAX5094C/MAX5095A	94.5	96	97.5	%
		MAX5094B/MAX5094D/MAX5095B/ MAX5095C	48	49.8	50	
Minimum Duty Cycle	D_{MIN}				0	%
SUPPLY CURRENT						
Startup Supply Current	I_{START}	V_{CC} = 7.5V		32	65	µA
Operating Supply Current	I_{CC}	V_{FB} = V_{CS} = 0V		3	5	mA
Zener Bias Voltage at V_{CC}	V_Z	I_{CC} = 25mA	24	26.5		V
THERMAL SHUTDOWN						
Thermal Shutdown	T_{SHDN}	Junction temperature rising		150		°C
Thermal Shutdown Hysteresis	T_{HYST}			4		°C
SYNCHRONIZATION (MAX5095A/MAX5095B Only) (Note 5)						
SYNC Frequency Range	f_{SYNC}		20		1000	kHz
SYNC Clock Input High Threshold	$V_{SYNCINH}$		3.5			V
SYNC Clock Input Low Threshold	$V_{SYNCINL}$				0.8	V
SYNC Clock Input Minimum Pulse Width	t_{PW_SYNCIN}		200			ns
SYNC Clock Output High Level	V_{SYNCOH}	1mA external pulldown	4.0	4.7		V
SYNC Clock Output Low Level	V_{SYNCOL}	R_{SYNC} = 5kΩ		0	0.1	V
SYNC Leakage Current	I_{SYNC}	V_{SYNC} = 0V		0.01	0.1	µA

High-Performance, Single-Ended, Current-Mode PWM Controllers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +15V, R_T = 10kΩ, C_T = 3.3nF, REF = open, C_{REF} = 0.1µF, COMP = open, V_{FB} = 2V, CS = GND, **$T_A = T_J$ = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADV_CLK (MAX5095C Only)						
ADV_CLK High Voltage	V_{ADV_CLKH}	I_{ADV_CLK} = 10mA source	2.4	3		V
ADV_CLK Low Voltage	V_{ADV_CLKL}	I_{ADV_CLK} = 10mA sink			0.4	V
ADV_CLK Output Pulse Width	t_{PULSE}			85		ns
ADV_CLK Rising Edge to OUT Rising Edge	t_{ADV_CLK}			110		ns
ADV_CLK Source and Sink Current	I_{ADV_CLK}		10			mA

ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, R_T = 10kΩ, C_T = 3.3nF, REF = open, C_{REF} = 0.1µF, COMP = open, V_{FB} = 2V, CS = GND, **$T_A = T_J$ = -40°C to +125°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
Output Voltage	V_{REF}	T_A = +25°C, I_{REF} = 1mA	4.950	5.000	5.050	V
Line Regulation	ΔV_{LINE}	12V ≤ V_{CC} ≤ 25V, I_{REF} = 1mA		0.4	4	mV
Load Regulation	ΔV_{LOAD}	1mA ≤ I_{REF} ≤ 20mA		6	25	mV
Total Output Variation	V_{REFT}	1mA ≤ I_{REF} ≤ 20mA, 12V ≤ V_{CC} ≤ 25V	4.9		5.1	V
Reference Output-Noise Voltage	V_{NOISE}	10Hz ≤ f ≤ 10kHz, T_A = +25°C		50		µV
Reference Output Short Circuit	I_{S_SC}	V_{REF} = 0V	-30	-100	-180	mA
OSCILLATOR						
Initial Accuracy		T_A = +25°C	51	54	57	kHz
Voltage Stability		12V ≤ V_{CC} ≤ 25V		0.2	0.5	%
Temp Stability		-40°C ≤ T_A ≤ +125°C		1		%
R_T/C_T Voltage Ramp (P-P)	V_{RAMP}			1.7		V
R_T/C_T Voltage Ramp Valley	V_{RAMP_VALLEY}			1.1		V
Discharge Current	I_{DIS}	$V_{RT/CT}$ = 2V, T_A = +25°C	7.9	8.3	8.7	mA
		$V_{RT/CT}$ = 2V, -40°C ≤ T_A ≤ +125°C	7.5	8.3	9.0	
Frequency Range	f_{OSC}		20		1000	kHz
ERROR AMPLIFIER (MAX5094)						
FB Input Voltage	V_{FB}	FB shorted to COMP	2.465	2.5	2.535	V
FB Input Bias Current	$I_{B(FB)}$			-0.01	-0.1	µA
Open-Loop Voltage Gain	A_{VOL}	2V ≤ V_{COMP} ≤ 4V		100		dB
Unity-Gain Bandwidth	f_{GBW}			1		MHz
Power-Supply Rejection Ratio	PSRR	12V ≤ V_{CC} ≤ 25V (Note 2)	60	80		dB
COMP Sink Current	I_{SINK}	V_{FB} = 2.7V, V_{COMP} = 1.1V	2	6		mA
COMP Source Current	I_{SOURCE}	V_{FB} = 2.3V, V_{COMP} = 5V	-0.5	-1.2	-1.8	mA
COMP Output High Voltage	V_{COMPH}	V_{FB} = 2.3V, R_{COMP} =15kΩ to GND	5	5.8		V
COMP Output Low Voltage	V_{COMPL}	V_{FB} = 2.7V, R_{COMP} = 15kΩ to REF		0.1	1.1	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +15V, R_T = 10kΩ, C_T = 3.3nF, REF = open, C_{REF} = 0.1µF, COMP = open, V_{FB} = 2V, CS = GND, **$T_A = T_J$ = -40°C to +125°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT-SENSE AMPLIFIER						
Gain (Notes 3, 4)	A_{CS}	MAX5094A/MAX5094B	2.85	3	3.26	V/V
		MAX5094C/D, MAX5095_	2.85	3	3.40	
Maximum Current-Sense Signal	V_{CS_MAX}	MAX5094A/B (Note 3)	0.95	1	1.05	V
		MAX5094C/MAX5094D (Note 3)	0.275	0.300	0.325	
		V_{COMP} = 5V, MAX5095_	0.275	0.300	0.325	
Power-Supply Rejection Ratio	PSRR	12V ≤ V_{CC} ≤ 25V		70		dB
Input Bias Current	I_{CS}	V_{COMP} = 0V		-1	-2.5	µA
Delay From CS to OUT	t_{CS_DELAY}	50mV overdrive		60		ns
MOSFET DRIVER						
OUT Low-Side On-Resistance	V_{RDS_ONL}	I_{SINK} = 200mA		4.5	12	Ω
OUT High-Side On-Resistance	V_{RDS_ONH}	I_{SOURCE} = 100mA		3.5	9	Ω
I_{SOURCE} (Peak)	I_{SOURCE}	C_{OUT} = 10nF		2		A
I_{SINK} (Peak)	I_{SINK}	C_{OUT} = 10nF		1		A
Rise Time	t_R	C_{OUT} = 1nF		15		ns
Fall Time	t_F	C_{OUT} = 1nF		22		ns
UNDERVOLTAGE LOCKOUT/STARTUP						
Startup Voltage Threshold	V_{CC_START}		7.98	8.4	8.82	V
Minimum Operating Voltage After Turn-On	V_{CC_MIN}		7.1	7.6	8.0	V
Undervoltage-Lockout Hysteresis	$UVLO_{HYST}$			0.8		V
PWM						
Maximum Duty Cycle	D_{MAX}	MAX5094A/MAX5094C/MAX5095A	94.5	96	97.5	%
		MAX5094B/MAX5094D/MAX5095B/ MAX5095C	48	49.8	50	
Minimum Duty Cycle	D_{MIN}				0	%
SUPPLY CURRENT						
Startup Supply Current	I_{START}	V_{CC} = 7.5V		32	65	µA
Operating Supply Current	I_{CC}	V_{FB} = V_{CS} = 0V		3	5	mA
Zener Bias Voltage at V_{CC}	V_Z	I_{CC} = 25mA	24	26.5		V
THERMAL SHUTDOWN						
Thermal Shutdown	T_{SHDN}	Junction temperature rising		150		°C
Thermal Shutdown Hysteresis	T_{HYST}			4		°C
SYNCHRONIZATION (MAX5095A/MAX5095B Only) (Note 5)						
SYNC Frequency Range	f_{SYNC}		20		1000	kHz
SYNC Clock Input High Threshold	$V_{SYNCINH}$		3.5			V
SYNC Clock Input-Low Threshold	$V_{SYNCINL}$				0.8	V
SYNC Clock Input Minimum Pulse Width	t_{PW_SYNCIN}		200			ns

High-Performance, Single-Ended, Current-Mode PWM Controllers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +15V, R_T = 10kΩ, C_T = 3.3nF, REF = open, C_{REF} = 0.1µF, COMP = open, V_{FB} = 2V, CS = GND, **$T_A = T_J$ = -40°C to +125°C**, unless otherwise noted.) (Note 1)

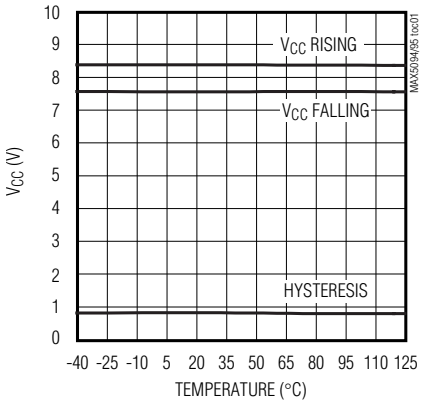
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Clock Output High Level	V_{SYNCOH}	1mA external pulldown	4.0	4.7		V
SYNC Clock Output Low Level	V_{SYNCOL}	R_{SYNC} = 5kΩ		0	0.1	V
SYNC Leakage Current	I_{SYNC}	V_{SYNC} = 0V		0.01	0.1	µA
ADV_CLK (MAX5095C Only)						
ADV_CLK High Voltage	V_{ADV_CLKH}	I_{ADV_CLK} = 10mA source	2.4	3		V
ADV_CLK Low Voltage	V_{ADV_CLKL}	I_{ADV_CLK} = 10mA sink			0.4	V
ADV_CLK Output Pulse Width	t_{PULSE}			85		ns
ADV_CLK Rising Edge to OUT Rising Edge	t_{ADV_CLK}			110		ns
ADV_CLK Source and Sink Current	I_{ADV_CLK}		10			mA

Note 1: All devices are 100% tested at +25°C. All limits over temperature are guaranteed by design, not production tested.
Note 2: Guaranteed by design, not production tested.
Note 3: Parameter measured at trip point of latch with V_{FB} = 0 (MAX5094 only).
Note 4: Gain is defined as $A = \Delta V_{COMP} / \Delta V_{CS}$, $0 \le V_{CS} \le 0.8V$ for MAX5094A/MAX5094B, $0 \le V_{CS} \le 0.2V$ for MAX5094C/MAX5094D/ MAX5095_.
Note 5: Output frequency equals oscillator frequency for MAX5094A/MAX5094C/MAX5095A. Output frequency is one-half oscillator frequency for MAX5094B/MAX5094D/MAX5095B/MAX5095C.

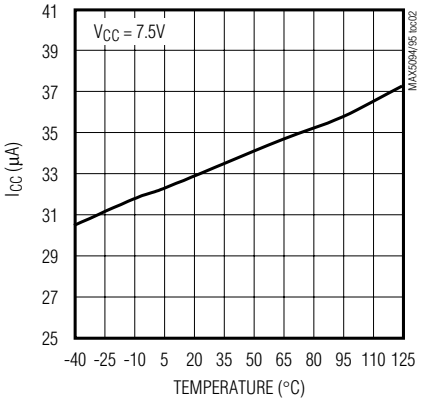
Typical Operating Characteristics

(V_{CC} = 15V, T_A = +25°C, unless otherwise noted.)

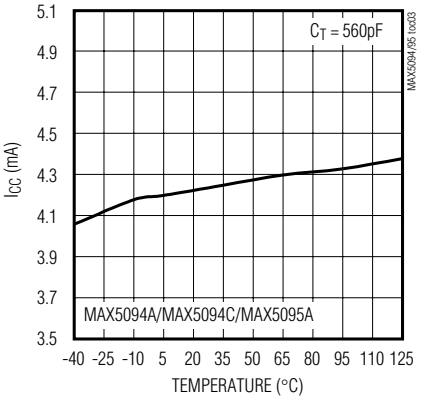
BOOTSTRAP UVLO vs. TEMPERATURE



STARTUP CURRENT vs. TEMPERATURE



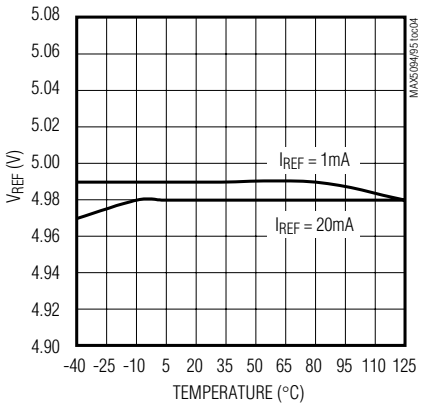
OPERATING SUPPLY CURRENT vs. TEMPERATURE AFTER STARTUP (f_{OSC} = f_{SW} = 300kHz)



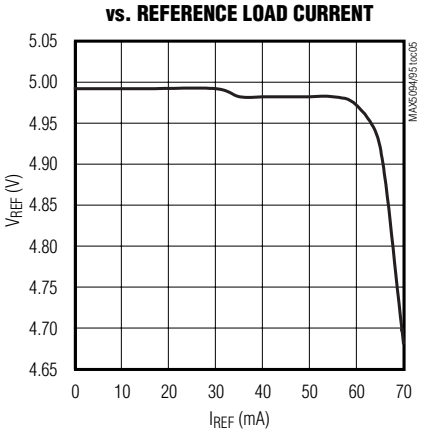
Typical Operating Characteristics (continued)

(V_{CC} = 15V, T_A = +25°C, unless otherwise noted.)

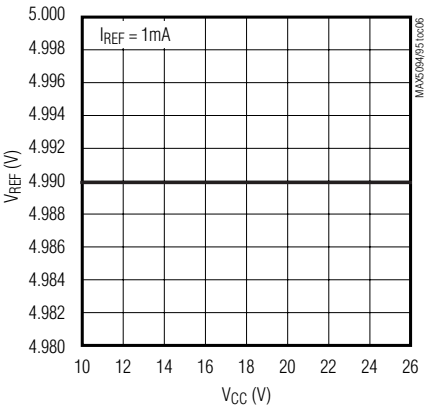
REFERENCE VOLTAGE vs. TEMPERATURE



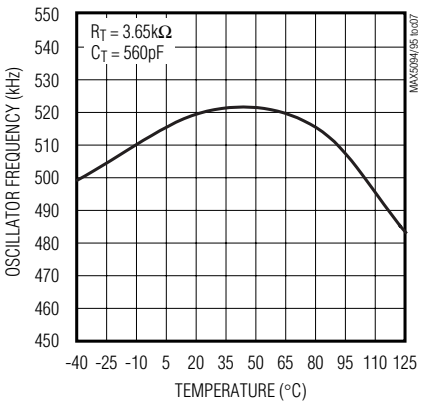
REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT



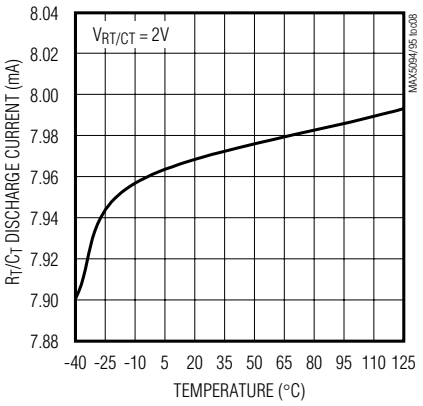
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



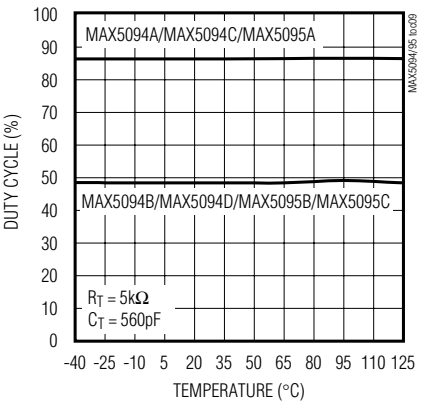
OSCILLATOR FREQUENCY (f_{OSC}) vs. TEMPERATURE



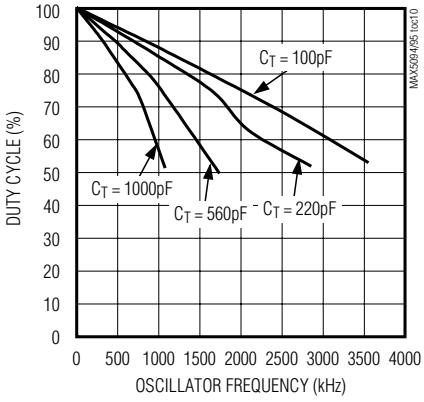
OSCILLATOR R_T/C_T DISCHARGE CURRENT vs. TEMPERATURE



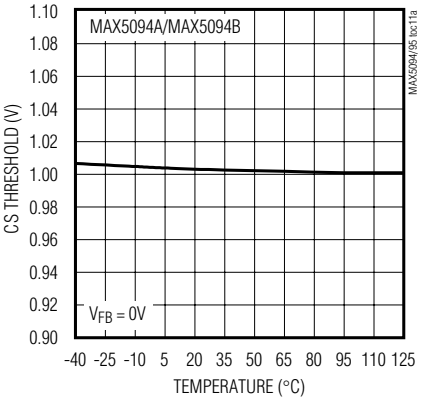
MAXIMUM DUTY CYCLE vs. TEMPERATURE



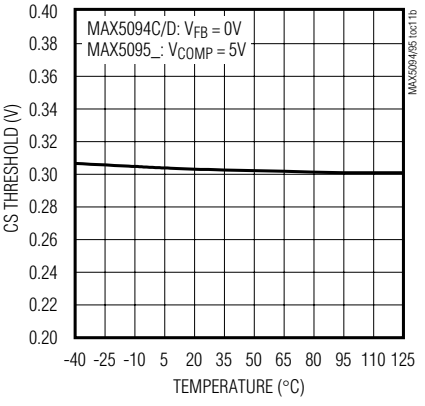
MAXIMUM DUTY CYCLE vs. FREQUENCY MAX5094A/MAX5094C/MAX5095A



CURRENT-SENSE TRIP THRESHOLD vs. TEMPERATURE



CURRENT-SENSE TRIP THRESHOLD vs. TEMPERATURE

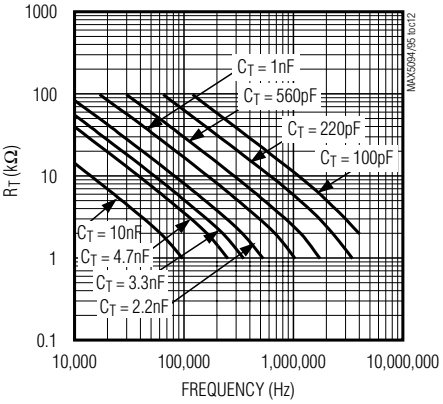


High-Performance, Single-Ended, Current-Mode PWM Controllers

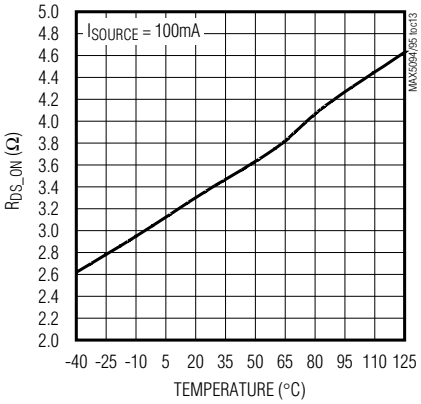
Typical Operating Characteristics (continued)

(V_{CC} = 15V, T_A = +25°C, unless otherwise noted.)

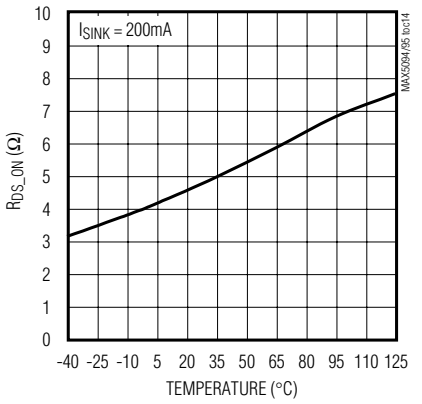
TIMING RESISTANCE vs. OSCILLATOR FREQUENCY



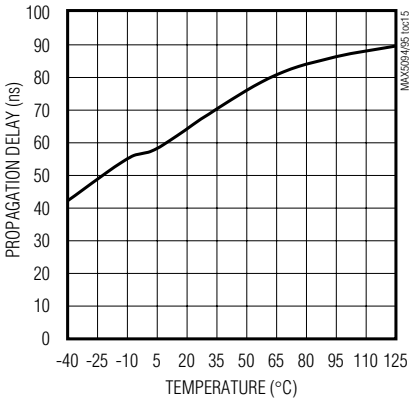
OUT IMPEDANCE vs. TEMPERATURE (R_{DS_ON} PMOS DRIVER)



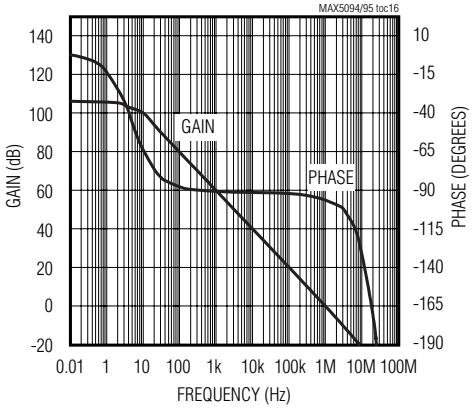
OUT IMPEDANCE vs. TEMPERATURE (R_{DS_ON} NMOS DRIVER)



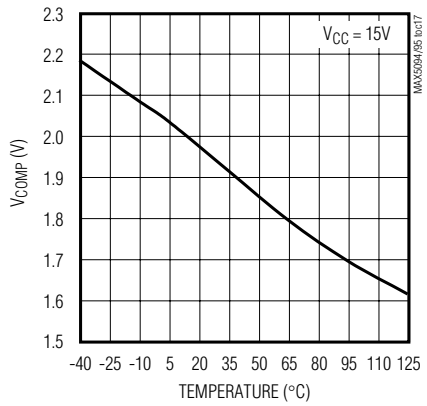
PROPAGATION DELAY FROM CURRENT-LIMIT COMPARATOR TO OUT vs. TEMPERATURE



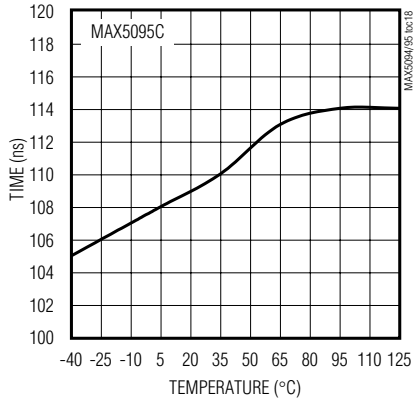
ERROR-AMPLIFIER OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



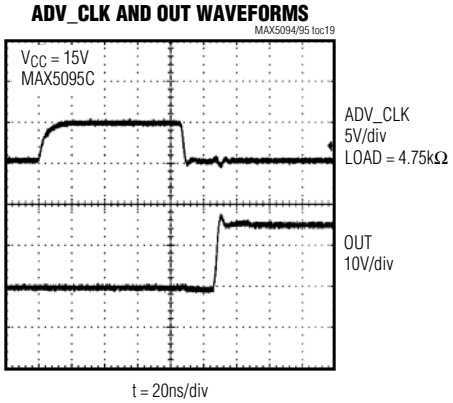
COMP VOLTAGE LEVEL TO TURN OFF DEVICE vs. TEMPERATURE



ADV_CLK RISING EDGE TO OUT RISING EDGE TIME vs. TEMPERATURE



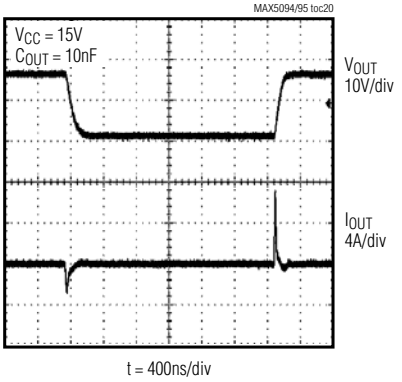
ADV_CLK AND OUT WAVEFORMS



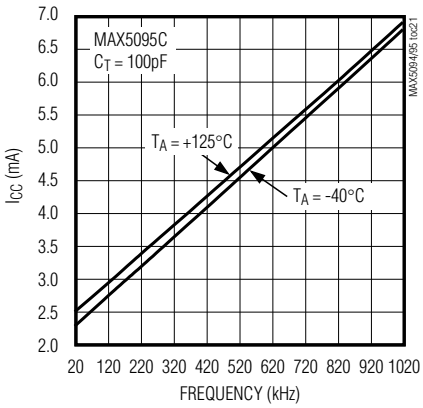
Typical Operating Characteristics (continued)

(V_{CC} = 15V, T_A = +25°C, unless otherwise noted.)

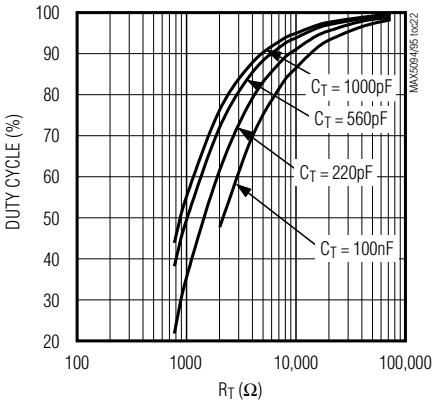
OUT SOURCE AND SINK CURRENTS



SUPPLY CURRENT vs. OSCILLATOR FREQUENCY



MAXIMUM DUTY CYCLE vs. R_T MAX5094A/MAX5095A



Pin Descriptions

MAX5094_

PIN	NAME	FUNCTION
1	COMP	Error-Amplifier Output. COMP can be used for soft-start.
2	FB	Error-Amplifier Inverting Input
3	CS	PWM Comparator and Overcurrent Protection Comparator Input. The current-sense signal is compared to a signal proportional to the error-amplifier output voltage.
4	R_T/C_T	Timing Resistor/Capacitor Connection. A resistor R_T from R_T/C_T to REF and capacitor C_T from R_T/C_T to GND set the oscillator frequency.
5	GND	Power-Supply Ground. Place the V_{CC} and REF bypass capacitors close to the IC to minimize ground loops.
6	OUT	MOSFET Driver Output. OUT connects to the gate of the external n-channel MOSFET.
7	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 0.1µF ceramic capacitor or a parallel combination of a 0.1µF and a higher value ceramic capacitor.
8	REF	5V Reference Output. Bypass REF to GND with a 0.1µF ceramic capacitor or a parallel combination of a 0.1µF and a higher value ceramic capacitor no larger then 4.7µF.

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Pin Descriptions (continued)

MAX5095_

PIN		NAME	FUNCTION
MAX5095A/ MAX5095B	MAX5095C		
1	1	COMP	Current Limit/PWM Comparator Input. COMP is level-shifted and connected to the inverting input of the PWM comparator. Pull up COMP to REF through a resistor and connect an optocoupler from COMP to GND for proper operation.
2	—	SYNC	Bidirectional Synchronization Input. When synchronizing with other MAX5095A/MAX5095Bs, the higher frequency part synchronizes all other devices.
—	2	ADV_CLK	Advance Clock Output. ADV_CLK is an 85ns clock output pulse preceding the rising edge of OUT (see Figure 4). Use the pulse to drive the secondary-side synchronous rectifiers through a pulse transformer or an optocoupler (see Figure 8).
3	3	CS	PWM Comparator/Overcurrent Protection Comparator Input. The current-sense signal is compared to the level shifted voltage at COMP.
4	4	R_T/C_T	Timing Resistor/Capacitor Connection. A resistor R_T from R_T/C_T to REF and capacitor C_T from R_T/C_T to GND set the oscillator frequency.
5	5	GND	Power-Supply Ground. Place the V_{CC} and REF bypass capacitors close to the IC to minimize ground loops.
6	6	OUT	MOSFET Driver Output. OUT connects to the gate of the external n-channel MOSFET.
7	7	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 0.1µF ceramic capacitor or a parallel combination of a 0.1µF and a higher value ceramic capacitor.
8	8	REF	5V Reference Output. Bypass REF to GND with a 0.1µF ceramic capacitor or a parallel combination of a 0.1µF and a higher value ceramic capacitor no larger than 4.7µF.

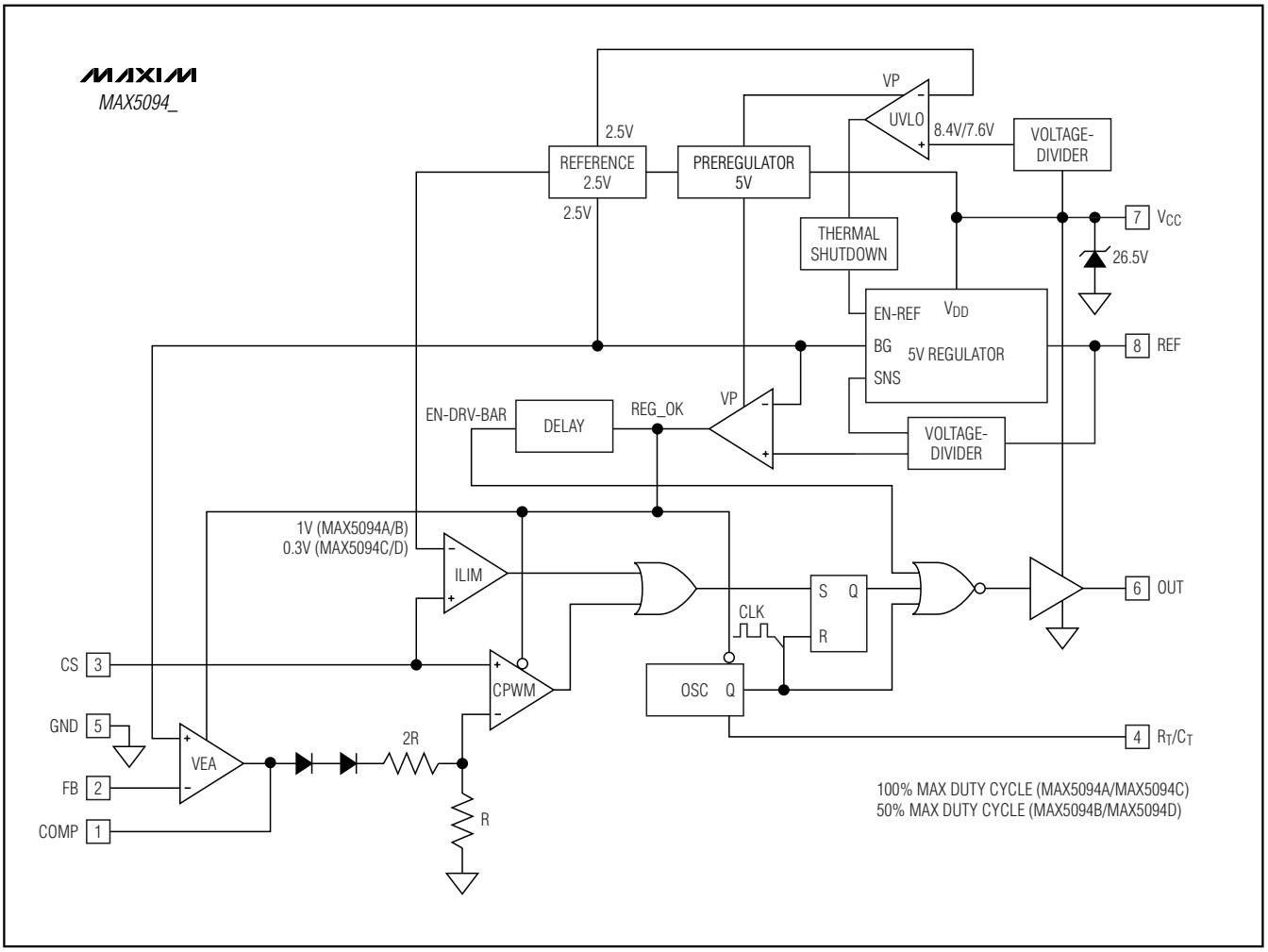


Figure 1. MAX5094_ Functional Diagram

Detailed Description

The MAX5094_/MAX5095_ current-mode PWM controllers are designed for use as the control and regulation core of flyback or forward topology switching power supplies. These devices incorporate an integrated low-side driver, adjustable oscillator, error amplifier (MAX5094_ only), current-sense amplifier, 5V reference, and external synchronization capability (MAX5095A/MAX5095B only). An internal +26.5V current-limited V_{CC} clamp prevents overvoltage during startup.

Eight different versions of the MAX5094/MAX5095 are available as shown in the Selector Guide. The MAX5094A/MAX5094B are the standard versions with a feedback input (FB) and internal error amplifier. The MAX5095A/MAX5095B include bidirectional synchronization (SYNC). This enables multiple MAX5095A/MAX5095Bs to be connected and synchronized to the device with the highest frequency. The MAX5095C includes an ADV_CLK output, which precedes the MAX5095C's drive output (OUT) by 110ns. Figures 1, 2, and 3 show the internal functional diagrams of the MAX5094_, MAX5095A/MAX5095B, and MAX5095C, respectively. The MAX5094A/MAX5094C/MAX5095A are capable of 100% maximum duty cycle. The MAX5094B/MAX5094D/MAX5095B/MAX5095C limit the maximum duty cycle to 50%.

High-Performance, Single-Ended, Current-Mode PWM Controllers

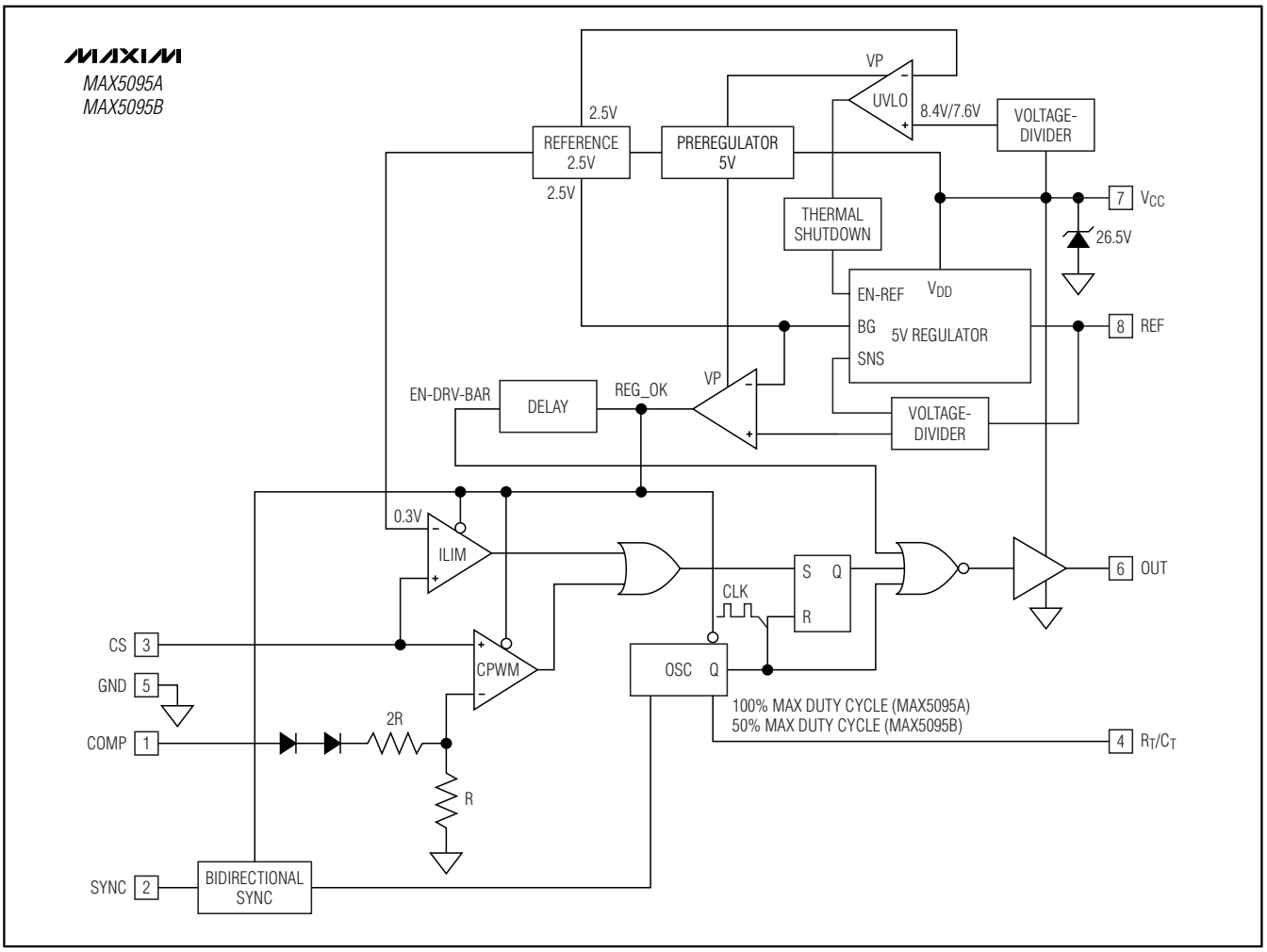


Figure 2. MAX5095A/B Functional Diagram

Current-Mode Control Loop

The advantages of current-mode control over voltage-mode control are twofold. First, there is the feed-forward characteristic brought on by the controller's ability to adjust for variations in the input voltage on a cycle-by-cycle basis. Secondly, the stability requirements of the current-mode controller are reduced to that of a single-pole system unlike the double pole in the voltage-mode control scheme.

The MAX5094/MAX5095 use a current-mode control loop where the output of the error amplifier is compared to the current-sense voltage (V_{CS}). When the current-sense signal is lower than the inverting input of the CPWM comparator, the output of the comparator is low and the switch is turned on at each clock pulse. When the current-sense signal is higher than the inverting input of the CPWM comparator, the output is high and the switch is turned off.

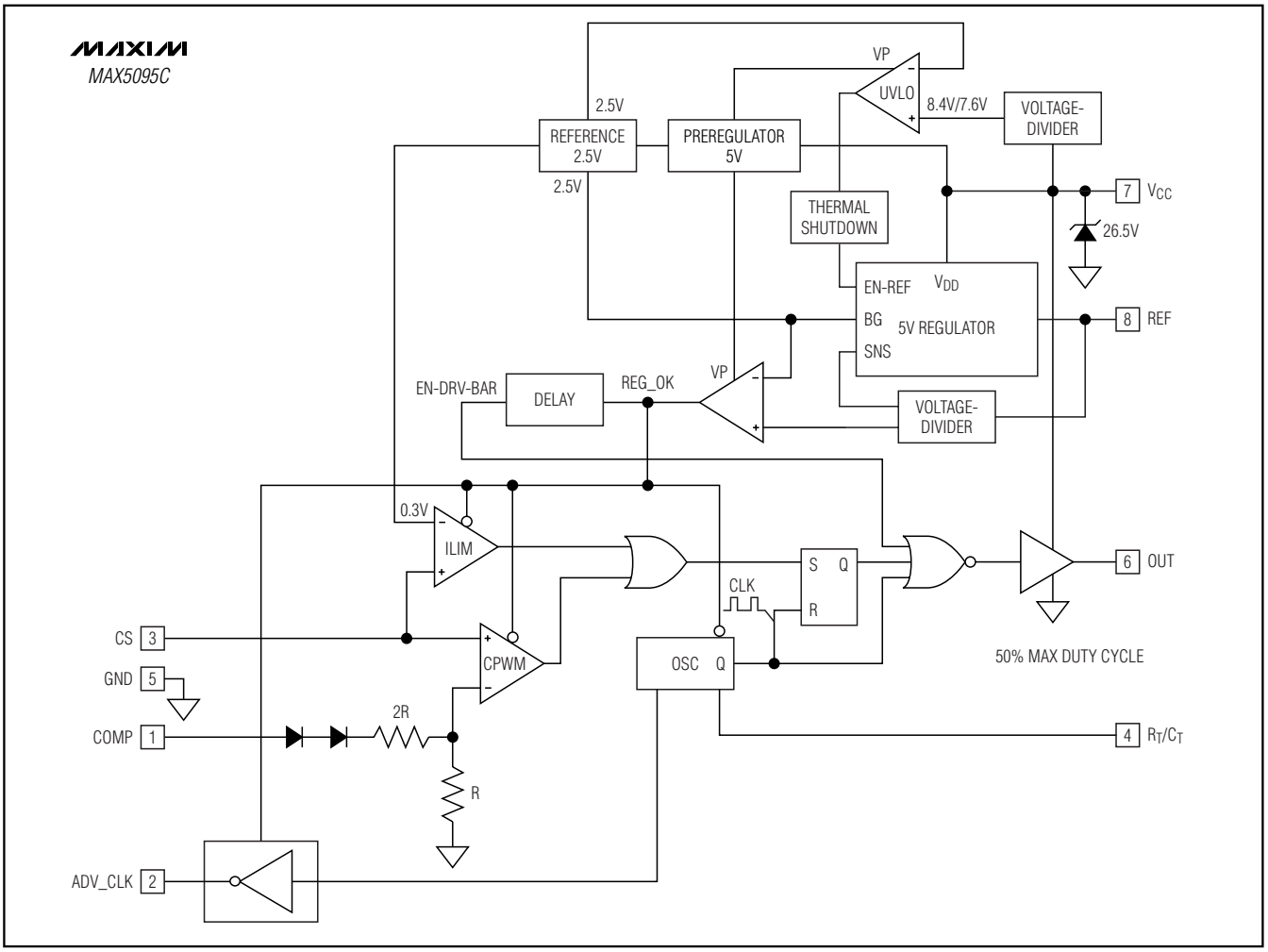


Figure 3. MAX5095C Functional Diagram

VCC and Startup

In normal operation, V_{CC} is derived from a tertiary winding of the transformer. However, at startup there is no energy delivered through the transformer, thus a resistor must be connected from V_{CC} to the input power source (see R_{ST} and C_{ST} in Figures 5 to 8). During startup, C_{ST} charges up through R_{ST}. The 5V reference generator, comparator, error amplifier, oscillator, and drive circuit remain off during UVLO to reduce startup current below 65µA. When V_{CC} reaches the undervoltage-lockout threshold of 8.4V, the output driver begins to switch and the tertiary winding supplies power to V_{CC}. V_{CC} has an internal 26.5V current-limited clamp at its input to protect the device from overvoltage during startup.

Size the startup resistor, R_{ST}, to supply both the maximum startup bias (I_{START}) of the device (65µA max) and the charging current for C_{ST}. The startup capacitor C_{ST} must charge to 8.4V within the desired time period t_{ST} (for example, 500ms). The size of the startup capacitor depends on:

1) IC operating supply current at a programmed oscillator frequency (f_{OSC}).
2) The time required for the bias voltage, derived from a bias winding, to go from 0 to 9V.
3) The MOSFET total gate charge.
4) The operating frequency of the converter (f_{SW}).

High-Performance, Single-Ended, Current-Mode PWM Controllers

To calculate the capacitance required, use the following formula:

$$C_{ST} = \frac{[I_{CC} + I_G](t_{SS})}{V_{HYST}}$$

where:

$$I_G = Q_G f_{SW}$$

I_{CC} is the MAX5094/MAX5095s' maximum internal supply current after startup (see the *Typical Operating Characteristics* to find the I_{IN} at a given f_{OSC}). Q_G is the total gate charge for the MOSFET, f_{SW} is the converter switching frequency, V_{HYST} is the bootstrap UVLO hysteresis (0.8V), and t_{SS} is the soft-start time, which is set by external circuitry.

Size the resistor R_{ST} according to the desired startup time period, t_{ST}, for the calculated C_{ST}. Use the following equations to calculate the average charging current (I_{CST}) and the startup resistor (R_{ST}):

$$I_{CST} = \frac{V_{SUVR} \times C_{ST}}{t_{ST}}$$

$$R_{ST} \cong \frac{\left(V_{INMIN} - \frac{V_{SUVR}}{2}\right)}{I_{CST} + I_{START}}$$

Where V_{INMIN} is the minimum input supply voltage for the application (36V for telecom), V_{SUVR} is the bootstrap UVLO wake-up level (8.4V), and I_{START} is the V_{IN} supply current at startup (65µA, max). Choose a higher value for R_{ST} than the one calculated above if longer startup times can be tolerated to minimize power loss in R_{ST}.

The equation for C_{ST} above gives a good approximation of C_{ST}, yet neglects the current through R_{ST}. Fine tune C_{ST} using:

$$C_{ST} = \left[\frac{I_{CC} + I_G - \left(\frac{V_{INMIN} - 8V}{R_{ST}}\right)}{V_{HYST}}\right](t_{SS})$$

The above startup method is applicable to circuits where the tertiary winding has the same phase as the output windings. Thus, the voltage on the tertiary winding at any given time is proportional to the output voltage and goes through the same soft-start period as the output voltage.

The minimum discharge time of C_{ST} from 8.4V to 7.6V must be greater than the soft-start time (t_{SS}).

Undervoltage Lockout (UVLO)

The minimum turn-on supply voltage for the MAX5094/MAX5095 is 8.4V. Once V_{CC} reaches 8.4V, the reference powers up. There is 0.8V of hysteresis from the minimum turn-on voltage to the UVLO threshold. Once V_{CC} reaches 8.4V, the MAX5094/MAX5095 operates with V_{CC} down to 7.6V. Once V_{CC} goes below 7.6V the device is in UVLO. When in UVLO, the quiescent supply current into V_{CC} falls back to 32µA (typ), and OUT and REF are pulled low.

MOSFET Driver

OUT drives an external n-channel MOSFET and swings from GND to V_{CC}. Ensure that V_{CC} remains below the absolute maximum V_{GS} rating of the external MOSFET. OUT is a push-pull output with the on-resistance of the PMOS typically 3.5Ω and the on-resistance of the NMOS typically 4.5Ω. The driver can source 2A typically and sink 1A typically. This allows for the MAX5094/MAX5095 to quickly turn on and off high gate-charge MOSFETs.

Bypass V_{CC} with one or more 0.1µF ceramic capacitors to GND, placed close to the MAX5094/MAX5095. The average current sourced to drive the external MOSFET depends on the total gate charge (Q_G) and operating frequency of the converter. The power dissipation in the MAX5094/MAX5095 is a function of the average output-drive current (I_{DRIVE}). Use the following equation to calculate the power dissipation in the device due to I_{DRIVE}:

$$I_{DRIVE} = Q_G \times f_{SW}$$

$$PD = (I_{DRIVE} + I_{CC}) \times V_{CC}$$

where, I_{CC} is the operating supply current. See the *Typical Operating Characteristics* for the operating supply current at a given frequency.

Error Amplifier (MAX5094)

The MAX5094 includes an internal error amplifier. The inverting input is at FB and the noninverting input is internally connected to a 2.5V reference. The internal error amplifier is useful for nonisolated converter design (see Figure 6) and isolated design with primary-side regulation through a bias winding (see Figure 5). In the case of a nonisolated power supply, the output voltage is:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times 2.5V$$

where, R1 and R2 are from Figure 6.

MAX5095_Feedback

The MAX5095A/MAX5095B/MAX5095C use either an external error amplifier when designed into a nonisolated converter or an error amplifier and optocoupler when designed into an isolated power supply. The COMP input is level-shifted and connected to the inverting terminal of the PWM comparator (CPWM). Connect the COMP input to the output of the external error amplifier for nonisolated design. Pull COMP high externally to 5V (or REF) and connect the optocoupler transistor as shown in Figures 7 and 8. COMP can be used for soft-start and also as a shutdown. See the *Typical Operating Characteristics* to find the turn-off COMP voltage at different temperatures.

Oscillator

The oscillator frequency is programmed by adding an external capacitor and resistor at R_T/C_T (see R_T and C_T in the *Typical Application Circuits*). R_T is connected from R_T/C_T to the 5V reference (REF) and C_T is connected from R_T/C_T to GND. REF charges C_T through R_T until its voltage reaches 2.8V. C_T then discharges through an 8.3mA internal current sink until C_T's voltage reaches 1.1V, at which time C_T is allowed to charge through R_T again. The oscillator's period will be the sum of the charge and discharge times of C_T. Calculate the charge time as

$$t_C = 0.57 \times R_T \times C_T$$

The discharge time is then

$$t_D = \frac{R_T \times C_T \times 10^3}{4.88 \times R_T - 1.8 \times 10^3}$$

The oscillator frequency will then be

$$f_{OSC} = \frac{1}{t_C + t_D}$$

For the MAX5094A/MAX5094C/MAX5095A, the converter output switching frequency (f_{SW}) is the same as the oscillator frequency (f_{OSC}). For the MAX5094B/MAX5094D/MAX5095B/MAX5095C, the output switching frequency is 1/2 the oscillator frequency.

Reference Output

REF is a 5V reference output that can source 20mA. Bypass REF to GND with a 0.1µF capacitor.

Current Limit

The MAX5094/MAX5095 include a fast current-limit comparator to terminate the ON cycle during an overload or a fault condition. The current-sense resistor (R_{CS}), connected between the source of the MOSFET and GND, sets the current limit. The CS input has a voltage trip level (V_{CS}) of 1V (MAX5094A/B) or 0.3V (MAX5094C/D, MAX5095_). Use the following equation to calculate R_{CS}:

$$R_{CS} = \frac{V_{CS}}{I_{P-P}}$$

I_{P-P} is the peak current in the primary that flows through the MOSFET. When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (OUT) will turn the switch off within 60ns. In most cases, a small RC filter is required to filter out the leading-edge spike on the sense waveform. Set the time constant of the RC filter at 50ns. Use a current transformer to limit the losses in the current-sense resistor and achieve higher efficiency especially at low input-voltage operation.

Synchronization (MAX5095A/MAX5095B)

SYNC

SYNC is a bidirectional input/output that outputs a synchronizing pulse and accepts a synchronizing pulse from other MAX5095A/MAX5095Bs (see Figures 7 and 9). As an output, SYNC is an open-drain p-channel MOSFET driven from the internal oscillator and requires an external pulldown resistor (R_{SYNC}) between 500Ω and 5kΩ. As an input, SYNC accepts the output pulses from other MAX5095A/MAX5095Bs.

Synchronize multiple MAX5095A/MAX5095Bs by connecting their SYNC pins together. All devices connected together will synchronize to the one operating at the highest frequency. The rising edge of SYNC will precede the rising edge of OUT by approximately the discharge time (t_D) of the oscillator (see the *Oscillator* section). The pulse width of the SYNC output is equal to the time required to discharge the stray capacitance at SYNC through R_{SYNC} plus the C_T discharge time t_D. Adjust R_T/C_T such that the minimum discharge time t_D is 200ns.

High-Performance, Single-Ended, Current-Mode PWM Controllers

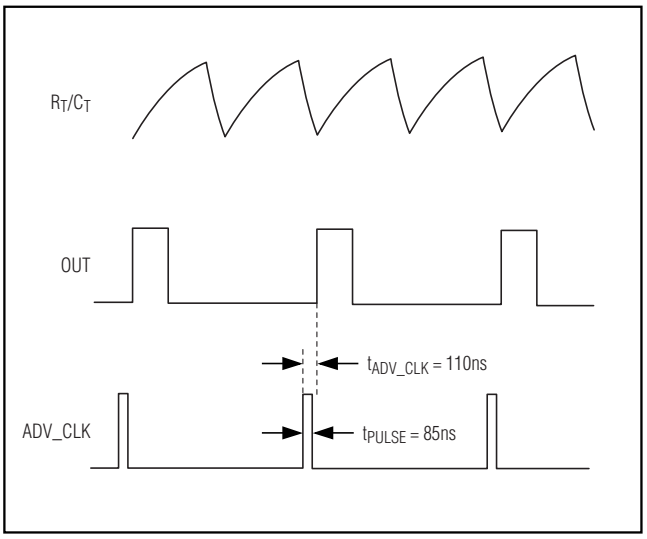


Figure 4. ADV_CLK

Advance Clock Output (ADV_CLK) (MAX5095C)

ADV_CLK is an advanced pulse output provided to facilitate the easy implementation of secondary-side synchronous rectification using the MAX5095C. The ADV_CLK pulse width is 85ns (typically) with its rising edge leading the rising edge of OUT by 110ns. Use this leading pulse to turn off the secondary-side synchronous-rectifier MOSFET (QS) before the voltage appears on the secondary (see Figure 8). Turning off the secondary-side synchronous MOSFET earlier avoids the shorting of the secondary in the forward converter. The ADV_CLK pulse can be propagated to the secondary side using a pulse transformer or high-speed optocoupler. The 85ns pulse, with 3V drive voltage (10mA source), significantly reduces the volt-second requirement of the pulse transformer and the advanced pulse alleviates the need for a high-speed optocoupler.

Thermal Shutdown

When the MAX5094/MAX5095's die temperature goes above +150°C, the thermal shutdown circuitry will shut down the 5V reference and pull OUT low.

Typical Application Circuits

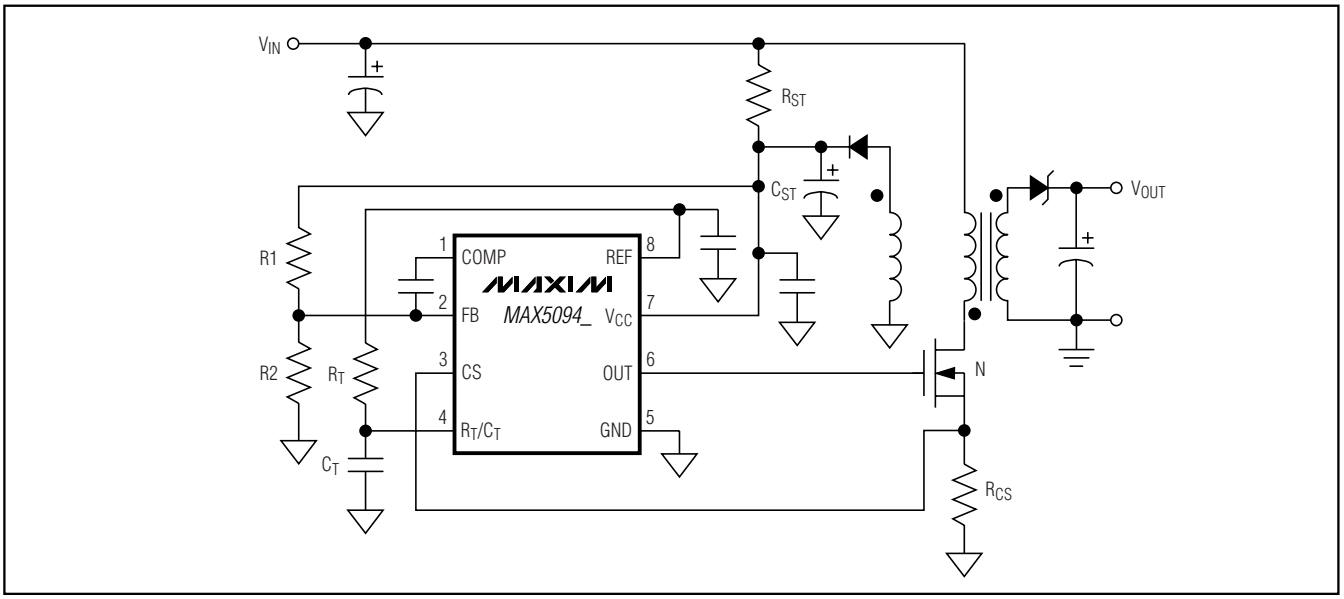


Figure 5. MAX5094_ Typical Application Circuit (Isolated Flyback with Primary-Side Regulation)

Typical Application Circuits (continued)

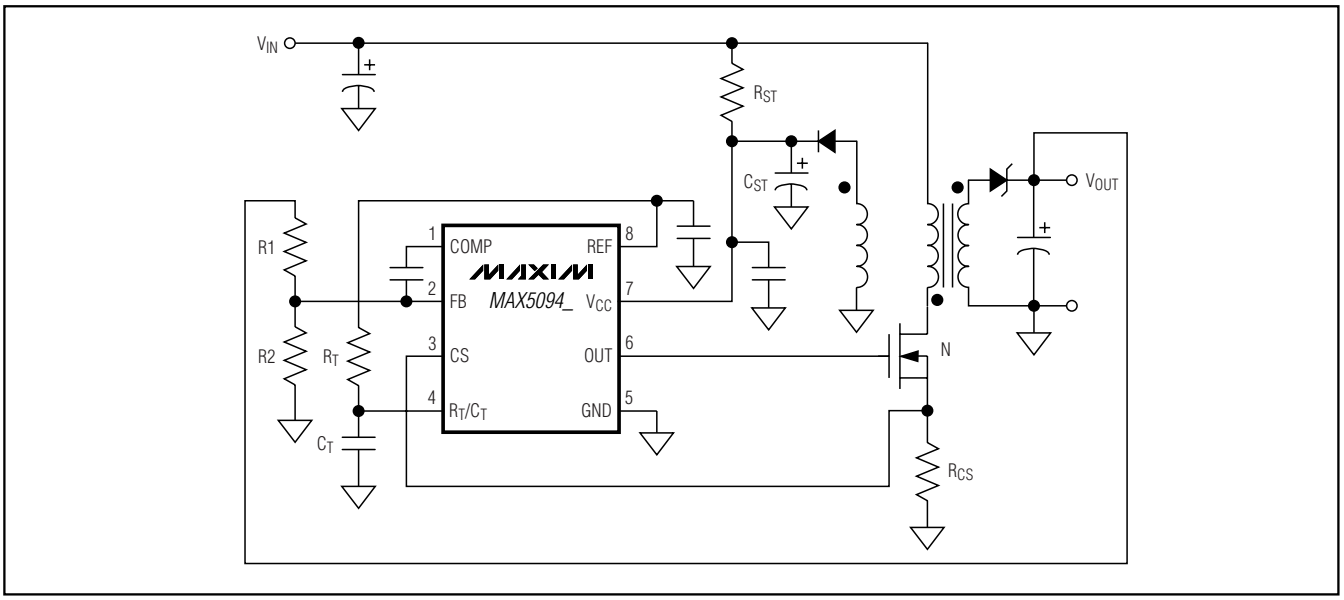


Figure 6. MAX5094_ Typical Application Circuit (Nonisolated Flyback)

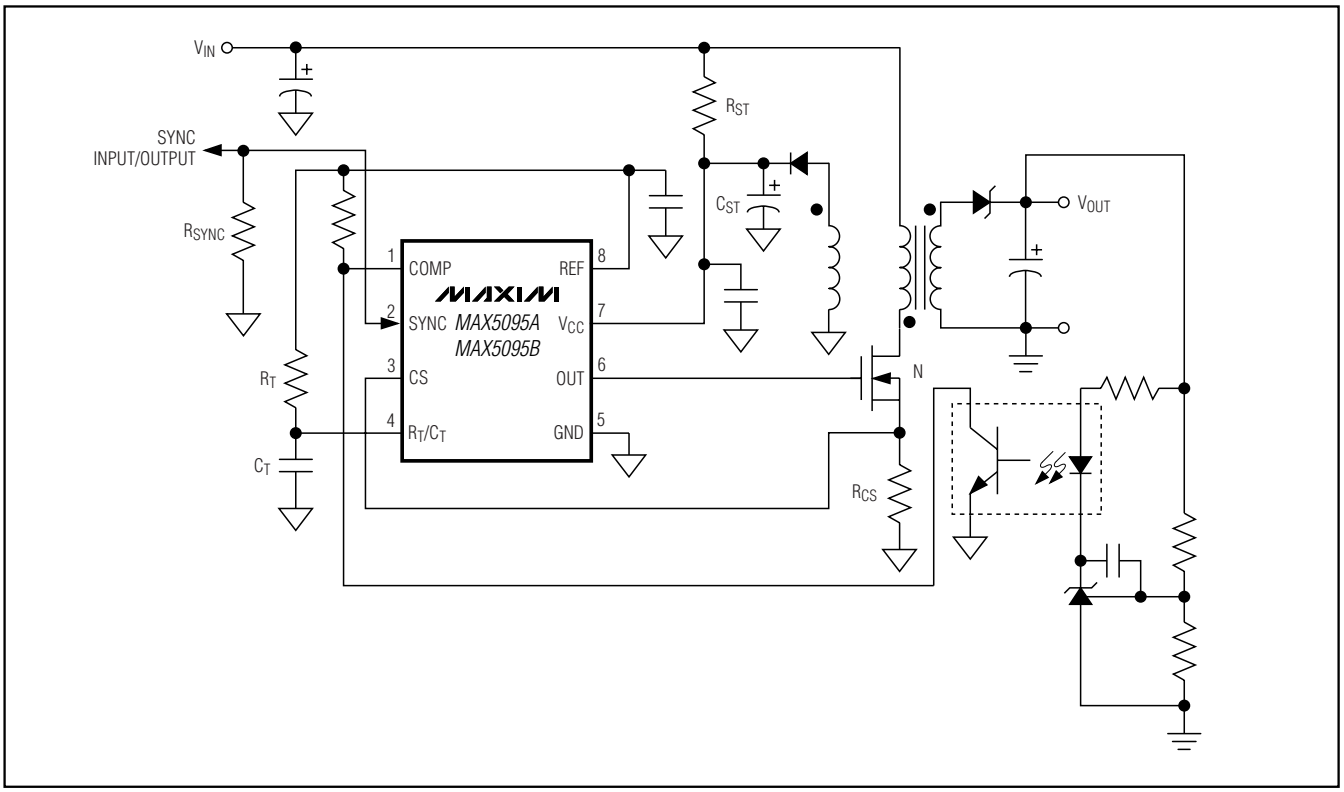


Figure 7. MAX5095A/MAX5095B Typical Application Circuit (Isolated Flyback)

High-Performance, Single-Ended, Current-Mode PWM Controllers

Typical Application Circuits (continued)

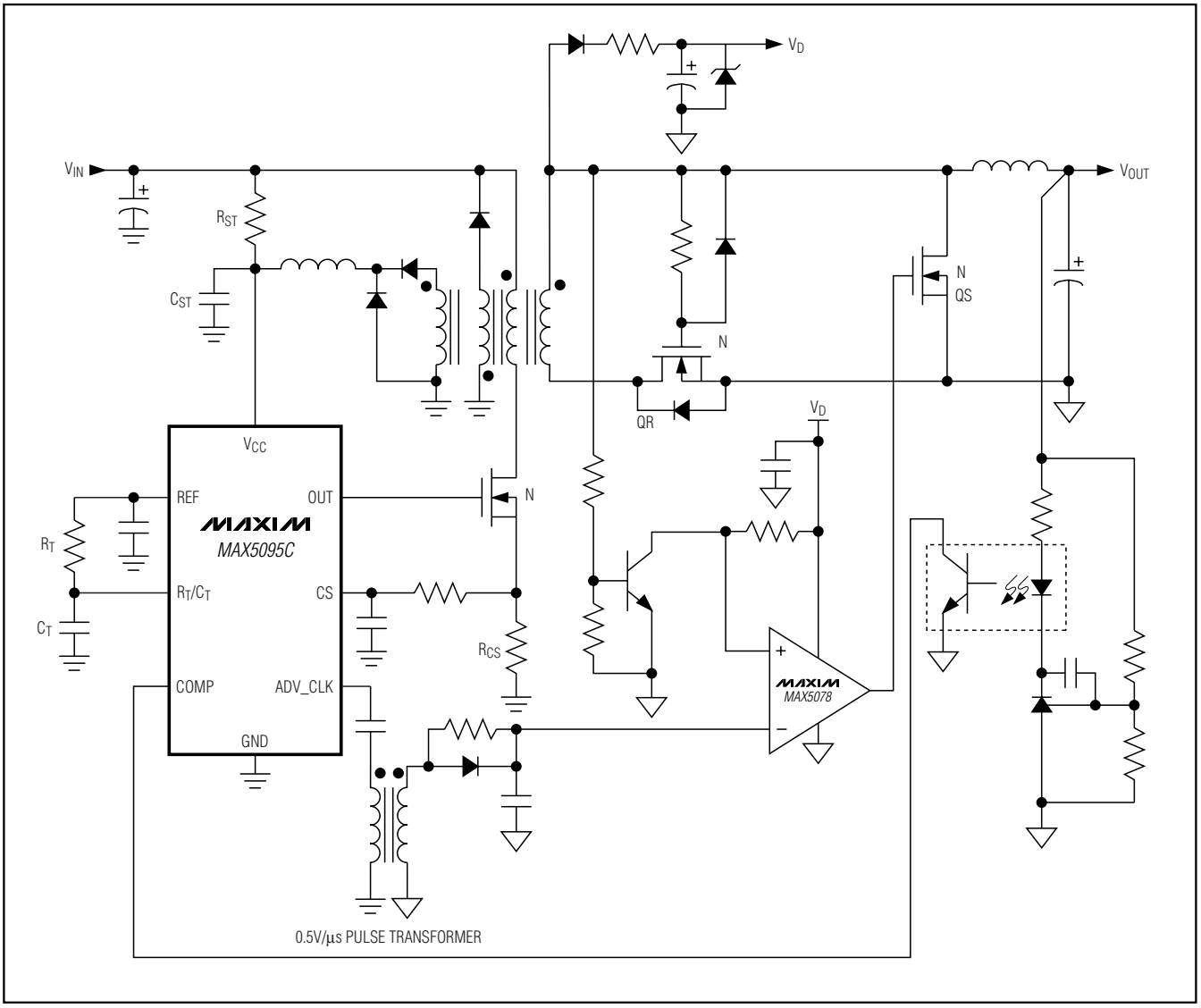


Figure 8. MAX5095C Typical Application Circuit (Isolated Forward with Secondary-Side Synchronous Rectification)

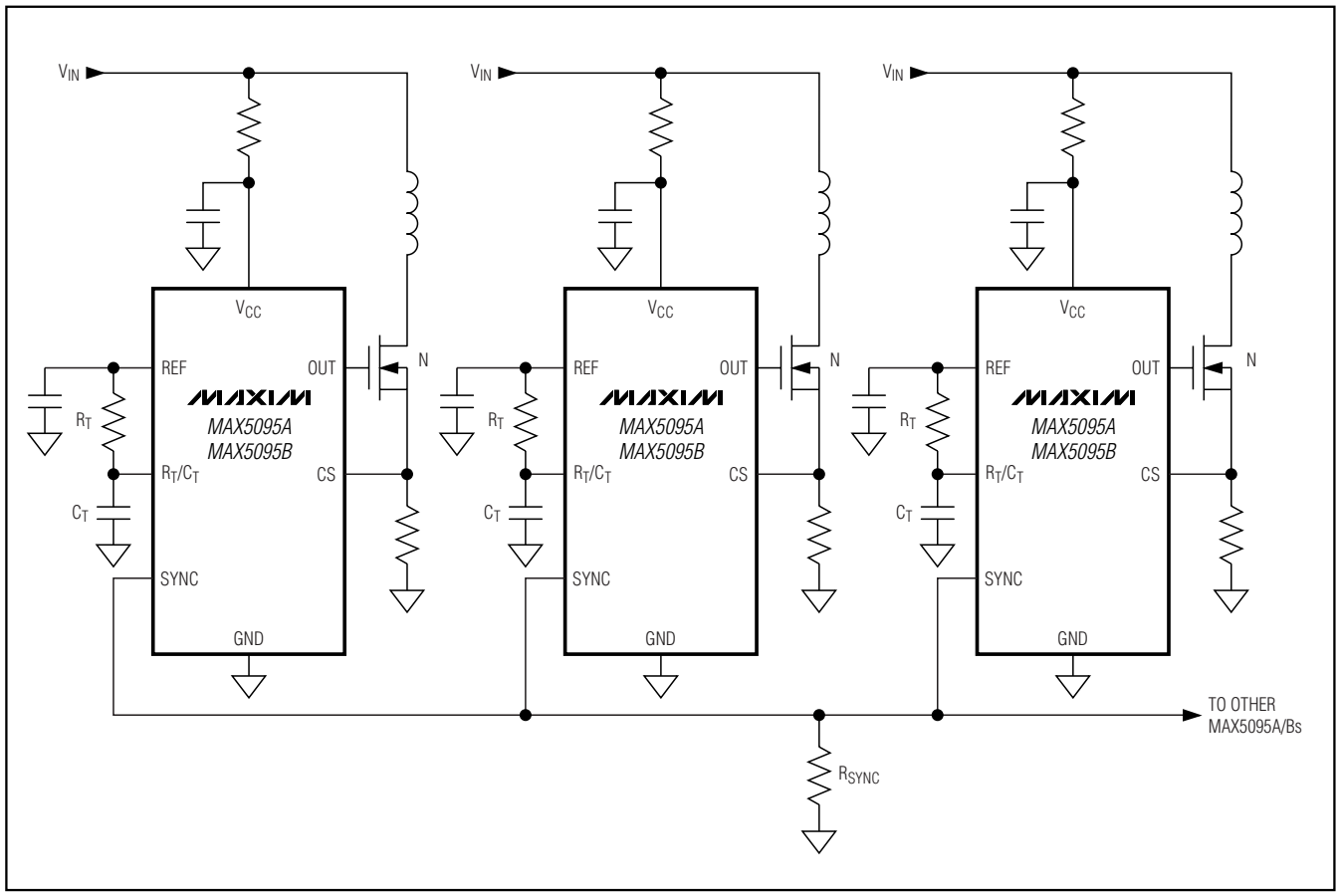


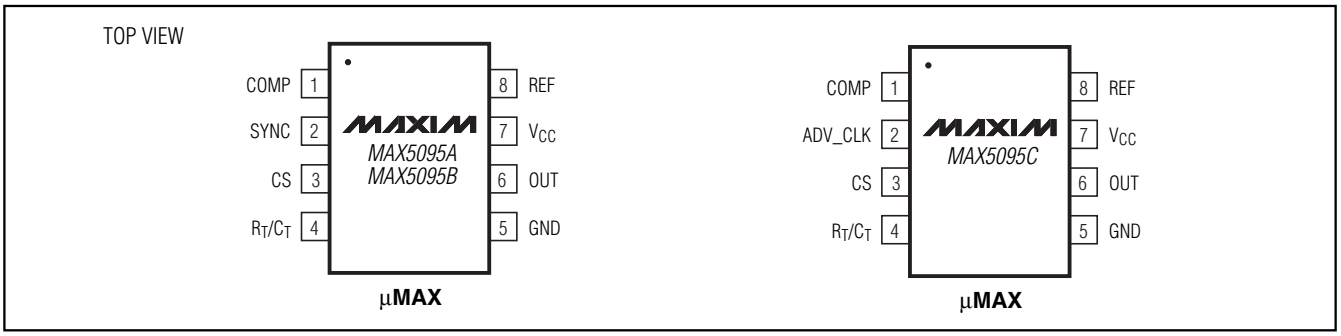
Figure 9. Synchronization of MAX5095A/MAX5095B

High-Performance, Single-Ended, Current-Mode PWM Controllers

Selector Guide

PART	FEATURE	UVLO THRESHOLD (V)	CS THRESHOLD (V)	MAX DUTY CYCLE (%)	COMPETITORS PART NUMBER	PIN-PACKAGE
MAX5094AASA	Feedback	8.4	1	100	UCC28C43 2nd source	8 SO
MAX5094AAUA	Feedback	8.4	1	100	UCC28C43 2nd source	8 µMAX
MAX5094BASA	Feedback	8.4	1	50	UCC28C45 2nd source	8 SO
MAX5094BAUA	Feedback	8.4	1	50	UCC28C45 2nd source	8 µMAX
MAX5094CASA	Feedback	8.4	0.3	100	Improved UCC28C43	8 SO
MAX5094CAUA	Feedback	8.4	0.3	100	Improved UCC28C43	8 µMAX
MAX5094DAUA	Feedback	8.4	0.3	50	Improved UCC28C45	8 µMAX
MAX5095AAUA	Sync	8.4	0.3	100	Improved UCC28C43	8 µMAX
MAX5095BAUA	Sync	8.4	0.3	50	Improved UCC28C45	8 µMAX
MAX5095CAUA	ADV_CLK	8.4	0.3	50	Improved UCC28C45	8 µMAX

Pin Configurations (continued)



Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5094CASA*	-40°C to +125°C	8 SO	S8-4
MAX5094CASA+	-40°C to +125°C	8 SO	S8-4
MAX5094CAUA*	-40°C to +125°C	8 µMAX	U8-1
MAX5094CAUA+	-40°C to +125°C	8 µMAX	U8-1
MAX5094DAUA*	-40°C to +125°C	8 µMAX	U8-1
MAX5094DAUA+	-40°C to +125°C	8 µMAX	U8-1
MAX5095AAUA	-40°C to +125°C	8 µMAX	U8-1
MAX5095AAUA+*	-40°C to +125°C	8 µMAX	U8-1
MAX5095BAUA*	-40°C to +125°C	8 µMAX	U8-1
MAX5095BAUA+	-40°C to +125°C	8 µMAX	U8-1
MAX5095CAUA*	-40°C to +125°C	8 µMAX	U8-1
MAX5095CAUA+	-40°C to +125°C	8 µMAX	U8-1

+Denotes lead-free package.

**Future product—contact factory for availability.*

Chip Information

TRANSISTOR COUNT: 1987

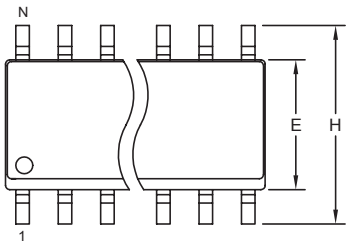
PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICN .EPS

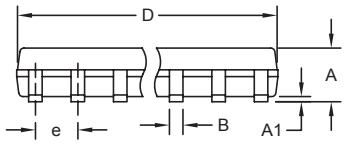
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



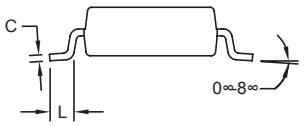
TOP VIEW

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

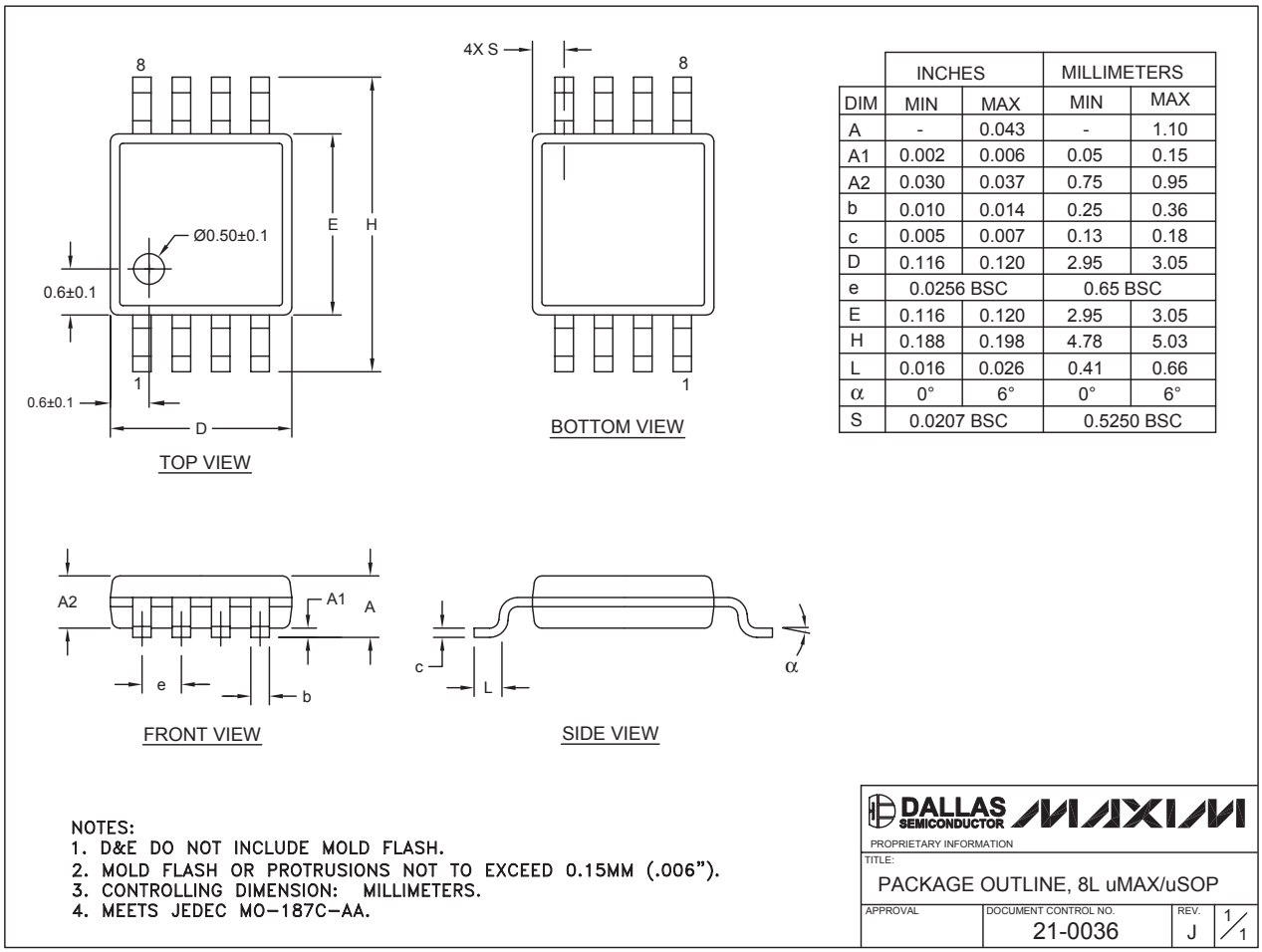
TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

High-Performance, Single-Ended, Current-Mode PWM Controllers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	