500mA LDO Linear Regulators with Current-Limiting Switch

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, $\overline{FLAG}$, OUT to GND .....-0.3V to +6V
$\overline{RESET}$ to GND .....-0.3V to (V_{OUT} + 0.3V)
SS to GND .....-0.3V to (V_{IN} + 0.3V)
IN to OUT .....±6V
OUT Short Circuit to GND .....Continuous
All Pins ESD Handling (Human Body Model).....2kV

Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 9.1mW/°C above +70°C).....727mW
6-Pin TDFN (derate 24.4mW/°C above +70°C) 1951.2mW
Operating Temperature Range .....-40°C to +85°C
Operating Junction Temperature Range.....-40°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{OUT} + 1V, $\overline{SHDN}$ = IN, C_{OUT} = 3.3µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage	V_{IN}			2.5		5.5	V
Input Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} rising		2.00		2.25	V
Input Undervoltage Lockout Threshold Hysteresis					50		mV
Quiescent Current	I_Q	$\overline{SHDN}$ = IN, I_{OUT} = 0			90	150	µA
		$\overline{SHDN}$ = IN, I_{OUT} = 0, V_{UVLO} < V_{IN} < V_{OUT} (nominal)			150		
		$\overline{SHDN}$ = GND, I_{OUT} = 0			0.1	2	
Dropout Voltage (Note 2)		I_{OUT} = 500mA	T_A = +25°C		200	300	mV
			T_A = -40°C to +85°C			330	
Output Voltage Accuracy		I_{OUT} = 1mA to 500mA, T_A = +25°C		-1.3		+1.3	%V_{NOM}
		I_{OUT} = 1mA to 500mA, T_A = -40°C to +85°C		-2		+2	
Output Current	I_{OUT}			500			mA
Output Current Limit		V_{OUT} = 0V		540		660	mA
Reverse Current at V_{IN}		V_{OUT} = 5.5V, V_{IN} = 0V to V_{OUT}			0.1	2	µA
Soft-Start Time (Note 3)	t_{SS}	C_{SS} = not connected		0.5	1	2.0	ms
		C_{SS} = 0.01µF		4	10	15	
		C_{SS} = 0.1µF		40	100	150	
Line Regulation (Note 4)		V_{OUT} + 0.5V < V_{IN} < 5.5V, I_{LOAD} = 100µA	T_A = +25°C	-0.04	+0.02	+0.065	%V_{NOM}/V
			T_A = -40°C to +85°C	-0.05	+0.03	+0.08	
Load Regulation		100µA < I_{LOAD} < 500mA, V_{IN} = V_{OUT} + 1V			1.3		%V_{NOM}
Output Noise		10Hz to 100kHz, C_{SS} = 0.01µF			70		µV_{RMS}
SHUTDOWN INPUT ($\overline{SHDN}$)							
OUT Discharge Resistance in Shutdown (MAX4837)		$\overline{SHDN}$ = GND			900		Ω
$\overline{SHDN}$ Input-Voltage High	V_{IH}			1.4			V
$\overline{SHDN}$ Input-Voltage Low	V_{IL}					0.5	V
$\overline{SHDN}$ Input Hysteresis					30		mV
$\overline{SHDN}$ Input Leakage Current		$\overline{SHDN}$ = IN or GND		-100		+100	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{OUT} + 1V, $\overline{SHDN}$ = IN, C_{OUT} = 3.3µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RESET}$ OUTPUT (MAX4837)						
$\overline{RESET}$ Threshold	$V_{\overline{RESET}}$		0.85 x V_{OUT}	0.875 x V_{OUT}	0.90 x V_{OUT}	V
OUT Drop to RESET Delay (Note 5)	t_{OR}			35		µs
$\overline{RESET}$ Timeout Period	$t_{\overline{RESET}}$	D1 timing option	2.5	3.75	5.0	ms
		D2 timing option	20	30	40	
		D3 timing option	150	225	300	
		D4 timing option	1200	1800	2400	
$\overline{RESET}$ Output-Voltage Low		V_{OUT} ≥ 1.0V, I_{SINK} = 50µA, $\overline{RESET}$ asserted			0.3	V
		V_{OUT} ≥ 1.5V, I_{SINK} = 3.2mA, $\overline{RESET}$ asserted			0.4	
$\overline{RESET}$ Output-Voltage High		V_{OUT} ≥ 2.0V, I_{SOURCE} ≤ 500µA, $\overline{RESET}$ deasserted	0.8 x V_{OUT}			V
$\overline{FLAG}$ OUTPUT (MAX4836)						
Blanking Time (Note 6)	t_{BLANK}	V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V, OUT = GND	5	10	17	ms
Open-Drain $\overline{FLAG}$ Output-Voltage Low		I_{SINK} = 3.2mA, $\overline{FLAG}$ asserted, V_{OUT} ≥ 1.5V			0.4	V
Open-Drain $\overline{FLAG}$ Leakage Current		$V_{\overline{FLAG}}$ = 5.5V		0.01	1	µA
THERMAL PROTECTION						
Thermal-Shutdown Temperature		Junction temperature rising		+165		°C
Thermal-Shutdown Hysteresis				15		°C

Note 1: Parts are 100% tested at +25°C. Limits across the full temperature range are guaranteed by design and correlation over the specified temperature range.

Note 2: The dropout voltage is measured from V_{IN} to V_{OUT} when V_{OUT} is 2% below its nominal value. The nominal output voltage is measured from V_{OUT} to GND when V_{IN} is 1V greater than V_{OUT}. Defined only for V_{OUT} ≥ 2.5V.

Note 3: Soft-start time is defined as the time required for the output to rise from 10% of its nominal value to 90% of its nominal value.

Note 4: For V_{OUT} < 2V, V_{IN} must be above 2.5V.

Note 5: This is the maximum time OUT can be out of tolerance before a reset is issued. It is implemented to ensure that momentary output glitches do not trigger a reset condition.

Note 6: In startup mode, the blanking time counter is not started until the soft-start time has elapsed. The total time from startup to $\overline{FLAG}$ issued is t_{SS} + t_{BLANK}.

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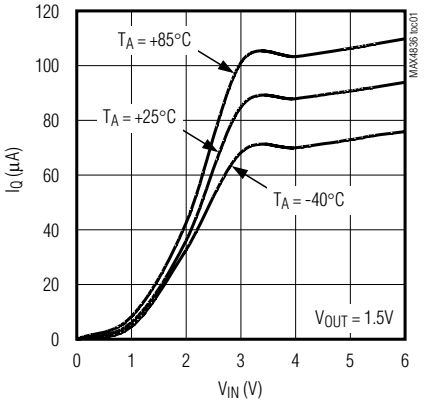
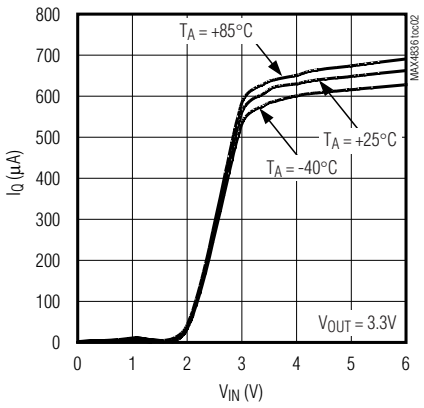
Typical Operating Characteristics

(V_{IN} = V_{OUT} + 1V, $\overline{SHDN}$ = IN, C_{OUT} = 3.3µF, T_A = +25°C, unless otherwise noted.)

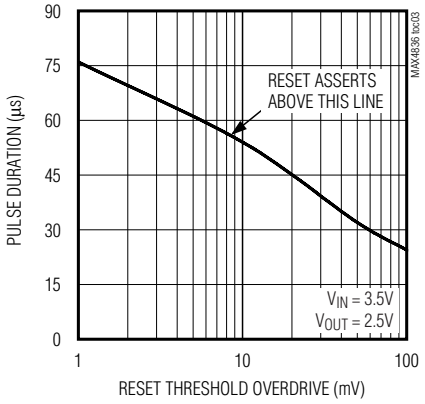
QUIESCENT CURRENT vs. INPUT VOLTAGE (NO LOAD)



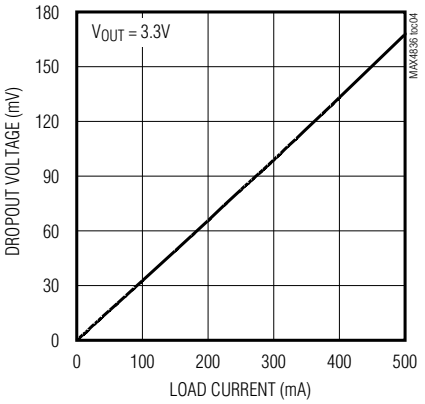
QUIESCENT CURRENT vs. INPUT VOLTAGE (500mA LOAD)



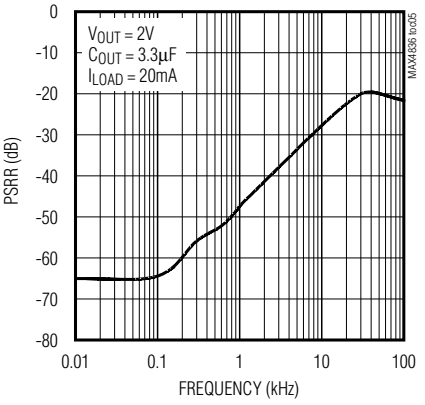
MAXIMUM TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



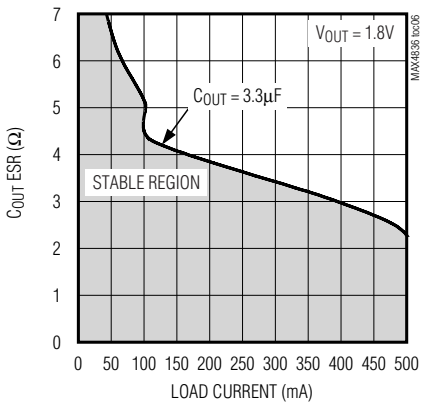
DROPOUT VOLTAGE vs. LOAD CURRENT



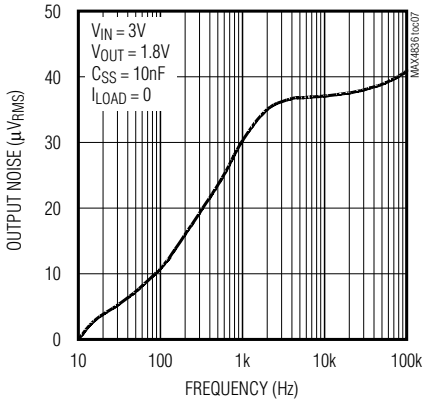
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



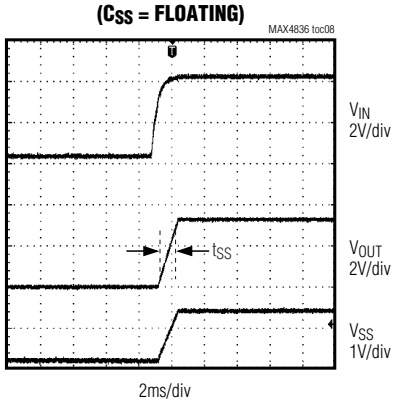
REGION OF STABLE C_{OUT} ESR vs. LOAD CURRENT



OUTPUT NOISE vs. FREQUENCY



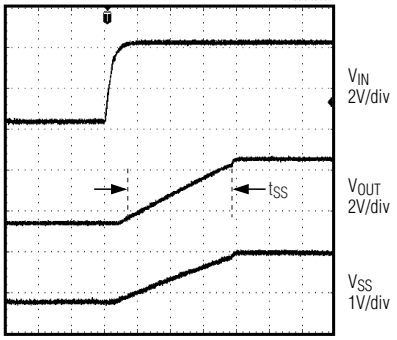
SOFT-START RESPONSE (C_{SS} = FLOATING)



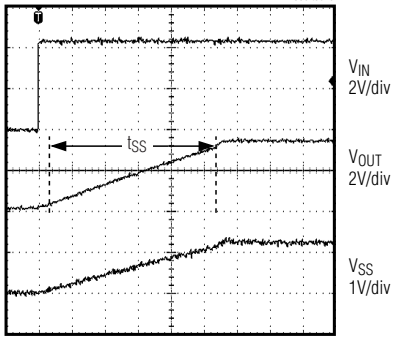
Typical Operating Characteristics (continued)

(V_{IN} = V_{OUT} + 1V, $\overline{SHDN}$ = IN, C_{OUT} = 3.3µF, T_A = +25°C, unless otherwise noted.)

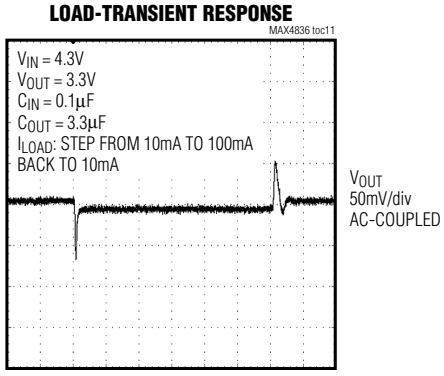
SOFT-START RESPONSE (C_{SS} = 0.01µF)



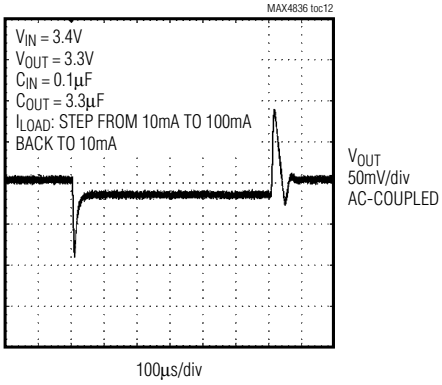
SOFT-START RESPONSE (C_{SS} = 0.1µF)



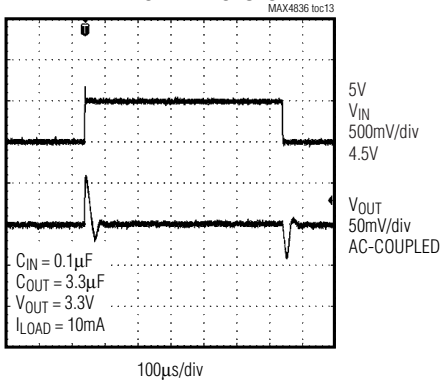
LOAD-TRANSIENT RESPONSE



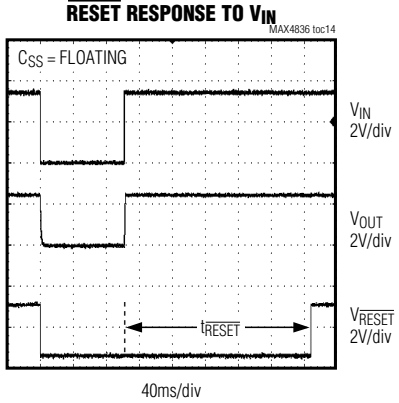
LOAD-TRANSIENT RESPONSE NEAR DROPOUT



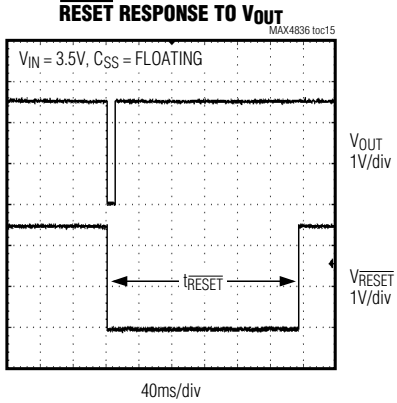
LINE-TRANSIENT RESPONSE



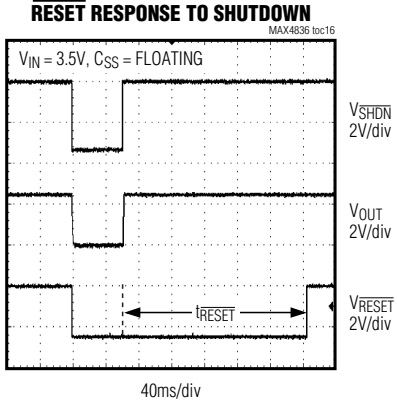
$\overline{RESET}$ RESPONSE TO V_{IN}



$\overline{RESET}$ RESPONSE TO V_{OUT}



$\overline{RESET}$ RESPONSE TO SHUTDOWN

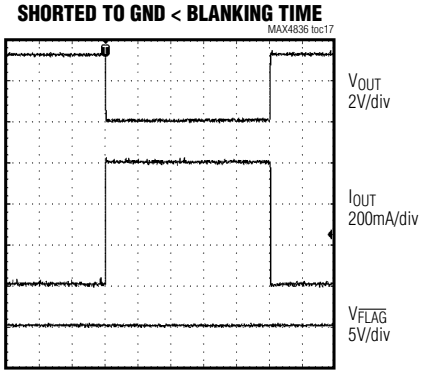


500mA LDO Linear Regulators with Current-Limiting Switch

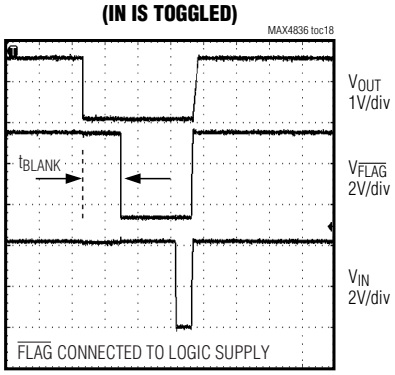
Typical Operating Characteristics (continued)

(V_{IN} = V_{OUT} + 1V, $\overline{SHDN}$ = IN, C_{OUT} = 3.3µF, T_A = +25°C, unless otherwise noted.)

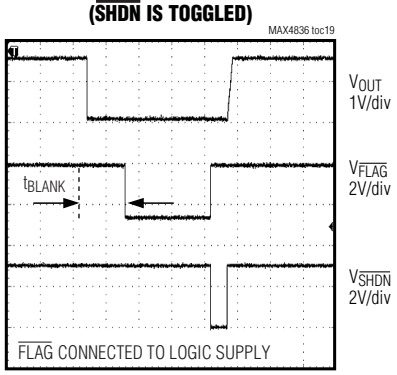
$\overline{FLAG}$ RESPONSE WHEN OUT IS SHORTED TO GND < BLANKING TIME



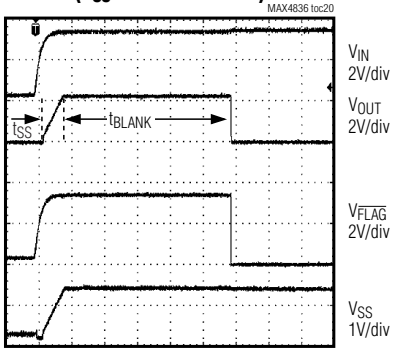
$\overline{FLAG}$ RESPONSE WHEN OUT IS SHORTED TO GND > BLANKING TIME (IN IS TOGGLED)



$\overline{FLAG}$ RESPONSE WHEN OUT IS SHORTED TO GND > BLANKING TIME ($\overline{SHDN}$ IS TOGGLED)

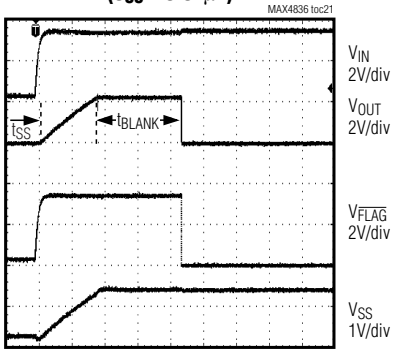


STARTUP IN AN OVERLOAD CONDITION (C_{SS} NOT CONNECTED)



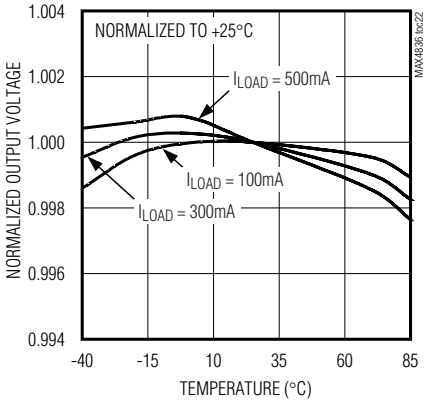
V_{OUT} = 2.5V
I_{LOAD} = I_{LIMIT} MAXIMUM
$\overline{FLAG}$ CONNECTED TO LOGIC SUPPLY

STARTUP IN AN OVERLOAD CONDITION (C_{SS} = 0.01µF)



V_{OUT} = 2.5V
I_{LOAD} = I_{LIMIT} MAXIMUM
$\overline{FLAG}$ CONNECTED TO LOGIC SUPPLY

NORMALIZED OUTPUT VOLTAGE vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
SOT23	TDFN		
1	1	IN	Regulator Power Input. Bypass IN to GND with a 0.1µF ceramic capacitor. Install the bypass capacitor as close to the device as possible.
2	2	GND	Ground
3	3	$\overline{SHDN}$	Active-Low Shutdown Input. Drive $\overline{SHDN}$ low to shutdown the regulator. Drive $\overline{SHDN}$ high or connect to IN for normal operation.
4	4	$\overline{FLAG}$ (MAX4836)	Overcurrent Flag. Open-drain $\overline{FLAG}$ goes low when the device senses sustained current exceeding the current-limit threshold for a duration longer than the blanking time. $\overline{FLAG}$ is high when $\overline{SHDN}$ is low or the device is in thermal shutdown.
		$\overline{RESET}$ (MAX4837)	Active-Low Reset Output. Push-pull $\overline{RESET}$ goes low when the voltage at OUT is below the reset threshold or when the voltage at OUT is greater than IN. $\overline{RESET}$ is low when $\overline{SHDN}$ is low or the device is in thermal shutdown. After the reset condition terminates, $\overline{RESET}$ remains low for the duration of the reset timeout period.
5	5	SS	Soft-Start Control. Connect a capacitor, C_{SS}, from SS to GND to program the output rise time at startup. No capacitor from SS to GND gives 1ms output rise time at startup. See the soft-start response time plots in the *Typical Operating Characteristics*.
6	6	OUT	Regulator Output. Bypass OUT to GND with a 3.3µF or larger ceramic capacitor. The capacitor's ESR should be less than 0.2Ω for stable operation.
—	EP	EP	Exposed Pad. EP is internally connected to GND. Externally connect EP to GND to provide a low thermal resistance path from the IC junction to the PC board.

Detailed Description

The MAX4836/MAX4837 are ultra-low quiescent current, low-dropout linear regulators with an integrated current limiter. These devices guarantee up to 500mA drive capabilities and regulate the preset output voltage.

The MAX4836 has a flag output that asserts low when the load current exceeds the current limit for more than the blanking time ($t_{\overline{BLANK}}$). The MAX4837 has a reset output that asserts low when the regulator output voltage is below the reset threshold voltage ($V_{\overline{RESET}}$). $V_{\overline{RESET}}$ is 87.5% of the nominal output voltage. Figure 1 shows the simplified functional diagram and Figure 2 shows the typical application circuits.

$\overline{FLAG}$ Output (MAX4836)

The open-drain $\overline{FLAG}$ output goes low and the LDO's pass transistor is latched off when the current in the pass transistor is at its output current limit for more than the blanking time (t_{BLANK}). Cycling IN or $\overline{SHDN}$ (high to low to high) brings the device out of its latched-off state and back into normal operation.

$\overline{RESET}$ Output (MAX4837)

The $\overline{RESET}$ output asserts when one of the following conditions occurs:

- The input voltage (V_{IN}) is below the input undervoltage lockout threshold (V_{UVLO}).
- The output voltage (V_{OUT}) is below the reset threshold ($V_{\overline{RESET}}$).
- $\overline{SHDN}$ is pulled low.
- The device is in thermal shutdown.
- When $V_{OUT} > V_{IN}$.

$\overline{RESET}$ remains low for the reset timeout period (t_{RESET}) after reset conditions are terminated. There are four $\overline{RESET}$ timeout periods available as shown in the *Electrical Characteristics* table. $\overline{RESET}$ is available in a push-pull configuration as shown in the *Selector Guide*.

Shutdown

Pull $\overline{SHDN}$ low to shut down the LDO and reduce the quiescent current consumption of the device from 90µA to 0.1µA. In shutdown mode, the pass transistor, control circuit, and reference circuit are turned off. Connect $\overline{SHDN}$ to a supply voltage greater than V_{IH} to turn on the LDO.

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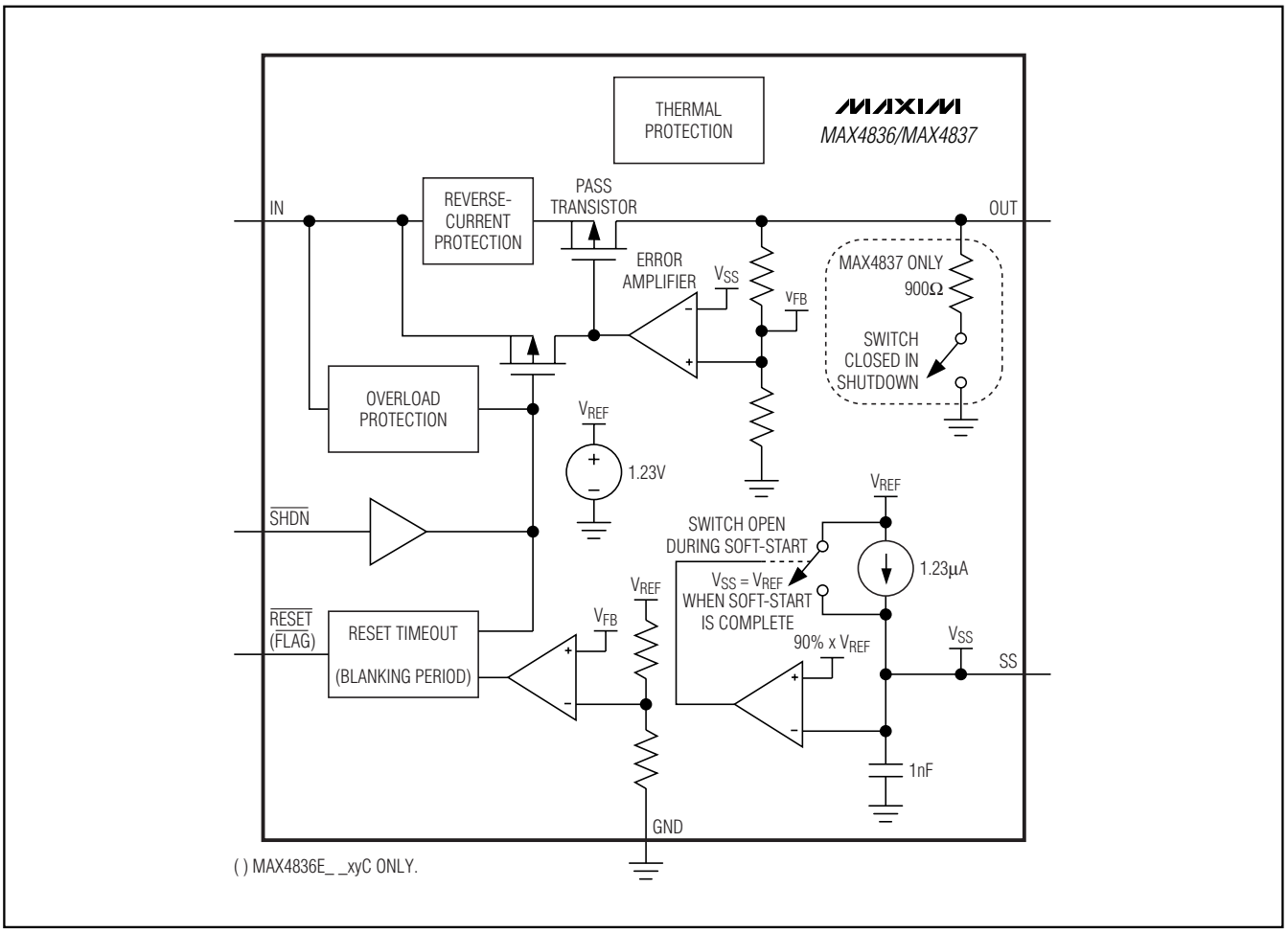


Figure 1. Functional Diagram

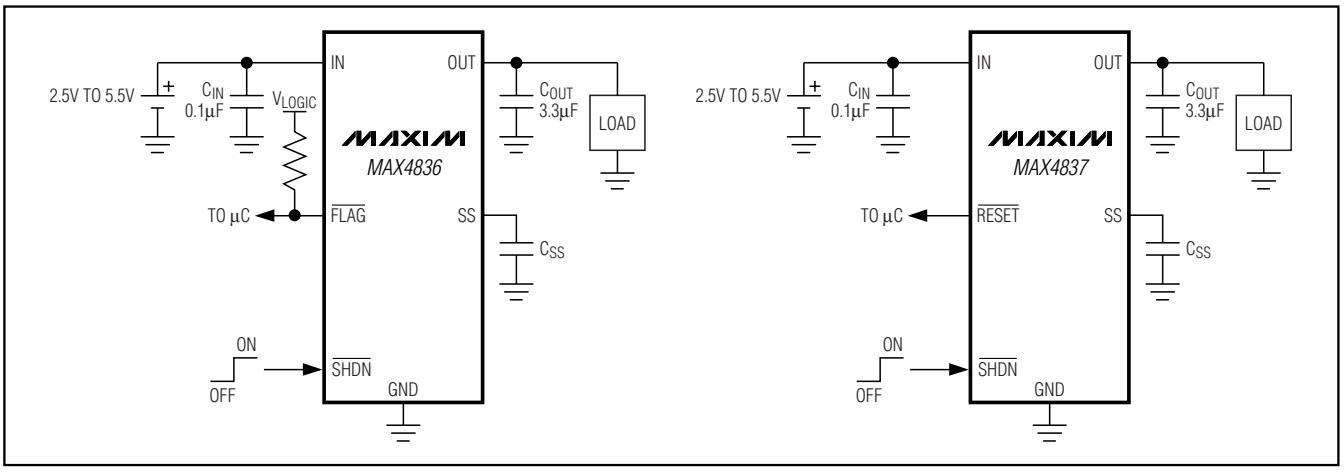


Figure 2. Typical Application Circuits

Shutdown Discharge (MAX4837)

OUT discharges through a 900Ω internal resistor during shutdown mode.

Reverse OUT to IN Current

When the output voltage is greater than the input voltage, the internal pass transistor turns off. To avoid reverse-charging the input source, the current at IN is guaranteed to be below 3µA when $V_{OUT} \geq V_{IN}$.

Current Limit

The MAX4836/MAX4837 include an accurate internal current-limiting circuit. OUT can be shorted to ground indefinitely without damaging the part.

The MAX4836 latches off if the load current exceeds the current limit for more than the blanking time (see the *$\overline{FLAG}$ Output* section). During soft-start, the device does not latch off to an overload condition. During an overload condition, the MAX4837 holds the current at current limit until the thermal limit is reached. Once the junction temperature reaches +165°C, thermal shutdown occurs.

Thermal Shutdown

When the junction temperature (T_J) exceeds +165°C, the LDO's pass transistor turns off allowing the junction to cool. The LDO's pass transistor turns on again after the IC's junction temperature cools by 15°C, resulting in a pulsed output during continuous thermal-overload conditions.

Soft-Start

During power-up, the soft-start ensures that the output ramps up slowly reducing inrush current peaks. See the soft-start response time plots in the *Typical Operating Characteristics*. The soft-start time (t_{SS}) is given by the following equation:

$$t_{SS} = C_{SS}\ (ms)$$

where C_{SS} is in nF.

A soft-start capacitor (C_{SS}) of 10nF gives a 10ms t_{SS}. A 1ms minimum soft-start time is fixed internally to ensure that the output rises slowly even without any external capacitor at SS pin to ground. The device is in soft-start mode when either the voltage at IN or $\overline{SHDN}$ is cycled high to low to high.

Applications Information

Capacitor Selection and Regulator Stability

For stable operation over the full temperature range and with load currents up to 500mA, use a 3.3µF (min) ceramic output capacitor with an ESR <0.2Ω. To reduce noise and improve load transient response, stability, and power-supply rejection, use larger output capacitor values such as 10µF (note that some ceramic capacitors exhibit large capacitance and ESR variation with temperature). X7R capacitors provide good performance over the -40°C to +85°C operating temperature range.

To improve power-supply rejection and transient response, use a 0.1µF capacitor between IN and GND. The MAX4836/MAX4837 remain stable with purely resistive loads or current loads up to 500mA.

15kV Operational ESD Protection

A 3.3µF or higher value ceramic capacitor from OUT to GND provides a 15kV (Human Body Model) protection at OUT. The ESR value of the capacitor should be less than 0.2Ω.

Reset Transient Immunity

The reset circuit is relatively immune to short duration, falling V_{OUT} transients. The *Typical Operating Characteristics* show a graph of the Maximum Transient Duration vs. Reset Threshold Overdrive for which reset is not asserted. The graph was produced using falling V_{OUT} transients starting at V_{OUT} and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a falling V_{OUT} transient can typically have without triggering the reset pulse. As the amplitude of the transient increases (i.e., goes further below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{OUT} transient that goes only 10mV below the reset threshold and lasts up to 54µs does not trigger a reset pulse.

Layout

When using the TDFN package, connect its exposed paddle to GND to provide a low thermal resistance path for heat transfer from the IC junction to the printed circuit board.

500mA LDO Linear Regulators with Current-Limiting Switch

Selector Guide

PART	PIN-PACKAGE	OUTPUT CURRENT (mA)	$\overline{\text{RESET}}$ OUTPUT CONFIGURATION	$\overline{\text{RESET}}$ ($\overline{\text{FLAG}}$)	SHUTDOWN DISCHARGE	LATCH OFF
MAX4836EUTxyC-T	6 SOT23-6	500	Open-Drain	$\overline{\text{FLAG}}$	No	Yes
MAX4836ETTxyC-T	6 TDFN-6	500	Open-Drain	$\overline{\text{FLAG}}$	No	Yes
MAX4837EUTxyBdd-T	6 SOT23-6	500	Push-Pull	$\overline{\text{RESET}}$	Yes	No
MAX4837ETTxyBdd-T	6 TDFN-6	500	Push-Pull	$\overline{\text{RESET}}$	Yes	No

Suffix 'xy' in the part number stands for nominal output voltage. 1.8V, 2.5V, 2.8V, 3.0V, 3.3V are the standard options. For other voltages between 1.5V to 3.3V, contact factory.

Table 1. Standard Output Voltage Suffix Guide

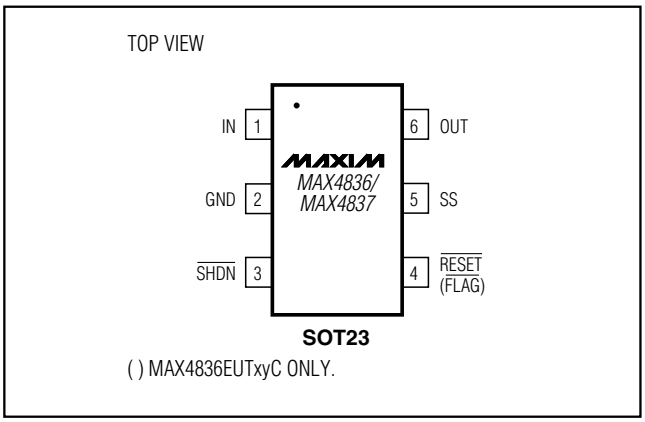
xy	OUTPUT VOLTAGE (V)
18	1.8
25	2.5
28	2.8
30	3.0
33	3.3

Nonstandard output voltages from 1.5V to 3.3V are available in 100mV increments. Contact factory for availability.

Table 2. $\overline{\text{RESET}}$ Timeout Period Suffix Guide

dd	$\overline{\text{RESET}}$ TIMEOUT (ms)
D1	3.75
D2	30
D3	225
D4	1800

Pin Configurations (continued)



Chip Information

TRANSISTOR COUNT: 1575

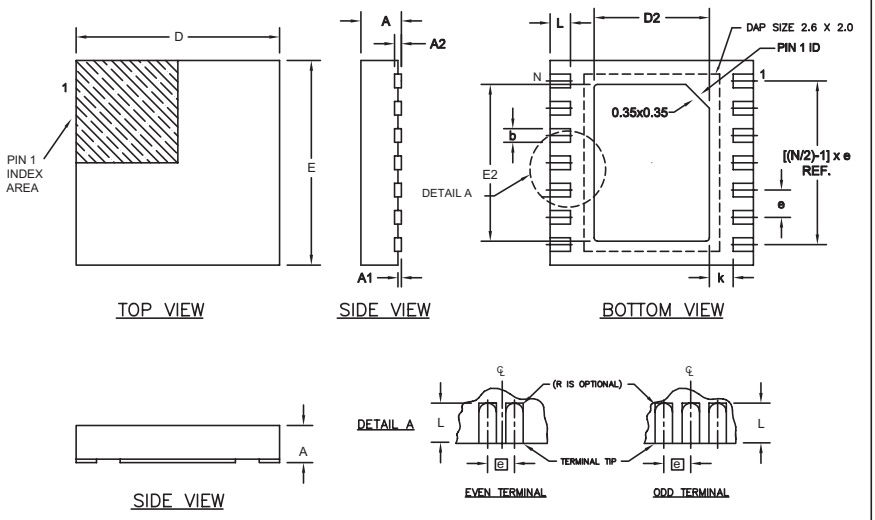
PROCESS: BiCMOS

TDFN Exposed Pad: Connected to GND

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

6, 8, &10L, DFN THIN.EPS



NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6, 8, 10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL | DOCUMENT CONTROL NO. 21-0137 | REV. F | 1/2

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.03	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.03	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.

DALLAS SEMICONDUCTOR MAXIM

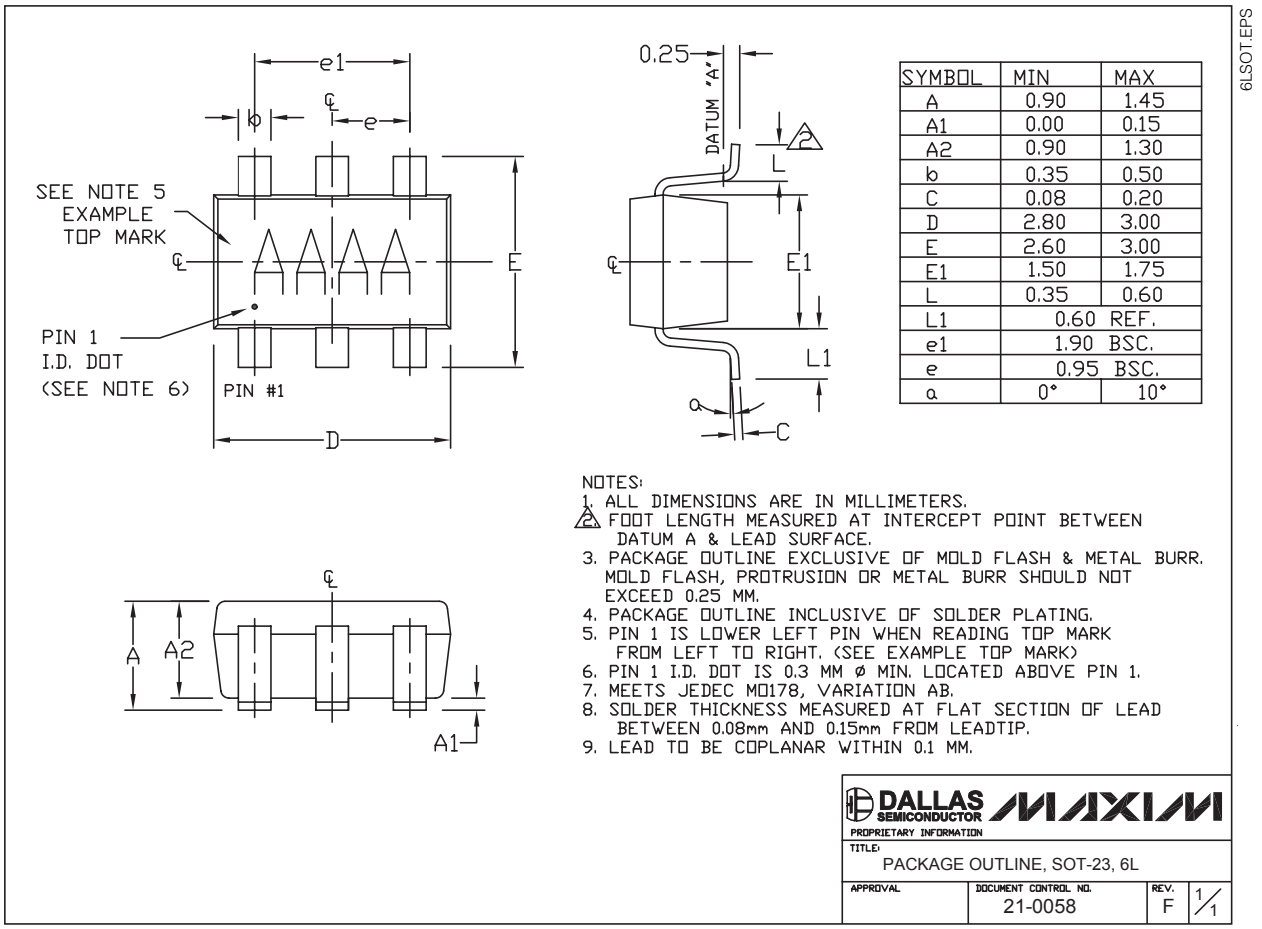
TITLE: PACKAGE OUTLINE, 6, 8, 10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL | DOCUMENT CONTROL NO. 21-0137 | REV. F | 2/2

500mA LDO Linear Regulators with Current-Limiting Switch

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.60
L1	0.60 REF.	
e1	1.90 BSC.	
e	0.95 BSC.	
α	0°	10°

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1 MM.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT-23, 6L

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0058	F	1/1