

MAX4245/MAX4246/ MAX4247

Ultra-Small, Rail-to-Rail I/O with Disable, Single-/Dual-Supply, Low-Power Op Amps

Absolute Maximum Ratings

Power-Supply Voltage (V_{DD} to V_{SS}).....-0.3V to +6V
 All Other Pins($V_{SS} - 0.3V$) to ($V_{DD} + 0.3V$)
 Output Short-Circuit Duration
 (OUT shorted to V_{SS} or V_{DD}) Continuous
 Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 6-Pin SC70 (derate 3.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....245mW
 6-Pin SOT23 (derate 8.7mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)695mW
 8-Pin SO (derate 5.9mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....471mW

8-Pin SOT23 (derate 9.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)727mW
 8-Pin μMAX (derate 4.5mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)362mW
 10-Pin μMAX (derate 5.6mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)444mW
 Operating Temperature Range..... -40°C to $+125^\circ\text{C}$
 Junction Temperature $+150^\circ\text{C}$
 Storage Temperature Range..... -65°C to $+160^\circ\text{C}$
 Lead Temperature (soldering, 10s) $+300^\circ\text{C}$
 Soldering Temperature (reflow) $+260^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

($V_{DD} = +2.7V$, $V_{SS} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{DD}/2$, R_L connected from OUT to $V_{DD}/2$, $\overline{\text{SHDN}} = V_{DD}$ (MAX4245/MAX4247 only), $T_A = +25^\circ\text{C}$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Inferred from PSRR test	2.5		5.5	V
Supply Current (Per Amplifier)	I_{DD}	$V_{DD} = +2.7V$		320	650	μA
		$V_{DD} = +5.5V$		375	700	
Supply Current in Shutdown	$I_{\overline{\text{SHDN}}}$	$\overline{\text{SHDN}} = V_{SS}$ (Note 2)		0.05	0.5	μA
Input Offset Voltage	V_{OS}	$V_{SS} - 0.1V \leq V_{CM} \leq V_{DD} + 0.1V$		± 0.4	± 1.5	mV
Input Bias Current	I_B	$V_{SS} - 0.1V \leq V_{CM} \leq V_{DD} + 0.1V$		± 10	± 50	nA
Input Offset Current	I_{OS}	$V_{SS} - 0.1V \leq V_{CM} \leq V_{DD} + 0.1V$		± 1	± 6	nA
Input Resistance	R_{IN}	$ V_{IN+} - V_{IN-} \leq 10\text{mV}$		4000		k Ω
Input Common-Mode Voltage Range	V_{CM}	Inferred from CMRR test	$V_{SS} - 0.1$		$V_{DD} + 0.1$	V
Common-Mode Rejection Ratio	CMRR	$V_{SS} - 0.1V \leq V_{CM} \leq V_{DD} + 0.1V$	65	80		dB
Power-Supply Rejection Ratio	PSRR	$2.5V \leq V_{DD} \leq 5.5V$	75	90		dB
Large-Signal Voltage Gain	A_V	$V_{SS} + 0.05V \leq V_{OUT} \leq V_{DD} - 0.05V$, $R_L = 100\text{k}\Omega$		120		dB
		$V_{SS} + 0.2V \leq V_{OUT} \leq V_{DD} - 0.2V$, $R_L = 2\text{k}\Omega$	95	110		
Output Voltage Swing High	V_{OH}	Specified as $V_{DD} - V_{OUT}$	$R_L = 100\text{k}\Omega$	1		mV
			$R_L = 2\text{k}\Omega$	35	60	
Output Voltage Swing Low	V_{OL}	Specified as $V_{OUT} - V_{SS}$	$R_L = 100\text{k}\Omega$	1		mV
			$R_L = 2\text{k}\Omega$	30	60	
Output Short-Circuit Current	$I_{OUT(SC)}$	$V_{DD} = +5.0V$	Sourcing	11		mA
			Sinking	30		
Output Leakage Current in Shutdown	$I_{OUT(SH)}$	Device in Shutdown Mode ($\overline{\text{SHDN}} = V_{SS}$), $V_{SS} \leq V_{OUT} \leq V_{DD}$ (Note 2)		± 0.01	± 0.5	μA
$\overline{\text{SHDN}}$ Logic Low	V_{IL}	(Note 2)		$0.3 \times V_{DD}$		V
$\overline{\text{SHDN}}$ Logic High	V_{IH}	(Note 2)	$0.7 \times V_{DD}$			V
$\overline{\text{SHDN}}$ Input Current	I_L/I_H	$V_{SS} \leq \overline{\text{SHDN}} \leq V_{DD}$ (Note 2)		0.5	50	nA

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Electrical Characteristics (continued)

($V_{DD} = +2.7V$, $V_{SS} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{DD}/2$, R_L connected from OUT to $V_{DD}/2$, $\overline{SHDN} = V_{DD}$ (MAX4245/MAX4247 only), $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBW			1.0		MHz
Phase Margin	Φ_M			70		degrees
Gain Margin	G_M			20		dB
Slew Rate	SR			0.4		V/ μs
Input Voltage-Noise Density	e_n	$f = 10kHz$		52		nV/ $\sqrt{Hz}$
Input Current-Noise Density	i_n	$f = 10kHz$		0.1		pA/ $\sqrt{Hz}$
Capacitive-Load Stability	C_{LOAD}	$A_V = 1$ (Note 3)			470	pF
Shutdown Delay Time	$t_{(SH)}$	(Note 2)		3		μs
Enable Delay Time	$t_{(EN)}$	(Note 2)		4		μs
Power-On Time	t_{ON}			4		μs
Input Capacitance	C_{IN}			2.5		pF
Total Harmonic Distortion	THD	$f = 10kHz$, $V_{OUT} = 2V_{P-P}$, $A_V = +1$, $V_{DD} = +5.0V$, Load = 100k Ω to $V_{DD}/2$		0.01		%
Settling Time to 0.01%	t_S	$V_{OUT} = 4V$ step, $V_{DD} = +5.0V$, $A_V = +1$		10		μs

Electrical Characteristics

($V_{DD} = +2.7V$, $V_{SS} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{DD}/2$, R_L connected from OUT to $V_{DD}/2$, $\overline{SHDN} = V_{DD}$ (MAX4245/MAX4247 only), $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Inferred from PSRR test	2.5		5.5	V
Supply Current (Per Amplifier)	I_{DD}	$V_{DD} = +2.7V$			800	μA
Supply Current in Shutdown	$I_{\overline{SHDN}}$	$\overline{SHDN} = V_{SS}$ (Note 2)			1	μA
Input Offset Voltage	V_{OS}	$V_{SS} \leq V_{CM} \leq V_{DD}$ (Note 4)			± 3.0	mV
Input Offset Voltage Drift	TCV_{OS}	$V_{SS} \leq V_{CM} \leq V_{DD}$ (Note 4)		± 2		$\mu V/^\circ C$
Input Bias Current	I_B	$V_{SS} \leq V_{CM} \leq V_{DD}$ (Note 4)			± 100	nA
Input Offset Current	I_{OS}	$V_{SS} \leq V_{CM} \leq V_{DD}$ (Note 4)			± 10	nA
Input Common-Mode Voltage Range	V_{CM}	Inferred from CMRR test (Note 4)	V_{SS}		V_{DD}	V
Common-Mode Rejection Ratio	CMRR	$V_{SS} \leq V_{CM} \leq V_{DD}$ (Note 4)	60			dB
Power-Supply Rejection Ratio	PSRR	$2.5V \leq V_{DD} \leq 5.5V$	70			dB
Large-Signal Voltage Gain	A_V	$V_{SS} + 0.2V \leq V_{OUT} \leq V_{DD} - 0.2V$, $R_L = 2k\Omega$	85			dB
Output Voltage Swing High	V_{OH}	Specified as $V_{DD} - V_{OUT}$, $R_L = 2k\Omega$			90	mV
Output Voltage Swing Low	V_{OL}	Specified as $V_{OUT} - V_{SS}$, $R_L = 2k\Omega$			90	mV
Output Leakage Current in Shutdown	$I_{OUT(SH)}$	Device in Shutdown Mode ($\overline{SHDN} = V_{SS}$), $V_{SS} \leq V_{OUT} \leq V_{DD}$ (Note 3)			± 1.0	μA

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Electrical Characteristics (continued)

(V_{DD} = +2.7V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD}/2, R_L connected from OUT to V_{DD}/2, $\overline{\text{SHDN_}}$ = V_{DD} (MAX4245/MAX4247 only), T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{SHDN_}}$ Logic Low	V _{IL}	(Note 2)		0.3 x V _{DD}		V
$\overline{\text{SHDN_}}$ Logic High	V _{IH}	(Note 2)	0.7 x V _{DD}			V
$\overline{\text{SHDN_}}$ Input Current	I _L /I _H	V _{SS} ≤ $\overline{\text{SHDN_}}$ ≤ V _{DD} (Notes 2, 3)		100		nA

Note 1: Specifications are 100% tested at T_A = +25°C. All temperature limits are guaranteed by design.

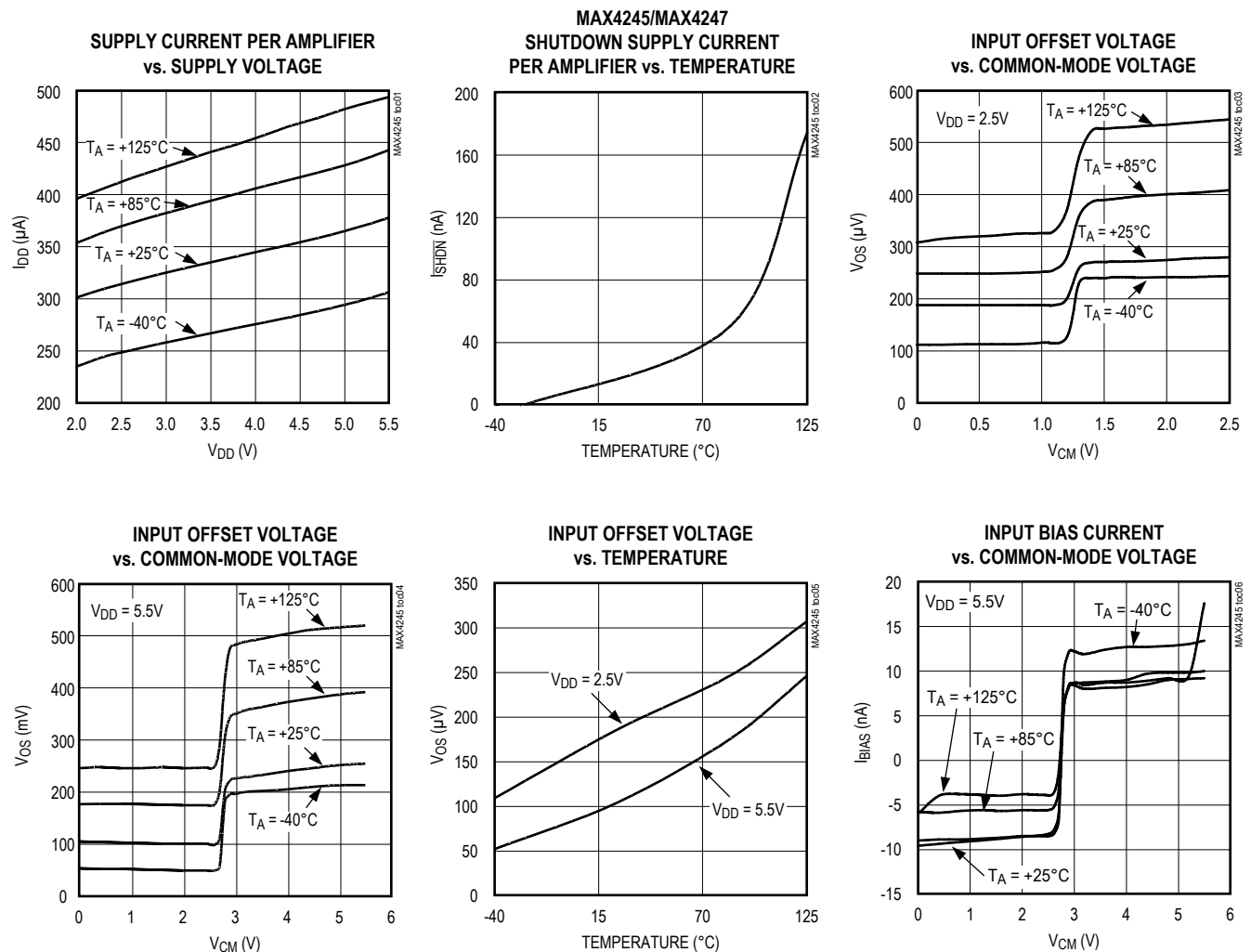
Note 2: Shutdown mode is only available in MAX4245 and MAX4247.

Note 3: Guaranteed by design, not production tested.

Note 4: For -40°C to +85°C, Input Common-Mode Range is V_{SS} - 0.1V ≤ V_{CM} ≤ V_{DD} + 0.1V.

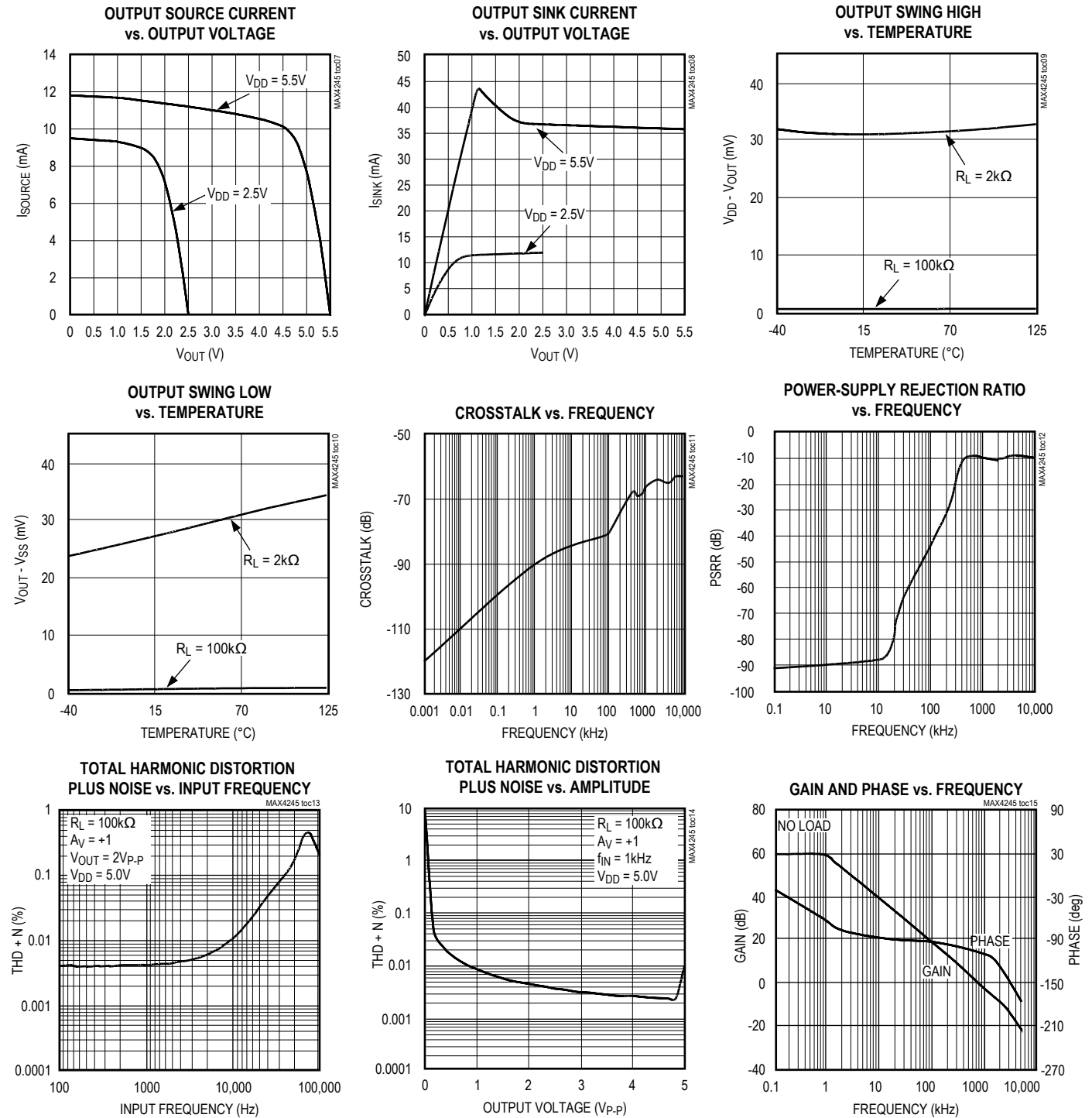
Typical Operating Characteristics

(V_{DD} = 2.7V, V_{SS} = V_{CM} = 0V, V_{OUT} = V_{DD}/2, no load, T_A = +25°C, unless otherwise noted.)



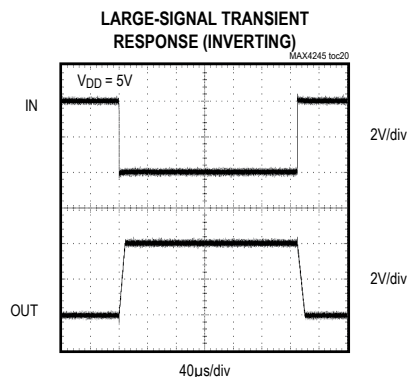
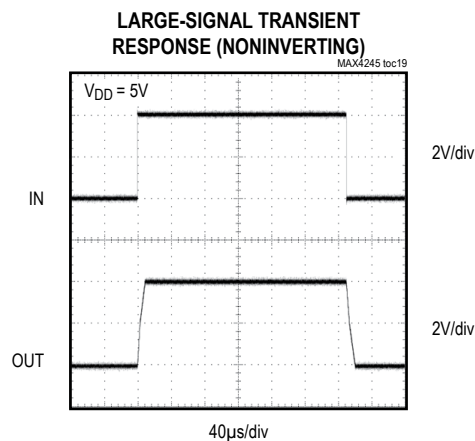
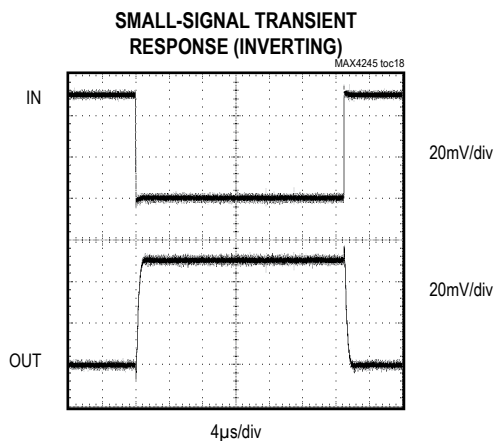
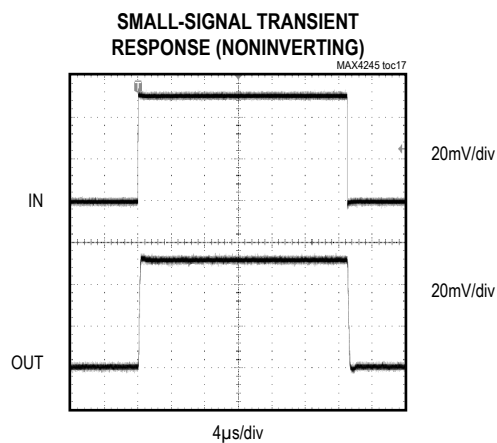
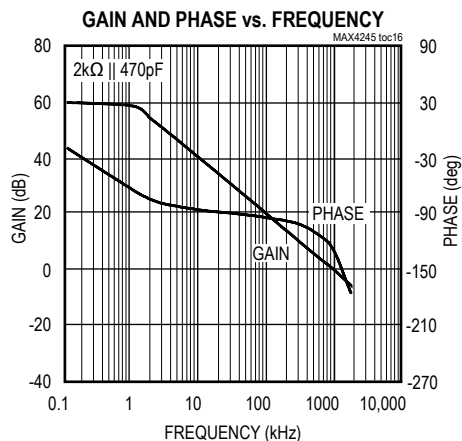
Typical Operating Characteristics

($V_{DD} = 2.7V$, $V_{SS} = V_{CM} = 0V$, $V_{OUT} = V_{DD}/2$, no load, $T_A = +25^\circ C$, unless otherwise noted.)



Typical Operating Characteristics (continued)

($V_{DD} = 2.7V$, $V_{SS} = V_{CM} = 0V$, $V_{OUT} = V_{DD}/2$, no load, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN			NAME	FUNCTION
MAX4245	MAX4246	MAX4247		
1	—	—	IN+	Noninverting Input
2	4	4	V _{SS}	Ground or Negative Supply
3	—	—	IN-	Inverting Input
4	—	—	OUT	Amplifier Output
5	—	—	SHDN	Shutdown
6	8	10	V _{DD}	Positive Supply
—	1	1	OUTA	Amplifier Output Channel A
—	2	2	INA-	Inverting Input Channel A
—	3	3	INA+	Noninverting Input Channel A
—	5	7	INB+	Noninverting Input Channel B
—	6	8	INB-	Inverting Input Channel B
—	7	9	OUTB	Amplifier Output Channel B
—	—	5	SHDNA	Shutdown Channel A
—	—	6	SHDNB	Shutdown Channel B

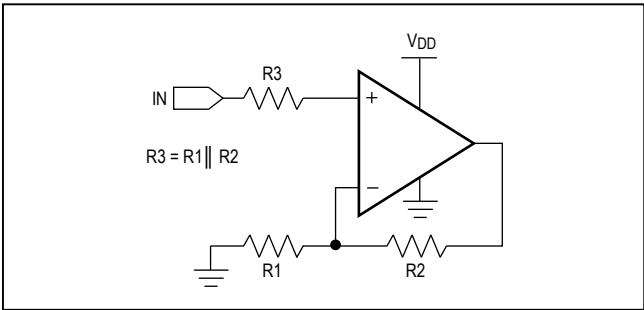


Figure 1a. Minimizing Offset Error Due to Input Bias Current (Noninverting)

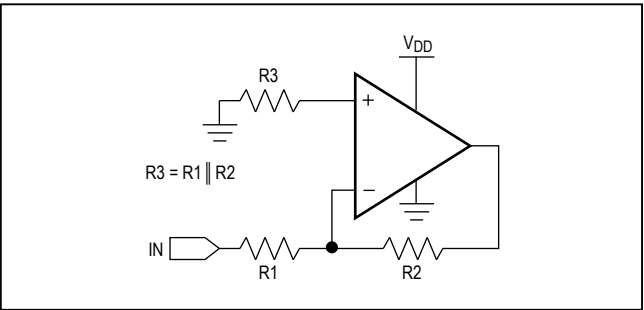


Figure 1b. Minimizing Offset Error Due to Input Bias Current (Inverting)

Detailed Description

Rail-to-Rail Input Stage

The MAX4245/MAX4246/MAX4247 have rail-to-rail input and output stages that are specifically designed for low-voltage, single-supply operation. The input stage consists of composite NPN and PNP differential stages, which operate together to provide a common-mode range extending to both supply rails. The crossover region of these two pairs occurs halfway between V_{DD} and V_{SS}. The input offset voltage is typically ±400μV. Low-operating supply voltage, low supply current and rail-to-rail outputs make this family of operational amplifiers an excellent choice for precision or general-purpose, low-voltage, battery-powered systems.

Since the input stage consists of NPN and PNP pairs, the input bias current changes polarity as the common-mode voltage passes through the crossover region. Match the effective impedance seen by each input to reduce the offset error caused by input bias currents flowing through external source impedance (Figures 1a and 1b).

The combination of high-source impedance plus input capacitance (amplifier input capacitance plus stray capacitance) creates a parasitic pole that can produce an underdamped signal response. Reducing input capacitance or placing a small capacitor across the feedback resistor improves response in this case.

The MAX4245/MAX4246/MAX4247 family's inputs are protected from large differential input voltages by internal 5.3kΩ series resistors and back-to-back triple-diode stacks across the inputs (Figure 2). For differential-input voltages

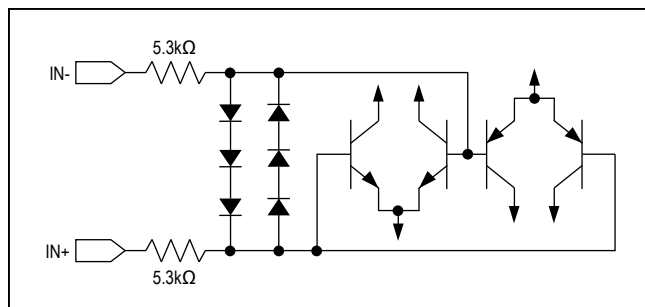


Figure 2. Input Protection Circuit

much less than 2.1V (triple-diode drop), input resistance is typically 4MΩ. For differential voltages greater than 2.1V, input resistance is around 10.6kΩ, and the input bias current can be approximated by the following equation:

$$I_B = (V_{DIFF} - 2.1V) / 10.6k\Omega$$

In the region where the differential input voltage approaches 2.1V, the input resistance decreases exponentially from 4MΩ to 10.6kΩ as the diodes begin to conduct. It follows that the bias current increases with the same curve.

In unity-gain configuration, high slew-rate input signals may capacitively couple to the output through the triple-diode stacks.

Rail-to-Rail Output Stage

The MAX4245/MAX4246/MAX4247 can drive a 2kΩ load and still typically swing within 35mV of the supply rails. Figure 3 shows the output voltage swing of the MAX4245 configured with $A_V = -1V/V$.

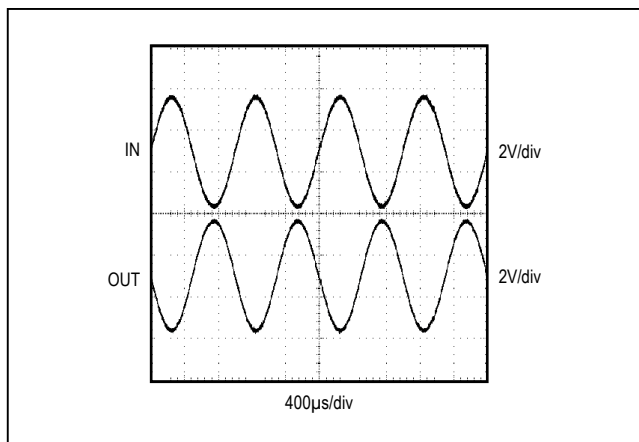


Figure 3. Rail-to-Rail Input/Output Voltage Range

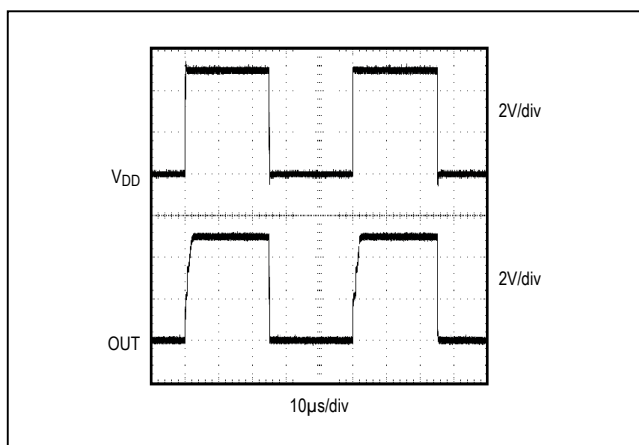


Figure 4. Power-Up/Power-Down Waveform

Applications Information

Power-Supply Considerations

The MAX4245/MAX4246/MAX4247 operate from a single +2.5V to +5.5V supply (or dual $\pm 1.25V$ to $\pm 2.75V$ supplies) and consume only 320μA of supply current per amplifier. A 90dB power-supply rejection ratio allows the amplifiers to be powered directly off a decaying battery voltage, simplifying design and extending battery life.

Power-Up

The MAX4245/MAX4246/MAX4247 output typically settles within 4μs after power-up. Figure 4 shows the output voltage on power-up and power-down.

Shutdown Mode

The MAX4245/MAX4247 feature a low-power shutdown mode. When $\overline{SHDN}$ is pulled low, the supply current drops to 50nA per amplifier, the amplifier is disabled, and

the output enters a high-impedance state. Pulling $\overline{SHDN}$ high enables the amplifier. Figure 5 shows the MAX4245/MAX4247's shutdown waveform.

Due to the output leakage currents of three-state devices and the small internal pullup current for $\overline{SHDN}$, do not leave $\overline{SHDN}$ open/high-impedance. Leaving $\overline{SHDN}$ open may result in indeterminate logic levels, and could adversely affect op amp operation. The logic threshold for $\overline{SHDN}$ is referred to V_{SS} . When using dual supplies, pull $\overline{SHDN}$ to V_{SS} , not GND, to shut down the op amp.

Driving Capacitive Loads

The MAX4245/MAX4246/MAX4247 are unity-gain stable for loads up to 470pF. Applications that require greater capacitive drive capability should use an isolation resistor

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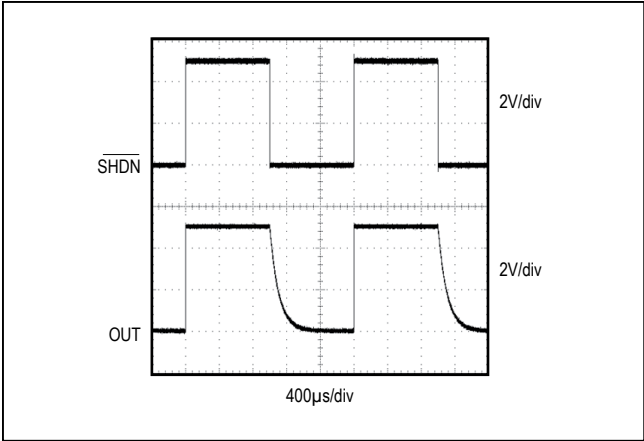


Figure 5. Shutdown Waveform

between the output and the capacitive load (Figures 6a, 6b, 6c). Note that this alternative results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_{LOAD} .

Power-Supply Bypassing and Layout

The MAX4245/MAX4246/MAX4247 family operates from either a single +2.5V to +5.5V supply or dual ±1.25V to ±2.75V supplies. For single-supply operation, bypass the power supply with a 100nF capacitor to V_{SS} (in this case GND). For dual-supply operation, both the V_{DD} and the V_{SS} supplies should be bypassed to ground with separate 100nF capacitors.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp’s inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components when possible.

Pin Configurations (continued)

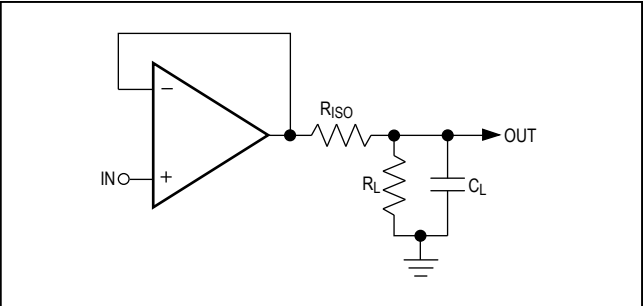
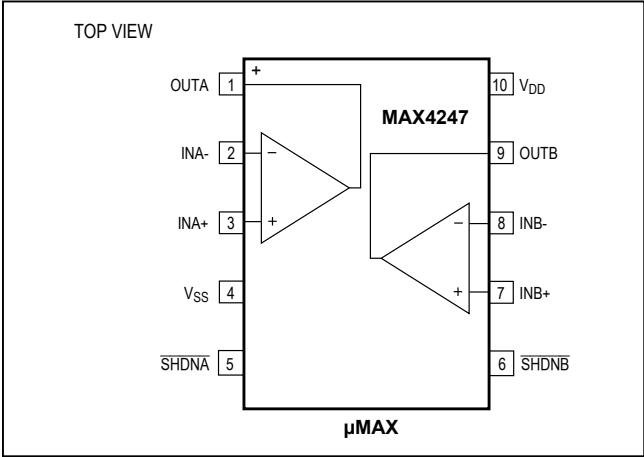


Figure 6a. Using a Resistor to Isolate a Capacitive Load from the Op Amp

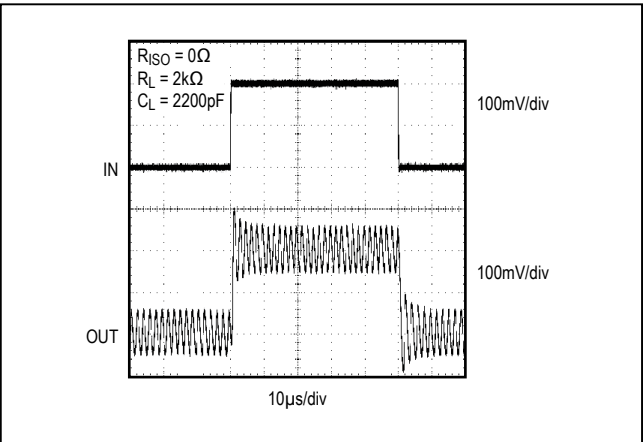


Figure 6b. Pulse Response Without Isolating Resistor

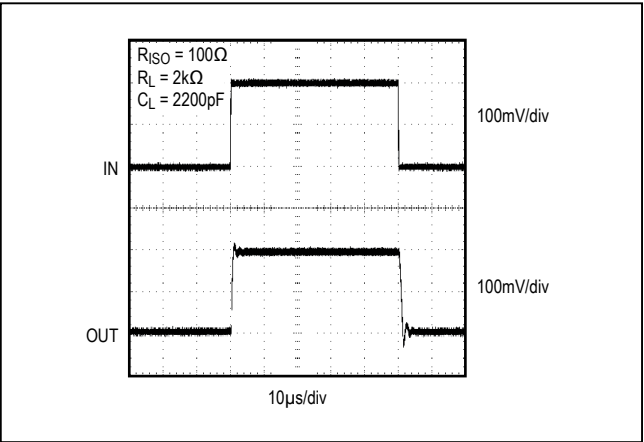


Figure 6c. Pulse Response With Isolating Resistor

Chip Information
PROCESS: BiCMOS

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Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
6 SOT23	U6+4	21-0058	90-0175
6 SC70	X6SN+1	21-0077	90-0189
8 SOT23	K8+5	21-0078	90-0176
8 SO	S8+4	21-0041	90-0096
8 μ MAX	U8+1	21-0036	90-0092
10 μ MAX	U10+2	21-0061	90-0330

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/01	Initial release	—
2	11/11	Added lead-free data to <i>Ordering Information</i> .	1
3	5/14	Updated the <i>General Description</i> .	1

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