

On/Off Controller with Debounce and $\pm 15\text{kV}$ ESD Protection

ABSOLUTE MAXIMUM RATINGS

V _{CC} to GND	-0.3V to +6V
IN to GND	-30V to +30V
CLEAR to GND	-0.3V to +6V
OUT, $\overline{\text{OUT}}$ to GND	-0.3V to (V _{CC} + 0.3V)
Short-Circuit Duration	
OUT, $\overline{\text{OUT}}$ to GND	Continuous

Continuous Power Dissipation (T _A = +70°C)	
6-Pin Thin SOT23	
(derate 9.1mW/°C at +70°C) (Note 1)	727mW
Operating Temperature Range	-40°C to +125°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: As per JEDEC 51 standard, multilayer board (PCB).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V _{CC}	(Note 3)	2.7		5.5	V
Supply Current	I _{CC}	V _{CC} = 5V, I _{OUT} = I $\overline{\text{OUT}}$ = 0, IN not connected		7	20	μA
Debounce Duration	t _{DP}	T _A = +25°C	20	50	80	ms
		T _A = -40°C to +125°C	5	50	99	
IN Threshold	V _{IL}				0.65	V
	V _{IH}	V _{CC} = 5V	2.5			
		V _{CC} = 2.7V	2.0			
IN Hysteresis				420		mV
IN Pullup Resistance			32	63	100	kΩ
IN Current	I _{IN}	V _{IN} = +25V			+1.5	mA
		V _{IN} = -25V	-1.5			
IN Voltage Range	V _{IN}		-25		+25	V
Undervoltage-Lockout Threshold	V _{UVLO}	V _{CC} falling		1.8	2.4	V
OUT/ $\overline{\text{OUT}}$ Output Voltage	V _{OL}	I _{SINK} = 1.6mA			0.4	V
	V _{OH}	I _{SOURCE} = 0.4mA	V _{CC} - 1.0			
CLEAR Threshold	V _{CLEAR_IL}				0.7	V
	V _{CLEAR_IH}	V _{CC} = 5V	2.4			
		V _{CC} = 2.7V	2.0			
CLEAR Input Current	I _{CLEAR}		-1		+1	μA
CLEAR High to OUT Low Propagation Delay	t _{CO}	R _L = 10kΩ, C _L = 100pF			200	ns
ESD CHARACTERISTICS						
ESD Protection		IN	IEC 61000-4-2 Air Discharge	±15		kV
			IEC 61000-4-2 Contact Discharge	±8		
			Human Body Model	±15		

Note 2: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

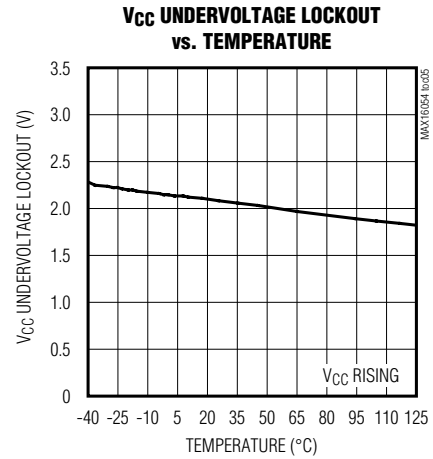
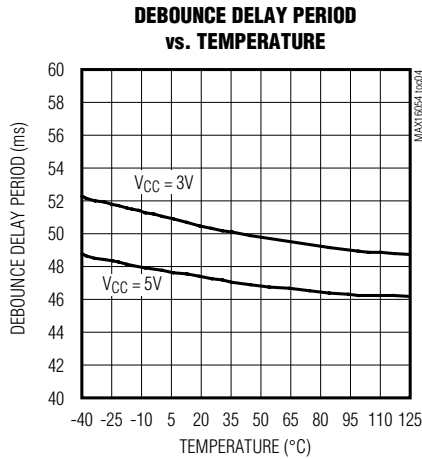
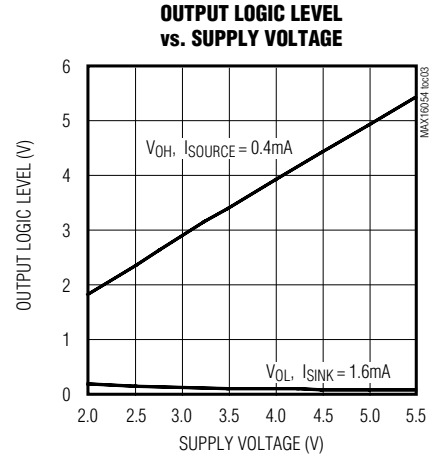
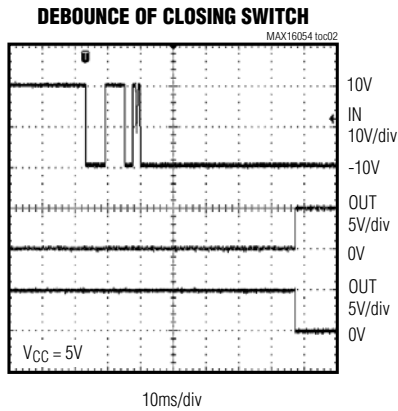
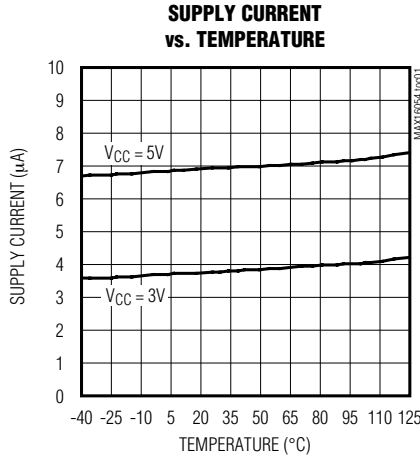
Note 3: OUT is guaranteed to be low for 1.0V ≤ V_{CC} ≤ V_{UVLO}.

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Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

MAX16054

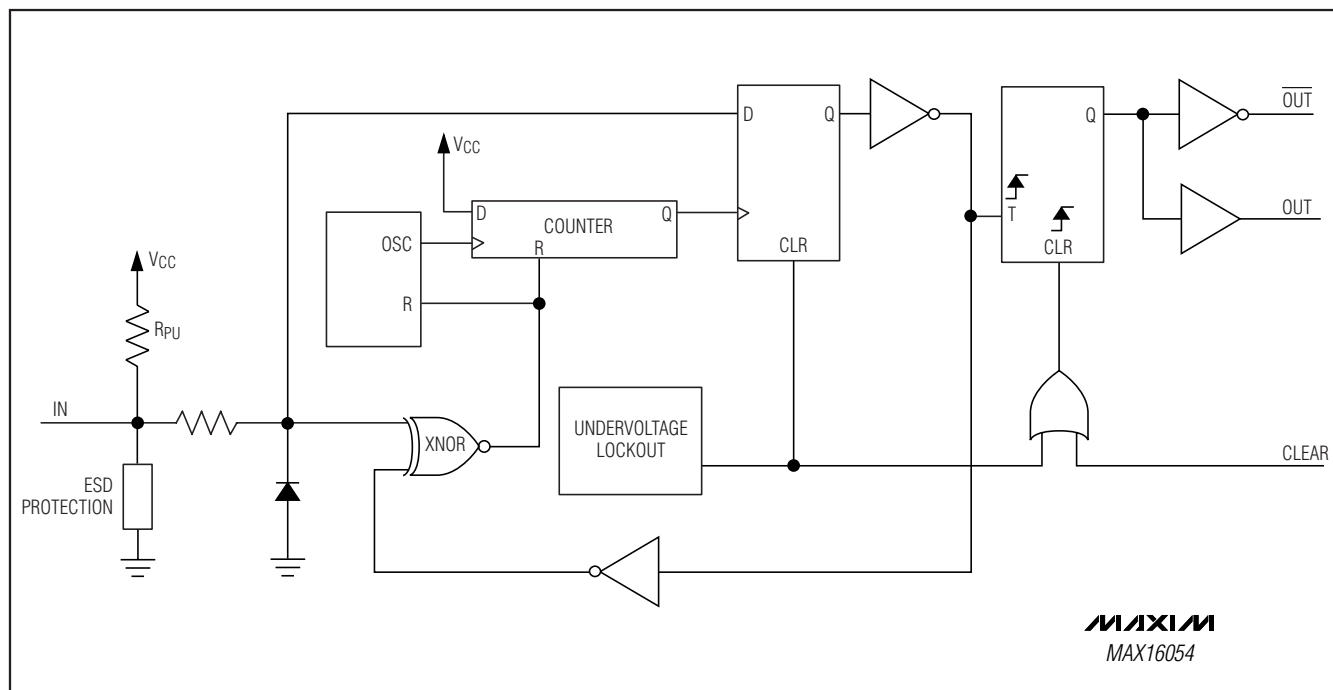


Pin Description

PIN	NAME	FUNCTION
1	IN	Switch Toggle Input. IN features a -25V to +25V maximum input range and includes an internal 63k Ω pullup resistor to V_{CC} . Connect a pushbutton from IN to GND.
2	GND	Ground
3	CLEAR	Clear Input. Pull CLEAR high to force OUT low. Connect CLEAR to GND if unused.
4	OUT	Active-Low CMOS Output
5	OUT	Active-High CMOS Output
6	V_{CC}	+2.7V to +5.5V Supply Input. In noisy environments, bypass V_{CC} to GND with a 0.1 μF or greater ceramic capacitor.

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Functional Diagram



Detailed Description

Theory of Operation

The MAX16054 creates a push-on, push-off function using a momentary-contact normally open SPST switch. The high-to-low transition that occurs when closing the switch causes OUT to go high and $\overline{\text{OUT}}$ to go low. The output state remains latched after the switch is released/opened. Closing the switch again causes OUT to go low and $\overline{\text{OUT}}$ to go high.

Debounce circuitry eliminates the extraneous level changes that result from interfacing with mechanical switches (switch bounce). Virtually all mechanical switches bounce upon opening and closing. The bounce when a switch opens or closes is eliminated by requiring that the sequentially clocked input remains in the same state for a number of sampling periods. The

output does not change state from high-to-low or low-to-high until the input is stable for at least 50ms (typ).

The *Functional Diagram* shows the functional blocks consisting of an on-chip oscillator, counter, exclusive-NOR gate, a D flip-flop, and a T (toggle) flip-flop. When the pushbutton input does not equal the internal debounced button state (the Q output of the D flip-flop), the XNOR gate issues a counter reset. When the switch input state is stable for the full qualification period, the counter clocks the D flip-flop, changing the internal pushbutton state. The Q output of the D flip-flop is connected to a toggle flip-flop that toggles when the internal pushbutton state goes through a high-to-low transition. Figure 1 shows the typical opening and closing switch debounce operation.

A rising pulse at CLEAR resets the T flip-flop and pulls OUT low and $\overline{\text{OUT}}$ high.

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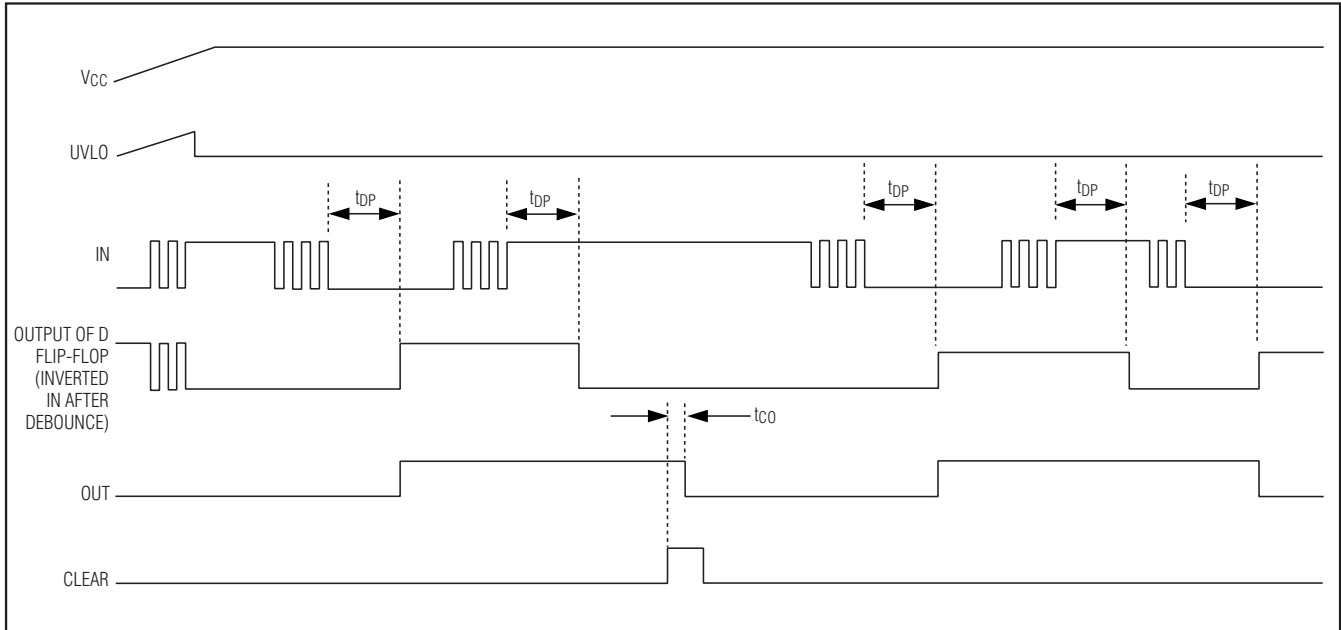


Figure 1. MAX16054 Timing Diagram

Undervoltage Lockout

The undervoltage-lockout circuitry ensures that the outputs are at the correct state on power-up. While V_{CC} is less than the 2.1V (typ) undervoltage threshold and greater than 1.0V, OUT remains low and transitions at IN are ignored.

Robust Switch Input

The switch input (IN) has overvoltage clamping diodes to protect against damaging fault conditions. Switch input voltages can safely swing $\pm 25\text{V}$ to ground. Proprietary ESD-protection structures protect against high ESD encountered in harsh industrial environments, membrane keypads, and portable applications. They are designed to withstand $\pm 15\text{kV}$ per the IEC 61000-4-2 Air-Gap Discharge test and $\pm 8\text{kV}$ per the IEC 61000-4-2 Contact-Discharge test.

Since there is a $63\text{k}\Omega$ (typ) pullup resistor connected to IN, driving the input to -25V draws approximately 0.5mA from the V_{CC} supply. Driving the input to $+25\text{V}$ causes approximately 0.32mA of current to flow back into the V_{CC} supply. If the total system V_{CC} supply current is less than the current flowing back into the V_{CC} supply,

V_{CC} rises above normal levels. In some low-current systems, a zener diode on V_{CC} may be required.

$\pm 15\text{kV}$ ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The MAX16054 has extra protection against static electricity to protect against ESD of $\pm 15\text{kV}$ at the switch input without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. A design advantage of the MAX16054 is that it continues working without latchup after an ESD event, which eliminates the need to power-cycle the device.

ESD protection can be tested in various ways; this product is characterized for protection to the following limits:

- 1) $\pm 15\text{kV}$ using the Human Body Model.
- 2) $\pm 8\text{kV}$ using the Contact-Discharge method specified in IEC 61000-4-2.
- 3) $\pm 15\text{kV}$ using the IEC 61000-4-2 Air-Gap method.

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Human Body Model

Figure 2a shows the Human Body Model, and Figure 2b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5k Ω resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX16054 helps in the design of equipment that meets IEC 61000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2, because series resistance is

lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 3a shows the IEC 61000-4-2 model, and Figure 3b shows the current waveform for the IEC 61000-4-2 ESD Contact-Discharge test.

The Air-Gap test involves approaching the device with a charged probe. The Contact-Discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing.

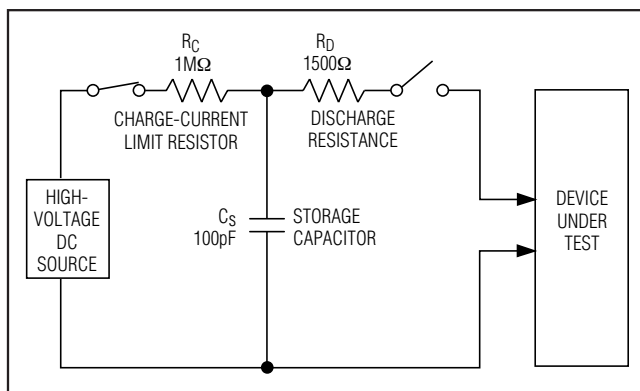


Figure 2a. Human Body ESD Test Model

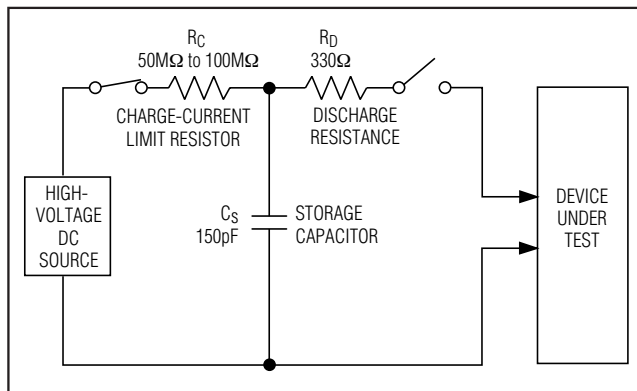


Figure 3a. IEC 61000-4-2 ESD Test Model

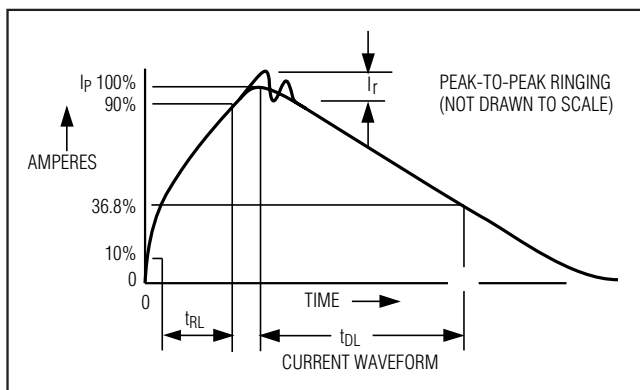


Figure 2b. Human Body Current Waveform

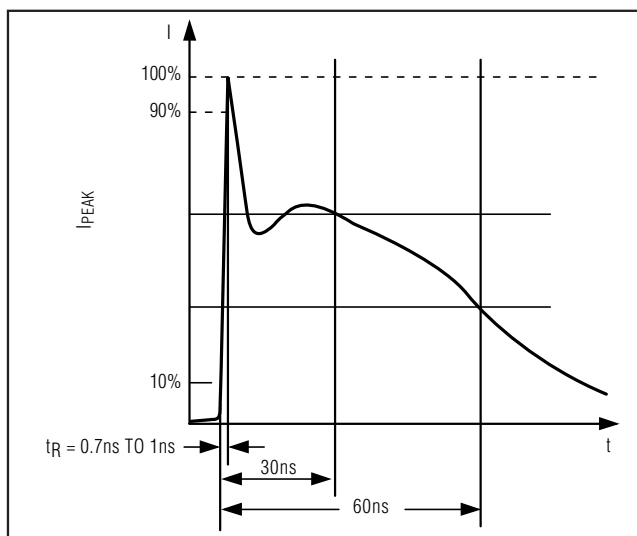
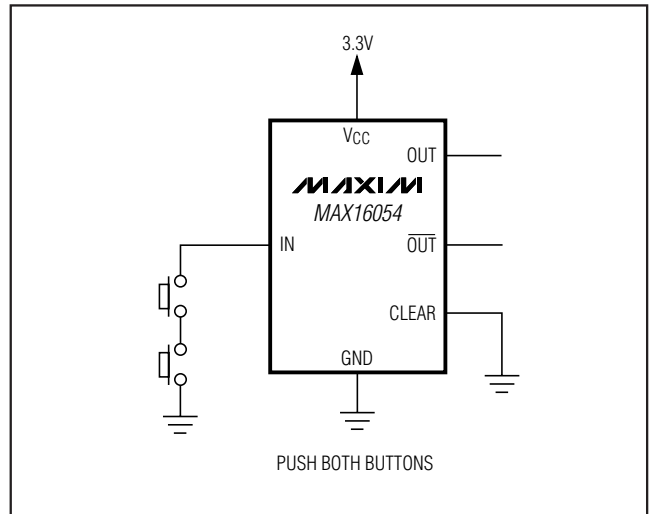
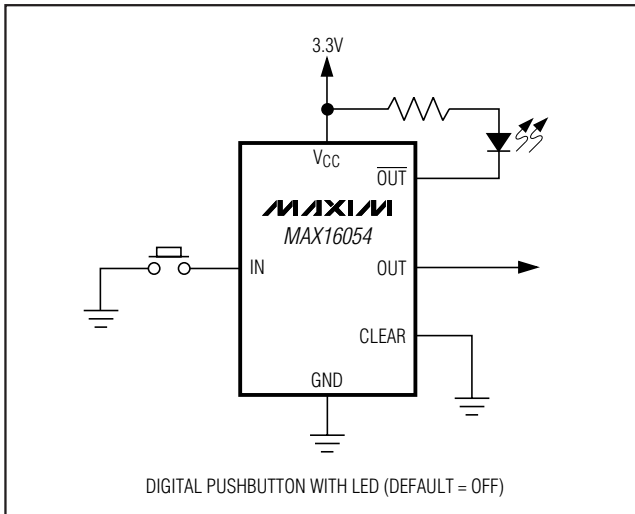
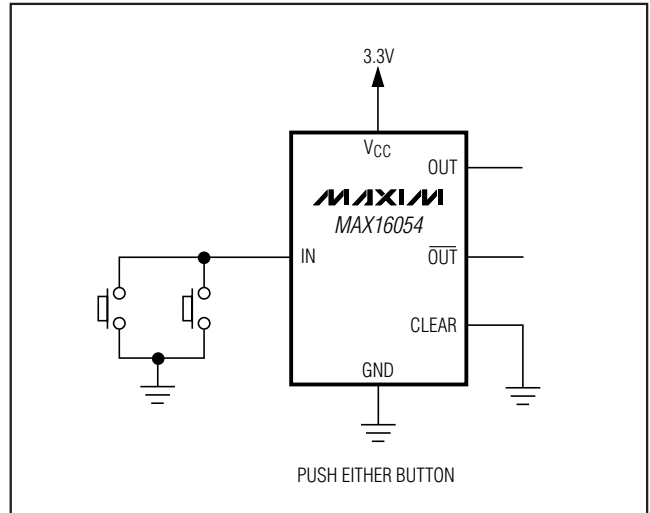
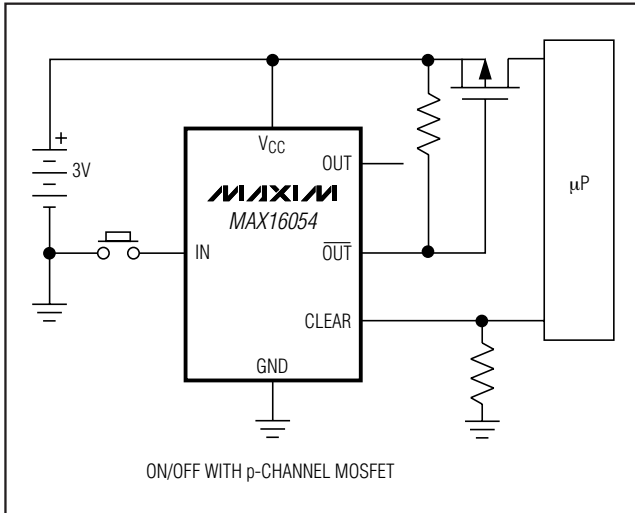


Figure 3b. IEC 61000-4-2 ESD Generator Current Waveform

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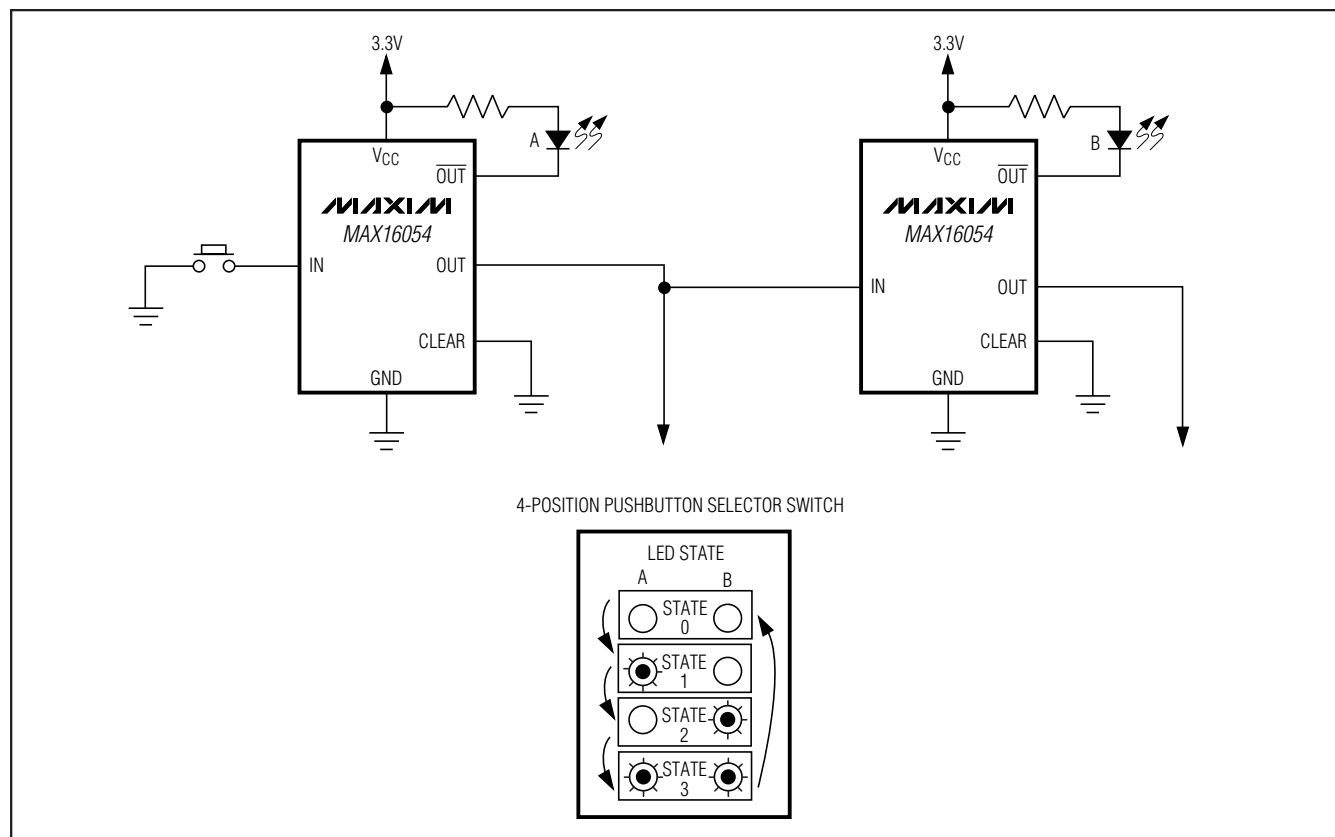
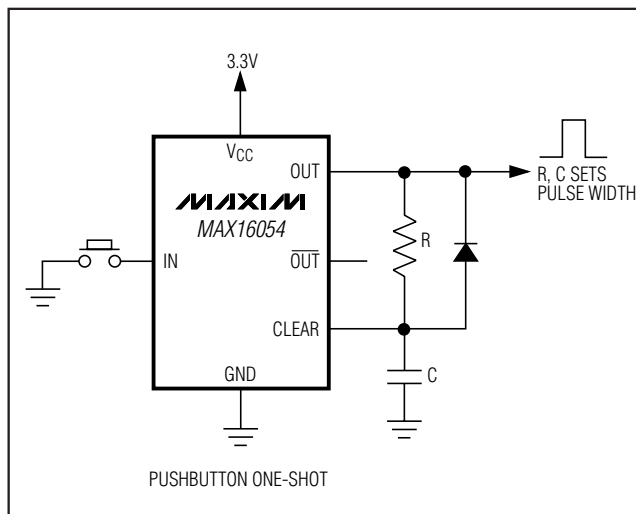
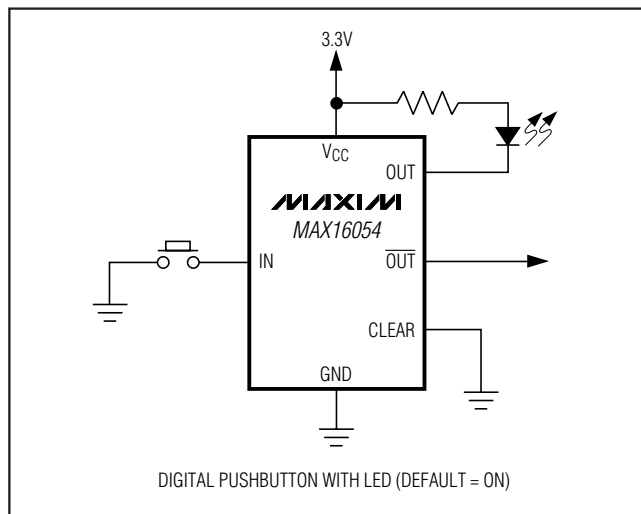
Typical Operating Circuits (continued)

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Typical Operating Circuits (continued)



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Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information, go to
www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
6 Thin SOT23	Z6-1	21-0114

MAX16054

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