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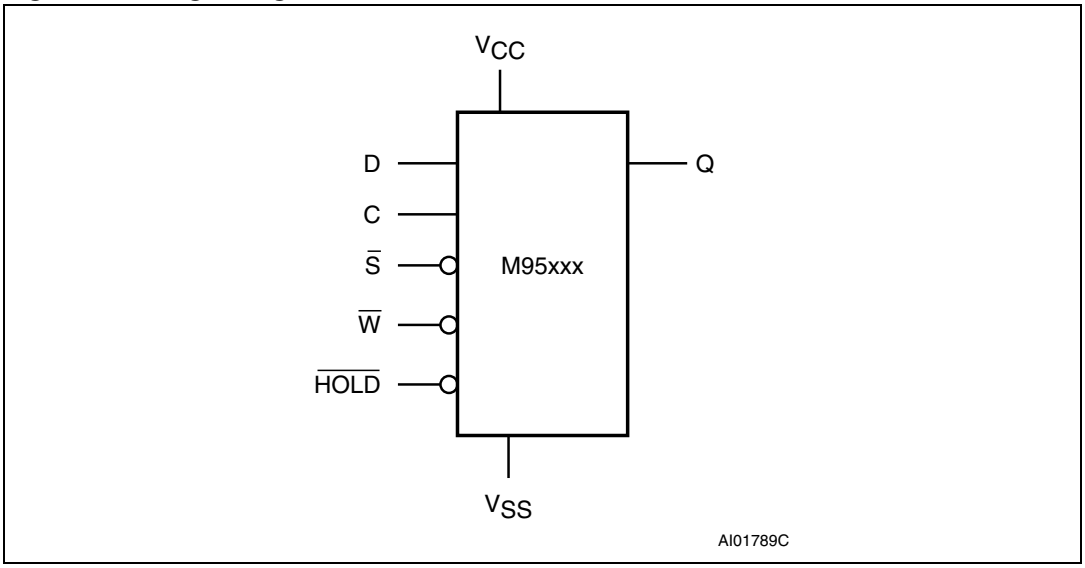
1 Description

The M95160-x and M95080-x are electrically erasable programmable memory (EEPROM) devices. They are accessed by a high-speed SPI-compatible bus. The memory array is organized as 2048 x 8 bit (M95160-x), and 1024 x 8 bit (M95080-x).

Figure 1. Logic diagram



The device is accessed by a simple serial interface that is SPI-compatible. The bus signals are C, D and Q, as shown in *Table 2* and *Figure 1*.

The device is selected when Chip Select ($\overline{S}$) is taken low. Communications with the device can be interrupted using Hold ($\overline{HOLD}$).

Table 2. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data input	Input
Q	Serial Data output	Output
$\overline{S}$	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{HOLD}$	Hold	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

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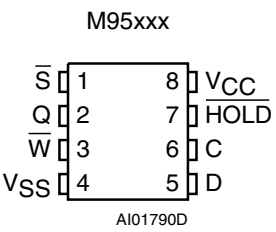
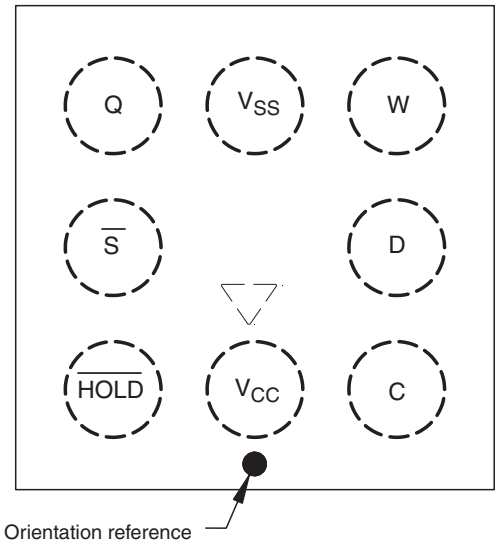
Figure 2. 8-pin package connections (top view)



1. See *Package mechanical data* section for package dimensions, and how to identify pin-1.

Figure 3. M95160 WLCSP connections (top view, marking side, with balls on the underside)



Caution: EEPROM cells loose their charge (and so their binary value) when exposed to ultra violet (UV) light. Consequently, EEPROM dice delivered in wafer form or in WLCSP package by STMicroelectronics must never be exposed to UV light.

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2 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals must be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in *Table 14.* to *Table 19.*). These signals are described next.

2.1 Serial Data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial Data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Write cycle is in progress, the device will be in the Standby Power mode. Driving Chip Select ($\overline{S}$) low selects the device, placing it in the Active Power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven low.

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2.6 Write Protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

This pin must be driven either high or low, and must be stable during all write instructions.

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

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3 Connecting to the SPI bus

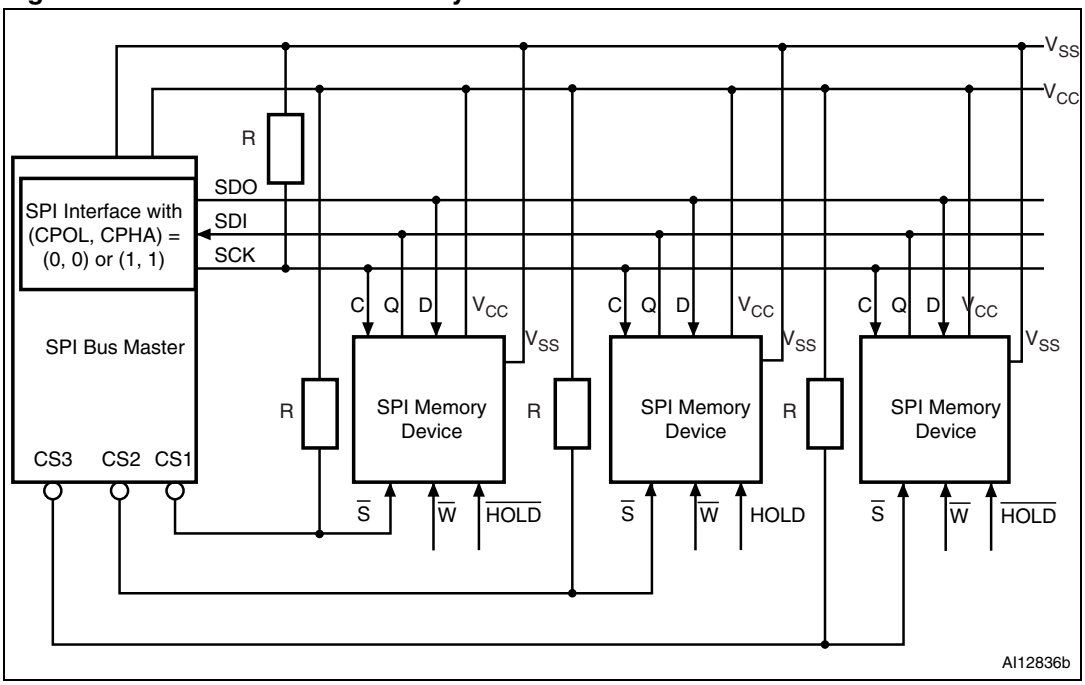
These devices are fully compatible with the SPI protocol.

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 4. shows three devices, connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the Serial Data output (Q) line at a time, all the others being high impedance.

Figure 4. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, high or low as appropriate.

Figure 4 shows an example of three memory devices connected to an MCU, on an SPI bus. Only one memory device is selected at a time, so only one memory device drives the Serial Data output (Q) line at a time, the other memory devices are high impedance.

The pull-up resistor R (represented in *Figure 4*) ensures that a device is not selected if the Bus Master leaves the $\overline{S}$ line in the high impedance state.

In applications where the Bus Master may be in a state where all input/output SPI buses are high impedance at the same time (for example, if the Bus Master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the $\overline{S}$ line is pulled high): this ensures that $\overline{S}$ and C do not become high at the same time, and so, that the t_{SHCH} requirement is met. The typical value of R is 100 kΩ

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3.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

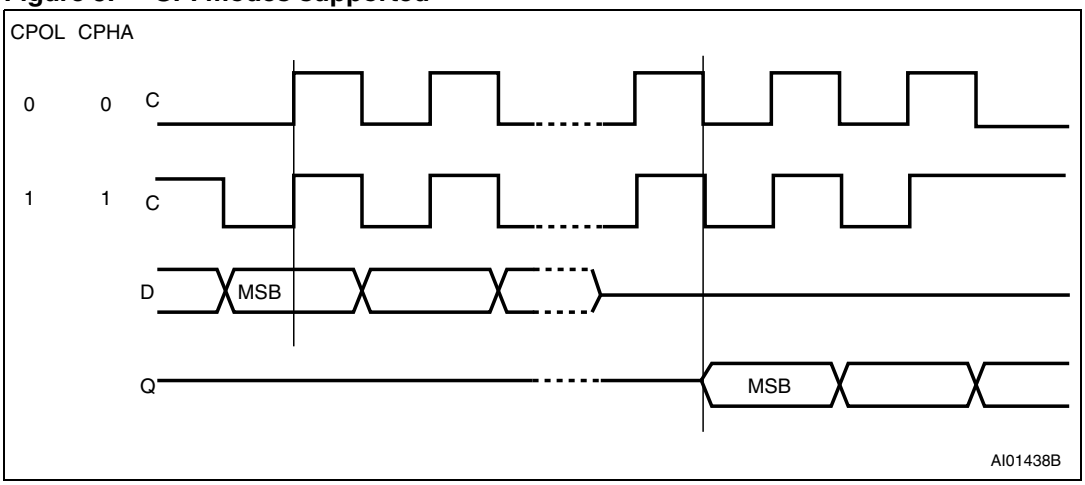
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 5.*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 5. SPI modes supported



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4 Operating features

4.1 Supply voltage (V_{CC})

4.1.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 9*, *Table 10* and *Table 11*). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

4.1.2 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until V_{CC} reaches the POR threshold voltage (this threshold is defined in DC characteristics tables *15*, *16*, *17*, *18*, *19* and *20* as V_{RES}).

When V_{CC} passes over the POR threshold, the device is reset and is in the following state:

- in Standby Power mode
- deselected (note that, to be executed, an instruction must be preceded by a falling edge on Chip Select ($\overline{S}$))
- Status Register value:
  - the Write Enable Latch (WEL) is reset to 0
  - Write In Progress (WIP) is reset to 0
  - The SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits)

When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode. The device must not be accessed until V_{CC} reaches a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range defined in *Table 9*, *Table 10* and *Table 11*.

4.1.3 Power-up conditions

When the power supply is turned on, V_{CC} rises continuously from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage. It is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see *Figure 4*).

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been high, prior to going low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in *Table 9*, *Table 10* and *Table 11* and the rise time must not vary faster than 1 V/µs.

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4.1.4 Power-down

During power-down (continuous decrease in the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined in *Table 9*, *Table 10* and *Table 11*), the device must be:

- deselected (Chip Select $\overline{S}$ should be allowed to follow the voltage applied on V_{CC})
- in Standby Power mode (there should not be any internal write cycle in progress).

4.2 Active Power and Standby Power modes

When Chip Select ($\overline{S}$) is low, the device is selected, and in the Active Power mode. The device consumes I_{CC}, as specified in *Table 14.* to *Table 19.*

When Chip Select ($\overline{S}$) is high, the device is deselected. If a Write cycle is not currently in progress, the device then goes into the Standby Power mode, and the device consumption drops to I_{CC1}.

4.3 Hold condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) low.

Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold ($\overline{HOLD}$) signal is driven low at the same time as Serial Clock (C) already being low.

The Hold condition ends when the Hold ($\overline{HOLD}$) signal is driven high at the same time as Serial Clock (C) already being low.

4.4 Status Register

Figure 6. shows the position of the Status Register in the control logic of the device. The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See *Section 6.3: Read Status Register (RDSR)* for a detailed description of the Status Register bits

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4.5 Data protection and protocol control

Non-volatile memory devices can be used in environments that are particularly noisy, and within applications that could experience problems if memory bytes are corrupted. Consequently, the device features the following data protection mechanisms:

- Write and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Write (WRITE) instruction completion
- The Block Protect (BP1, BP0) bits in the Status Register allow part of the memory to be configured as read-only.
- The Write Protect ($\overline{W}$) signal allows the Block Protect (BP1, BP0) bits of the Status Register to be protected.

For any instruction to be accepted, and executed, Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) for the last bit of the instruction, and before the next rising edge of Serial Clock (C).

Two points need to be noted in the previous sentence:

- The ‘last bit of the instruction’ can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for Read Status Register (RDSR) and Read (READ) instructions).
- The ‘next rising edge of Serial Clock (C)’ might (or might not) be the next bus transaction for some other device on the SPI bus.

Table 3. Write-protected block size

Status Register bits		Protected block	Protected array addresses	
BP1	BP0		M95160-x	M95080-x
0	0	none	none	none
0	1	Upper quarter	0600h - 07FFh	0300h - 03FFh
1	0	Upper half	0400h - 07FFh	0200h - 03FFh
1	1	Whole memory	0000h - 07FFh	0000h - 03FFh

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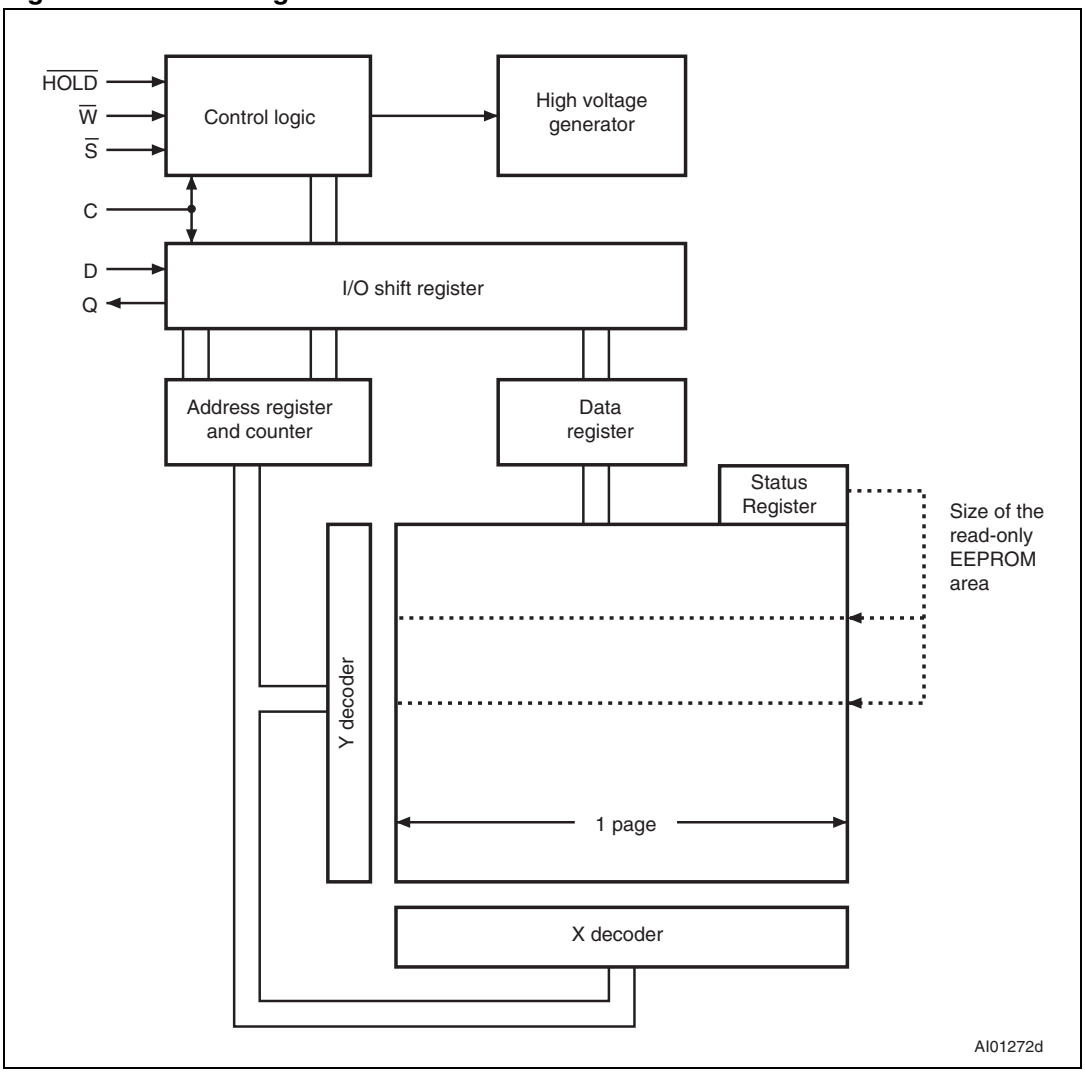
5 Memory organization

The memory is organized as shown in *Figure 6.*

Figure 6. Block diagram



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6 Instructions

Each instruction starts with a single-byte code, as summarized in *Table 4.*

If an invalid instruction is sent (one not contained in *Table 4.*), the device automatically deselects itself.

Table 4. Instruction set

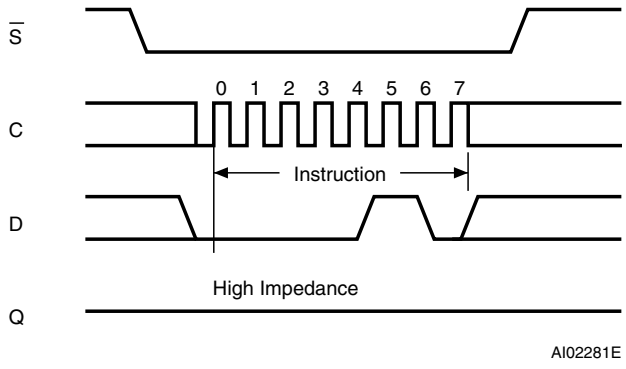
Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

6.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in *Figure 7.*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

Figure 7. Write Enable (WREN) sequence



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6.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

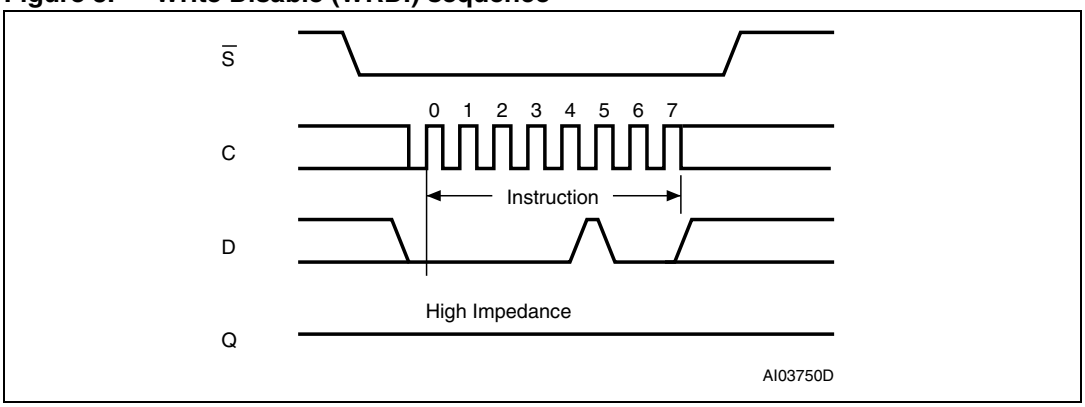
As shown in *Figure 8.*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.

Figure 8. Write Disable (WRDI) sequence



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6.3 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in *Figure 9.*

The status and control bits of the Status Register are as follows:

6.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

6.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write or Write Status Register instruction is accepted.

6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in *Table 5.*) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

6.3.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Table 5. Status Register format

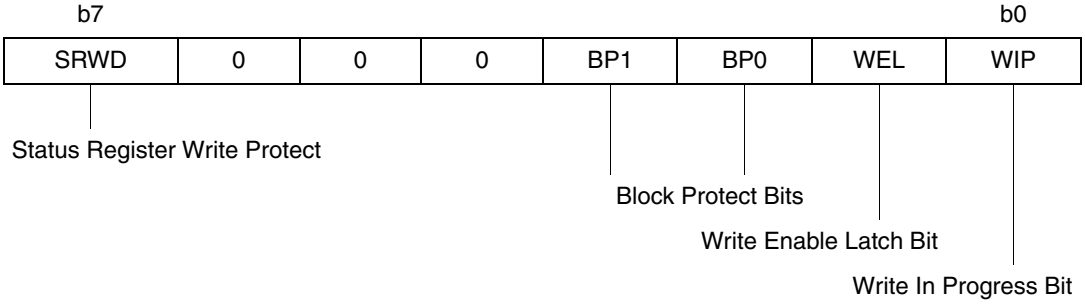

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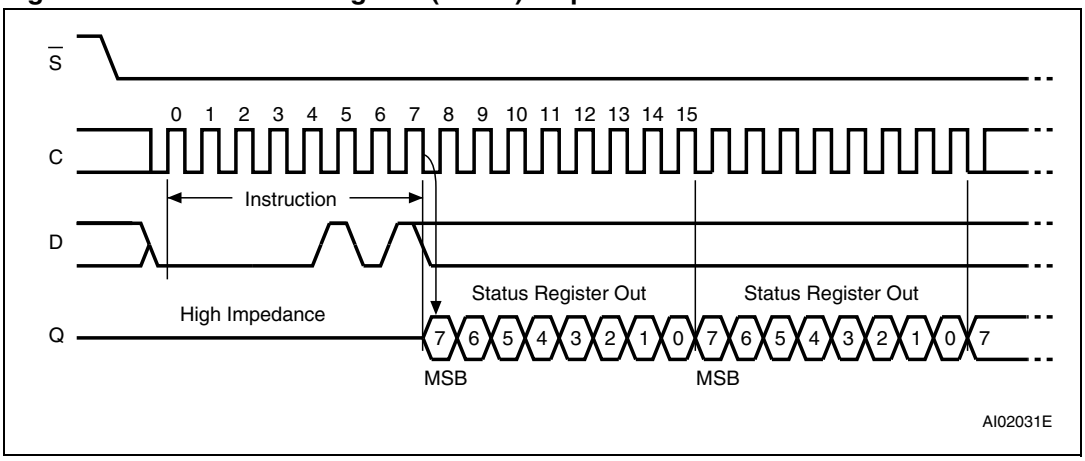
Figure 9. Read Status Register (RDSR) sequence



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6.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed.

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) low, followed by the instruction code, the data byte on Serial Data input (D) and Chip Select ($\overline{S}$) driven high. Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Write Status Register (WRSR) instruction is not executed.

The instruction sequence is shown in *Figure 10.*

Driving the Chip Select ($\overline{S}$) signal high at a byte boundary of the input data triggers the self-timed write cycle that takes t_W to complete (as specified in *Table 21*, *Table 22*, *Table 23*, *Table 24*, *Table 26* and *Table 27*).

While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write in progress (WIP) bit: the WIP bit is 1 during the self-timed write cycle t_W, and, 0 when the write cycle is complete. The WEL bit (Write enable latch) is also reset at the end of the write cycle t_W.

The Write Status Register (WRSR) instruction allows the user to change the values of the BP1, BP0 and SRWD bits:

- The Block Protect (BP1, BP0) bits define the size of the area that is to be treated as read only, as defined in *Table 3*.
- The SRWD bit (Status Register Write Disable bit), in accordance with the signal read on the Write Protect pin ($\overline{W}$), allows the user to set or reset the Write protection mode of the Status Register itself, as defined in *Table 6*. When in Write-protected mode, the Write Status Register (WRSR) instruction is not executed.

The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the t_W Write cycle.

The Write Status Register (WRSR) instruction has no effect on the b6, b5, b4, b1, b0 bits in the Status Register. Bits b6, b5, b4 are always read as 0.

Table 6. Protection modes

$\overline{W}$ signal	SRWD bit	Mode	Write protection of the Status Register	Memory content	
				Protected area(1)	Unprotected area(1)
1	0	Software-protected (SPM)	Status Register is writable (if the WREN instruction has set the WEL bit) The values in the BP1 and BP0 bits can be changed	Write-protected	Ready to accept Write instructions
0	0				
1	1				
0	1	Hardware-protected (HPM)	Status Register is Hardware write-protected The values in the BP1 and BP0 bits cannot be changed	Write-protected	Ready to accept Write instructions

1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register, as shown in *Table 3*.

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The protection features of the device are summarized in *Table 6*.

When the Status Register Write Disable (SRWD) bit in the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction), regardless of the logic level applied on the Write Protect ($\overline{W}$) input pin.

When the Status Register Write Disable (SRWD) bit in the Status Register is set to 1, two cases need to be considered, depending on the state of the Write Protect ($\overline{W}$) input pin:

- If Write Protect ($\overline{W}$) is driven high, it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction.
- If Write Protect ($\overline{W}$) is driven low, it is not possible to write to the Status Register even if the WEL bit has previously been set by a WREN instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area, which are software-protected (SPM) by the Block Protect (BP1, BP0) bits in the Status Register, are also hardware-protected against data modification.

Regardless of the order of the two events, the Hardware-protected mode (HPM) can be entered by:

- either setting the SRWD bit after driving the Write Protect ($\overline{W}$) input pin low
- or driving the Write Protect ($\overline{W}$) input pin low after setting the SRWD bit

Once the Hardware-protected mode (HPM) has been entered, the only way of exiting it is to pull high the Write Protect ($\overline{W}$) input pin.

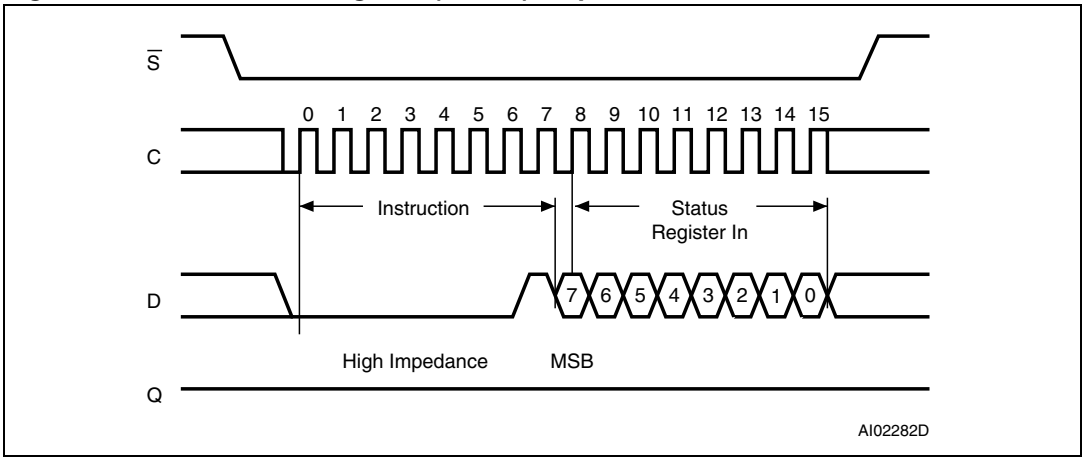
If the Write Protect ($\overline{W}$) input pin is permanently tied high, the Hardware-protected mode (HPM) can never be activated, and only the Software-protected mode (SPM), using the Block Protect (BP1, BP0) bits in the Status Register, can be used.

Table 7. Address range bits(1)

Device	M95160-x	M95080-x
Address bits	A10-A0	A9-A0

1. b15 to b11 are Don't Care on the M95160-x.
b15 to b10 are Don't Care on the M95080-x.

Figure 10. Write Status Register (WRSR) sequence



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6.5 Read from Memory Array (READ)

As shown in *Figure 11.*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte and address bytes are then shifted in, on Serial Data Input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

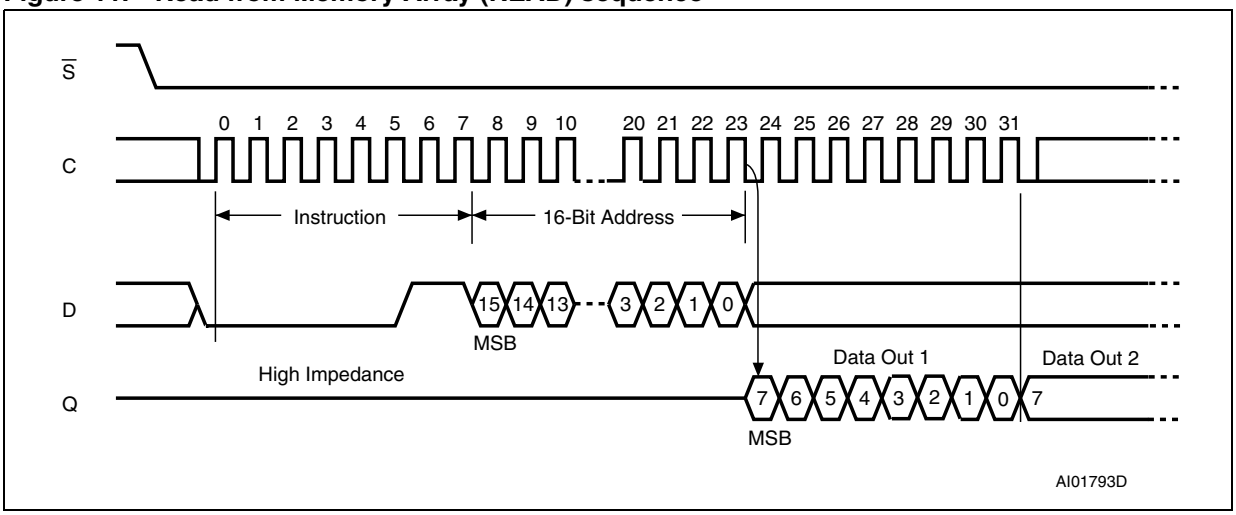
When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Figure 11. Read from Memory Array (READ) sequence



1. Depending on the memory size, as shown in *Table 7.*, the most significant address bits are Don't Care.

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6.6 Write to Memory Array (WRITE)

As shown in *Figure 12.*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. The self-timed Write cycle, triggered by the Chip Select ($\overline{S}$) rising edge, continues for a period t_W (as specified in *Table 22.* to *Table 26.*), at the end of which the Write in Progress (WIP) bit is reset to 0.

In the case of *Figure 12.*, Chip Select ($\overline{S}$) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. If, though, Chip Select ($\overline{S}$) continues to be driven low, as shown in *Figure 13.*, the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle.

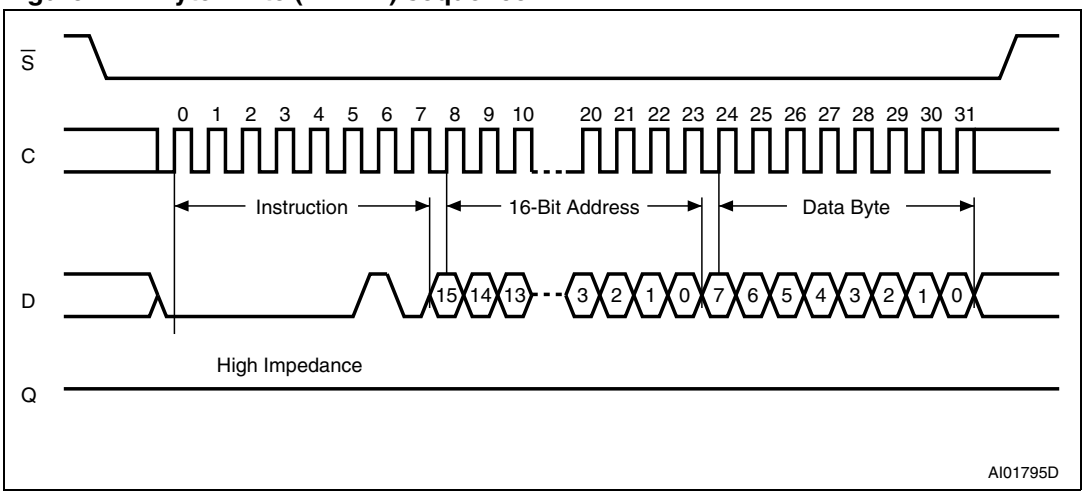
Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there are overwritten with the incoming data. (The page size of these devices is 32 bytes).

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a Write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in)
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

Note: The self-timed write cycle t_W is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as "0" and a programmed bit is read as "1".

Figure 12. Byte Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 7.*, the most significant address bits are Don't Care.

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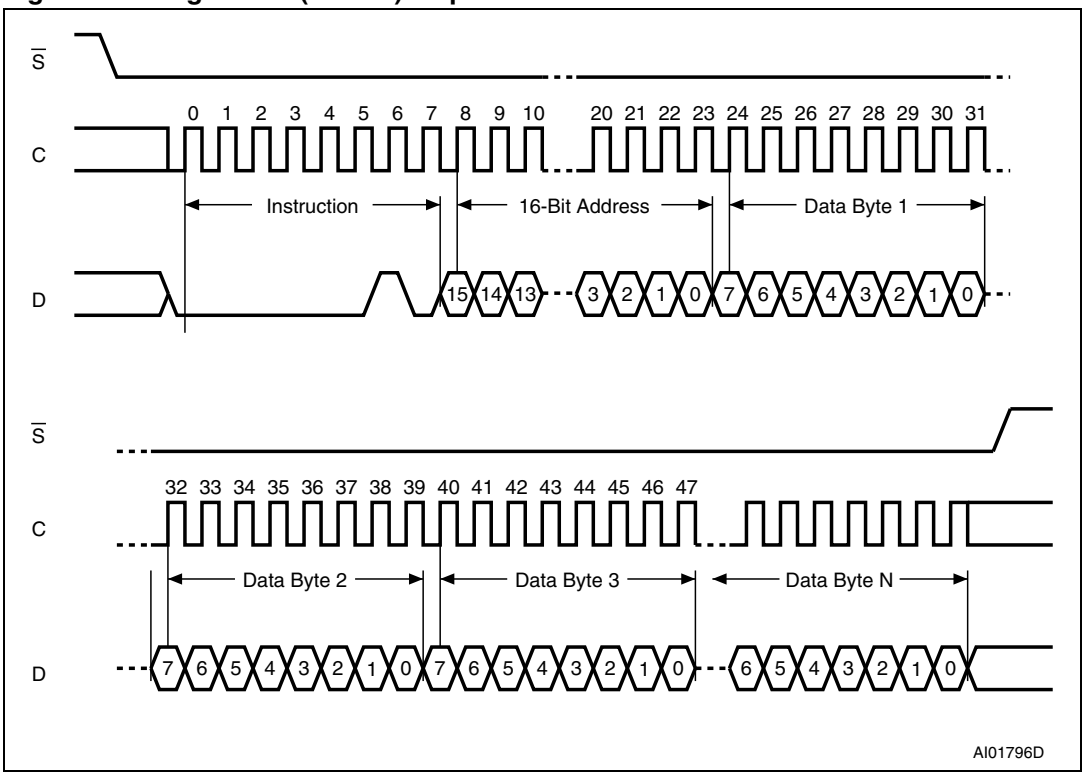
Figure 13. Page Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 7.*, the most significant address bits are Don't Care.

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7 Delivery state

7.1 Initial delivery state

The device is delivered with the memory array set at all 1s (FFh). The Status Register Write Disable (SRWD) and Block Protect (BP1 and BP0) bits are initialized to 0.

8 Maximum rating

Stressing the device outside the ratings listed in *Table 8.* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 8. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_O	Output voltage	–0.50	V_{CC}+0.6	V
V_I	Input voltage	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model)(2)	–4000	4000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU
2. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω, R2=500 Ω)

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9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 9. Operating conditions (M95160 and M95080)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	4.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 3)	–40	125	°C

Table 10. Operating conditions (M95160-W and M95080-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 3)	–40	125	°C

Table 11. Operating conditions (M95160-R and M95080-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 12. Operating conditions (M95160-F)(1)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	–40	85	°C

1. Preliminary data.

Table 13. AC measurement conditions(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_L	Load capacitance		30		pF
	Input rise and fall times			50	ns
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$			V
	Input and output timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$			V

1. Output Hi-Z is defined as the point where data out is no longer driven.

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Figure 14. AC measurement I/O waveform

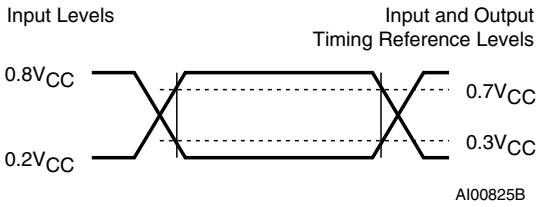

Table 14. Capacitance(1)

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (D)	V_{IN} = 0 V		8	pF
	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Sampled only, not 100% tested, at T_A = 25 °C and a frequency of 5 MHz.

Table 15. DC characteristics (M95160 and M95080, device grade 3)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current	C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 5 V, Q = open		3	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, V_{CC} = 5 V, $V_{IN} = V_{SS}$ or V_{CC}		5	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL} (1)	Output low voltage	I_{OL} = 2 mA, V_{CC} = 5 V		0.4	V
V_{OH} (1)	Output high voltage	I_{OH} = –2 mA, V_{CC} = 5 V	0.8 V_{CC}		V
V_{RES}(2)	Internal reset threshold voltage		2.5	3.5	V

1. For all 5 V range devices, the device meets the output requirements for both TTL and CMOS standards.
2. Characterized only, not 100% tested.

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Table 16. DC characteristics (M95160 and M95080, device grade 6)

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current	C = 0.1V_{CC}/0.9V_{CC} at 10 MHz, V_{CC} = 5 V, Q = open		5	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, V_{CC} = 5 V, $V_{IN} = V_{SS}$ or V_{CC}		2	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}(1)	Output low voltage	I_{OL} = 2 mA, V_{CC} = 5 V		0.4	V
V_{OH} (1)	Output high voltage	I_{OH} = –2 mA, V_{CC} = 5 V	0.8 V_{CC}		V
V_{RES}(2)	Internal reset threshold voltage		2.5	3.5	V

1. For all 5 V range devices, the device meets the output requirements for both TTL and CMOS standards.
2. Characterized only, not 100% tested.

Table 17. DC characteristics (M95160-W and M95080-W, device grade 3)

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current	C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 2.5 V, Q = open		2	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, V_{CC} = 2.5 V, $V_{IN} = V_{SS}$ or V_{CC}		2	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 1.5 mA, V_{CC} = 2.5 V		0.4	V
V_{OH}	Output high voltage	I_{OH} = –0.4 mA, V_{CC} = 2.5 V	0.8 V_{CC}		V
V_{RES}(1)	Internal reset threshold voltage		1.0	1.65	V

1. Characterized only, not 100% tested.

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Table 18. DC characteristics (M95160-W and M95080-W, device grade 6)

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current	C = $0.1V_{CC}/0.9V_{CC}$ at 5 MHz, V_{CC} = 2.5V, Q = open, Process SA		2	mA
		C = $0.1V_{CC}/0.9V_{CC}$ at 10 MHz, V_{CC} = 2.5 V, Q = open, Process GB or SB		5	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, 2.5 V <V_{CC} < 5.5 V $V_{IN} = V_{SS}$ or V_{CC}		2	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 1.5 mA, V_{CC} = 2.5 V		0.4	V
V_{OH}	Output high voltage	I_{OH} = –0.4 mA, V_{CC} = 2.5 V	0.8 V_{CC}		V
V_{RES}(1)	Internal reset threshold voltage		1.0	1.65	V

1. Characterized only, not 100% tested.

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Table 19. DC characteristics (M95160-R and M95080-R)(1)

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	S = V_{CC}, voltage applied on Q = V_{SS} or V_{CC}		± 2	µA
I_{CCR}	Supply current (Read)	V_{CC} = 2.5 V, C = 0.1 V_{CC} or 0.9V_{CC}, f_C = 5 MHz, Q = open		3	mA
		V_{CC} = 1.8 V, C = 0.1V_{CC} or 0.9V_{CC} at max clock frequency, Q = open		2	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 5.0 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		2	µA
		V_{CC} = 2.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		1	µA
		V_{CC} = 1.8 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		1	µA
V_{IL}	Input low voltage	2.5V < V_{CC} < 5.5V	–0.45	0.3V_{CC}	V
		1.8V < V_{CC} < 2.5V	–0.45	0.25V_{CC}	V
V_{IH}	Input high voltage	2.5V < V_{CC} < 5.5V	0.7V_{CC}	V_{CC}+1	V
		1.8V < V_{CC} < 2.5V	0.75V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	V_{CC} = 2.5 V, I_{OL} = 1.5 mA, or V_{CC} = 5.5 V, I_{OL} = 2 mA		0.2V_{CC}	V
		V_{CC} = 1.8 V, I_{OL} = 0.15 mA		0.3	V
V_{OH}	Output high voltage	V_{CC} = 2.5 V, I_{OH} = –0.4 mA, or V_{CC} = 5.5 V, I_{OH} = –2 mA, or V_{CC} = 1.8 V, I_{OH} = –0.1 mA	0.8V_{CC}		V
V_{RES}(2)	Internal reset threshold voltage		1.0	1.65	V

1. If the application uses the M95080-R and M95160-R at 2.5 V ≤V_{CC} ≤5.5 V and –40 °C ≤T_A ≤+85 °C, please refer to *Table 16: DC characteristics (M95160 and M95080, device grade 6)* instead of the above table.
2. Characterized only, not 100% tested.

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Table 20. DC characteristics (M95160-F)

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	S = V_{CC}, voltage applied on Q = V_{SS} or V_{CC}		± 2	µA
I_{CCR}	Supply current (Read)	V_{CC} = 2.5 V, C = 0.1 V_{CC} or 0.9V_{CC}, f_C = 5 MHz, Q = open		3	mA
		V_{CC} = 1.7 V, C = 0.1V_{CC} or 0.9V_{CC} at max clock frequency, Q = open		2	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 5.0 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		2	µA
		V_{CC} = 2.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		1	µA
		V_{CC} = 1.7 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		1	µA
V_{IL}	Input low voltage	2.5 V < V_{CC} < 5.5 V	–0.45	0.3V_{CC}	V
		1.8 < V_{CC} < 2.5 V	–0.45	0.25V_{CC}	V
		1.7 V < V_{CC} < 1.8 V	–0.45	0.20V_{CC}	V
V_{IH}	Input high voltage	2.5 V < V_{CC} < 5.5 V	0.7V_{CC}	V_{CC}+1	V
		1.7 V < V_{CC} < 2.5 V	0.75V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	V_{CC} = 2.5 V, I_{OL} = 1.5 mA, or V_{CC} = 5.5 V, I_{OL} = 2 mA		0.2V_{CC}	V
		V_{CC} = 1.7 V, I_{OL} = 0.15 mA		0.2	V
V_{OH}	Output high voltage	V_{CC} = 2.5 V, I_{OH} = –0.4 mA, or V_{CC} = 5.5 V, I_{OH} = –2 mA, or V_{CC} = 1.7 V, I_{OH} = –0.1 mA	0.8V_{CC}		V
V_{RES}(1)	Internal reset threshold voltage		1.0	1.65	V

1. Characterized only, not 100% tested.

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Table 21. AC characteristics (M95160 and M95080, device grade 3)

Test conditions specified in *Table 13.* and *Table 9.*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		ns
t_{CH} (1)	t_{CLH}	Clock high time	90		ns
t_{CL} (1))	t_{CLL}	Clock low time	90		ns
t_{CLCH} (2)	t_{RC}	Clock rise time		1	µs
t_{CHCL} (2)	t_{FC}	Clock fall time		1	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	30		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		100	ns
t_{CLQV}	t_V	Clock low to output valid		60	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		50	ns
t_{QHQL}(2)	t_{FO}	Output fall time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		100	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.

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Table 22. AC characteristics (M95160 and M95080, device grade 6)

Test conditions specified in *Table 13.* and *Table 9.*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	15		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	15		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	25		ns
t_{CHSL}		$\overline{S}$ not active hold time	15		ns
t_{CH}(1)	t_{CLH}	Clock high time	40		ns
t_{CL} (1)	t_{CLL}	Clock low time	40		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		1	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		1	µs
t_{DVCH}	t_{DSU}	Data in setup time	15		ns
t_{CHDX}	t_{DH}	Data in hold time	15		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	15		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	20		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		25	ns
t_{CLQV}	t_V	Clock low to output valid		35	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		20	ns
t_{QHQL}(2)	t_{FO}	Output fall time		20	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		25	ns
t_{HLQZ} ((2))	t_{HZ}	$\overline{HOLD}$ low to output high-Z		35	ns
t_W	t_{WC}	Write Time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.

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Table 23. AC characteristics (M95160-W and M95080-W, device grade 3)

Test conditions specified in *Table 13.* and *Table 10.*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		ns
t_{CH}(1)	t_{CLH}	Clock high time	90		ns
t_{CL}(1)	t_{CLL}	Clock low time	90		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		1	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		1	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	30		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		100	ns
t_{CLQV}	t_V	Clock low to output valid		60	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		50	ns
t_{QHQL}(2)	t_{FO}	Output fall time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		100	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.

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Table 24. AC characteristics (M95160-W and M95080-W, device grade 6)

Test conditions specified in *Table 13.* and *Table 10.*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	30		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	30		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	30		ns
t_{CHSL}		$\overline{S}$ not active hold time	30		ns
t_{CH}(1)	t_{CLH}	Clock high time	40		ns
t_{CL} (1)	t_{CLL}	Clock low time	40		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	10		ns
t_{CHDX}	t_{DH}	Data in hold time	10		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	30		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	30		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		40	ns
t_{CLQV}	t_V	Clock low to output valid		40(3)	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		40	ns
t_{QHQL}(2)	t_{FO}	Output fall time		40	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		40	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		40	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.
3. t_{CLQV} must be compatible with t_{CL} (clock low time): if the SPI bus master offers a Read setup time t_{SU} = 0 ns, t_{CL} can be equal to (or greater than) t_{CLQV}. In all other cases, t_{CL} must be equal to (or greater than) $t_{CLQV} + t_{SU}$.

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Table 25. AC characteristics for M95160-Wxx6/S and M95080-Wxx6/S

Test conditions specified in *Table 10* and *Table 13*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		ns
t_{CH}(1)	t_{CLH}	Clock high time	90		ns
t_{CL} (1)	t_{CLL}	Clock low time	90		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		1	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		1	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	30		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		100	ns
t_{CLQV}	t_V	Clock low to output valid		60	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		50	ns
t_{QHQL}(2)	t_{FO}	Output fall time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		100	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.

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Table 26. AC characteristics (M95160-R and M95080-R)

Test conditions specified in *Table 13* and *Table 11*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	60		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	60		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	90		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	60		ns
t_{CHSL}		$\overline{S}$ not active hold time	60		ns
t_{CH}(1)	t_{CLH}	Clock high time	80		ns
t_{CL}(1)	t_{CLL}	Clock low time	80		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	20		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	60		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	60		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		0
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		0
t_{SHQZ}(2)	t_{DIS}	Output disable time		80	ns
t_{CLQV}	t_V	Clock low to output valid		80	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		80	ns
t_{QHQL}(2)	t_{FO}	Output fall time		80	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		80	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		80	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.

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Table 27. AC characteristics (M95160-F)(1)

Test conditions specified in *Table 12*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	3.5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	85		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	85		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	120		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	85		ns
t_{CHSL}		$\overline{S}$ not active hold time	85		ns
t_{CH}(2)	t_{CLH}	Clock high time	110		ns
t_{CL}(1)	t_{CLL}	Clock low time	110		ns
t_{CLCH}(3)	t_{RC}	Clock rise time		2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	30		ns
t_{CHDX}	t_{DH}	Data in hold time	30		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	85		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	85		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		0
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		0
t_{SHQZ}(2)	t_{DIS}	Output disable time		120	ns
t_{CLQV}	t_V	Clock low to output valid		120	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		100	ns
t_{QHQL}(2)	t_{FO}	Output fall time		100	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		110	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		110	ns
t_W	t_{WC}	Write time		5	ms

1. Preliminary data.
2. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
3. Value guaranteed by characterization, not 100% tested in production.

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Figure 15. Serial input timing

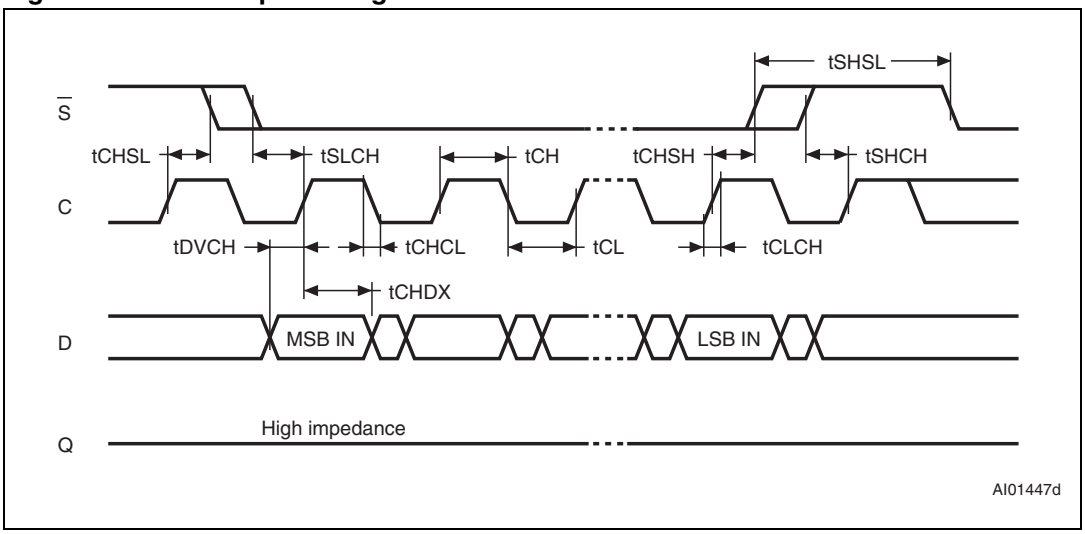

Figure 16. Hold timing

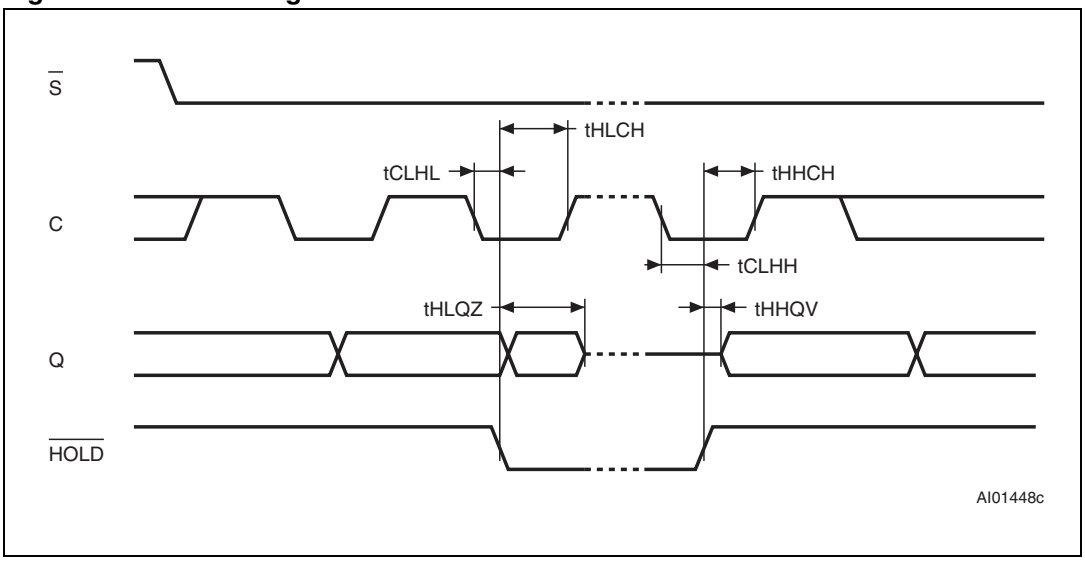

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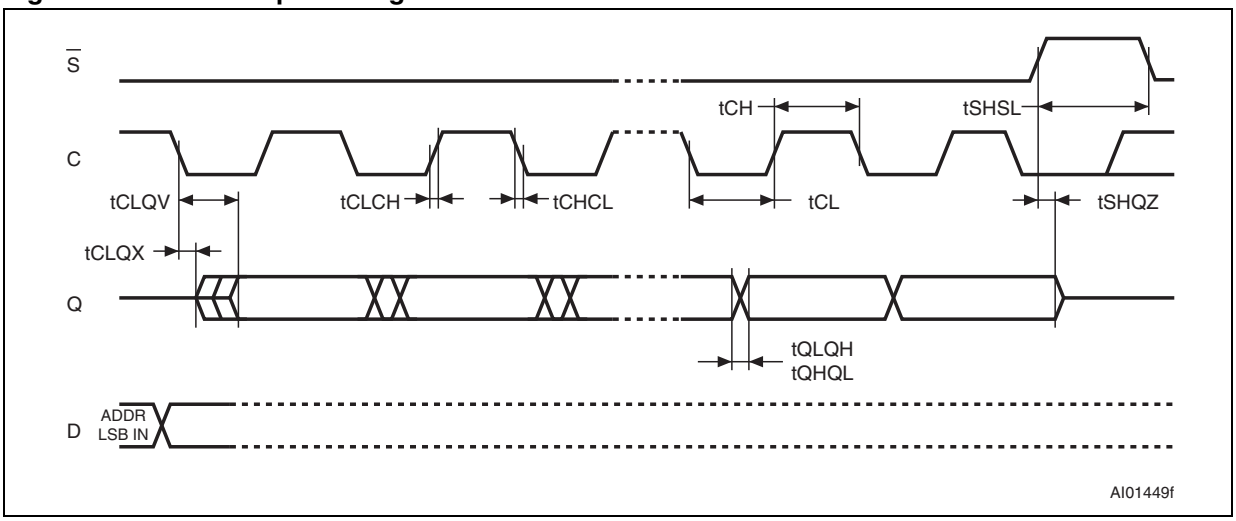
Figure 17. Serial output timing



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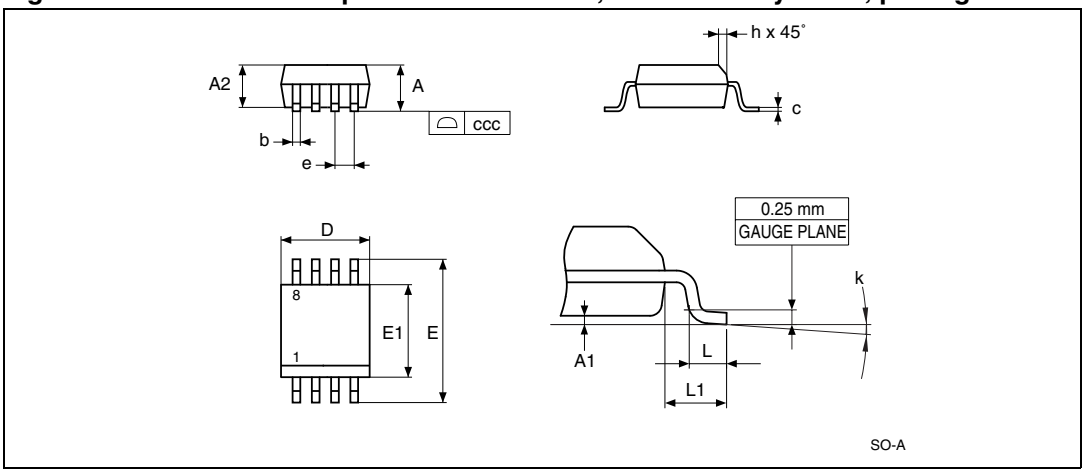
10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 18. SO8N – 8-lead plastic small outline, 150 mils body width, package outline



1. Drawing is not to scale.

Table 28. SO8N – 8-lead plastic small outline, 150 mils body width, mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.0689
A1		0.1	0.25		0.0039	0.0098
A2		1.25			0.0492	
b		0.28	0.48		0.011	0.0189
c		0.17	0.23		0.0067	0.0091
ccc			0.1			0.0039
D	4.9	4.8	5	0.1929	0.189	0.1969
E	6	5.8	6.2	0.2362	0.2283	0.2441
E1	3.9	3.8	4	0.1535	0.1496	0.1575
e	1.27	-	-	0.05	-	-
h		0.25	0.5		0.0098	0.0197
k		0°	8°		0°	8°
L		0.4	1.27		0.0157	0.05
L1	1.04			0.0409		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

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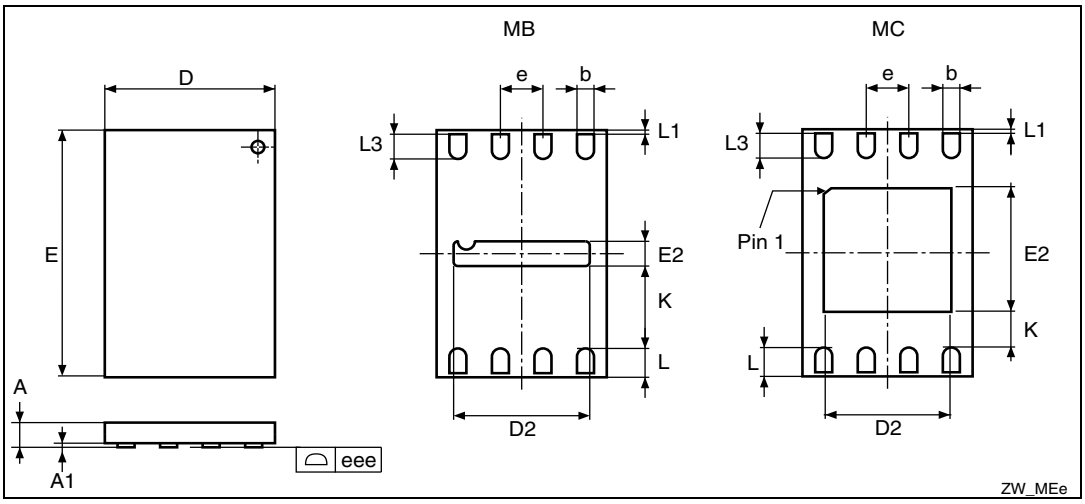
Figure 19. UFDFPN8 (MLP8) - 8-lead ultra thin fine pitch dual flat no lead, package outline



1. Drawing is not to scale.
2. The central pad (the area E2 by D2 in the above illustration) is internally pulled to V_{SS}. It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 29. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MB)	1.600	1.500	1.700	0.0630	0.0591	0.0669
D2 (rev MC)		1.200	1.600		0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MB)	0.200	0.100	0.300	0.0079	0.0039	0.0118
E2 (rev MC)		1.200	1.600		0.0472	0.0630
e	0.500			0.0197		
K (rev MB)		0.800			0.0315	
K (rev MC)		0.300			0.0118	
L		0.300	0.500		0.0118	0.0197
L1			0.150			0.0059
L3		0.300			0.0118	
eee(2)		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

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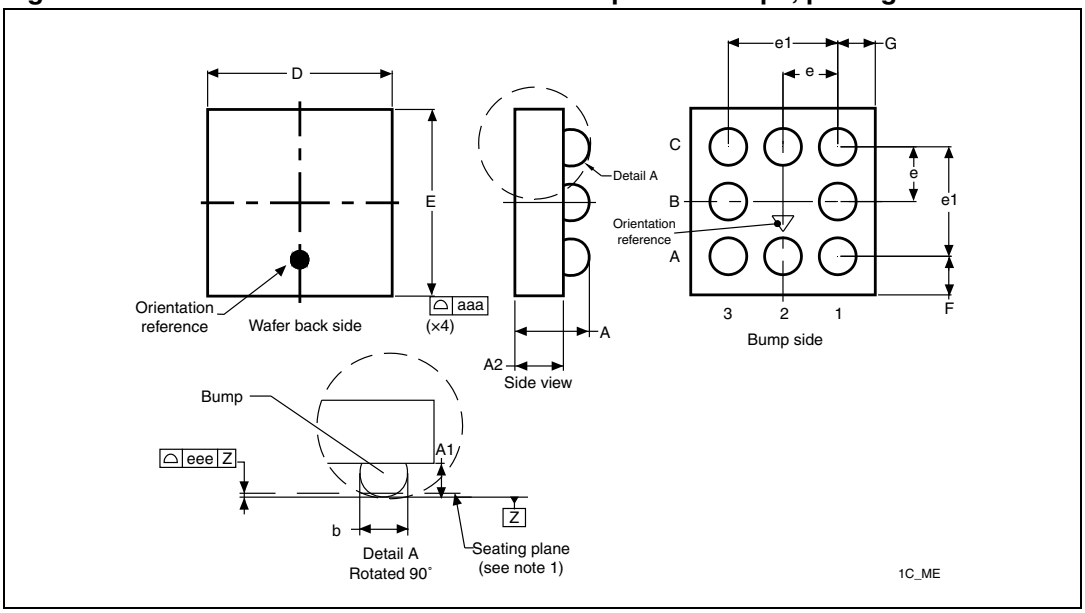
Figure 20. WLCSP-R 1.350 x 1.365 mm 0.4 mm pitch 8 bumps, package outline



1. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
2. Drawing is not to scale.
3. Preliminary data.

Table 30. WLCSP-R 1.350 x 1.365 mm 0.4 mm pitch 8 bumps, package mechanical data(1)

Symbol	millimeters			inches(2)		
	Typ	Min	Max	Typ	Min	Max
A	0.545	0.490	0.600	0.0193	0.0215	0.0236
A1	0.190			0.0075		
A2	0.355			0.014		
b(3)	0.270	0.240	0.300	0.0106	0.0094	0.0118
D	1.350		1.475	0.0531		0.0581
E	1.365		1.490	0.0537		0.0587
e	0.400			0.0157		
e1	0.800			0.0315		
F	0.282			0.0111		
G	0.275			0.0108		
N (total number of terminals)	8			8		
aaa	0.110			0.0043		
eee	0.060			0.0024		

1. Preliminary data.
2. Values in inches are converted from mm and rounded to 4 decimal digits.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

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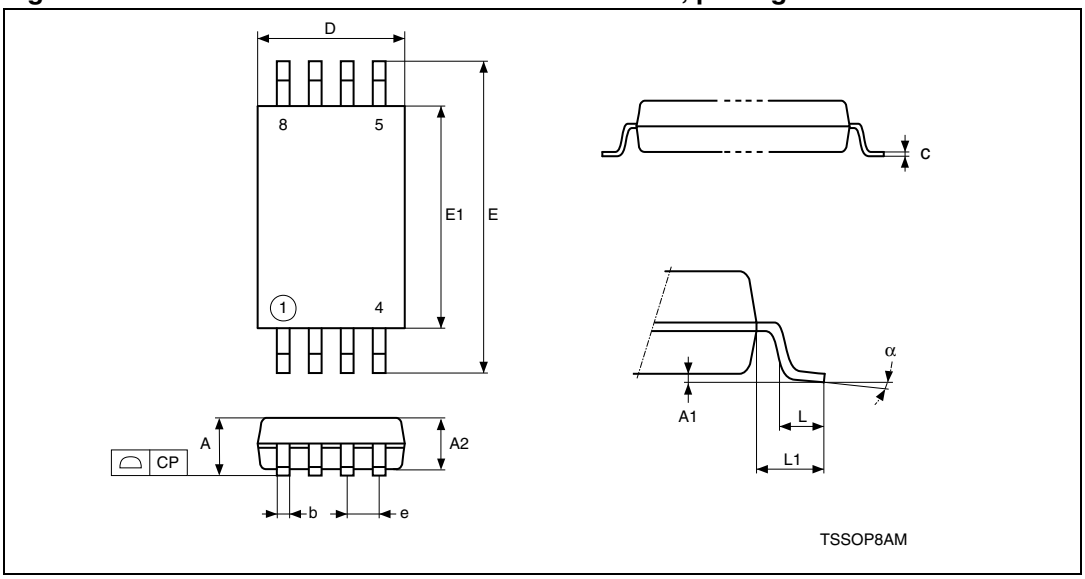
Figure 21. TSSOP8 – 8-lead thin shrink small outline, package outline



1. Drawing is not to scale.

Table 31. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.2			0.0472
A1		0.05	0.15		0.002	0.0059
A2	1	0.8	1.05	0.0394	0.0315	0.0413
b		0.19	0.3		0.0075	0.0118
c		0.09	0.2		0.0035	0.0079
CP			0.1			0.0039
D	3	2.9	3.1	0.1181	0.1142	0.122
e	0.65	-	-	0.0256	-	-
E	6.4	6.2	6.6	0.252	0.2441	0.2598
E1	4.4	4.3	4.5	0.1732	0.1693	0.1772
L	0.6	0.45	0.75	0.0236	0.0177	0.0295
L1	1			0.0394		
α		0°	8°		0°	8°
N	8			8		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

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11 Part numbering

Table 32. Ordering information scheme

Example: M95160 – W MN 6 T P /S

Device type

M95 = SPI serial access EEPROM

Device function

160 = 16 Kbit (2048 x 8)

080 = 8 Kbit (1024 x 8)

Operating voltage

blank = V_{CC} = 4.5 to 5.5 V

W = V_{CC} = 2.5 to 5.5 V

R = V_{CC} = 1.8 to 5.5 V

F = V_{CC} = 1.7 to 5.5 V

Package

MN = SO8 (150 mil width)

DW = TSSOP8

MB or MC(1) = UFDFPN8 (MLP8)

CS = WLCSP(2)

Device grade

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow

3 = Device tested with high reliability certified flow(3).
Automotive temperature range (–40 to 125 °C)

Option

blank = Standard packing

T = Tape and reel packing

Plating technology

G or P = ECOPACK® (RoHS compliant)

Process(4)

/G or /S = F6SP36%

1. For M95080 only.
2. Preliminary data.
3. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The high reliability certified flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
4. The Process letter (/G or /S) applies only to Range 3 devices. For Range 6 devices, the process letters do not appear in the Ordering Information but only appear on the device package (marking) and on the shipment box. Please contact your nearest ST Sales Office. For more information on how to identify products by the Process Identification Letter, please refer to AN2043: Serial EEPROM Device Marking.

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12 Revision history

Table 33. Document revision history

Date	Revision	Changes
19-Jul-2001	1.0	Document written from previous M95640/320/160/080 datasheet
06-Feb-2002	1.1	Announcement made of planned upgrade to 10MHz clock for the 5V, –40 to 85°C, range
18-Oct-2002	1.2	TSSOP8 (3x3mm body size, MSOP8) package added
04-Nov-2002	1.3	New products, identified by the process letter W, added
13-Nov-2002	1.4	Correction to footnote in Ordering Information table
21-Nov-2003	2.0	Table of contents, and Pb-free options added. V_{IL}(min) improved to –0.45V
08-Jun-2004	3.0	MLP8 package added. Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) improved. Soldering temperature information clarified for RoHS compliant devices. Device Grade 3 clarified, with reference to HRCF and automotive environments. Process identification letter “G” information added. SO8 narrow and TSSOP8 Package mechanical specifications updated.
07-Oct-2004	4.0	Product List summary table added. AEC-Q100-002 compliance. tHHQX corrected to tHHQV. 10MHz, 5ms Write is now the present product. tCH+tCL<1/fC constraint clarified
21-Sep-2005	5.0	Added 20MHz and -S product information. Removed DIP package. Info on Pull-up resistors, VCC lines and Note *2.* added to *Figure 4.: Bus master and memory devices on the SPI bus*. *Device internal reset* paragraph clarified. Packages compliant with the JEDEC Std J-STD-020C. Process info updated in *DC and AC parameters* and *Table 32.: Ordering information scheme*.

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Table 33. Document revision history (continued)

Date	Revision	Changes
24-May-2007	6	Document reformatted. Small text changes. TSSOP8 3 x 3 mm (DS) package removed, 1.65 V to 5.5 V operating voltage range removed (M95080-S and M95160-S removed). *Figure 4: Bus master and memory devices on the SPI bus* updated, note 2 removed and explanatory paragraph added (see *Section 3: Connecting to the SPI bus*). *Section 2.7: VCC supply voltage* and *Section 2.8: VSS ground* added. Power-up, Device Internal Reset and Power-down replaced by *Section 4.1: Supply voltage (VCC)*. Command termination specified in *Section 6.4: Write Status Register (WRSR)*. Blank process no longer available for M95160, M95080, M95160-W and M95080-W in the device grade 3 range. L, GB and SB processes no longer available for M95160 and M95080, in the device grade 6 range. L process no longer available for M95160-W and M95080-W in the device grade 6 range. I_{CC1} value and test conditions modified in *Table 19: DC characteristics (M95160-R and M95080-R)*. End timing line of t_{SHQZ} modified in *Figure 17: Serial output timing*. SO8N and UFDFPN8 package specifications updated. All packages are ECOPACK® compliant. Blank option removed below Plating technology and Note 2 modified in *Table 32: Ordering information scheme*. *Table 33: Available M95160 products (package, voltage range, temperature grade)* and *Table 34: Available M95080 products (package, voltage range, temperature grade)* added.
06-Mar-2008	7	Endurance modified *on page 1*. Small text changes. *Section 4.1: Supply voltage (VCC) on page 12* modified. *Section 6.6: Write to Memory Array (WRITE) on page 23* modified. *Table 19: DC characteristics (M95160-R and M95080-R)* updated. Note removed below *Table 24: AC characteristics (M95160-W and M95080-W, device grade 6) on page 35*. Inch values are calculated from millimeters and rounded to 4 decimal digits and UFDFPN package specifications updated (see *Section 10: Package mechanical data on page 41*).
26-Jan-2009	8	WLCSP (CS) package added (see *Figure 20* and *Table 30: WLCSP-R 1.350 x 1.365 mm 0.4 mm pitch 8 bumps, package mechanical data*). M95160-F part number added (delivered in WLCSP package and device grade 6 only). *Section 2.7: VCC supply voltage* and *Section 6.4: Write Status Register (WRSR)* updated. *Table 27: AC characteristics (M95160-F)* added. *Figure 15: Serial input timing*, *Figure 16: Hold timing* and *Figure 17: Serial output timing* updated.

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Table 33. Document revision history (continued)

Date	Revision	Changes
12-May-2009	9	*Section 4.1.2: Device reset* updated. V_{RES} added to DC characteristics tables *15*, *16*, *17*, *18*, *19* and *20*. Note added to *Section 6.6: Write to Memory Array (WRITE)*. *Note 1* added to *Table 19: DC characteristics (M95160-R and M95080-R)*. VIL and VOL modified in *Table 20: DC characteristics (M95160-F)*. *Table 24: AC characteristics (M95160-W and M95080-W, device grade 6)* split into two tables: *Table 24* for process GB or SB and *Table 25* for process SA. M95160-F is now available in device grade 6 (*Table 33: Available M95160 products (package, voltage range, temperature grade)* updated.
09-Oct-2009	10	Revision number of 12-May-2009 corrected in *Table 33: Document revision history*. V_{RES} corrected in *Table 15: DC characteristics (M95160 and M95080, device grade 3)* and *Table 16: DC characteristics (M95160 and M95080, device grade 6)*.
21-Jul-2011	11	MC package added (UFDFPN8) Two tables removed in *Section 11: Part numbering*.

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