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1 Description

The M93C86, M93C76, M93C66, M93C56 and M93C46 are electrically erasable programmable memory (EEPROM) devices. They are accessed through a Serial Data input (D) and Serial Data output (Q) using the MICROWIRE bus protocol.

Figure 1. Logic diagram

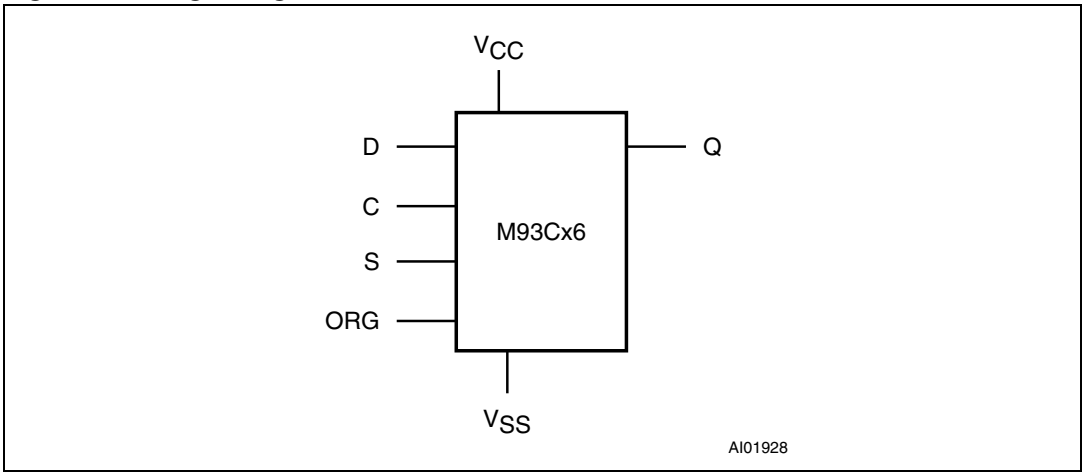


Table 2. Signal names

Signal name	Function	Direction
S	Chip Select	Input
D	Serial Data input	Input
Q	Serial Data output	Output
C	Serial Clock	Input
ORG	Organisation Select	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

The memory array organization may be divided into either bytes (x8) or words (x16) which may be selected by a signal applied on Organization Select (ORG). The bit, byte and word sizes of the memories are as shown in *Table 3.*

Table 3. Memory size versus organization

Device	Number of bits	Number of 8-bit bytes	Number of 16-bit words
M93C86	16384	2048	1024
M93C76	8192	1024	512
M93C66	4096	512	256
M93C56	2048	256	128
M93C46	1024	128	64

The M93Cx6 is accessed by a set of instructions, as summarized in *Table 4.*, and in more detail in *Table 5.* to *Table 7.*).

Table 4. Instruction set for the M93Cx6

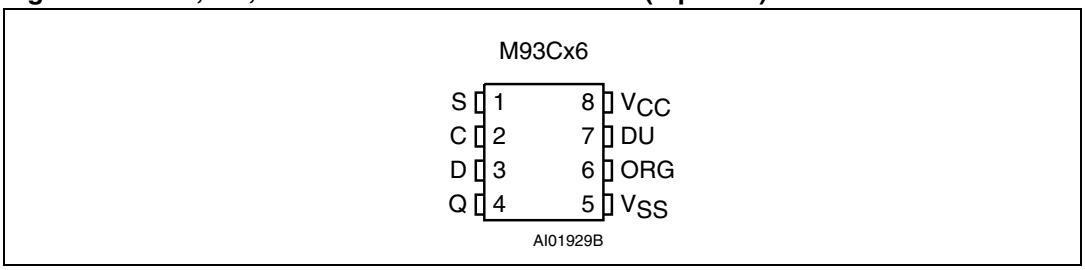
Instruction	Description	Data
READ	Read Data from Memory	Byte or Word
WRITE	Write Data to Memory	Byte or Word
WEN	Write Enable	
WDS	Write Disable	
ERASE	Erase Byte or Word	Byte or Word
ERAL	Erase All Memory	
WRAL	Write All Memory with same Data	

A Read Data from Memory (READ) instruction loads the address of the first byte or word to be read in an internal address register. The data at this address is then clocked out serially. The address register is automatically incremented after the data is output and, if Chip Select Input (S) is held High, the M93Cx6 can output a sequential stream of data bytes or words. In this way, the memory can be read as a data stream from eight to 16384 bits long (in the case of the M93C86), or continuously (the address counter automatically rolls over to 00h when the highest address is reached).

Programming is internally self-timed (the external clock signal on Serial Clock (C) may be stopped or left running after the start of a Write cycle) and does not require an Erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at a time into one of the byte or word locations of the M93Cx6. After the start of the programming cycle, a Busy/Ready signal is available on Serial Data Output (Q) when Chip Select Input (S) is driven High.

An internal Power-on Data Protection mechanism in the M93Cx6 inhibits the device when the supply is too low.

Figure 2. DIP, SO, TSSOP and MLP connections (top view)



1. See *Package mechanical data* section for package dimensions, and how to identify pin-1.
2. DU = Don't Use.

The DU (do not use) pin does not contribute to the normal operation of the device. It is reserved for use by STMicroelectronics during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}.

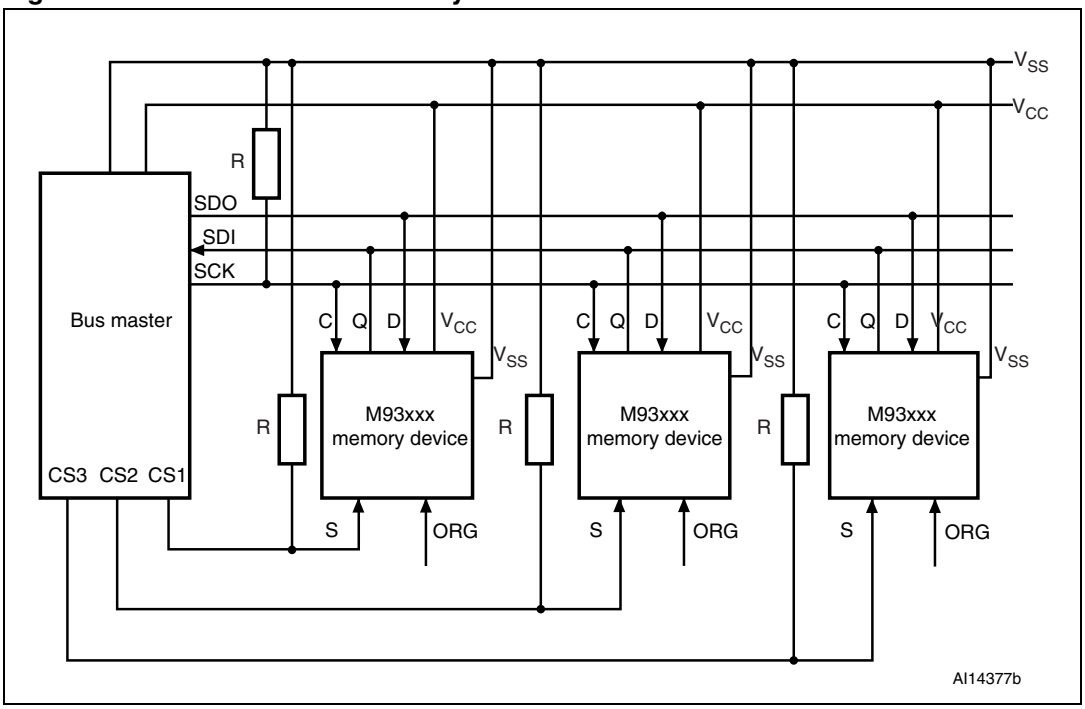
2 Connecting to the serial bus

Figure 3 shows an example of three memory devices connected to an MCU, on a serial bus. Only one device is selected at a time, so only one device drives the Serial Data output (Q) line at a time, the other devices are high impedance.

The pull-down resistor R (represented in *Figure 3*) ensures that no device is selected if the bus master leaves the S line in the high impedance state.

In applications where the bus master may be in a state where all inputs/outputs are high impedance at the same time (for example, if the bus master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the S line is pulled low): this ensures that C does not become high at the same time as S goes low, and so, that the t_{SLCH} requirement is met. The typical value of R is 100 kΩ

Figure 3. Bus master and memory devices on the serial bus



3 Operating features

3.1 Supply voltage (V_{CC})

3.1.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied. In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

3.1.2 Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. During this time, the Chip Select (S) line is not allowed to float and should be driven to V_{SS}, it is therefore recommended to connect the S line to V_{SS} via a suitable pull-down resistor.

The V_{CC} rise time must not vary faster than 1 V/µs.

3.1.3 Power-up and device reset

In order to prevent inadvertent Write operations during power-up, a power on reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the device does not respond to any instruction until V_{CC} has reached the power on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 9*, *Table 10* and *Table 11*).

When V_{CC} passes the POR threshold, the device is reset and is in the following state:

- Standby Power mode
- deselected (assuming that there is a pull-down resistor on the S line)

3.1.4 Power-down

At power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops from the normal operating voltage to below the power on reset threshold voltage, the device stops responding to any instruction sent to it.

During power-down, the device must be deselected and in the Standby Power mode (that is, there should be no internal Write cycle in progress).

4 Memory organization

The M93Cx6 memory is organized either as bytes (x8) or as words (x16). If Organization Select (ORG) is left unconnected (or connected to V_{CC}) the x16 organization is selected; when Organization Select (ORG) is connected to Ground (V_{SS}) the x8 organization is selected. When the M93Cx6 is in Standby mode, Organization Select (ORG) should be set either to V_{SS} or V_{CC} for minimum power consumption. Any voltage between V_{SS} and V_{CC} applied to Organization Select (ORG) may increase the Standby current.

5 Instructions

The instruction set of the M93Cx6 devices contains seven instructions, as summarized in *Table 5.* to *Table 7.*. Each instruction consists of the following parts, as shown in *Figure 4.*:

- Each instruction is preceded by a rising edge on Chip Select Input (S) with Serial Clock (C) being held low.
- A start bit, which is the first '1' read on Serial Data Input (D) during the rising edge of Serial Clock (C).
- Two op-code bits, read on Serial Data Input (D) during the rising edge of Serial Clock (C). (Some instructions also use the first two bits of the address to define the op-code).
- The address bits of the byte or word that is to be accessed. For the M93C46, the address is made up of 6 bits for the x16 organization or 7 bits for the x8 organization (see *Table 5.*). For the M93C56 and M93C66, the address is made up of 8 bits for the x16 organization or 9 bits for the x8 organization (see *Table 6.*). For the M93C76 and M93C86, the address is made up of 10 bits for the x16 organization or 11 bits for the x8 organization (see *Table 7.*).

The M93Cx6 devices are fabricated in CMOS technology and are therefore able to run as slow as 0 Hz (static input signals) or as fast as the maximum ratings specified in *Table 20.* to *Table 23.*.

Table 5. Instruction set for the M93C46

Instruction	Description	Start bit	Op-code	x8 origination (ORG = 0)			x16 origination (ORG = 1)		
				Address (1)	Data	Required clock cycles	Address (1)	Data	Required clock cycles
READ	Read Data from Memory	1	10	A6-A0	Q7-Q0		A5-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A6-A0	D7-D0	18	A5-A0	D15-D0	25
WEN	Write Enable	1	00	11X XXXX		10	11 XXXX		9
WDS	Write Disable	1	00	00X XXXX		10	00 XXXX		9
ERASE	Erase Byte or Word	1	11	A6-A0		10	A5-A0		9
ERAL	Erase All Memory	1	00	10X XXXX		10	10 XXXX		9
WRAL	Write All Memory with same Data	1	00	01X XXXX	D7-D0	18	01 XXXX	D15-D0	25

1. X = Don't Care bit.

Table 6. Instruction set for the M93C56 and M93C66

Instruction	Description	Start bit	Op-code	x8 origination (ORG = 0)			x16 origination (ORG = 1)		
				Address (1) (2)	Data	Required clock cycles	Address (1) (3)	Data	Required clock cycles
READ	Read Data from Memory	1	10	A8-A0	Q7-Q0		A7-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A8-A0	D7-D0	20	A7-A0	D15-D0	27
WEN	Write Enable	1	00	1 1XXX XXXX		12	11XX XXXX		11
WDS	Write Disable	1	00	0 0XXX XXXX		12	00XX XXXX		11
ERASE	Erase Byte or Word	1	11	A8-A0		12	A7-A0		11
ERAL	Erase All Memory	1	00	1 0XXX XXXX		12	10XX XXXX		11
WRAL	Write All Memory with same Data	1	00	0 1XXX XXXX	D7-D0	20	01XX XXXX	D15-D0	27

1. X = Don't Care bit.
2. Address bit A8 is not decoded by the M93C56.
3. Address bit A7 is not decoded by the M93C56.

Table 7. Instruction set for the M93C76 and M93C86

Instruction	Description	Start bit	Op-code	x8 Origination (ORG = 0)			x16 Origination (ORG = 1)		
				Address(1), (2)	Data	Required clock cycles	Address (1) (3)	Data	Required clock cycles
READ	Read Data from Memory	1	10	A10-A0	Q7-Q0		A9-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A10-A0	D7-D0	22	A9-A0	D15-D0	29
WEN	Write Enable	1	00	11X XXXX XXXX		14	11 XXXX XXXX		13
WDS	Write Disable	1	00	00X XXXX XXXX		14	00 XXXX XXXX		13
ERASE	Erase Byte or Word	1	11	A10-A0		14	A9-A0		13
ERAL	Erase All Memory	1	00	10X XXXX XXXX		14	10 XXXX XXXX		13
WRAL	Write All Memory with same Data	1	00	01X XXXX XXXX	D7-D0	22	01 XXXX XXXX	D15-D0	29

1. X = Don't Care bit.
2. Address bit A10 is not decoded by the M93C76.
3. Address bit A9 is not decoded by the M93C76.

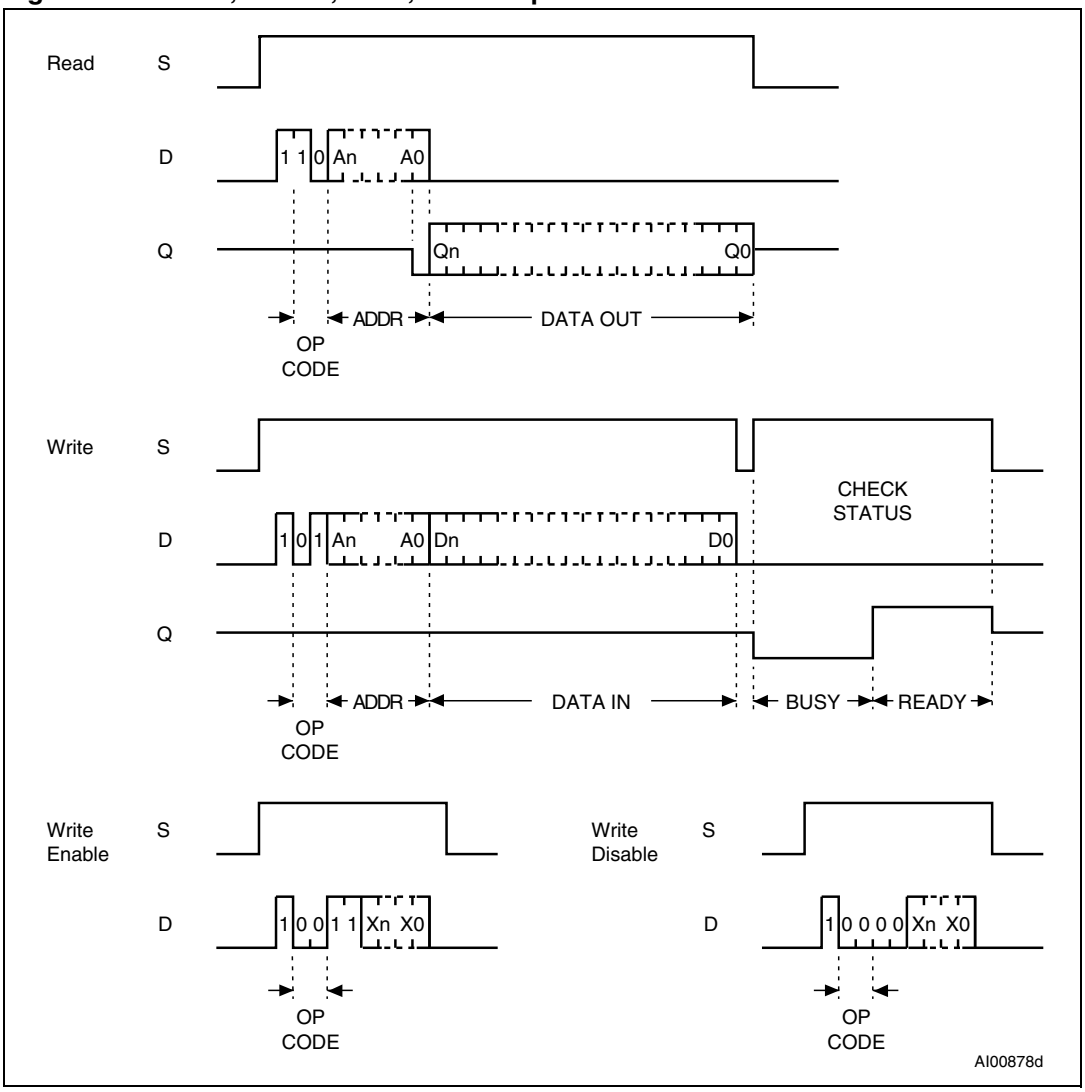
5.1 Read Data from Memory

The Read Data from Memory (READ) instruction outputs data on Serial Data Output (Q). When the instruction is received, the op-code and address are decoded, and the data from the memory is transferred to an output shift register. A dummy 0 bit is output first, followed by the 8-bit byte or 16-bit word, with the most significant bit first. Output data changes are triggered by the rising edge of Serial Clock (C). The M93Cx6 automatically increments the internal address register and clocks out the next byte (or word) as long as the Chip Select Input (S) is held High. In this case, the dummy 0 bit is *not* output between bytes (or words) and a continuous stream of data can be read.

5.2 Write Enable and Write Disable

The Write Enable (WEN) instruction enables the future execution of erase or write instructions, and the Write Disable (WDS) instruction disables it. When power is first applied, the M93Cx6 initializes itself so that erase and write instructions are disabled. After an Write Enable (WEN) instruction has been executed, erasing and writing remains enabled until an Write Disable (WDS) instruction is executed, or until V_{CC} falls below the power-on reset threshold voltage. To protect the memory contents from accidental corruption, it is advisable to issue the Write Disable (WDS) instruction after every write cycle. The Read Data from Memory (READ) instruction is not affected by the Write Enable (WEN) or Write Disable (WDS) instructions.

Figure 4. READ, WRITE, WEN, WDS sequences



1. For the meanings of An, Xn, Qn and Dn, see *Table 5.*, *Table 6.* and *Table 7.*.

5.3 Erase Byte or Word

The Erase Byte or Word (ERASE) instruction sets the bits of the addressed memory byte (or word) to 1. Once the address has been correctly decoded, the falling edge of the Chip Select Input (S) starts the self-timed Erase cycle. The completion of the cycle can be detected by monitoring the READY/$\overline{\text{BUSY}}$ line, as described in the *READY/BUSY status* section.

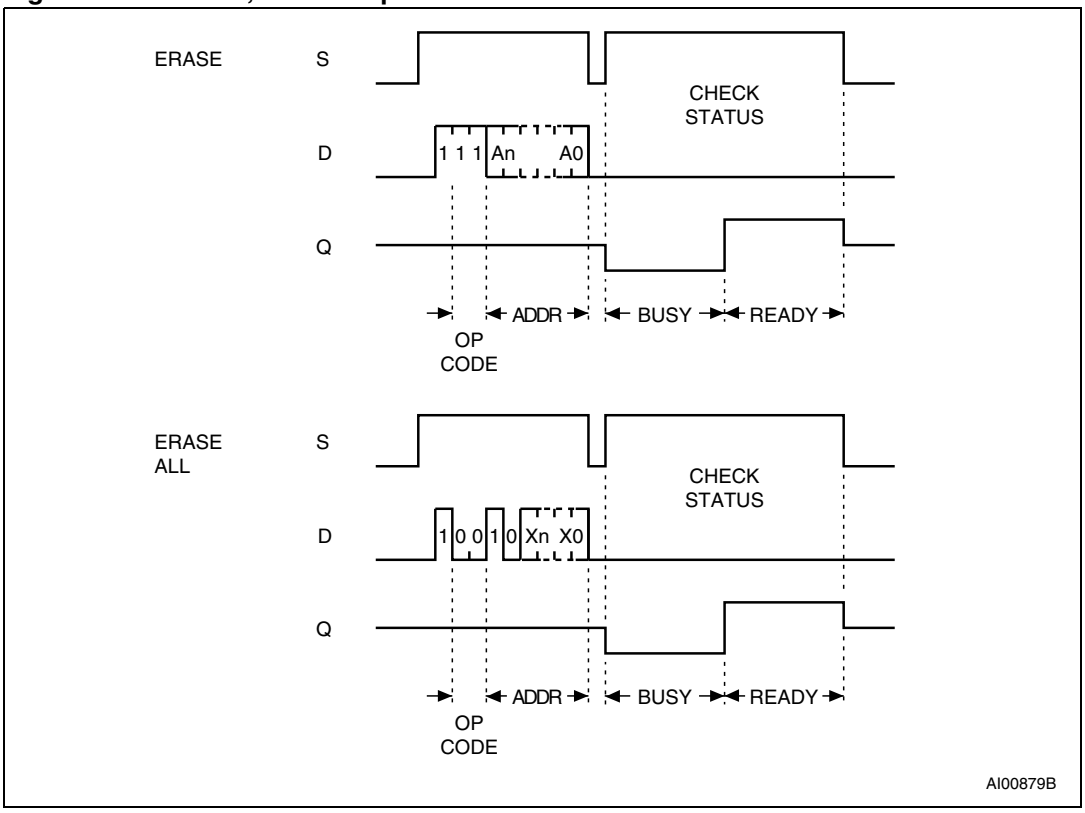
5.4 Write

For the Write Data to Memory (WRITE) instruction, 8 or 16 data bits follow the op-code and address bits. These form the byte or word that is to be written. As with the other bits, Serial Data Input (D) is sampled on the rising edge of Serial Clock (C).

After the last data bit has been sampled, *the Chip Select Input (S) must be taken low before the next rising edge of Serial Clock (C).* If Chip Select Input (S) is brought low before or after this specific time frame, the self-timed programming cycle will not be started, and the addressed location will not be programmed. The completion of the cycle can be detected by monitoring the READY/$\overline{\text{BUSY}}$ line, as described later in this document.

Once the Write cycle has been started, it is internally self-timed (the external clock signal on Serial Clock (C) may be stopped or left running after the start of a Write cycle). The cycle is automatically preceded by an Erase cycle, so it is unnecessary to execute an explicit erase instruction before a Write Data to Memory (WRITE) instruction.

Figure 5. ERASE, ERAL sequences



1. For the meanings of An and Xn, please see *Table 5.*, *Table 6.* and *Table 7.*.

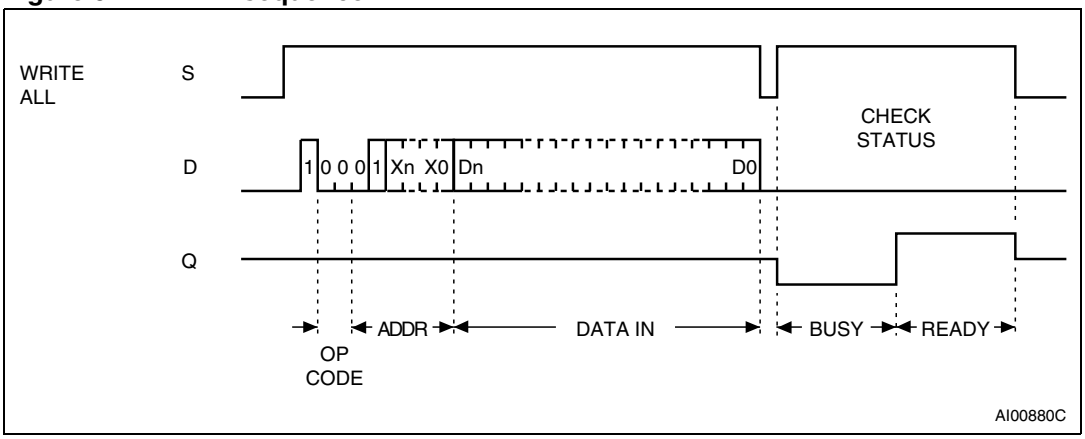
5.5 Erase All

The Erase All Memory (ERAL) instruction erases the whole memory (all memory bits are set to 1). The format of the instruction requires that a dummy address be provided. The Erase cycle is conducted in the same way as the Erase instruction (ERASE). The completion of the cycle can be detected by monitoring the READY/$\overline{\text{BUSY}}$ line, as described in the *READY/BUSY status* section.

5.6 Write All

As with the Erase All Memory (ERAL) instruction, the format of the Write All Memory with same Data (WRAL) instruction requires that a dummy address be provided. As with the Write Data to Memory (WRITE) instruction, the format of the Write All Memory with same Data (WRAL) instruction requires that an 8-bit data byte, or 16-bit data word, be provided. This value is written to all the addresses of the memory device. The completion of the cycle can be detected by monitoring the READY/$\overline{\text{BUSY}}$ line, as described next.

Figure 6. WRAL sequence



1. For the meanings of Xn and Dn, please see *Table 5.*, *Table 6.* and *Table 7.*.

6 READY/$\overline{\text{BUSY}}$ status

While the Write or Erase cycle is underway, for a WRITE, ERASE, WRAL or ERAL instruction, the Busy signal (Q=0) is returned whenever Chip Select input (S) is driven high. (Please note, though, that there is an initial delay, of t_{SLSH}, before this status information becomes available). In this state, the M93Cx6 ignores any data on the bus. When the Write cycle is completed, and Chip Select Input (S) is driven high, the Ready signal (Q=1) indicates that the M93Cx6 is ready to receive the next instruction. Serial Data Output (Q) remains set to 1 until the Chip Select Input (S) is brought low or until a new start bit is decoded.

7 Initial delivery state

The device is delivered with all bits in the memory array set to 1 (each byte contains FFh).

8 Common I/O operation

Serial Data Output (Q) and Serial Data Input (D) can be connected together, through a current limiting resistor, to form a common, single-wire data bus. Some precautions must be taken when operating the memory in this way, mostly to prevent a short circuit current from flowing when the last address bit (A0) clashes with the first data bit on Serial Data Output (Q). Please see the application note *AN394* for details.

9 Clock pulse counter

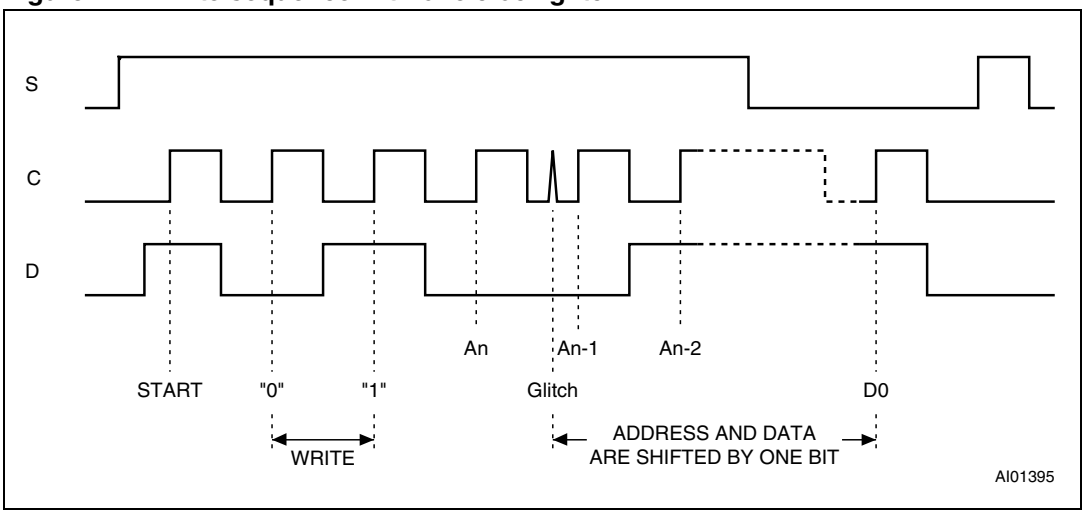
In a noisy environment, the number of pulses received on Serial Clock (C) may be greater than the number delivered by the master (the microcontroller). This can lead to a misalignment of the instruction of one or more bits (as shown in *Figure 7.*) and may lead to the writing of erroneous data at an erroneous address.

To combat this problem, the M93Cx6 has an on-chip counter that counts the clock pulses from the start bit until the falling edge of the Chip Select Input (S). If the number of clock pulses received is not the number expected, the WRITE, ERASE, ERAL or WRAL instruction is aborted, and the contents of the memory are not modified.

The number of clock cycles expected for each instruction, and for each member of the M93Cx6 family, are summarized in *Table 5.* to *Table 7.*. For example, a Write Data to Memory (WRITE) instruction on the M93C56 (or M93C66) expects 20 clock cycles (for the x8 organization) from the start bit to the falling edge of Chip Select Input (S). That is:

1 Start bit
+ 2 Op-code bits
+ 9 Address bits
+ 8 Data bits

Figure 7. Write sequence with one clock glitch



10 Maximum rating

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 8. Absolute maximum ratings

Symbol	Parameter		Min.	Max.	Unit
T_A	Ambient operating temperature		–40	130	°C
T_{STG}	Storage temperature		–65	150	°C
T_{LEAD}	lead temperature during soldering	PDIP		260(1)	
		other packages	See note (2)		°C
V_{OUT}	Output range (Q = V_{OH} or Hi-Z)		–0.50	V_{CC}+0.5	V
V_{IN}	Input range		–0.50	V_{CC}+1	V
V_{CC}	Supply voltage		–0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model)(3)		–4000	4000	V

1. T_{LEAD}max must *not* be applied for more than 10 s.
2. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω).

11 DC and AC parameters

This section summarizes the operating and measurement conditions, and the dc and ac characteristics of the device. The parameters in the dc and ac characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 9. Operating conditions (M93Cx6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	4.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 3)	–40	125	°C

Table 10. Operating conditions (M93Cx6-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 3)	–40	125	°C

Table 11. Operating conditions (M93Cx6-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C

Table 12. AC measurement conditions (M93Cx6)(1)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
	Input rise and fall times		50	ns
	Input pulse voltages	0.4 V to 2.4 V		V
	Input timing reference voltages	1.0 V and 2.0 V		V
	Output timing reference voltages	0.8 V and 2.0 V		V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Table 13. AC measurement conditions (M93Cx6-W and M93Cx6-R)(1)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
	Input rise and fall times		50	ns
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
	Output timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 8. AC testing input output waveforms

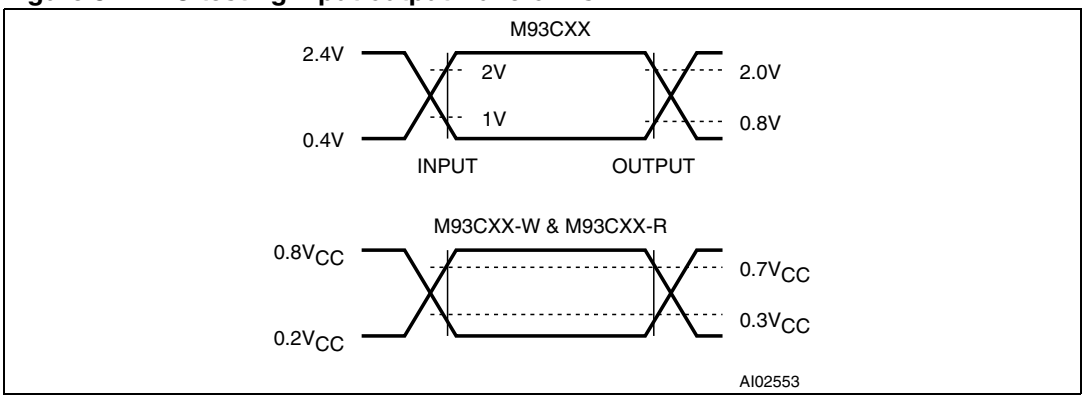


Table 14. Capacitance(1)

Symbol	Parameter	Test condition	Min	Max	Unit
C_{OUT}	Output capacitance	V_{OUT} = 0V		5	pF
C_{IN}	Input capacitance	V_{IN} = 0V		5	pF

1. Sampled only, not 100% tested, at T_A = 25 °C and a frequency of 1 MHz.

Table 15. DC characteristics (M93Cx6, device grade 6)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	0V ≤V_{IN} ≤V_{CC}		±2.5	µA
I_{LO}	Output leakage current	0V ≤V_{OUT} ≤V_{CC}, Q in Hi-Z		±2.5	µA
I_{CC}	Supply current	V_{CC} = 5 V, S = V_{IH}, f = 2 MHz, Q = open		2	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 5 V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, pin7 = V_{CC}, V_{SS} or Hi-Z		15	µA
V_{IL}(1)	Input low voltage	V_{CC} = 5 V ± 10%	–0.45	0.8	V
V_{IH}(1)	Input high voltage	V_{CC} = 5 V ± 10%	2	V_{CC} + 1	V
V_{OL}(1)	Output low voltage	V_{CC} = 5 V, I_{OL} = 2.1 mA		0.4	V
V_{OH}(1)	Output high voltage	V_{CC} = 5 V, I_{OH} = –400 µA	0.8V_{CC}		V

1. Please note that the input and output levels defined in this table are compatible with TTL logic levels and are NOT fully compatible with CMOS levels (as defined in *Table 17*)

Table 16. DC characteristics (M93Cx6, device grade 3)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply current	V_{CC} = 5 V, S = V_{IH}, f = 2 MHz, Q = open		2	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 5 V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, pin7 = V_{CC}, V_{SS} or Hi-Z		15	µA
V_{IL}(1)	Input low voltage	V_{CC} = 5 V ± 10%	–0.45	0.8	V
V_{IH}(1)	Input high voltage	V_{CC} = 5 V ± 10%	2	V_{CC} + 1	V
V_{OL}(1)	Output low voltage	V_{CC} = 5 V, I_{OL} = 2.1 mA		0.4	V
V_{OH}(1)	Output high voltage	V_{CC} = 5 V, I_{OH} = –400 µA	0.8 V_{CC}		V

1. Please note that the input and output levels defined in this table are compatible with TTL logic levels and are NOT fully compatible with CMOS levels (as defined in *Table 17*)

Table 17. DC characteristics (M93Cx6-W, device grade 6)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply current (CMOS inputs)	V_{CC} = 5 V, S = V_{IH}, f = 2 MHz, Q = open		2	mA
		V_{CC} = 2.5 V, S = V_{IH}, f = 2 MHz, Q = open		1	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 2.5 V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, pin7 = V_{CC}, V_{SS} or Hi-Z		5	µA
V_{IL}	Input low voltage (D, C, S)		–0.45	0.2 V_{CC}	V
V_{IH}	Input high voltage (D, C, S)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output low voltage (Q)	V_{CC} = 5 V, I_{OL} = 2.1 mA		0.4	V
		V_{CC} = 2.5 V, I_{OL} = 100 µA		0.2	V
V_{OH}	Output high voltage (Q)	V_{CC} = 5 V, I_{OH} = –400 µA	0.8 V_{CC}		V
		V_{CC} = 2.5 V, I_{OH} = –100 µA	V_{CC}–0.2		V

Table 18. DC characteristics (M93Cx6-W, device grade 3)

Symbol	Parameter	Test condition	Min.(1)	Max. (1)	Unit
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply current (CMOS inputs)	V_{CC} = 5 V, S = V_{IH}, f = 2 MHz, Q = open		2	mA
		V_{CC} = 2.5 V, S = V_{IH}, f = 2 MHz, Q = open		1	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 2.5 V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, pin7 = V_{CC}, V_{SS} or Hi-Z		5	µA
V_{IL}	Input low voltage (D, C, S)		–0.45	0.2 V_{CC}	V
V_{IH}	Input high voltage (D, C, S)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output low voltage (Q)	V_{CC} = 5 V, I_{OL} = 2.1 mA		0.4	V
		V_{CC} = 2.5 V, I_{OL} = 100 µA		0.2	V
V_{OH}	Output high voltage (Q)	V_{CC} = 5 V, I_{OH} = –400 µA	0.8 V_{CC}		V
		V_{CC} = 2.5 V, I_{OH} = –100 µA	V_{CC}–0.2		V

1. New product: identified by Process Identification letter W or G or S.

Table 19. DC characteristics (M93Cx6-R)

Symbol	Parameter	Test condition	Min.(1)	Max. (1)	Unit
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply current (CMOS inputs)	V_{CC} = 5 V, S = V_{IH}, f = 2 MHz, Q = open		2	mA
		V_{CC} = 1.8 V, S = V_{IH}, f = 1 MHz, Q = open		1	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 1.8 V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}, pin7 = V_{CC}, V_{SS} or Hi-Z		2	µA
V_{IL}	Input low voltage (D, C, S)		–0.45	0.2 V_{CC}	V
V_{IH}	Input high voltage (D, C, S)		0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output low voltage (Q)	V_{CC} = 1.8 V, I_{OL} = 100 µA		0.2	V
V_{OH}	Output high voltage (Q)	V_{CC} = 1.8 V, I_{OH} = –100 µA	V_{CC}–0.2		V

1. This product is under development. For more information, please contact your nearest ST sales office.

Table 20. AC characteristics (M93Cx6, device grade 6 or 3)

Test conditions specified in *Table 12.* and *Table 9.*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SK}	Clock frequency	D.C.	2	MHz
t_{SLCH}		Chip Select low to Clock high	50		ns
t_{SHCH}	t_{CSS}	Chip Select setup time M93C46, M93C56, M93C66	50		ns
		Chip Select setup time M93C76, M93C86	50		ns
t_{SLSH}(1)	t_{CS}	Chip Select low to Chip Select high	200		ns
t_{CHCL}(2)	t_{SKH}	Clock high time	200		ns
t_{CLCH}(2)	t_{SKL}	Clock low time	200		ns
t_{DVCH}	t_{DIS}	Data in setup time	50		ns
t_{CHDX}	t_{DIH}	Data in hold time	50		ns
t_{CLSH}	t_{SKS}	Clock setup time (relative to S)	50		ns
t_{CLSL}	t_{CSH}	Chip Select hold time	0		ns
t_{SHQV}	t_{SV}	Chip Select to READY/$\overline{\text{BUSY}}$ status		200	ns
t_{SLQZ}	t_{DF}	Chip Select low to output Hi-Z		100	ns
t_{CHQL}	t_{PD0}	Delay to output low		200	ns
t_{CHQV}	t_{PD1}	Delay to output valid		200	ns
t_W	t_{WP}	Erase or Write cycle time		5	ms

1. Chip Select Input (S) must be brought low for a minimum of t_{SLSH} between consecutive instruction cycles.
2. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.

Table 21. AC characteristics (M93Cx6-W, device grade 6)

Test conditions specified in *Table 13.* and *Table 10.*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SK}	Clock frequency	D.C.	2	MHz
t_{SLCH}		Chip Select low to Clock high	50		ns
t_{SHCH}	t_{CSS}	Chip Select setup time	50		ns
t_{SLSH}(1)	t_{CS}	Chip Select low to Chip Select high	200		ns
t_{CHCL}(2)	t_{SKH}	Clock high time	200		ns
t_{CLCH}(2)	t_{SKL}	Clock low time	200		ns
t_{DVCH}	t_{DIS}	Data in setup time	50		ns
t_{CHDX}	t_{DIH}	Data in hold time	50		ns
t_{CLSH}	t_{SKS}	Clock setup time (relative to S)	50		ns
t_{CLSL}	t_{CSH}	Chip Select hold time	0		ns
t_{SHQV}	t_{SV}	Chip Select to READY/$\overline{\text{BUSY}}$ status		200	ns

Table 21. AC characteristics (M93Cx6-W, device grade 6)

Test conditions specified in *Table 13.* and *Table 10.*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
t_{SLQZ}	t_{DF}	Chip Select low to output Hi-Z		100	ns
t_{CHQL}	t_{PD0}	Delay to output low		200	ns
t_{CHQV}	t_{PD1}	Delay to output valid		200	ns
t_W	t_{WP}	Erase or Write cycle time		5	ms

1. Chip Select Input (S) must be brought low for a minimum of t_{SLSH} between consecutive instruction cycles.
2. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.

Table 22. AC characteristics (M93Cx6-W, device grade 3)

Test conditions specified in *Table 13.* and *Table 10.*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SK}	Clock frequency	D.C.	2	MHz
t_{SLCH}		Chip Select low to Clock high	50		ns
t_{SHCH}	t_{CSS}	Chip Select set-up time	50		ns
t_{SLSH}(1)	t_{CS}	Chip Select low to Chip Select high	200		ns
t_{CHCL}(2)	t_{SKH}	Clock high time	200		ns
t_{CLCH}(2)	t_{SKL}	Clock low time	200		ns
t_{DVCH}	t_{DIS}	Data in set-up time	50		ns
t_{CHDX}	t_{DIH}	Data in hold time	50		ns
t_{CLSH}	t_{SKS}	Clock set-up time (relative to S)	50		ns
t_{CLSL}	t_{CSH}	Chip Select hold time	0		ns
t_{SHQV}	t_{SV}	Chip Select to READY/$\overline{\text{BUSY}}$ status		200	ns
t_{SLQZ}	t_{DF}	Chip Select low to output Hi-Z		100	ns
t_{CHQL}	t_{PD0}	Delay to output low		200	ns
t_{CHQV}	t_{PD1}	Delay to output valid		200	ns
t_W	t_{WP}	Erase or Write cycle time		5	ms

1. Chip Select Input (S) must be brought low for a minimum of t_{SLSH} between consecutive instruction cycles.
2. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.

Table 23. AC characteristics (M93Cx6-R)

Test conditions specified in *Table 13.* and *Table 11.*					
Symbol	**Alt.**	**Parameter**	**Min.(1)**	**Max.(1)**	**Unit**
f_C	f_{SK}	Clock frequency	D.C.	1	MHz
t_{SLCH}		Chip Select low to Clock high	250		ns
t_{SHCH}	t_{CSS}	Chip Select setup time	50		ns
t_{SLSH}(2)	t_{CS}	Chip Select low to Chip Select high	250		ns
t_{CHCL}(3)	t_{SKH}	Clock high time	250		ns
t_{CLCH}(3)	t_{SKL}	Clock low time	250		ns
t_{DVCH}	t_{DIS}	Data in setup time	100		ns
t_{CHDX}	t_{DIH}	Data in hold time	100		ns
t_{CLSH}	t_{SKS}	Clock setup time (relative to S)	100		ns
t_{CLSL}	t_{CSH}	Chip Select hold time	0		ns
t_{SHQV}	t_{SV}	Chip Select to READY/$\overline{\text{BUSY}}$ status		400	ns
t_{SLQZ}	t_{DF}	Chip Select low to output Hi-Z		200	ns
t_{CHQL}	t_{PD0}	Delay to output low		400	ns
t_{CHQV}	t_{PD1}	Delay to output valid		400	ns
t_W	t_{WP}	Erase or Write cycle time		10	ms

1. This product is under development. For more information, please contact your nearest ST sales office.
2. Chip Select Input (S) must be brought low for a minimum of t_{SLSH} between consecutive instruction cycles.
3. $t_{CHCL} + t_{CLCH} \geq 1 / f_C$.

Figure 9. Synchronous timing (start and op-code input)

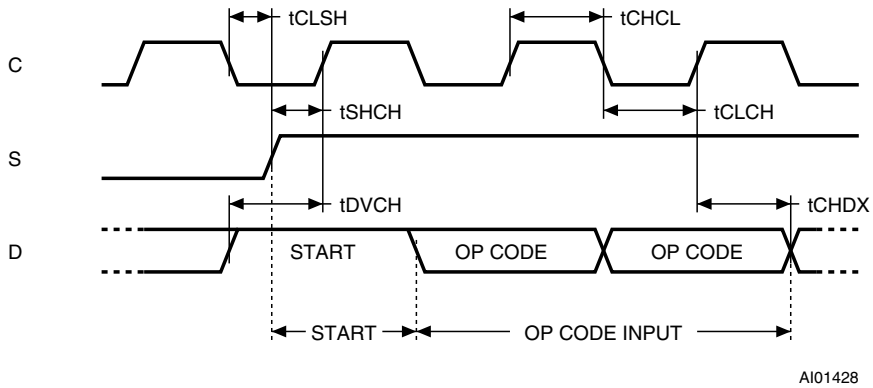


Figure 10. Synchronous timing (Read or Write)

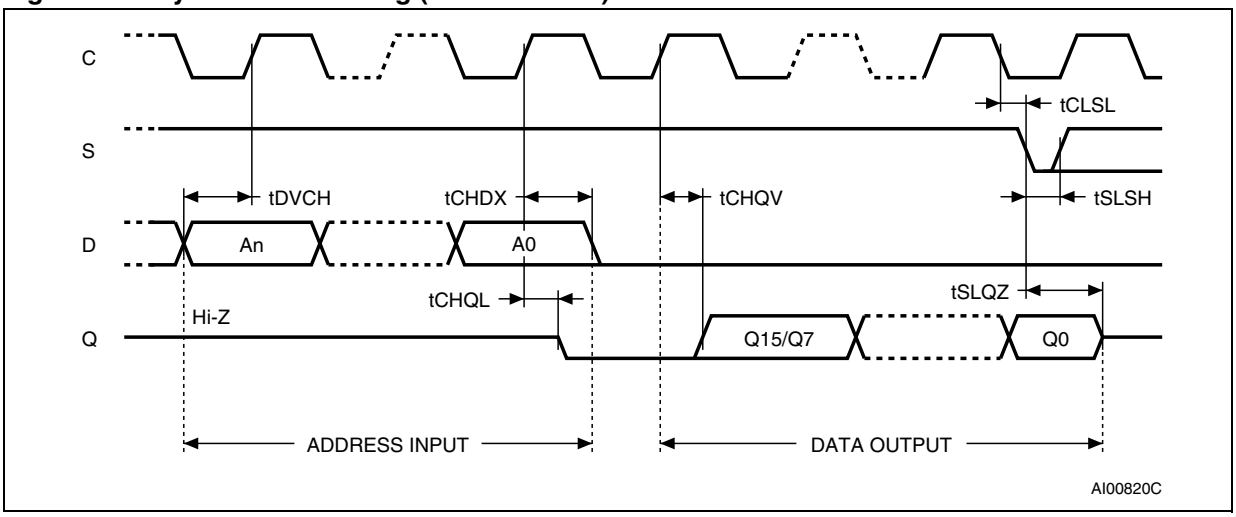
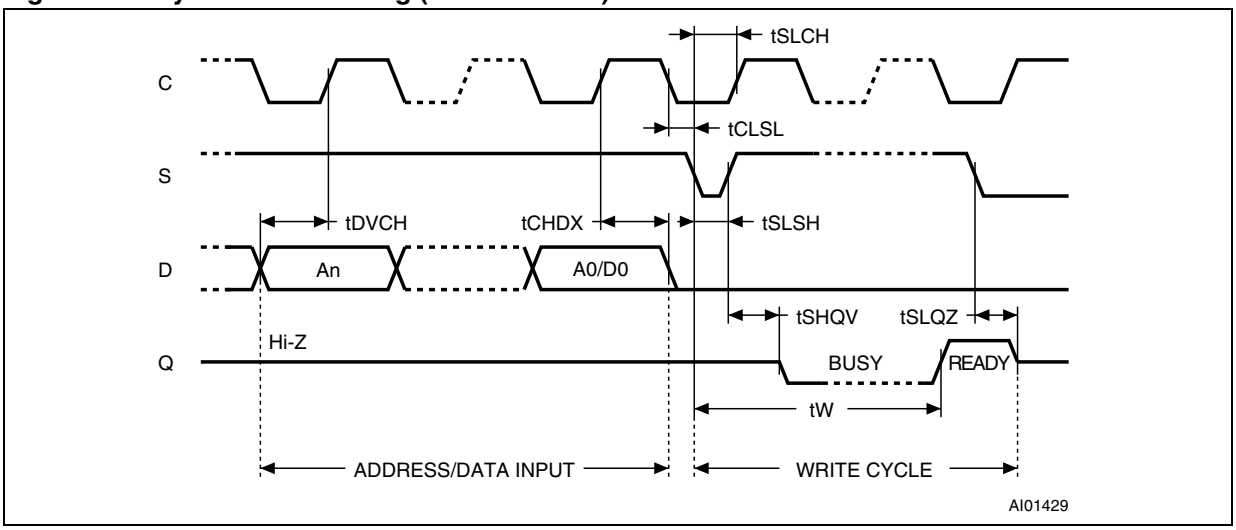


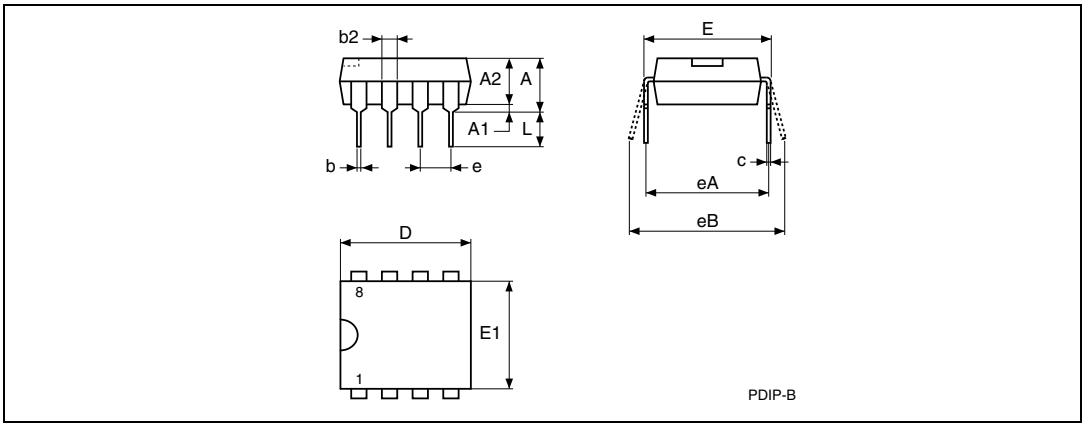
Figure 11. Synchronous timing (Read or Write)



12 Package mechanical data

In order to meet environmental requirements, ST offers the M93C86, M93C76, M93C66, M93C56 and M93C46 in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 12. PDIP8 – 8 lead plastic dual in-line package, 300 mils body width, package outline



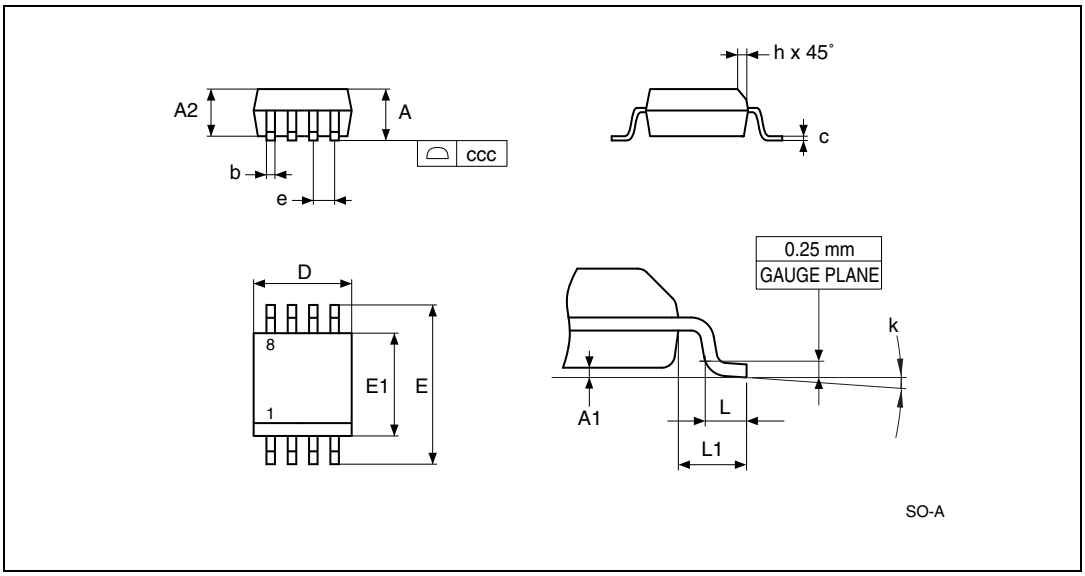
1. Drawing is not to scale.

Table 24. PDIP8 – 8 lead plastic dual in-line package, 300 mils body width, package mechanical data

Symbol	millimeters			inches(1)		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.2098
A1		0.38			0.015	
A2	3.3	2.92	4.95	0.1299	0.115	0.1949
b	0.46	0.36	0.56	0.0181	0.0142	0.022
b2	1.52	1.14	1.78	0.0598	0.0449	0.0701
c	0.25	0.2	0.36	0.0098	0.0079	0.0142
D	9.27	9.02	10.16	0.365	0.3551	0.4
E	7.87	7.62	8.26	0.3098	0.3	0.3252
E1	6.35	6.1	7.11	0.25	0.2402	0.2799
e	2.54	-	-	0.1	-	-
eA	7.62	-	-	0.3	-	-
eB			10.92			0.4299
L	3.3	2.92	3.81	0.1299	0.115	0.15

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 13. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package outline



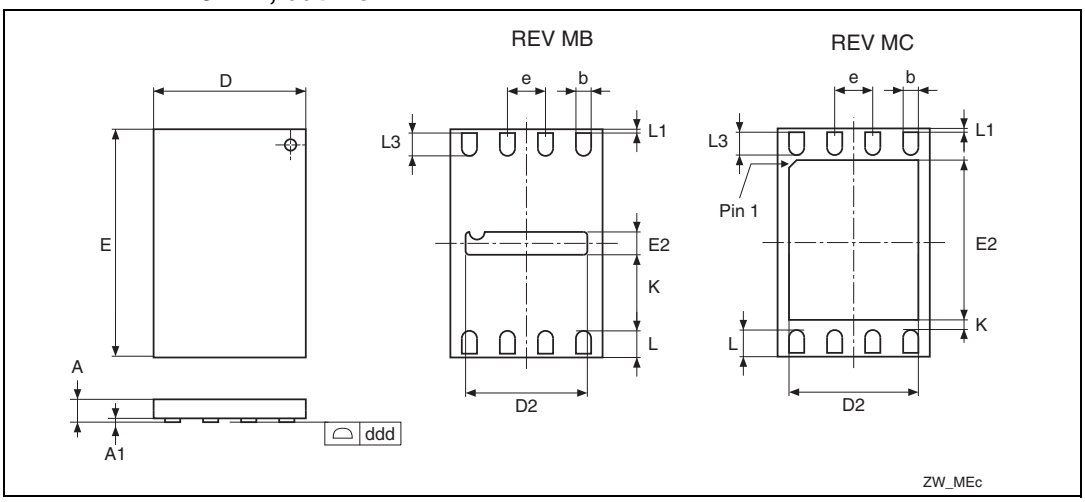
1. Drawing is not to scale.

Table 25. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.0689
A1		0.1	0.25		0.0039	0.0098
A2		1.25			0.0492	
b		0.28	0.48		0.011	0.0189
c		0.17	0.23		0.0067	0.0091
ccc			0.1			0.0039
D	4.9	4.8	5	0.1929	0.189	0.1969
E	6	5.8	6.2	0.2362	0.2283	0.2441
E1	3.9	3.8	4	0.1535	0.1496	0.1575
e	1.27	-	-	0.05	-	-
h		0.25	0.5		0.0098	0.0197
k		0°	8°		0°	8°
L		0.4	1.27		0.0157	0.05
L1	1.04			0.0409		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 14. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, outline



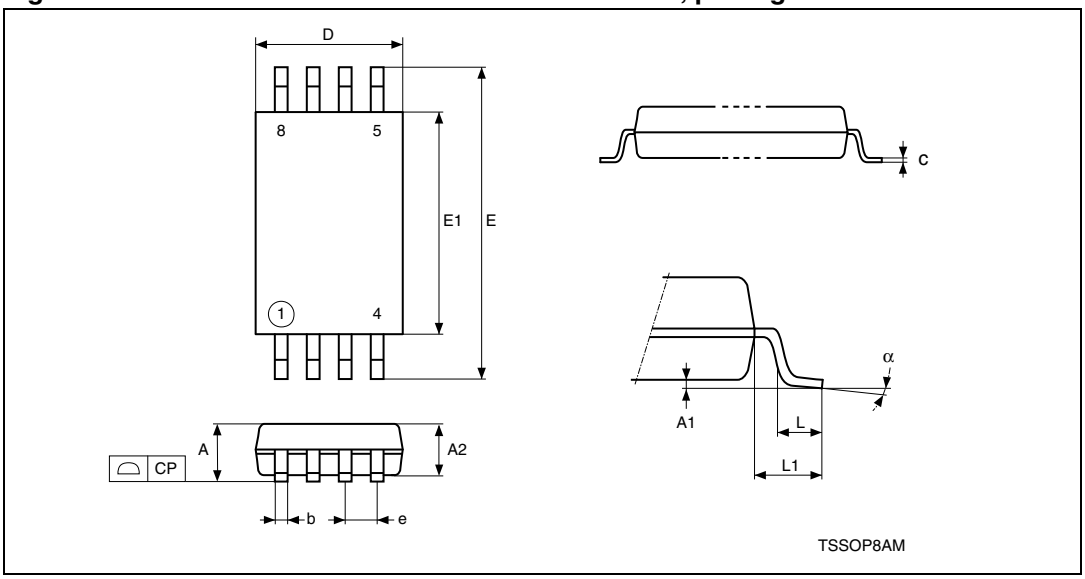
1. Drawing is not to scale.
2. The central pad (the area E2 by D2 in the above illustration) is pulled, internally, to V_{SS}. It must not be allowed to be connected to any other voltage or signal line on the PCB, for example during the soldering process.
3. The circle in the top view of the package indicates the position of pin 1.

Table 26. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.55	0.45	0.6	0.0217	0.0177	0.0236
A1	0.02	0	0.05	0.0008	0	0.002
b	0.25	0.2	0.3	0.0098	0.0079	0.0118
D	2	1.9	2.1	0.0787	0.0748	0.0827
D2 (rev MB)	1.6	1.5	1.7	0.063	0.0591	0.0669
D2 (rev MC)		1.45	1.7		0.0571	0.0669
E	3	2.9	3.1	0.1181	0.1142	0.122
E2 (rev MB)	0.2	0.1	0.3	0.0079	0.0039	0.0118
E2 (rev MC)		1.25	1.6		0.0492	0.063
e	0.5	-	-	0.0197	-	-
K	-	0.3	-	-	0.0118	-
L	-	0.3	0.5	-	0.0118	0.0197
L1	-	-	0.15	-		0.0059
L3		0.3	-	-	0.0118	-
ddd[2]	0.05	-	-	0.002	-	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

Figure 15. TSSOP8 – 8 lead thin shrink small outline, package outline



1. Drawing is not to scale.

Table 27. TSSOP8 – 8 lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.2			0.0472
A1		0.05	0.15		0.002	0.0059
A2	1	0.8	1.05	0.0394	0.0315	0.0413
b		0.19	0.3		0.0075	0.0118
c		0.09	0.2		0.0035	0.0079
CP			0.1			0.0039
D	3	2.9	3.1	0.1181	0.1142	0.122
e	0.65	-	-	0.0256	-	-
E	6.4	6.2	6.6	0.252	0.2441	0.2598
E1	4.4	4.3	4.5	0.1732	0.1693	0.1772
L	0.6	0.45	0.75	0.0236	0.0177	0.0295
L1	1			0.0394		
α		0°	8°		0°	8°
N (pin number)	8			8		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

13 Part numbering

Table 28. Ordering information scheme

Example: M93C86 – W MN 6 T P /S

Device type

M93 = MICROWIRE serial access EEPROM

Device function

86 = 16 Kbit (2048 x 8)
76 = 8 Kbit (1024 x 8)
66 = 4 Kbit (512 x 8)
56 = 2 Kbit (256 x 8)
46 = 1 Kbit (128 x 8)

Operating voltage

blank = V_{CC} = 4.5 to 5.5 V
W = V_{CC} = 2.5 to 5.5 V
R = V_{CC} = 1.8 to 5.5 V

Package

BN = PDIP8
MN = SO8 (150 mils width)
MB or MC = UFDFPN8 (MLP8)
DW = TSSOP8 (169 mils width)

Device grade

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow
3 = Device tested with high reliability certified flow(1).
Automotive temperature range (–40 to 125 °C)

Packing

blank = standard packing
T = tape and reel packing

Plating technology

P or G = ECOPACK® (RoHS compliant)

Process(2)

/W or /S = F6SP36%

1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
2. Used only for device grade 3.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 29. Available M93C46-x products (package, voltage range, temperature grade)

Package	M93C46 4.5 V to 5.5 V	M93C46-W 2.5 V to 5.5 V	M93C46-R 1.8 V to 5.5 V
DIP8 (BN)	Range 3	Range 6 Range 3	-
SO8 (MN)	Range 6 Range 3	Range 6 Range 3	-
TSSOP (DW)	-	Range 6 Range 3	-

Table 30. Available M93C56-x products (package, voltage range, temperature grade)

Package	M93C56 4.5 V to 5.5 V	M93C56-W 2.5 V to 5.5 V	M93C56-R 1.8 V to 5.5 V
SO8 (MN)	Range 6 Range3	Range 6 Range3	Range 6
TSSOP (DW)	-	Range 6	Range 6

Table 31. Available M93C66-x products (package, voltage range, temperature grade)

Package	M93C66 4.5 V to 5.5 V	M93C66-W 2.5 V to 5.5 V	M93C66-R 1.8 V to 5.5 V
SO8 (MN)	Range 6 Range3	Range 6 Range3	-
TSSOP (DW)	-	Range 6 Range3	-
UFDFPN 2 x 3 mm (MB or MC)	-	-	Range 6

Table 32. Available M93C76-x products (package, voltage range, temperature grade)

Package	M93C76 4.5 V to 5.5 V	M93C76-W 2.5 V to 5.5 V	M93C76-R 1.8 V to 5.5 V
SO8 (MN)	Range3	Range 6 Range3	-
TSSOP (DW)	-	Range 6	Range 6

Table 33. Available M93C86-x products (package, voltage range, temperature grade)

Package	M93C86 4.5 V to 5.5 V	M93C86-W 2.5 V to 5.5 V	M93C86-R 1.8 V to 5.5 V
DIP8 (BN)	-	Range 6	-
SO8 (MN)	Range 6 Range3	Range 6 Range3	-
TSSOP (DW)	-	Range 6	-

14 Revision history

Table 34. Document revision history

Date	Revision	Changes
04-Feb-2003	2.0	Document reformatted, and reworded, using the new template. Temperature range 1 removed. TSSOP8 (3x3mm) package added. New products, identified by the process letter W, added, with fc(max) increased to 1MHz for -R voltage range, and to 2MHz for all other ranges (and corresponding parameters adjusted)
26-Mar-2003	2.1	Value of standby current (max) corrected in DC characteristics tables for -W and -R ranges V_{OUT} and V_{IN} separated from V_{IO} in the Absolute Maximum Ratings table
04-Apr-2003	2.2	Values corrected in AC characteristics tables for -W range (t_{SLSH}, t_{DVCH}, t_{CLSL}) for devices with Process Identification Letter W
23-May-2003	2.3	Standby current corrected for -R range
27-May-2003	2.4	Turned-die option re-instated in Ordering Information Scheme
25-Nov-2003	3.0	Table of contents, and Pb-free options added. Temperature range 7 added. V_{IL}(min) improved to –0.45V.
30-Mar-2004	4.0	MLP package added. Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) changed. Soldering temperature information clarified for RoHS compliant devices. Device grade information clarified. Process identification letter “G” information added
16-Aug-2004	5.0	M93C06 removed. Device grade information further clarified. Process identification letter “S” information added. Turned-die package option removed. Product list summary added.
27-Oct-2005	6.0	current product/new product distinction removed. I_{CC} and I_{CC1} values for current product removed from tables *15*, *16* and *17* and AC characteristics for current product removed from Tables *20* and *21*. Clock rate added to *Features*. “Q = open” added to I_{CC} Test conditions in DC Characteristics Tables *15*, *16*, *17*, *18* and *19*. *Process* added to *Table 28.: Ordering information scheme*. POWER ON DATA PROTECTION section removed, replaced by *Operating features* and *Active Power and Standby Power modes*. *Initial delivery state* added. SO8N and TSSOP8 packages updated. PDIP-specific T_{LEAD} added to *Table 8.: Absolute maximum ratings*.

Table 34. Document revision history (continued)

Date	Revision	Changes
31-Jul-2007	7	Document reformatted. TSSOP8 3 × 3 mm (DS) package removed. Erase/Write Enable (EWEN) instruction replaced by Write Enable (WEN). Erase/Write Disable (EWDS) instruction replaced by Write Disable (WDS). *Section 7: Initial delivery state* modified, ACTIVE POWER AND STANDBY POWER MODES section removed. I_{CC1} test conditions modified in *Table 15*, *Table 16*, *Table 17*, *Table 18* and *Table 19*. Note 1 added to *Table 15*. t_W parameter description modified in *Table 20*, *Table 21*, *Table 22* and *Table 23*.. SO8 narrow and UFDFPN8 package specifications updated (see *Section 12: Package mechanical data*). *Table 29*, *Table 30*, *Table 31*, *Table 32* and *Table 33* added. Blank option removed under Plating technology in *Table 27: TSSOP8 – 8 lead thin shrink small outline, package mechanical data*. *Section 2: Connecting to the serial bus* added. Device grade 7 removed.
29-Jan-2008	8	Small text changes. M93C76-R root part number added. *Section 2: Connecting to the serial bus* modified (pull-down resitor added to *Figure 3: Bus master and memory devices on the serial bus* and paragraph added). *Section 3.1.2: Power-up conditions* corrected. T_{LEAD} modified in *Table 8: Absolute maximum ratings*. V_{OH} min guaranteed at a higher value in DC characteristics tables *15*, *16*, *17* and *18*. M93C56-R is also offered in TSSOP8 package (see *Table 30*). Package mechanical inch values calculated from mm and rounded to 4 decimal digits in *Section 12: Package mechanical data* TSSOP8 (DW) package specifications updated.
01-Apr-2010	9	Modified footnote in *Table 15* and *Table 16 on page 23* Updated *Figure 14: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, outline* and *Table 26 on page 31*
29-Apr-2010	10	Updated *Figure 31: Available M93C66-x products (package, voltage range, temperature grade)* UFDFPN option.

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