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Functional Description

The M25P16 is an 16Mb (2Mb x 8) serial Flash memory device with advanced write protection mechanisms accessed by a high speed SPI-compatible bus. The device supports high-performance commands for clock frequency up to 75MHz.

The memory can be programmed 1 to 256 bytes at a time using the PAGE PROGRAM command. It is organized as 32 sectors, each containing 256 pages. Each page is 256 bytes wide. Memory can be viewed either as 8,192 pages or as 2,097,152 bytes. The entire memory can be erased using the BULK ERASE command, or it can be erased one sector at a time using the SECTOR ERASE command.

This datasheet details the functionality of the M25P16 device based on 110nm process.

Figure 1: Logic Diagram

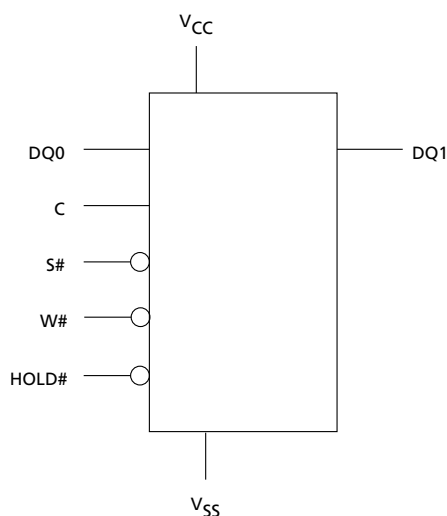


Table 1: Signal Names

| Signal Name | Function | Direction |
|-----------------|--------------------|-----------|
| C | Serial clock | Input |
| DQ0 | Serial data input | Input |
| DQ1 | Serial data output | Output |
| S# | Chip select | Input |
| W# | Write protect | Input |
| HOLD# | Hold | Input |
| V _{CC} | Supply voltage | – |
| V _{SS} | Ground | – |

Figure 2: Pin Connections: SO8, VFQFPN , VDFPN

| | | | |
|-----------------|-----|-----|-----------------|
| S# | □ 1 | 8 □ | V _{CC} |
| DQ1 | □ 2 | 7 □ | HOLD# |
| W# | □ 3 | 6 □ | C |
| V _{SS} | □ 4 | 5 □ | DQ0 |

Note: 1. There is an exposed central pad on the underside of the MLP8 package that is pulled internally to V_{SS}, and must not be connected to any other voltage or signal line on the PCB. The Package Mechanical section provides information on package dimensions and how to identify pin 1.

Figure 3: Pin Connections: SO16

| | | | |
|-----------------|-----|------|--------------------|
| HOLD# | □ 1 | 16 □ | C |
| V _{CC} | □ 2 | 15 □ | DQ0 |
| DNU | □ 3 | 14 □ | DNU |
| DNU | □ 4 | 13 □ | DNU |
| DNU | □ 5 | 12 □ | DNU |
| DNU | □ 6 | 11 □ | DNU |
| S# | □ 7 | 10 □ | V _{SS} |
| DQ1 | □ 8 | 9 □ | W#/V _{PP} |

Notes: 1. DU = Don't Use
2. The Package Mechanical section provides information on package dimensions and how to identify pin 1.

Signal Descriptions

Table 2: Signal Descriptions

| Signal | Type | Description |
|--------------------|--------|---|
| DQ1 | Output | Serial data: The DQ1 output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock (C). |
| DQ0 | Input | Serial data: The DQ0 input signal is used to transfer data serially into the device. It receives commands, addresses, and the data to be programmed. Values are latched on the rising edge of the serial clock (C). |
| C | Input | Clock: The C input signal provides the timing of the serial interface. Commands, addresses, or data present at serial data input (DQ0) is latched on the rising edge of the serial clock (C). Data on DQ1 changes after the falling edge of C. |
| S# | Input | Chip select: When the S# input signal is HIGH, the device is deselected and DQ1 is at high impedance. Unless an internal PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress, the device will be in the standby power mode (not the deep power-down mode). Driving S# LOW enables the device, placing it in the active power mode. After power-up, a falling edge on S# is required prior to the start of any command. |
| HOLD# | Input | Hold: The HOLD# signal is used to pause any serial communications with the device without deselecting the device. During the hold condition, DQ1 is High-Z. DQ0 and C are "Don't Care." To start the hold condition, the device must be selected, with S# driven LOW. |
| W#/V _{PP} | Input | Write protect: The W#/V _{PP} signal is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin. If the W#/V _{PP} input is kept in a low voltage range (0 V to V _{CC}) the pin is seen as a control input. The W# input signal is used to freeze the size of the area of memory that is protected against program or erase commands as specified by the values in BP2, BP1, and BP0 bits of the Status Register. V _{PP} acts as an additional power supply if it is in the range of V _{PPH} , as defined in the AC Measurement Conditions table. Avoid applying V _{PPH} to the W#/V _{PP} pin during a BULK ERASE operation. |
| V _{CC} | Power | Device core power supply: Source voltage. |
| V _{SS} | Ground | Ground: Reference for the V _{CC} supply voltage. |
| DNU | – | Do not use. |

SPI Modes

These devices can be driven by a microcontroller with its serial peripheral interface (SPI) running in either of the following two SPI modes:

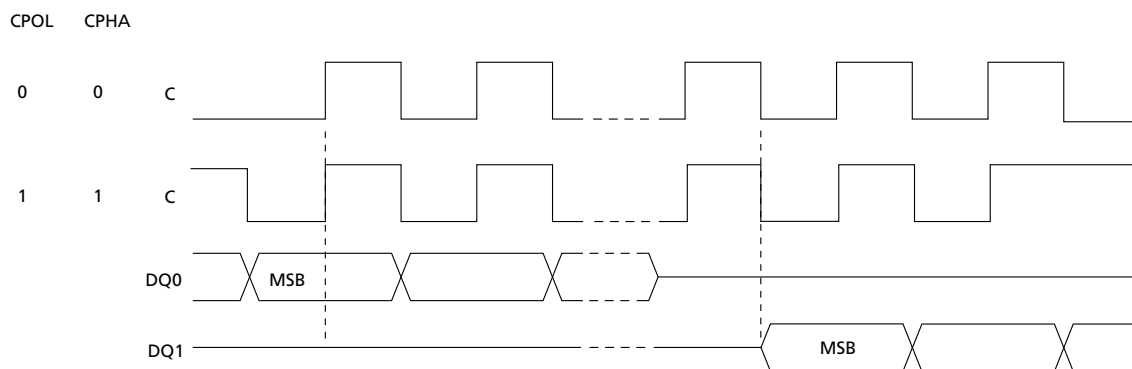
- CPOL = 0, CPHA = 0
- CPOL = 1, CPHA = 1

For these two modes, input data is latched in on the rising edge of serial clock (C), and output data is available from the falling edge of C.

The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring data:

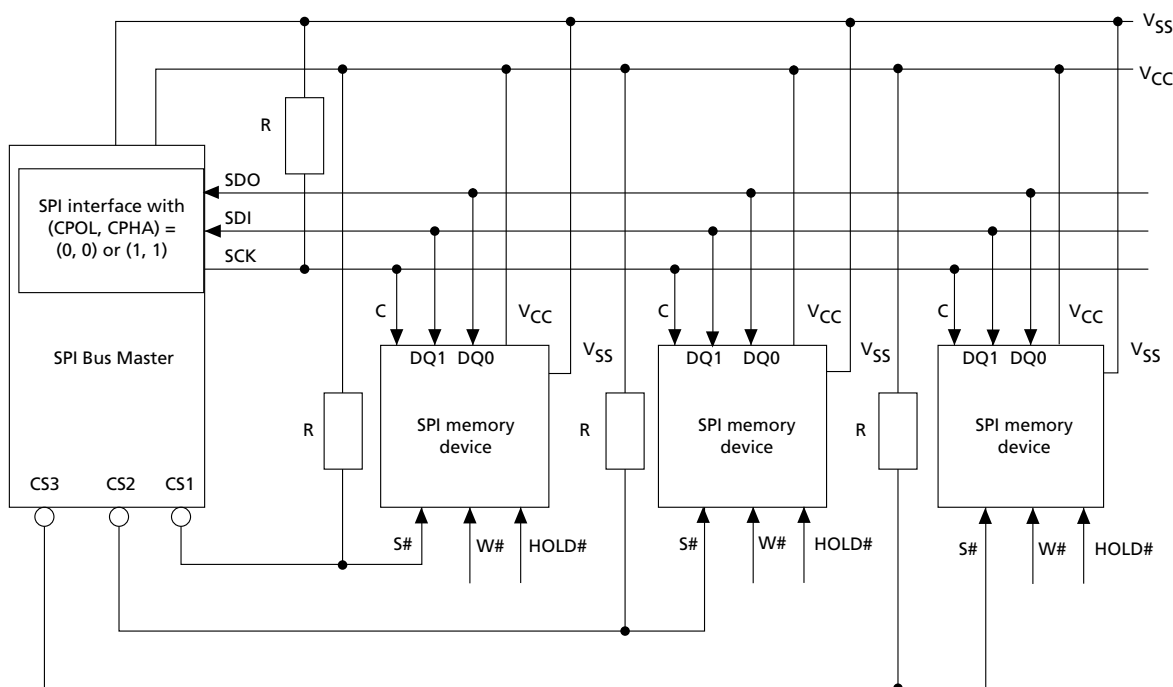
- C remains at 0 for (CPOL = 0, CPHA = 0)
- C remains at 1 for (CPOL = 1, CPHA = 1)

Figure 4: SPI Modes Supported



Because only one device is selected at a time, only one device drives the serial data output (DQ1) line at a time, while the other devices are High-Z. An example of three devices connected to an MCU on an SPI bus is shown here.

Figure 5: Bus Master and Memory Devices on the SPI Bus



- Notes:
1. WRITE PROTECT (W#) and HOLD# should be driven HIGH or LOW as appropriate.
 2. Resistors (R) ensure that the memory device is not selected if the bus master leaves the S# line High-Z.
 3. The bus master may enter a state where all I/O are High-Z at the same time; for example, when the bus master is reset. Therefore, C must be connected to an external pull-down resistor so that when all I/O are High-Z, S# is pulled HIGH while C is pulled LOW. This ensures that S# and C do not go HIGH at the same time and that the t_{SHCH} requirement is met.
 4. The typical value of R is 100k Ω , assuming that the time constant $R \times C_p$ (C_p = parasitic capacitance of the bus line) is shorter than the time during which the bus master leaves the SPI bus High-Z.
 5. Example: Given that $C_p = 50\text{pF}$ ($R \times C_p = 5\mu\text{s}$), the application must ensure that the bus master never leaves the SPI bus High-Z for a time period shorter than 5 μs .

Operating Features

Page Programming

To program one data byte, two commands are required: WRITE ENABLE, which is one byte, and a PAGE PROGRAM sequence, which is four bytes plus data. This is followed by the internal PROGRAM cycle of duration t_{PP} . To spread this overhead, the PAGE PROGRAM command allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided they lie in consecutive addresses on the same page of memory. To optimize timings, it is recommended to use the PAGE PROGRAM command to program all consecutive targeted bytes in a single sequence than to use several PAGE PROGRAM sequences with each containing only a few bytes.

Sector Erase, Bulk Erase

The PAGE PROGRAM command allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved a sector at a time using the SECTOR ERASE command, or throughout the entire memory using the BULK ERASE command. This starts an internal ERASE cycle of duration t_{SE} or t_{BE} . The ERASE command must be preceded by a WRITE ENABLE command.

Polling during a Write, Program, or Erase Cycle

An improvement in the time to complete the following commands can be achieved by not waiting for the worst case delay (t_W , t_{PP} , t_{SE} , or t_{BE}).

- WRITE STATUS REGISTER
- PROGRAM
- ERASE (SECTOR ERASE, BULK ERASE)

The write in progress (WIP) bit is provided in the status register so that the application program can monitor this bit in the status register, polling it to establish when the previous WRITE cycle, PROGRAM cycle, or ERASE cycle is complete.

Active Power, Standby Power, and Deep Power-Down

When chip select ($S\#$) is LOW, the device is selected, and in the ACTIVE POWER mode. When $S\#$ is HIGH, the device is deselected, but could remain in the ACTIVE POWER mode until all internal cycles have completed (PROGRAM, ERASE, WRITE STATUS REGISTER). The device then goes in to the STANDBY POWER mode. The device consumption drops to I_{CC1} .

The DEEP POWER-DOWN mode is entered when the DEEP POWER-DOWN command is executed. The device consumption drops further to I_{CC2} . The device remains in this mode until the RELEASE FROM DEEP POWER-DOWN command is executed. While in the DEEP POWER-DOWN mode, the device ignores all WRITE, PROGRAM, and ERASE commands. This provides an extra software protection mechanism when the device is not in active use, by protecting the device from inadvertent WRITE, PROGRAM, or ERASE operations. For further information, see the DEEP POWER DOWN command.

Status Register

The status register contains a number of status and control bits that can be read or set (as appropriate) by specific commands. For a detailed description of the status register bits, see READ STATUS REGISTER (page 25).

Data Protection by Protocol

Non-volatile memory is used in environments that can include excessive noise. The following capabilities help protect data in these noisy environments.

Power on reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification.

PROGRAM, ERASE, and WRITE STATUS REGISTER commands are checked before they are accepted for execution to ensure they consist of a number of clock pulses that is a multiple of eight.

All commands that modify data must be preceded by a WRITE ENABLE command to set the write enable latch (WEL) bit.

In addition to the low power consumption feature, the DEEP POWER-DOWN mode offers extra software protection since all PROGRAM, and ERASE commands are ignored when the device is in this mode.

Software Data Protection

Memory can be configured as read-only using the block protect bits (BP2, BP1, BP0) as shown in the Protected Area Sizes table.

Hardware Data Protection

Hardware data protection is implemented using the write protect signal applied on the W# pin. This freezes the status register in a read-only mode. In this mode, the block protect (BP) bits and the status register write disable bit (SRWD) are protected.

Table 3: Protected Area Sizes

| Status Register Content | | Memory Content | |
|-------------------------|----------|------------------------------|-------------------------------|
| BP Bit 1 | BP Bit 0 | Protected Area | Unprotected Area |
| 0 | 0 | none | All sectors (sectors 0 to 3) |
| 0 | 1 | Upper 4th (sector 3) | Lower 3/4ths (sectors 0 to 2) |
| 1 | 0 | Upper half (sectors 2 and 3) | Lower half (sectors 0 and 1) |
| 1 | 1 | All sectors (sectors 0 to 3) | none |

Note: 1. 0 0 = unprotected area (sectors): The device is ready to accept a BULK ERASE command only if all block protect bits (BP1, BP0) are 0.

Table 4: Protected Area Sizes

| Status Register Content | | | Memory Content | |
|-------------------------|----------|----------|----------------|------------------------------|
| BP Bit 2 | BP Bit 1 | BP Bit 0 | Protected Area | Unprotected Area |
| 0 | 0 | 0 | none | All sectors (sectors 0 to 7) |

Table 4: Protected Area Sizes (Continued)

| Status Register Content | | | Memory Content | |
|-------------------------|----------|----------|------------------------------|-------------------------------|
| BP Bit 2 | BP Bit 1 | BP Bit 0 | Protected Area | Unprotected Area |
| 0 | 0 | 1 | Upper 8th (sectors 7) | Lower 7/8ths (sectors 0 to 6) |
| 0 | 1 | 0 | Upper 4th (sectors 6 and 7) | Lower 3/4ths (sectors 0 to 5) |
| 0 | 1 | 1 | Upper half (sectors 4 to 7) | Lower half (sectors 0 to 3) |
| 1 | 0 | 0 | All sectors (sectors 0 to 7) | none |
| 1 | 0 | 1 | All sectors (sectors 0 to 7) | none |
| 1 | 1 | 0 | All sectors (sectors 0 to 7) | none |
| 1 | 1 | 1 | All sectors (sectors 0 to 7) | none |

Note: 1. 0 0 0 = unprotected area (sectors): The device is ready to accept a BULK ERASE command only if all block protect bits (BP2, BP1, BP0) are 0.

Table 5: Protected Area Sizes

| Status Register Content | | | Memory Content | |
|-------------------------|----------|----------|-------------------------------|----------------------------------|
| BP Bit 2 | BP Bit 1 | BP Bit 0 | Protected Area | Unprotected Area |
| 0 | 0 | 0 | none | All sectors (sectors 0 to 15) |
| 0 | 0 | 1 | Upper 16th (sector 15) | Lower 15/16ths (sectors 0 to 14) |
| 0 | 1 | 0 | Upper 8th (sectors 14 and 15) | Lower 7/8ths (sectors 0 to 13) |
| 0 | 1 | 1 | Upper 4th (sectors 12 to 15) | Lower 3/4ths (sectors 0 to 11) |
| 1 | 0 | 0 | Upper half (sectors 8 to 15) | Lower half (sectors 0 to 7) |
| 1 | 0 | 1 | All sectors (sectors 0 to 15) | none |
| 1 | 1 | 0 | All sectors (sectors 0 to 15) | none |
| 1 | 1 | 1 | All sectors (sectors 0 to 15) | none |

Note: 1. 0 0 0 = unprotected area (sectors): The device is ready to accept a BULK ERASE command only if all block protect bits (BP2, BP1, BP0) are 0.

Table 6: Protected Area Sizes

| Status Register Content | | | Memory Content | |
|-------------------------|----------|----------|--------------------------------|----------------------------------|
| BP Bit 2 | BP Bit 1 | BP Bit 0 | Protected Area | Unprotected Area |
| 0 | 0 | 0 | none | All sectors (sectors 0 to 31) |
| 0 | 0 | 1 | Upper 32nd (sector 31) | Lower 31/32nds (sectors 0 to 30) |
| 0 | 1 | 0 | Upper 16th (sectors 30 and 31) | Lower 15/16ths (sectors 0 to 29) |
| 0 | 1 | 1 | Upper 8th (sectors 28 to 31) | Lower 7/8ths (sectors 0 to 27) |
| 1 | 0 | 0 | Upper 4th (sectors 24 to 31) | Lower 3/4ths (sectors 0 to 23) |
| 1 | 0 | 1 | Upper half (sectors 16 to 31) | Lower half (sectors 0 to 15) |
| 1 | 1 | 0 | All sectors (sectors 0 to 31) | none |

Table 6: Protected Area Sizes (Continued)

| Status Register Content | | | Memory Content | |
|-------------------------|----------|----------|-------------------------------|------------------|
| BP Bit 2 | BP Bit 1 | BP Bit 0 | Protected Area | Unprotected Area |
| 1 | 1 | 1 | All sectors (sectors 0 to 31) | none |

Note: 1. 0 0 0 = unprotected area (sectors): The device is ready to accept a BULK ERASE command only if all block protect bits (BP2, BP1, BP0) are 0.

Table 7: Protected Area Sizes

| Status Register Content | | | Memory Content | |
|-------------------------|----------|----------|--------------------------------|----------------------------------|
| BP Bit 2 | BP Bit 1 | BP Bit 0 | Protected Area | Unprotected Area |
| 0 | 0 | 0 | none | All sectors (sectors 0 to 63) |
| 0 | 0 | 1 | Upper 64th (sector 63) | Lower 63/64ths (sectors 0 to 62) |
| 0 | 1 | 0 | Upper 32nd (sectors 62 and 63) | Lower 31/32nds (sectors 0 to 61) |
| 0 | 1 | 1 | Upper 16th (sectors 60 and 63) | Lower 15/16ths (sectors 0 to 59) |
| 1 | 0 | 0 | Upper 8th (sectors 56 to 63) | Lower 7/8ths (sectors 0 to 55) |
| 1 | 0 | 1 | Upper 4th (sectors 48 to 63) | Lower 3/4ths (sectors 0 to 47) |
| 1 | 1 | 0 | Upper half (sectors 32 to 63) | Lower half (sectors 0 to 31) |
| 1 | 1 | 1 | All sectors (sectors 0 to 63) | none |

Note: 1. 0 0 0 = unprotected area (sectors): The device is ready to accept a BULK ERASE command only if all block protect bits (BP2, BP1, BP0) are 0.

Table 8: Protected Area Sizes

| Status Register Content | | | Memory Content | |
|-------------------------|----------|----------|----------------------------------|-----------------------------------|
| BP Bit 2 | BP Bit 1 | BP Bit 0 | Protected Area | Unprotected Area |
| 0 | 0 | 0 | none | All sectors (sectors 0 to 127) |
| 0 | 0 | 1 | Upper 64th (sectors 126 and 127) | Lower 63/64ths (sectors 0 to 125) |
| 0 | 1 | 0 | Upper 32nd (sectors 124 to 127) | Lower 31/32nds (sectors 0 to 123) |
| 0 | 1 | 1 | Upper 16th (sectors 120 to 127) | Lower 15/16ths (sectors 0 to 119) |
| 1 | 0 | 0 | Upper 8th (sectors 112 to 127) | Lower 7/8ths (sectors 0 to 111) |
| 1 | 0 | 1 | Upper 4th (sectors 96 to 127) | Lower 3/4ths (sectors 0 to 95) |
| 1 | 1 | 0 | Upper half (sectors 64 to 127) | Lower half (sectors 0 to 63) |
| 1 | 1 | 1 | All sectors (sectors 0 to 127) | none |

Note: 1. The device is ready to accept a BULK ERASE command only if all block protect bits (BP2, BP1, BP0) are 0.

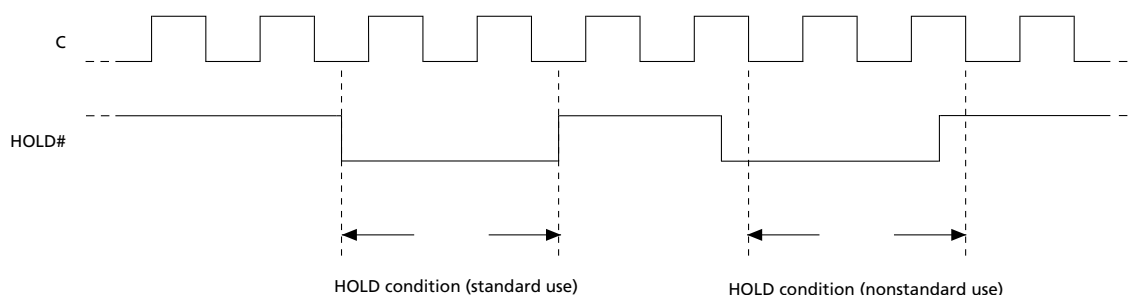
Hold Condition

The HOLD# signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal LOW does not terminate any WRITE STATUS REGISTER, PROGRAM, or ERASE cycle that is currently in progress.

To enter the hold condition, the device must be selected, with S# LOW. The hold condition starts on the falling edge of the HOLD# signal, if this coincides with serial clock (C) being LOW. The hold condition ends on the rising edge of the HOLD# signal, if this coincides with C being LOW. If the falling edge does not coincide with C being LOW, the hold condition starts after C next goes LOW. Similarly, if the rising edge does not coincide with C being LOW, the hold condition ends after C next goes LOW.

During the hold condition, DQ1 is HIGH impedance while DQ0 and C are Don't Care. Typically, the device remains selected with S# driven LOW for the duration of the hold condition. This ensures that the state of the internal logic remains unchanged from the moment of entering the hold condition. If S# goes HIGH while the device is in the hold condition, the internal logic of the device is reset. To restart communication with the device, it is necessary to drive HOLD# HIGH, and then to drive S# LOW. This prevents the device from going back to the hold condition.

Figure 6: Hold Condition Activation



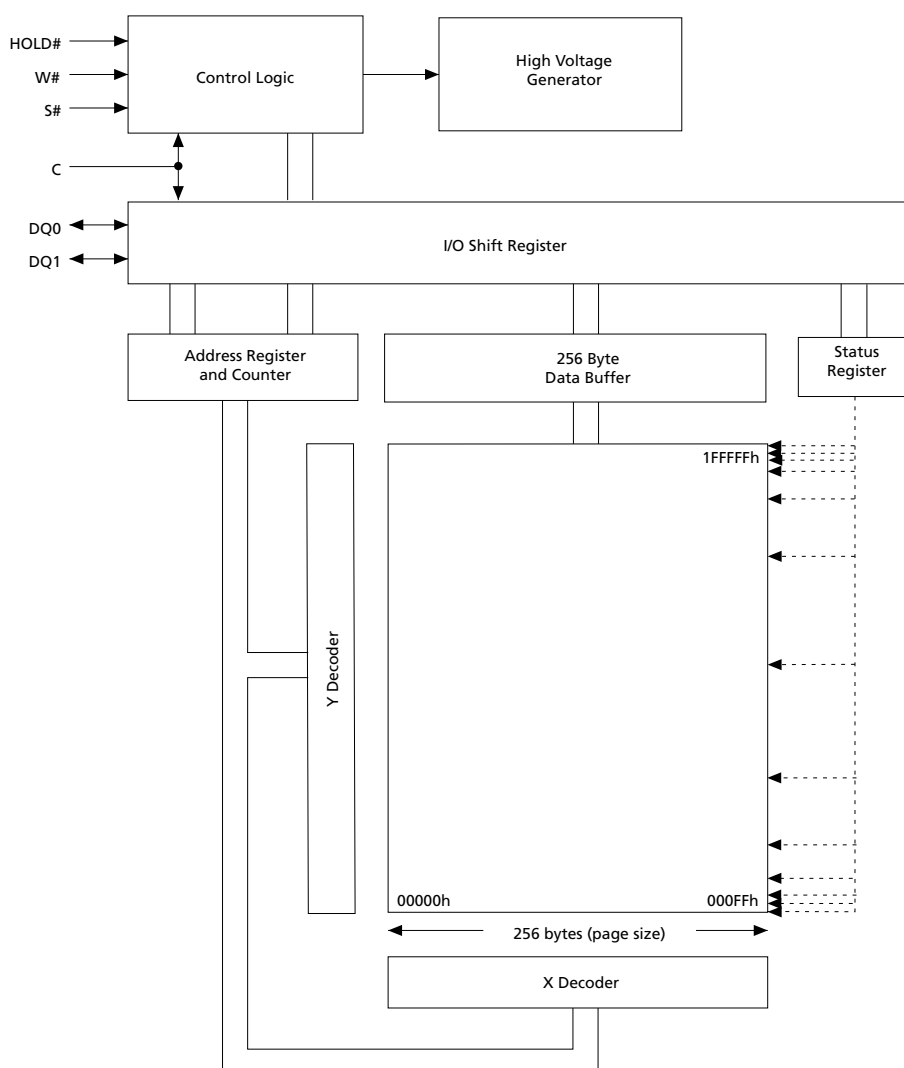
Configuration and Memory Map

Memory Configuration and Block Diagram

Each page of memory can be individually programmed; bits are programmed from 1 to 0. The device is sector or bulk-erasable, but not page-erasable; bits are erased from 0 to 1. The memory is configured as follows:

- 2,097,152 bytes (8 bits each)
- 32 sectors (512Kb, 65KB each)
- 8,192 pages (256 bytes each)

Figure 7: Block Diagram





Memory Map – 16Mb Density

Table 9: Sectors 31:0

| Sector | Address Range | |
|--------|---------------|-----------|
| | Start | End |
| 31 | 001F 0000 | 001F FFFF |
| 30 | 001E 0000 | 001E FFFF |
| 29 | 001D 0000 | 001D FFFF |
| 28 | 001C 0000 | 001C FFFF |
| 27 | 001B 0000 | 001B FFFF |
| 26 | 001A 0000 | 001A FFFF |
| 25 | 0019 0000 | 0019 FFFF |
| 24 | 0018 0000 | 0018 FFFF |
| 23 | 0017 0000 | 0017 FFFF |
| 22 | 0016 0000 | 0016 FFFF |
| 21 | 0015 0000 | 0015 FFFF |
| 20 | 0014 0000 | 0014 FFFF |
| 19 | 0013 0000 | 0013 FFFF |
| 18 | 0012 0000 | 0012 FFFF |
| 17 | 0011 0000 | 0011 FFFF |
| 16 | 0010 0000 | 0010 FFFF |
| 15 | 000F 0000 | 000F FFFF |
| 14 | 000E 0000 | 000E FFFF |
| 13 | 000D 0000 | 000D FFFF |
| 12 | 000C 0000 | 000C FFFF |
| 11 | 000B 0000 | 000B FFFF |
| 10 | 000A 0000 | 000A FFFF |
| 9 | 0009 0000 | 0009 FFFF |
| 8 | 0008 0000 | 0008 FFFF |
| 7 | 0007 0000 | 0007 FFFF |
| 6 | 0006 0000 | 0006 FFFF |
| 5 | 0005 0000 | 0005 FFFF |
| 4 | 0004 0000 | 0004 FFFF |
| 3 | 0003 0000 | 0003 FFFF |
| 2 | 0002 0000 | 0002 FFFF |
| 1 | 0001 0000 | 0001 FFFF |
| 0 | 0000 0000 | 0000 FFFF |

Command Set Overview

All commands, addresses, and data are shifted in and out of the device, most significant bit first.

Serial data inputs DQ0 and DQ1 are sampled on the first rising edge of serial clock (C) after chip select (S#) is driven LOW. Then, the one-byte command code must be shifted in to the device, most significant bit first, on DQ0 and DQ1, each bit being latched on the rising edges of C.

Every command sequence starts with a one-byte command code. Depending on the command, this command code might be followed by address or data bytes, by address and data bytes, or by neither address or data bytes. For the following commands, the shifted-in command sequence is followed by a data-out sequence. S# can be driven HIGH after any bit of the data-out sequence is being shifted out.

- READ DATA BYTES (READ)
- READ DATA BYTES at HIGHER SPEED
- READ STATUS REGISTER
- READ IDENTIFICATION
- RELEASE from DEEP POWER-DOWN

For the following commands, S# must be driven HIGH exactly at a byte boundary. That is, after an exact multiple of eight clock pulses following S# being driven LOW, S# must be driven HIGH. Otherwise, the command is rejected and not executed.

- PAGE PROGRAM
- SECTOR ERASE
- BULK ERASE
- WRITE STATUS REGISTER
- WRITE ENABLE
- WRITE DISABLE

All attempts to access the memory array are ignored during a WRITE STATUS REGISTER command cycle, a PROGRAM command cycle, or an ERASE command cycle. In addition, the internal cycle for each of these commands continues unaffected.

Table 10: Command Set Codes

| Command Name | One-Byte Command Code | | Bytes | | |
|---------------------------------|--------------------------|-----|---------|-------|----------|
| | | | Address | Dummy | Data |
| WRITE ENABLE | 0000 0110 | 06h | 0 | 0 | 0 |
| WRITE DISABLE | 0000 0100 | 04h | 0 | 0 | 0 |
| READ IDENTIFICATION | 1001 1111 | 9Fh | 0 | 0 | 1 to 20 |
| | 1001 1110 | 9Eh | | | |
| READ STATUS REGISTER | 0000 0101 | 05h | 0 | 0 | 1 to ∞ |
| WRITE STATUS REGISTER | 0000 0001 | 01h | 0 | 0 | 1 |
| READ DATA BYTES | 0000 0011 | 03h | 3 | 0 | 1 to ∞ |
| READ DATA BYTES at HIGHER SPEED | 0000 1011 | 0Bh | 3 | 1 | 1 to ∞ |
| PAGE PROGRAM | 0000 0010 | 02h | 3 | 0 | 1 to 256 |
| SECTOR ERASE | 1101 1000 | D8h | 3 | 0 | 0 |
| BULK ERASE | 1100 0111 | C7h | 0 | 0 | 0 |
| DEEP POWER-DOWN | 1011 1001 | B9h | 0 | 0 | 0 |
| RELEASE from DEEP POWER-DOWN | 1010 1011 | ABh | 0 | 0 | 1 to ∞ |

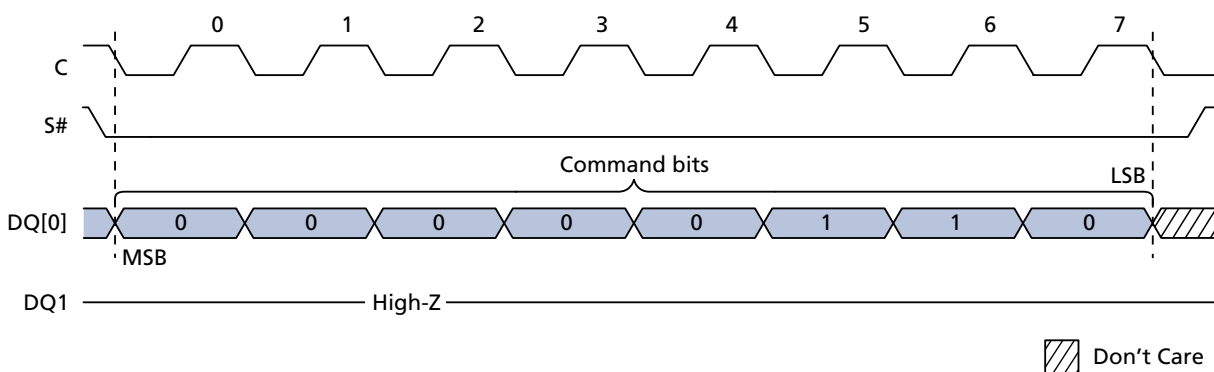
WRITE ENABLE

The WRITE ENABLE command sets the write enable latch (WEL) bit.

The WEL bit must be set before execution of every PROGRAM, ERASE, and WRITE command.

The WRITE ENABLE command is entered by driving chip select (S#) LOW, sending the command code, and then driving S# HIGH.

Figure 8: WRITE ENABLE Command Sequence



WRITE DISABLE

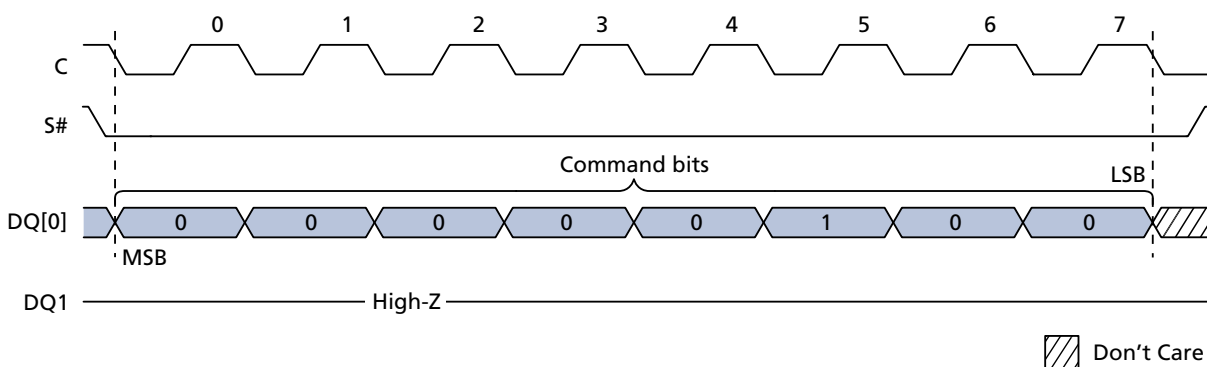
The WRITE DISABLE command resets the write enable latch (WEL) bit.

The WRITE DISABLE command is entered by driving chip select (S#) LOW, sending the command code, and then driving S# HIGH.

The WEL bit is reset under the following conditions:

- Power-up
- Completion of any ERASE operation
- Completion of any PROGRAM operation
- Completion of any WRITE STATUS REGISTER operation
- Completion of WRITE DISABLE operation

Figure 9: WRITE DISABLE Command Sequence



READ IDENTIFICATION

The READ IDENTIFICATION command reads the following device identification data:

- Manufacturer identification (1 byte): This is assigned by JEDEC.
- Device identification (2 bytes): This is assigned by device manufacturer; the first byte indicates memory type and the second byte indicates device memory capacity.
- A Unique ID code (UID) (17 bytes, 16 available upon customer request): The first byte contains length of data to follow; the remaining 16 bytes contain optional Customized Factory Data (CFD) content.

Table 11: READ IDENTIFICATION Data Out Sequence

| Manufacturer Identification | Device Identification | | UID | |
|-----------------------------|-----------------------|-----------------|------------|-------------|
| | Memory Type | Memory Capacity | CFD Length | CFD Content |
| 20h | 20h | 12h | 10h | 16 bytes |
| | | 13h | | |
| | | 14h | | |
| | | 15h | | |
| | | 16h | | |
| | | 17h | | |
| | | 18h | | |

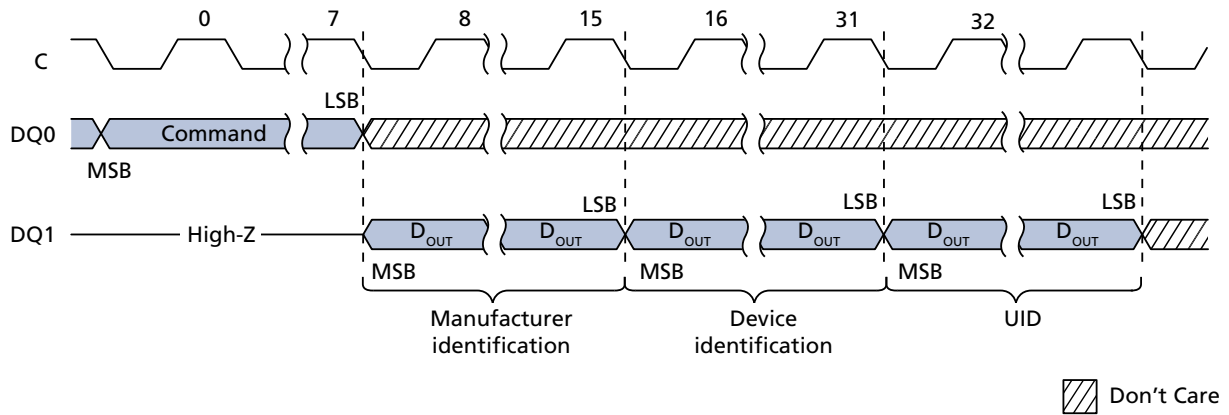
Note: 1. The CFD bytes are read-only and can be programmed with customer data on demand. If customers do not make requests, the devices are shipped with all the CFD bytes programmed to zero. Parts with a top marking year and week code greater than "06/2015" and assembled in the UDFPN8 4mm x 3mm CFD package area are programmed with an UID. To decode top marking year and week codes (week of assembly), see TN-12-24 "Serial Flash Memory Device Marking for the M25P/PE/PX, M45PE, and N25Q Product Families" on micron.com.

A READ IDENTIFICATION command is not decoded while an ERASE or PROGRAM cycle is in progress and has no effect on a cycle in progress. The READ IDENTIFICATION command must not be issued while the device is in DEEP POWER-DOWN mode.

The device is first selected by driving S# LOW. Then the 8-bit command code is shifted in and content is shifted out on DQ1 as follows: the 24-bit device identification that is stored in the memory, the 8-bit CFD length, followed by 16 bytes of CFD content. Each bit is shifted out during the falling edge of serial clock (C).

The READ IDENTIFICATION command is terminated by driving S# HIGH at any time during data output. When S# is driven HIGH, the device is put in the STANDBY POWER mode and waits to be selected so that it can receive, decode, and execute commands.

Figure 10: READ IDENTIFICATION Command Sequence



READ STATUS REGISTER

The READ STATUS REGISTER command allows the status register to be read. The status register may be read at any time, even while a PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress. When one of these cycles is in progress, it is recommended to check the write in progress (WIP) bit before sending a new command to the device. It is also possible to read the status register continuously.

Figure 11: READ STATUS REGISTER Command Sequence

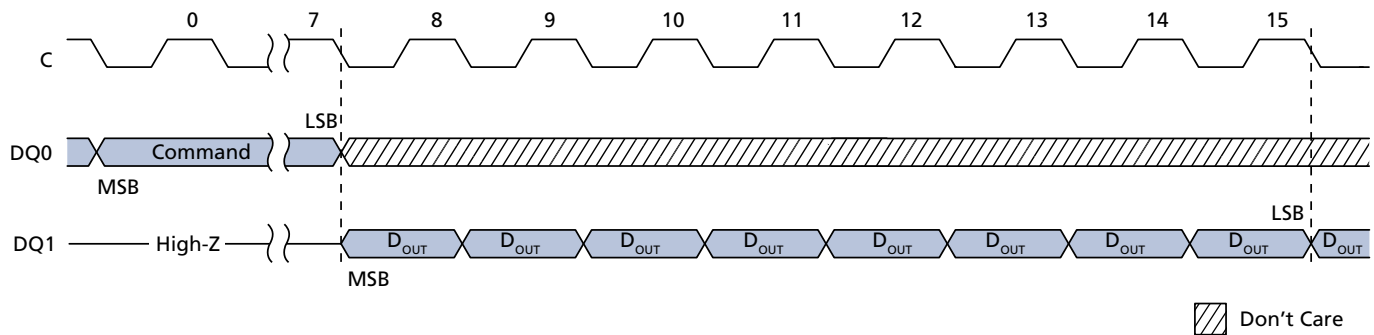


Figure 12: Status Register Format

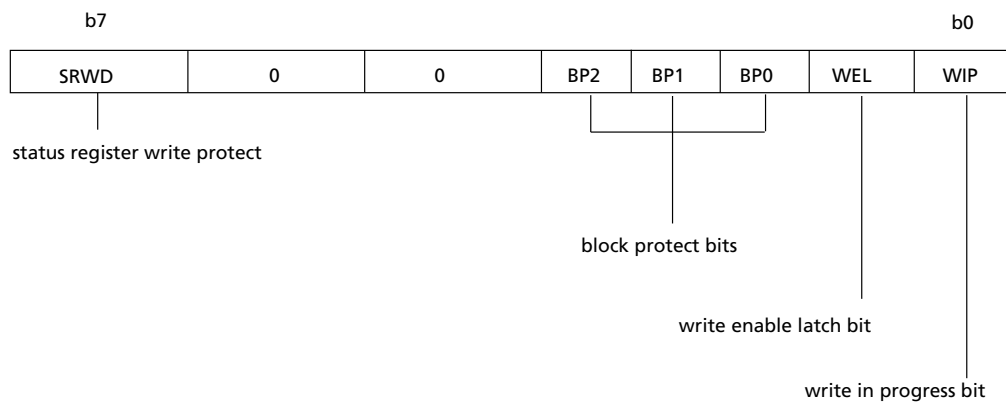
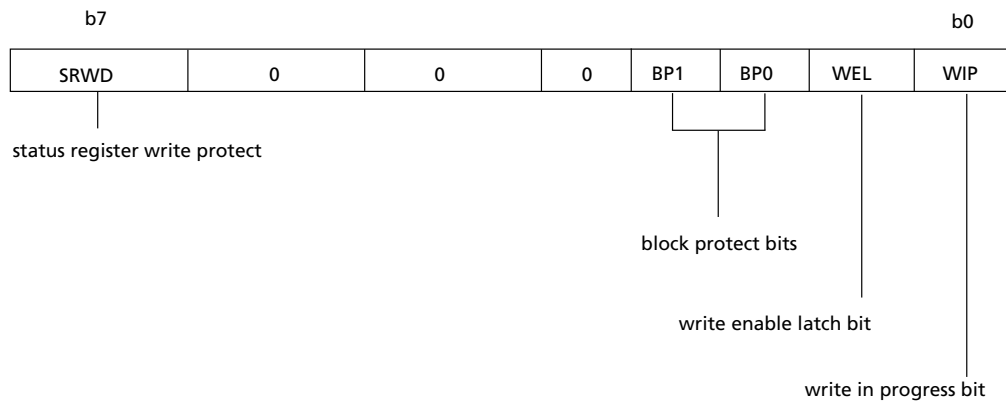


Figure 13: Status Register Format



WIP Bit

The write in progress (WIP) bit indicates whether the memory is busy with a WRITE STATUS REGISTER cycle, a PROGRAM cycle, or an ERASE cycle. When the WIP bit is set to 1, a cycle is in progress; when the WIP bit is set to 0, a cycle is not in progress.

WEL Bit

The write enable latch (WEL) bit indicates the status of the internal write enable latch. When the WEL bit is set to 1, the internal write enable latch is set; when the WEL bit is set to 0, the internal write enable latch is reset and no WRITE STATUS REGISTER, PROGRAM, or ERASE command is accepted.

Block Protect Bits

The block protect bits are non-volatile. They define the size of the area to be software protected against PROGRAM and ERASE commands. The block protect bits are written with the WRITE STATUS REGISTER command.

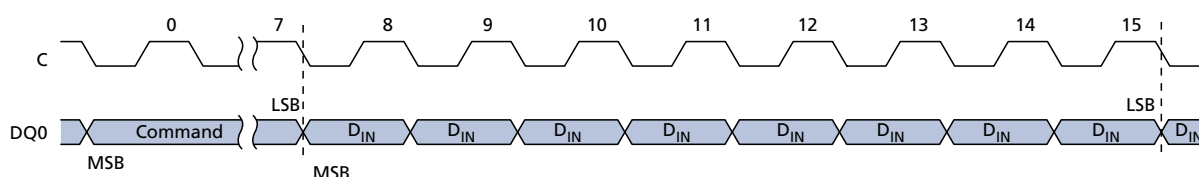
When one or more of the block protect bits is set to 1, the relevant memory area, as defined in the Protected Area Sizes table, becomes protected against PAGE PROGRAM and SECTOR ERASE commands. The block protect bits can be written provided that the hardware protected mode has not been set. The BULK ERASE command is executed only if all block protect bits are 0.

SRWD Bit

The status register write disable (SRWD) bit is operated in conjunction with the write protect ($W\#/V_{PP}$) signal. When the SRWD bit is set to 1 and $W\#/V_{PP}$ is driven LOW, the device is put in the hardware protected mode. In the hardware protected mode, the non-volatile bits of the status register (SRWD, and the block protect bits) become read-only bits and the WRITE STATUS REGISTER command is no longer accepted for execution.

The WRITE STATUS REGISTER command allows new values to be written to the status register. Before the WRITE STATUS REGISTER command can be accepted, a WRITE ENABLE command must have been executed previously. After the WRITE ENABLE command has been decoded and executed, the device sets the write enable latch (WEL) bit.

Figure 14: WRITE STATUS REGISTER Command Sequence



The WRITE STATUS REGISTER command allows the user to change the values of the block protect bits (BP2, BP1, BP0). Setting these bit values defines the size of the area that is to be treated as read-only, as defined in the Protected Area Sizes table.

The WRITE STATUS REGISTER command also allows the user to set and reset the status register write disable (SRWD) bit in accordance with the write protect (W#/V_{PP}) signal. The SRWD bit and the W#/V_{PP} signal allow the device to be put in the hardware protected (HPM) mode. The WRITE STATUS REGISTER command is not executed once the HPM is entered. The options for enabling the status register protection modes are summarized here.

Table 12: Status Register Protection Modes

| W#/V _{pp} Signal | SRWD Bit | Protection Mode (PM) | Status Register Write Protection | Memory Content | | Notes |
|---------------------------|----------|-------------------------------|----------------------------------|-----------------------|-------------------|----------|
| | | | | Protected Area | Unprotected Area | |
| 1 | 0 | Software protected mode (SPM) | Software protection | Commands not accepted | Commands accepted | 1, 2, 3 |
| 0 | 0 | | | | | |
| 1 | 1 | | | | | |
| 0 | 1 | Hardware protected mode (HPM) | Hardware protection | Commands not accepted | Commands accepted | 3, 4, 5, |

- Notes:
1. Software protection: status register is writable (SRWD, BP2, BP1, and BP0 bit values can be changed) if the WRITE ENABLE command has set the WEL bit.
 2. PAGE PROGRAM, SECTOR ERASE, and BULK ERASE commands are not accepted.
 3. PAGE PROGRAM and SECTOR ERASE commands can be accepted.
 4. Hardware protection: status register is not writable (SRWD, BP2, BP1, and BP0 bit values cannot be changed).
 5. PAGE PROGRAM, SECTOR ERASE, and BULK ERASE commands are not accepted.

When the SRWD bit of the status register is 0 (its initial delivery state), it is possible to write to the status register provided that the WEL bit has been set previously by a WRITE ENABLE command, regardless of whether the W#/V_{pp} signal is driven HIGH or LOW. When the status register SRWD bit is set to 1, two cases need to be considered depending on the state of the W#/V_{pp} signal:

- If the W#/V_{pp} signal is driven HIGH, it is possible to write to the status register provided that the WEL bit has been set previously by a WRITE ENABLE command.
- If the W#/V_{pp} signal is driven LOW, it is not possible to write to the status register even if the WEL bit has been set previously by a WRITE ENABLE command. Therefore, attempts to write to the status register are rejected, and are not accepted for execution. The result is that all the data bytes in the memory area that have been put in SPM by the status register block protect bits (BP2, BP1, BP0) are also hardware protected against data modification.

Regardless of the order of the two events, the HPM can be entered in either of the following ways:

- Setting the status register SRWD bit after driving the W#/V_{pp} signal LOW
- Driving the W#/V_{pp} signal LOW after setting the status register SRWD bit.

The only way to exit the HPM is to pull the W#/V_{pp} signal HIGH. If the W#/V_{pp} signal is permanently tied HIGH, the HPM can never be activated. In this case, only the SPM is available, using the status register block protect bits (BP2, BP1, BP0).

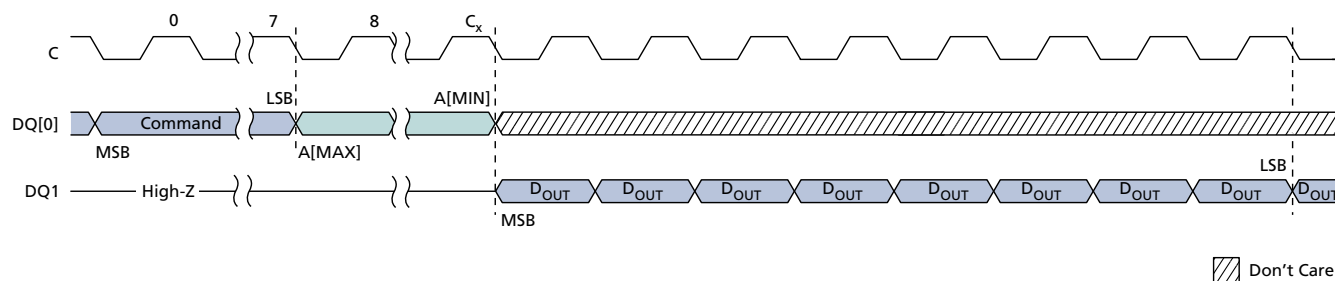
READ DATA BYTES

The device is first selected by driving chip select (S#) LOW. The command code for READ DATA BYTES is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of serial clock (C). Then the memory contents at that address is shifted out on serial data output (DQ1), each bit being shifted out at a maximum frequency f_R during the falling edge of C.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Therefore, the entire memory can be read with a single READ DATA BYTES command. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The READ DATA BYTES command is terminated by driving S# HIGH. S# can be driven HIGH at any time during data output. Any READ DATA BYTES command issued while an ERASE, PROGRAM, or WRITE cycle is in progress is rejected without any effect on the cycle that is in progress.

Figure 15: READ DATA BYTES Command Sequence



Note: 1. $C_x = 7 + (A[MAX] + 1)$.

The device is first selected by driving chip select (S#) LOW. The command code for the READ DATA BYTES at HIGHER SPEED command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of serial clock (C). Then the memory contents at that address are shifted out on serial data output (DQ1) at a maximum frequency ^fC, during the falling edge of C.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Therefore, the entire memory can be read with a single READ DATA BYTES at HIGHER SPEED command. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The READ DATA BYTES at HIGHER SPEED command is terminated by driving S# HIGH. S# can be driven HIGH at any time during data output. Any READ DATA BYTES at HIGHER SPEED command issued while an ERASE, PROGRAM, or WRITE cycle is in progress is rejected without any effect on the cycle that is in progress.

The diagram illustrates the timing of a 16-bit data bus. The clock signal C is shown at the top. The data bus $DQ0$ and $DQ1$ are shown below. The $DQ0$ signal shows a Command phase (MSB to LSB), followed by a High-Z phase, and then a series of data cycles (D_OUT) from MSB to LSB. The $DQ1$ signal shows a High-Z phase followed by a series of data cycles (D_OUT) from MSB to LSB. A legend indicates that the hatched area represents 'Don't Care'.

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SECTOR ERASE

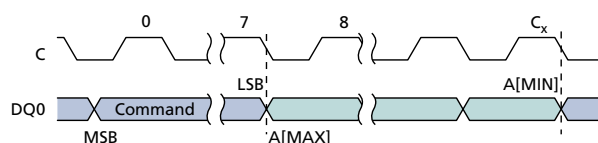
The SECTOR ERASE command sets to 1 (FFh) all bits inside the chosen sector. Before the SECTOR ERASE command can be accepted, a WRITE ENABLE command must have been executed previously. After the WRITE ENABLE command has been decoded, the device sets the write enable latch (WEL) bit.

The SECTOR ERASE command is entered by driving chip select (S#) LOW, followed by the command code, and three address bytes on serial data input (DQ0). Any address inside the sector is a valid address for the SECTOR ERASE command. S# must be driven LOW for the entire duration of the sequence.

S# must be driven HIGH after the eighth bit of the last address byte has been latched in. Otherwise the SECTOR ERASE command is not executed. As soon as S# is driven HIGH, the self-timed SECTOR ERASE cycle is initiated; the cycle's duration is t_{SE} . While the SECTOR ERASE cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The WIP bit is 1 during the self-timed SECTOR ERASE cycle, and is 0 when the cycle is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

A SECTOR ERASE command is not executed if it applies to a sector that is hardware or software protected.

Figure 18: SECTOR ERASE Command Sequence



Note: 1. $Cx = 7 + (A[MAX] + 1)$.

BULK ERASE

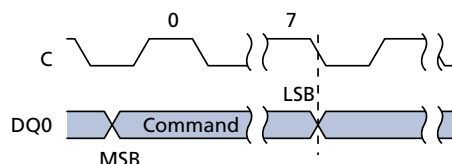
The BULK ERASE command sets all bits to 1 (FFh). Before the BULK ERASE command can be accepted, a WRITE ENABLE command must have been executed previously. After the WRITE ENABLE command has been decoded, the device sets the write enable latch (WEL) bit.

The BULK ERASE command is entered by driving chip select (S#) LOW, followed by the command code on serial data input (DQ0). S# must be driven LOW for the entire duration of the sequence.

S# must be driven HIGH after the eighth bit of the command code has been latched in. Otherwise the BULK ERASE command is not executed. As soon as S# is driven HIGH, the self-timed BULK ERASE cycle is initiated; the cycle's duration is t_{BE} . While the BULK ERASE cycle is in progress, the status register may be read to check the value of the write In progress (WIP) bit. The WIP bit is 1 during the self-timed BULK ERASE cycle, and is 0 when the cycle is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

The BULK ERASE command is executed only if all block protect (BP2, BP1, BP0) bits are 0. The BULK ERASE command is ignored if one or more sectors are protected.

Figure 19: BULK ERASE Command Sequence



DEEP POWER-DOWN

Executing the DEEP POWER-DOWN command is the only way to put the device in the lowest power consumption mode, the DEEP POWER-DOWN mode. The DEEP POWER-DOWN command can also be used as a software protection mechanism while the device is not in active use because in the DEEP POWER-DOWN mode the device ignores all WRITE, PROGRAM, and ERASE commands.

Driving chip select (S#) HIGH deselects the device, and puts it in the STANDBY POWER mode if there is no internal cycle currently in progress. Once in STANDBY POWER mode, the DEEP POWER-DOWN mode can be entered by executing the DEEP POWER-DOWN command, subsequently reducing the standby current from I_{CC1} to I_{CC2} .

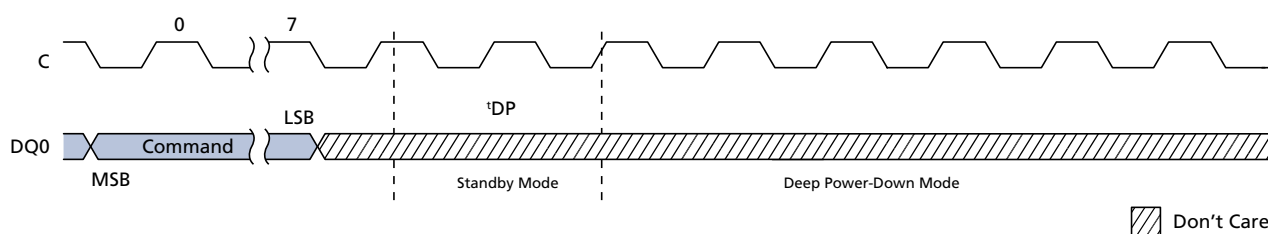
To take the device out of DEEP POWER-DOWN mode, the RELEASE from DEEP POWER-DOWN command must be issued. Other commands must not be issued while the device is in DEEP POWER-DOWN mode. The DEEP POWER-DOWN mode stops automatically at power-down. The device always powers up in STANDBY POWER mode.

The DEEP POWER-DOWN command is entered by driving S# LOW, followed by the command code on serial data input (DQ0). S# must be driven LOW for the entire duration of the sequence.

S# must be driven HIGH after the eighth bit of the command code has been latched in. Otherwise the DEEP POWER-DOWN command is not executed. As soon as S# is driven HIGH, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the DEEP POWER-DOWN mode is entered.

Any DEEP POWER-DOWN command issued while an ERASE, PROGRAM, or WRITE cycle is in progress is rejected without any effect on the cycle that is in progress.

Figure 20: DEEP POWER-DOWN Command Sequence



RELEASE from DEEP POWER-DOWN

Once the device has entered DEEP POWER-DOWN mode, all commands are ignored except RELEASE from DEEP POWER-DOWN and READ ELECTRONIC SIGNATURE. Executing either of these commands takes the device out of the DEEP POWER-DOWN mode.

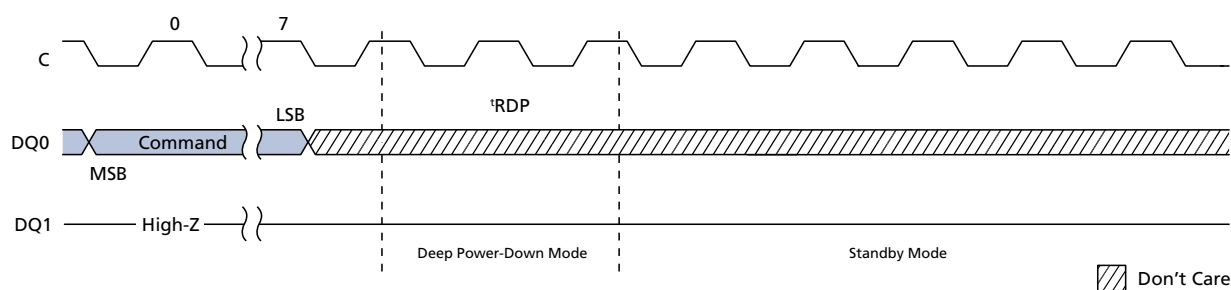
The RELEASE from DEEP POWER-DOWN command is entered by driving chip select (S#) LOW, followed by the command code on serial data input (DQ0). S# must be driven LOW for the entire duration of the sequence.

The RELEASE from DEEP POWER-DOWN command is terminated by driving S# HIGH. Sending additional clock cycles on serial clock C while S# is driven LOW causes the command to be rejected and not executed.

After S# has been driven HIGH, followed by a delay, t_{RES} , the device is put in the STANDBY mode. S# must remain HIGH at least until this period is over. The device waits to be selected so that it can receive, decode, and execute commands.

Any RELEASE from DEEP POWER-DOWN command issued while an ERASE, PROGRAM, or WRITE cycle is in progress is rejected without any effect on the cycle that is in progress.

Figure 21: RELEASE from DEEP POWER-DOWN Command Sequence



READ ELECTRONIC SIGNATURE

Once the device enters DEEP POWER-DOWN mode, all commands are ignored except READ ELECTRONIC SIGNATURE and RELEASE from DEEP POWER-DOWN. Executing either of these commands takes the device out of the DEEP POWER-DOWN mode.

The READ ELECTRONIC SIGNATURE command is entered by driving chip select (S#) LOW, followed by the command code and three dummy bytes on serial data input (DQ0). Each bit is latched in on the rising edge of serial clock C. The 8-bit electronic signature is shifted out on serial data output DQ1 on the falling edge of C; S# must be driven LOW the entire duration of the sequence for the electronic signature to be read. However, driving S# HIGH after the command code, but before the entire 8-bit electronic signature has been output for the first time, still ensures that the device is put into STANDBY mode.

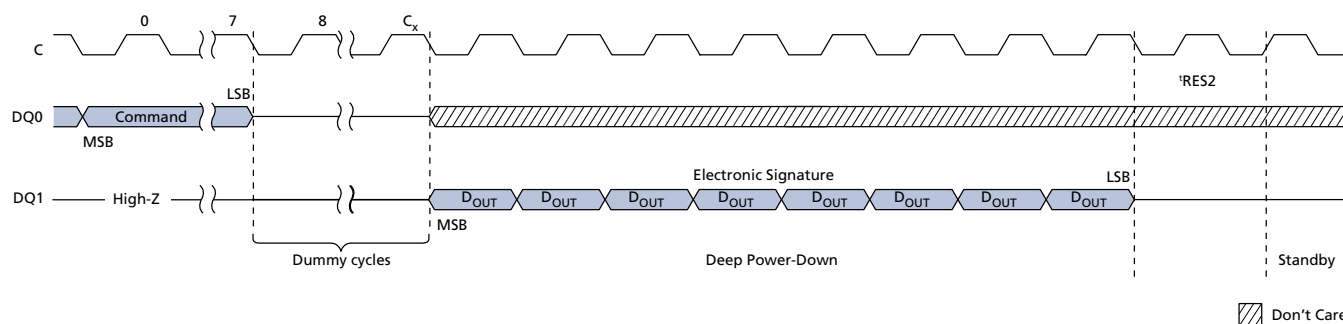
Except while an ERASE, PROGRAM, or WRITE STATUS REGISTER cycle is in progress, the READ ELECTRONIC SIGNATURE command provides access to the 8-bit electronic signature of the device, and can be applied even if DEEP POWER-DOWN mode has not been entered. The READ ELECTRONIC SIGNATURE command is not executed while an ERASE, PROGRAM, or WRITE STATUS REGISTER cycle is in progress and has no effect on the cycle in progress.

The READ ELECTRONIC SIGNATURE command is terminated by driving S# high after the electronic signature has been read at least once. Sending additional clock cycles C while S# is driven LOW causes the electronic signature to be output repeatedly.

If S# is driven HIGH, the device is put in STANDBY mode immediately unless it was previously in DEEP POWER-DOWN mode. If previously in DEEP POWER-DOWN mode, the device transitions to STANDBY mode with delay as described here. Once in STANDBY mode, the device waits to be selected so that it can receive, decode, and execute instructions.

- If S# is driven HIGH before the electronic signature is read, transition to STANDBY mode is delayed by tRES1, as shown in the RELEASE from DEEP POWER-DOWN command sequence. S# must remain HIGH for at least tRES1(max).
- If S# is driven HIGH after the electronic signature is read, transition to STANDBY mode is delayed by tRES2. S# must remain HIGH for at least tRES2(max).

Figure 22: READ ELECTRONIC SIGNATURE Command Sequence



Note: 1. $C_x = 7 + (A[\text{MAX}] + 1)$.

Power-Up/Down and Supply Line Decoupling

At power-up and power-down, the device must not be selected; that is, chip select (S#) must follow the voltage applied on V_{CC} until V_{CC} reaches the correct value:

- $V_{CC,min}$ at power-up, and then for a further delay of t_{VSL}
- V_{SS} at power-down

A safe configuration is provided in the SPI Modes section.

To avoid data corruption and inadvertent write operations during power-up, a power-on-reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the POR threshold voltage, V_{WI} – all operations are disabled, and the device does not respond to any instruction. Moreover, the device ignores the following instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold:

- WRITE ENABLE
- PAGE PROGRAM
- SECTOR ERASE
- BULK ERASE
- WRITE STATUS REGISTER

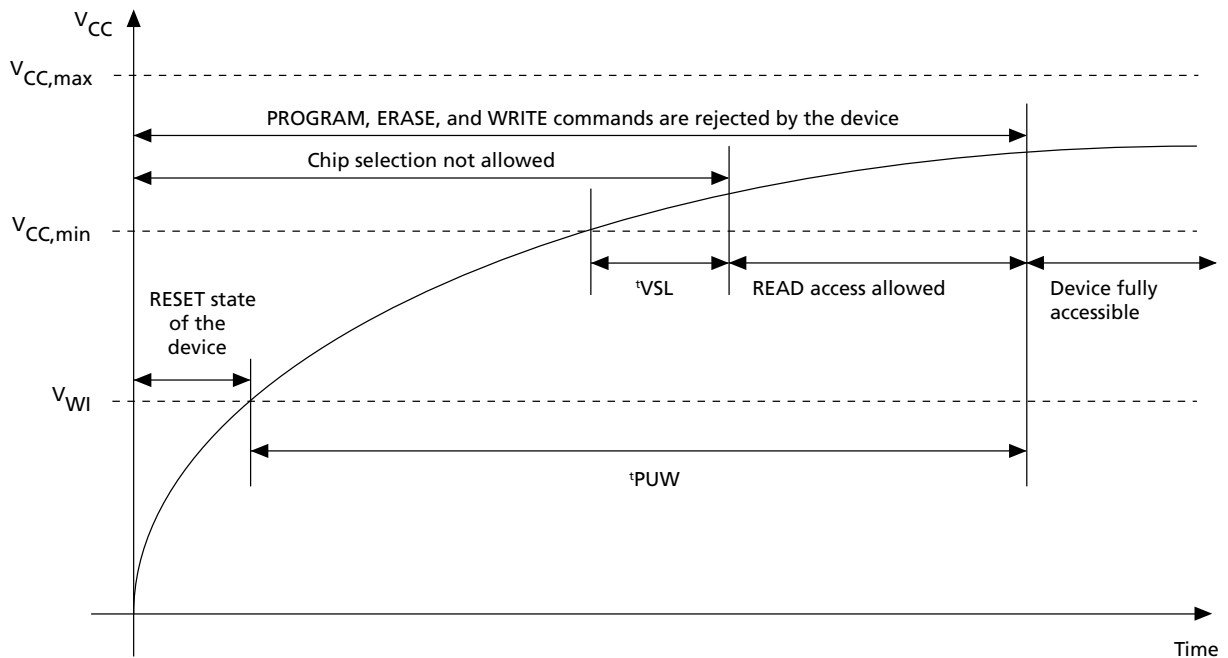
However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below $V_{CC,min}$. No WRITE STATUS REGISTER, PROGRAM, or ERASE instruction should be sent until:

- t_{PUW} after V_{CC} has passed the V_{WI} threshold
- t_{VSL} after V_{CC} has passed the $V_{CC,min}$ level

If the time, t_{VSL} , has elapsed, after V_{CC} rises above $V_{CC,min}$, the device can be selected for READ instructions even if the t_{PUW} delay has not yet fully elapsed.

V_{PPH} must be applied only when V_{CC} is stable and in the $V_{CC,min}$ to $V_{CC,max}$ voltage range.

Figure 23: Power-Up Timing



After power-up, the device is in the following state:

- Standby power mode (not the deep power-down mode)
- Write enable latch (WEL) bit is reset
- Write in progress (WIP) bit is reset
- Write lock bit = 0
- Lock down bit = 0

Normal precautions must be taken for supply line decoupling to stabilize the V_{CC} supply. Each device in a system should have the V_{CC} line decoupled by a suitable capacitor close to the package pins; generally, this capacitor is of the order of 100 nF.

At power-down, when V_{CC} drops from the operating voltage to below the POR threshold voltage V_{WL} , all operations are disabled and the device does not respond to any instruction.

Note: If power-down occurs while a WRITE, PROGRAM, or ERASE cycle is in progress, some data corruption may result.



Power-Up Timing and Write Inhibit Voltage Threshold Specifications

Table 13: Power-Up Timing and V_{WI} Threshold

| Symbol | Parameter | Min | Max | Unit |
|-----------|---------------------------------|-----|-----|---------------|
| t_{VSL} | $V_{CC}(\text{min})$ to S# LOW | 30 | – | μs |
| t_{PUW} | Time delay to write instruction | 1.0 | 10 | ms |
| V_{WI} | Write Inhibit voltage | 1.0 | 2.1 | V |

Note: 1. Parameters are characterized only.

If the time, t_{VSL} , has elapsed, after V_{CC} rises above $V_{CC}(\text{min})$, the device can be selected for READ instructions even if the t_{PUW} delay has not yet fully elapsed.

V_{PPH} must be applied only when V_{CC} is stable and in the $V_{CC\text{min}}$ to $V_{CC\text{max}}$ voltage range.

Maximum Ratings and Operating Conditions

Caution: Stressing the device beyond the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device beyond any specification or condition in the operating sections of this data sheet is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 14: Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units | Notes |
|-------------------|--|-------|----------------------|-------|-------|
| T _{STG} | Storage temperature | –65 | 150 | °C | |
| T _{LEAD} | Lead temperature during soldering | – | See note | °C | 1 |
| V _{IO} | Input and output voltage (with respect to ground) | –0.6 | V _{CC} +0.6 | V | 2 |
| V _{CC} | Supply voltage | –0.6 | 4.0 | V | |
| V _{PP} | FAST PROGRAM / ERASE voltage | –0.2 | 10.0 | V | |
| V _{ESD} | Electrostatic discharge voltage (Human Body model) | –2000 | 2000 | V | 3 |

- Notes:
1. The T_{LEAD} signal is compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the Micron RoHS-compliant 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
 2. The minimum voltage may reach the value of –2V for no more than 20ns during transitions; the maximum may reach the value of V_{CC} +2V for no more than 20ns during transitions.
 3. The V_{ESD} signal: JEDEC Std JESD22-A114A (C1 = 100 pF, R1 = 1500Ω, R2 = 500Ω).

Table 15: Operating Conditions

| Symbol | Parameter | Min | Typical | Max | Unit | Notes |
|-------------------|---|-----|---------|-----|------|-------|
| V _{CC} | Supply voltage | 2.7 | – | 3.6 | V | |
| V _{PPH} | Supply voltage on W#/V _{PP} pin for FAST PROGRAM / ERASE | 8.5 | – | 9.5 | V | |
| T _A | Ambient operating temperature (grade 6) | –40 | – | 85 | °C | 1 |
| T _A | Ambient operating temperature (grade 3) | –40 | – | 125 | °C | 2 |
| T _{AVPP} | Ambient operating temperature for FAST PROGRAM / ERASE | 15 | 25 | 35 | °C | |

- Notes:
1. Autograde 6 and standard parts (grade 6) are tested to 85 °C. Autograde 6 follows the high reliability certified test flow.
 2. Autograde 3 is tested to 125 °C.

Table 16: Data Retention and Endurance

| Symbol | Condition | Min | Max | Unit |
|----------------------|-------------------------------|---------|-----|------------------|
| Program/Erase Cycles | Grade 6, grade 3, autograde 6 | 100,000 | – | Cycles per block |
| Data Retention | at 55°C | 20 | – | Years |



Micron M25P16 Serial Flash Embedded Memory Maximum Ratings and Operating Conditions

Electrical Characteristics

Table 17: DC Current Specifications

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|-------------------|--|---|-----|-----------|-------|
| I _{LI} | Input leakage current | – | – | ±2 | μA |
| I _{LO} | Output leakage current | – | – | ±2 | μA |
| I _{CC1} | Standby current (grade 6) | S# = V _{CC} , V _{IN} = V _{SS} or V _{CC} | – | 50 | μA |
| I _{CC1} | Standby current (grade 3) | | – | 100 | μA |
| I _{CC2} | Deep power-down current (grade 6) | S# = V _{CC} , V _{IN} = V _{SS} or V _{CC} | – | 10 | μA |
| I _{CC2} | Deep power-down current (grade 3) | | – | 100 | μA |
| | | | | 100 50 | |
| I _{CC3} | Operating current (READ) | C = 0.1V _{CC} / 0.9V _{CC} at 75MHz, DQ1 = open | – | 8 | mA |
| | | C = 0.1V _{CC} / 0.9V _{CC} at 33MHz, DQ1 = open | – | 4 | mA |
| I _{CC4} | Operating current (PAGE PROGRAM) | S# = V _{CC} | – | 15 | mA |
| I _{CC5} | Operating current (WRITE STATUS REGISTER) | S# = V _{CC} | – | 15 | mA |
| I _{CC6} | Operating current (SECTOR ERASE) | S# = V _{CC} | – | 15 | mA |
| I _{CC7} | Operating current (BULK ERASE) | S# = V _{CC} | – | 15 | mA |
| I _{CCPP} | Operating current (FAST PROGRAM/ERASE) | S# = V _{CC} , V _{pp} = V _{PPH} | – | 20 | mA |
| I _{PP} | V _{pp} operating current (FAST PROGRAM/ERASE) | S# = V _{CC} , V _{pp} = V _{PPH} | – | 20 | mA |

Table 18: DC Voltage Specifications

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|----------|---------------------|----------------------|--------------|--------------|-------|
| V_{IL} | Input LOW voltage | – | –0.5 | $0.3V_{CC}$ | V |
| V_{IH} | Input HIGH voltage | – | $0.7V_{CC}$ | $V_{CC}+0.4$ | V |
| V_{OL} | Output LOW voltage | $I_{OL} = 1.6mA$ | – | 0.4 | V |
| V_{OH} | Output HIGH voltage | $I_{OH} = -100\mu A$ | $V_{CC}-0.2$ | – | V |

AC Characteristics

In the following AC specifications, output HIGH-Z is defined as the point where data out is no longer driven; however, this is not applicable to the M25PX64 device.

Table 19: AC Measurement Conditions

| Symbol | Parameter | Min | Max | Unit |
|--------|----------------------------------|--------------|--------------|------|
| C_L | Load capacitance | 30 | 30 | pF |
| | Input rise and fall times | – | 5 | ns |
| | Input pulse voltages | $0.2 V_{CC}$ | $0.8 V_{CC}$ | V |
| | Input timing reference voltages | $0.3 V_{CC}$ | $0.7 V_{CC}$ | V |
| | Output timing reference voltages | $V_{CC} / 2$ | $V_{CC} / 2$ | V |

Figure 24: AC Measurement I/O Waveform

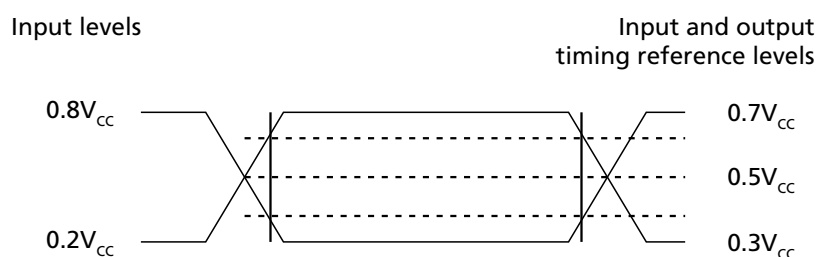


Table 20: Capacitance

| Symbol | Parameter | Test Condition | Min | Max | Unit | Notes |
|-----------|--------------------------------|-----------------|-----|-----|------|-------|
| C_{OUT} | Output capacitance (DQ1) | $V_{OUT} = 0 V$ | – | 8 | pF | 1 |
| C_{IN} | Input capacitance (other pins) | $V_{IN} = 0 V$ | – | 6 | pF | |

Note: 1. Values are sampled only, not 100% tested, at $T_A = 25^\circ C$ and a frequency of 25 MHz.

Table 21: AC Specifications (25 MHz, Device Grade 3, $V_{CC}[\min]=2.7V$)

| Symbol | Alt. | Parameter | Min | Typ | Max | Unit | Notes |
|------------|-----------|---|------|-----|-----|------|-------|
| f_C | f_C | Clock frequency for commands (See note) | D.C. | – | 25 | MHz | 1 |
| f_R | – | Clock frequency for READ command | D.C. | – | 20 | MHz | |
| t_{CH} | t_{CLH} | Clock HIGH time | 18 | – | – | ns | 2 |
| t_{CL} | t_{CLL} | Clock LOW time | 18 | – | – | ns | 2 |
| t_{CLCH} | – | Clock rise time (peak to peak) | 0.1 | – | – | V/ns | 3, 4 |
| t_{CHCL} | – | Clock fall time (peak to peak) | 0.1 | – | – | V/ns | 3, 4 |
| t_{SLCH} | t_{CSS} | S# active setup time (relative to C) | 10 | – | – | ns | |

Table 21: AC Specifications (25 MHz, Device Grade 3, $V_{CC}[\min]=2.7V$) (Continued)

| Symbol | Alt. | Parameter | Min | Typ | Max | Unit | Notes |
|------------|-----------|--|-----|-----|-----|---------|-------|
| t_{CHSL} | — | S# not active hold time (relative to C) | 10 | — | — | ns | |
| t_{DVCH} | t_{DSU} | Data in setup time | 5 | — | — | ns | |
| t_{CHDX} | t_{DH} | Data in hold time | 5 | — | — | ns | |
| t_{CHSH} | — | S# active hold time (relative to C) | 10 | — | — | ns | |
| t_{SHCH} | — | S# not active setup time (relative to C) | 10 | — | — | ns | |
| t_{SHSL} | t_{CSH} | S# deselect time | 100 | — | — | ns | |
| t_{SHQZ} | t_{DIS} | Output disable time | — | — | 15 | ns | 3 |
| t_{CLQV} | t_V | Clock LOW to output valid | — | — | 15 | ns | |
| t_{CLQX} | t_{HO} | Output hold time | 0 | — | — | ns | |
| t_{HLCH} | — | HOLD# setup time (relative to C) | 10 | — | — | ns | |
| t_{CHHH} | — | HOLD# hold time (relative to C) | 10 | — | — | ns | |
| t_{HHCH} | — | HOLD# setup time (relative to C) | 10 | — | — | ns | |
| t_{CHHL} | — | HOLD# hold time (relative to C) | 10 | — | — | ns | |
| t_{HHQX} | t_{LZ} | HOLD# to output LOW-Z | — | — | 15 | ns | 3 |
| t_{HLQZ} | t_{HZ} | HOLD# to output HIGH-Z | — | — | 20 | ns | 3 |
| t_{WHSL} | — | WRITE PROTECT setup time | 20 | — | — | ns | 5 |
| t_{SHWL} | — | WRITE PROTECT hold time | 100 | — | — | ns | 5 |
| t_{DP} | — | S# HIGH to DEEP POWER-DOWN mode | — | — | 3 | μs | 3 |
| t_{RES1} | — | S# HIGH to STANDBY without READ ELECTRONIC SIGNATURE | — | — | 30 | μs | 3 |
| t_{RES2} | — | S# HIGH to STANDBY with READ ELECTRONIC SIGNATURE | — | — | 30 | μs | 3 |

- Notes:
1. READ DATA BYTES at HIGHER SPEED, PAGE PROGRAM, SECTOR ERASE, BLOCK ERASE, DEEP POWER-DOWN, READ ELECTRONIC SIGNATURE, WRITE ENABLE/DISABLE, READ ID, READ/WRITE STATUS REGISTER
 2. The t_{CH} and t_{CL} signals must be greater than or equal to $1/f_C$.
 3. The t_{CLCH} , t_{CHCL} , t_{SHQZ} , t_{HHQX} , t_{HLQZ} , t_{DP} , t_{RES1} , and t_{RES2} signal values are guaranteed by characterization, not 100% tested in production.
 4. The t_{CLCH} and t_{CHCL} signals clock rise and fall time values are expressed as a slew-rate.
 5. The t_{WHSL} and t_{SHWL} signals are only applicable as a constraint for a WRITE STATUS REGISTER command when SRWD bit is set at 1.

Table 22: Instruction Times (25 MHz, Device Grade 3, $V_{CC}[\min]=2.7V$)

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|----------|--------------------------------------|-----|--------------------------------|-----|-------|-------|
| t_W | WRITE STATUS REGISTER cycle time | — | 1.5 | 15 | ms | |
| t_{PP} | PAGE PROGRAM cycle time (256 bytes) | — | 0.8 | 5 | ms | 2, 3 |
| t_{PP} | PAGE PROGRAM cycle time (n bytes) | — | $\text{int}(n/8) \times 0.025$ | | | |
| t_{SE} | SECTOR ERASE cycle time | — | 0.8 | 3 | s | |

Table 22: Instruction Times (25 MHz, Device Grade 3, $V_{CC}[\min]=2.7V$) (Continued)

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|----------|-----------------------|-----|-----|-----|-------|-------|
| t_{BE} | BULK ERASE cycle time | – | 10 | 20 | s | |

- Notes:
1. Applies to the entire table: Typical values are given for $T_A = 85^\circ C$.
 2. When using the PAGE PROGRAM command to program consecutive bytes, optimized timings are obtained in one sequence that includes all the bytes rather than in several sequences of only a few bytes ($1 \leq n \leq 256$).
 3. $\text{int}(A)$ corresponds to the upper integer part of A. For example, $\text{int}(12/8) = 2$ and $\text{int}(32/8) = 4$.

Table 23: AC Specifications (75 MHz, Device Grade 3 and 6, $V_{CC}[\min]=2.7V$)

| Symbol | Alt. | Parameter | Min | Typ | Max | Unit | Notes |
|------------|-----------|--|------|-----|-----|---------|-------|
| f_C | f_C | Clock frequency for all commands (except READ) | D.C. | – | 75 | MHz | |
| f_R | – | Clock frequency for READ command | D.C. | – | 33 | MHz | |
| t_{CH} | t_{CLH} | Clock HIGH time | 6 | – | – | ns | 2 |
| t_{CL} | t_{CLL} | Clock LOW time | 6 | – | – | ns | 2 |
| t_{CLCH} | – | Clock rise time (peak to peak) | 0.1 | – | – | V/ns | 3, 4 |
| t_{CHCL} | – | Clock fall time (peak to peak) | 0.1 | – | – | V/ns | 3, 4 |
| t_{SLCH} | t_{CSS} | S# active setup time (relative to C) | 5 | – | – | ns | |
| t_{CHSL} | | S# not active hold time (relative to C) | 5 | – | – | ns | |
| t_{DVCH} | t_{DSU} | Data In setup time | 2 | – | – | ns | |
| t_{CHDX} | t_{DH} | Data In hold time | 5 | – | – | ns | |
| t_{CHSH} | – | S# active hold time (relative to C) | 5 | – | – | ns | |
| t_{SHCH} | – | S# not active setup time (relative to C) | 5 | – | – | ns | |
| t_{SHSL} | t_{CSH} | S# deselect time | 100 | – | – | ns | |
| t_{SHQZ} | t_{DIS} | Output disable time | – | – | 8 | ns | 3 |
| t_{CLQV} | t_V | Clock LOW to output valid under 30 pF | – | – | 8 | ns | |
| | | Clock LOW to output valid under 10 pF | – | – | 6 | ns | |
| t_{CLQX} | t_{HO} | Output hold time | 0 | – | – | ns | |
| t_{HLCH} | – | HOLD# setup time (relative to C) | 5 | – | – | ns | |
| t_{CHHH} | – | HOLD# hold time (relative to C) | 5 | – | – | ns | |
| t_{HHCH} | – | HOLD# setup time (relative to C) | 5 | – | – | ns | |
| t_{CHHL} | – | HOLD# hold time (relative to C) | 5 | – | – | ns | |
| t_{HHQX} | t_{LZ} | HOLD# to output LOW-Z | – | – | 8 | ns | 3 |
| t_{HLQZ} | t_{HZ} | HOLD# to output HIGH-Z | – | – | 8 | ns | 3 |
| t_{WHSL} | – | WRITE PROTECT setup time | 20 | – | – | ns | 5 |
| t_{SHWL} | – | WRITE PROTECT hold time | 100 | – | – | ns | 5 |
| t_{DP} | – | S# HIGH to DEEP POWER-DOWN mode | – | – | 3 | μs | 3 |
| t_{RES1} | – | S# HIGH to STANDBY without READ ELECTRONIC SIGNATURE | – | – | 30 | μs | 3 |

Table 23: AC Specifications (75 MHz, Device Grade 3 and 6, V_{CC}[min]=2.7V) (Continued)

| Symbol | Alt. | Parameter | Min | Typ | Max | Unit | Notes |
|-------------------|------|---|-----|-----|-----|------|-------|
| t _{RES2} | — | S# HIGH to STANDBY with READ ELECTRONIC SIGNATURE | — | — | 30 | μs | 3 |

- Notes:
1. Applies to entire table: 110nm technology devices are identified by the process identification digit 4 in the device marking and the process letter B in the part number.
 2. The t_{CH} and t_{CL} signal values must be greater than or equal to 1/f_C.
 3. The t_{CLCH}, t_{CHCL}, t_{SHQZ}, t_{HHQX}, t_{HLQZ}, t_{DP}, and t_{RDP} signal values are guaranteed by characterization, not 100% tested in production.
 4. The t_{CLCH} and t_{CHCL} signals clock rise and fall time values are expressed as a slew-rate.
 5. The t_{WHSL} and t_{SHWL} signal values are only applicable as a constraint for a WRITE STATUS REGISTER command when SRWD bit is set at 1.

Table 24: Instruction Times (75 MHz, Device Grade 3 and 6, V_{CC}[min]=2.7V)

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|-----------------|---|-----|------------------|-----|-------|-------|
| t _W | WRITE STATUS REGISTER cycle time | — | 1.3 | 15 | ms | |
| t _{PP} | PAGE PROGRAM cycle time (256 bytes) | — | 0.64 | 5 | ms | 3, 4 |
| t _{PP} | PAGE PROGRAM cycle time (n bytes, where n = 1 to 4) | — | 0.01 | | | |
| t _{PP} | PAGE PROGRAM cycle time (n bytes, where n = 5 to 246) | — | int (n/8) x 0.02 | | | |
| t _{SE} | SECTOR ERASE cycle time | — | 0.6 | 3 | s | |
| t _{BE} | BULK ERASE cycle time | — | 8 | 20 | s | |
| | | | 13 | 40 | | |

- Notes:
1. Applies to the entire table: Typical values are given for T_A = 25 °C.
 2. Applies to the entire table: 110nm technology devices are identified by the process identification digit 4 in the device marking and the process letter B in the part number.
 3. When using the PAGE PROGRAM command to program consecutive bytes, optimized timings are obtained in one sequence that includes all the bytes rather than in several sequences of only a few bytes (1 ≤ n ≤ 256).
 4. int(A) corresponds to the upper integer part of A. For example, int(12/8) = 2 and int(32/8) = 4.

Figure 25: Serial Input Timing

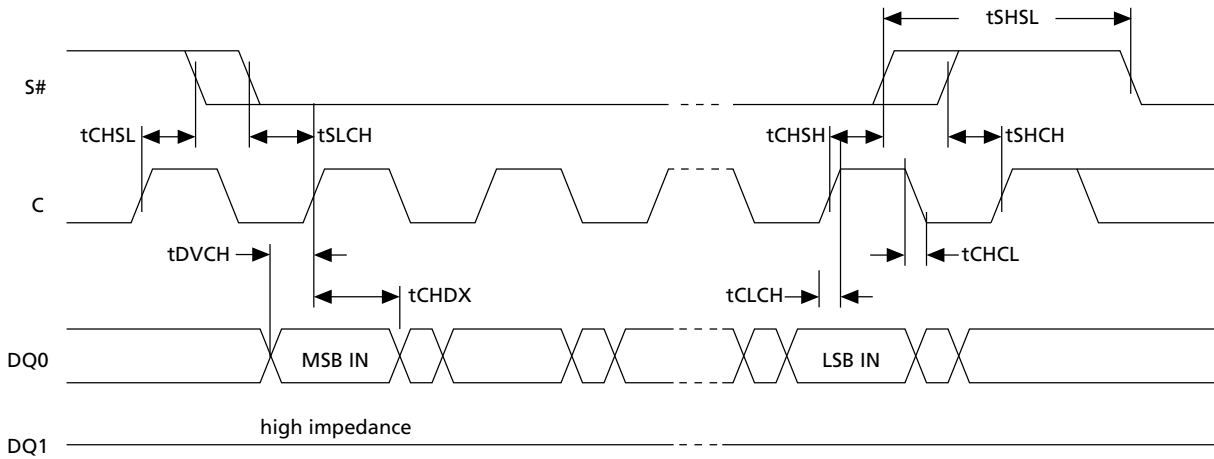


Figure 26: Write Protect Setup and Hold during WRSR when SRWD=1 Timing

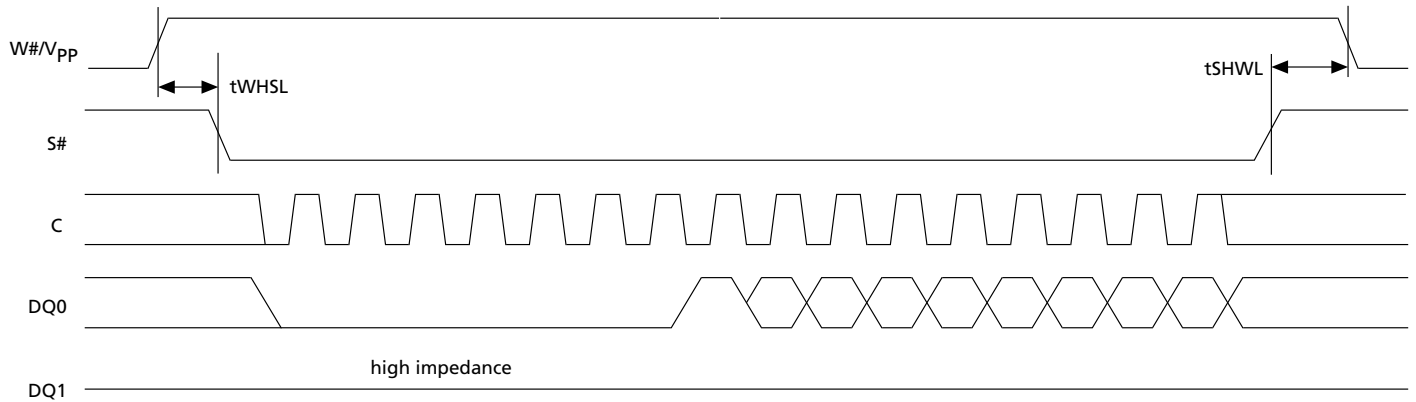


Figure 27: Hold Timing

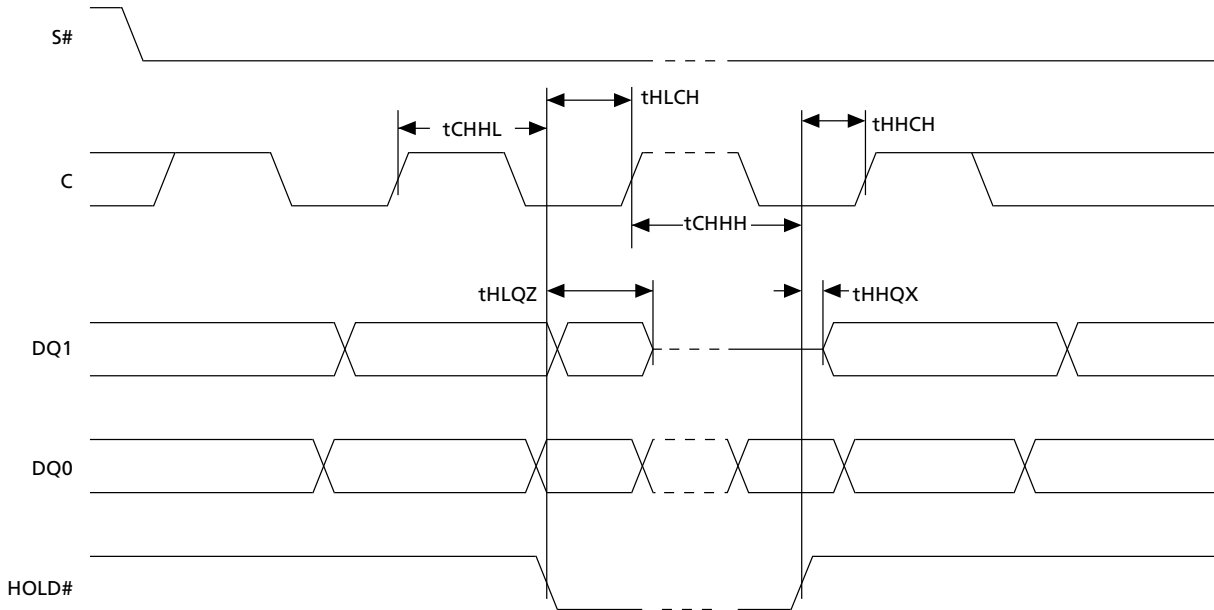
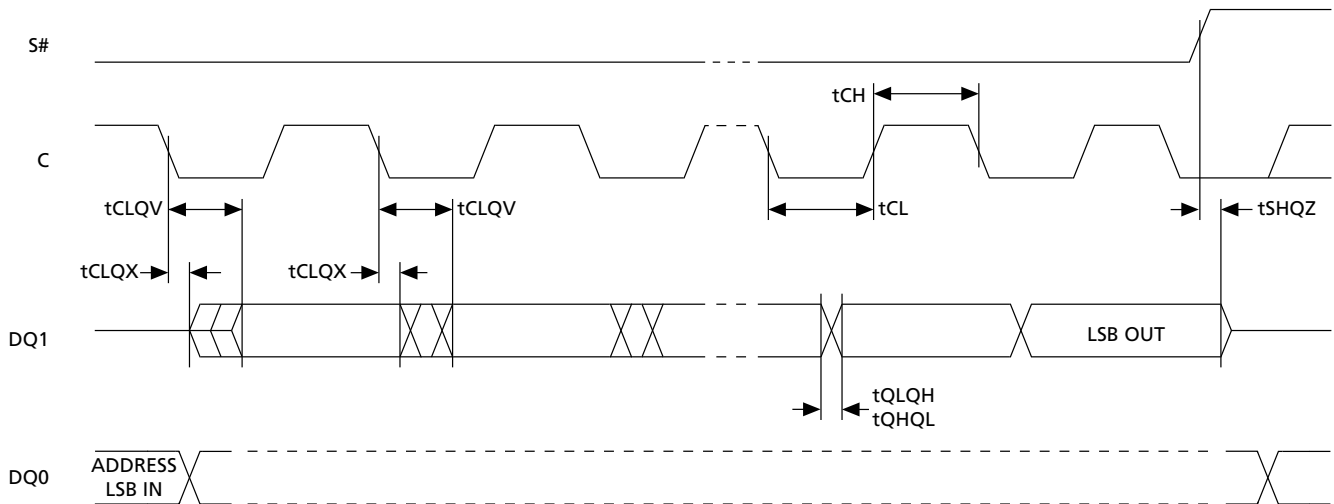
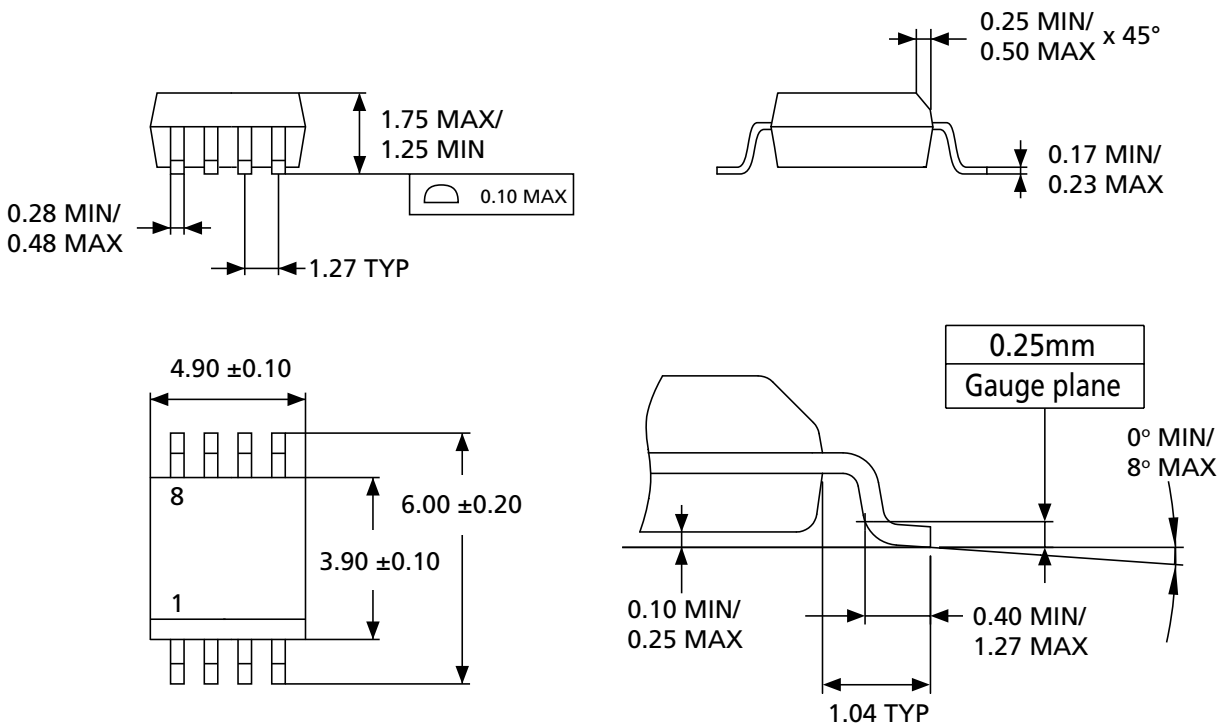


Figure 28: Output Timing



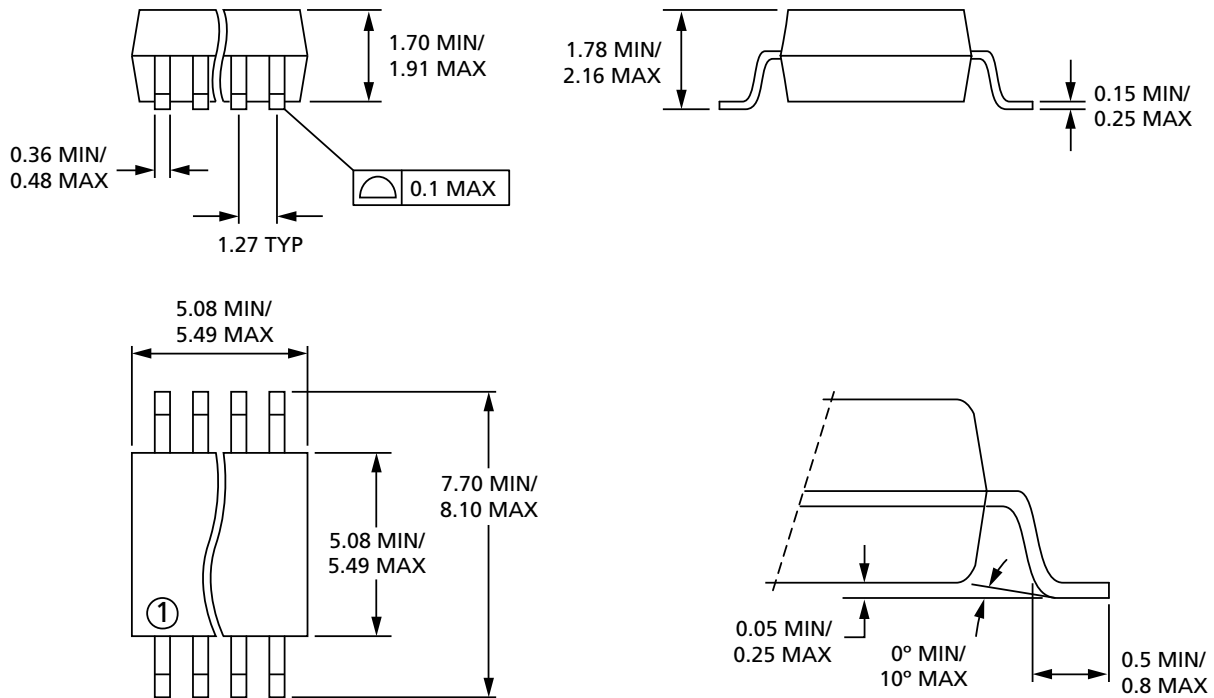
Package Information

Figure 29: SO8N 150 mils Body Width



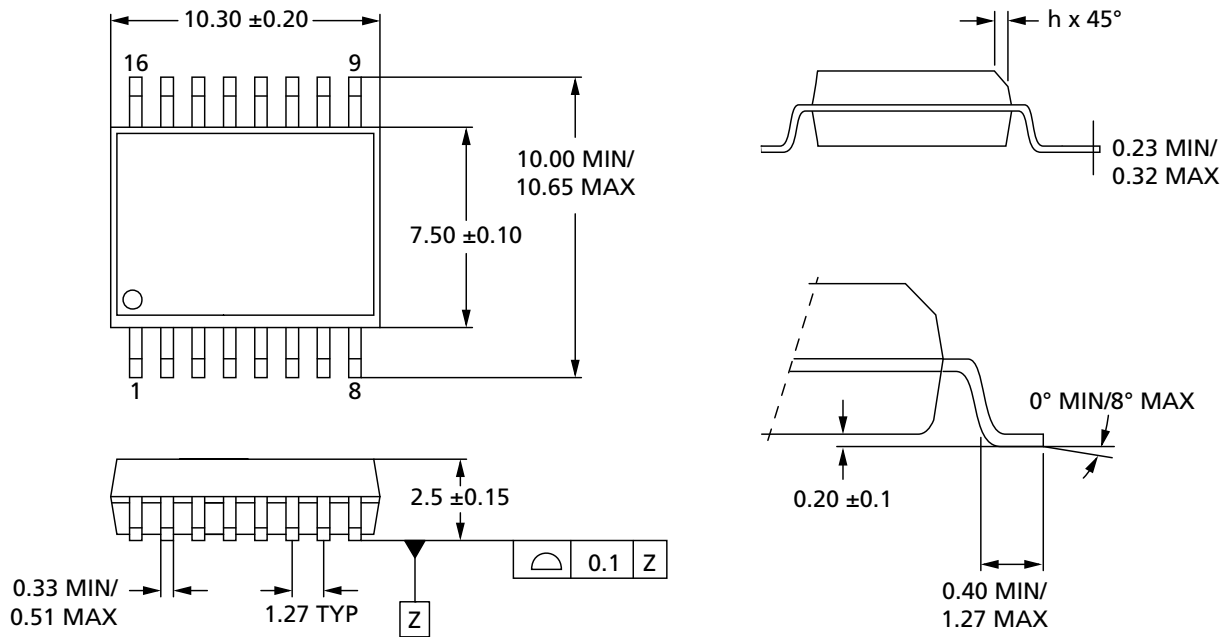
- Notes:
1. The 1 that appears in the top view of the package indicates the position of pin 1.
 2. Drawing is not to scale.

Figure 30: SO8W 208 mils Body Width



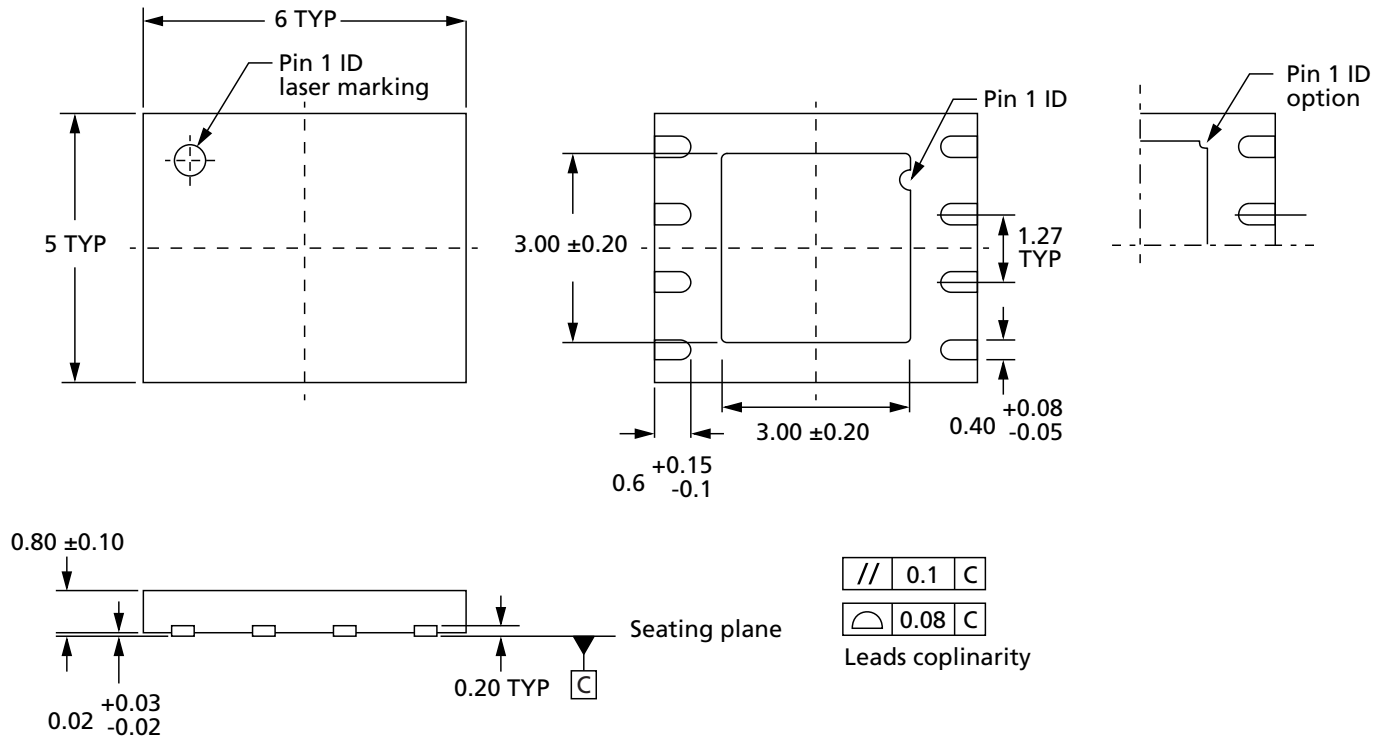
Note: 1. Drawing is not to scale.

Figure 31: SO16W 300 mils Body Width



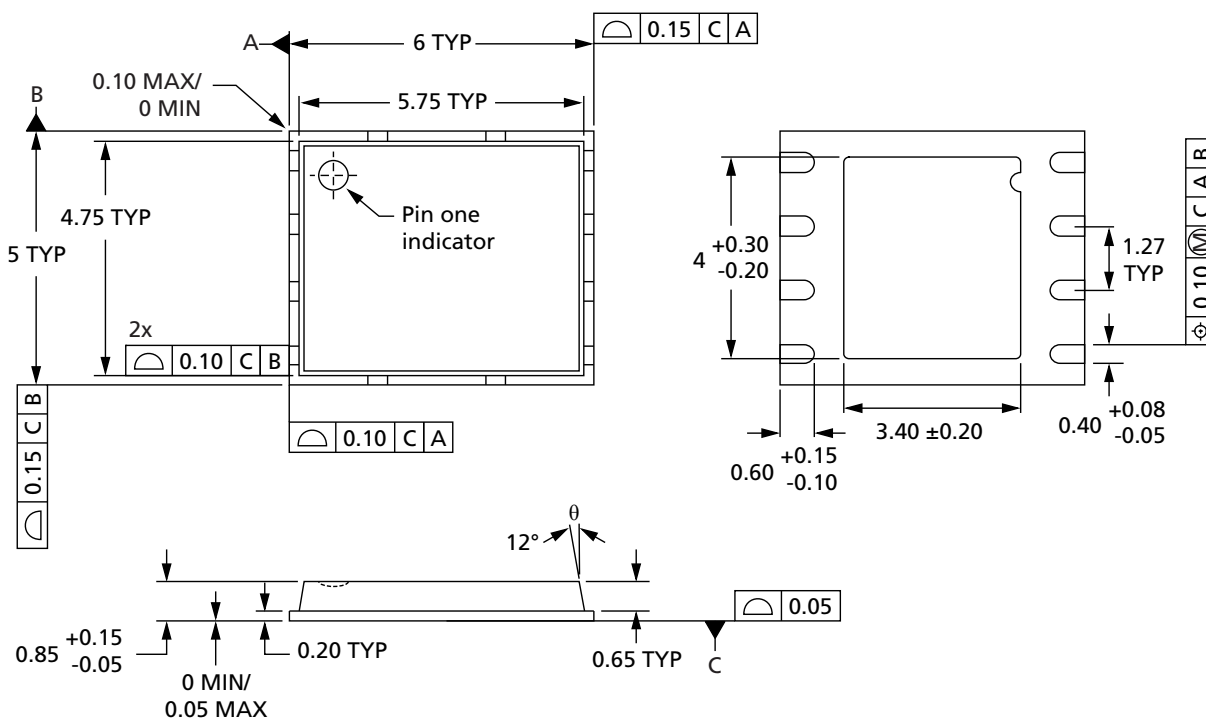
Note: 1. $h = 0.25$ mm MIN, 0.75 mm MAX

Figure 32: DFN8 6mm x 5mm



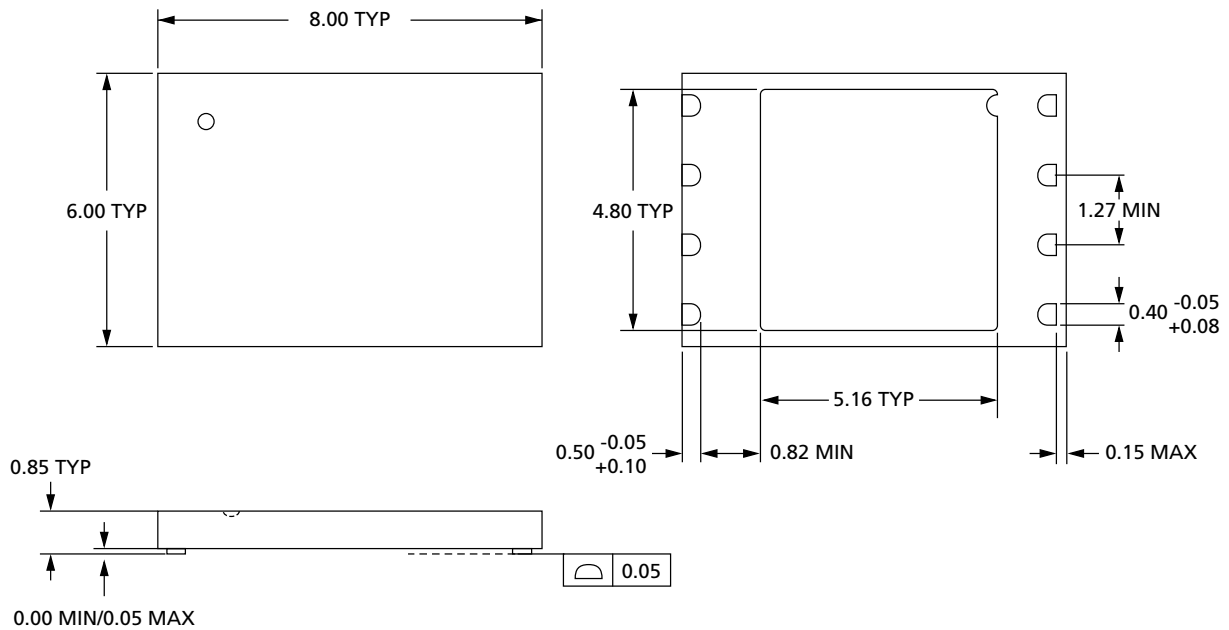
Note: 1. Drawing is not to scale.

Figure 33: VFDFPN8 (MLP8) 6mm x 5mm



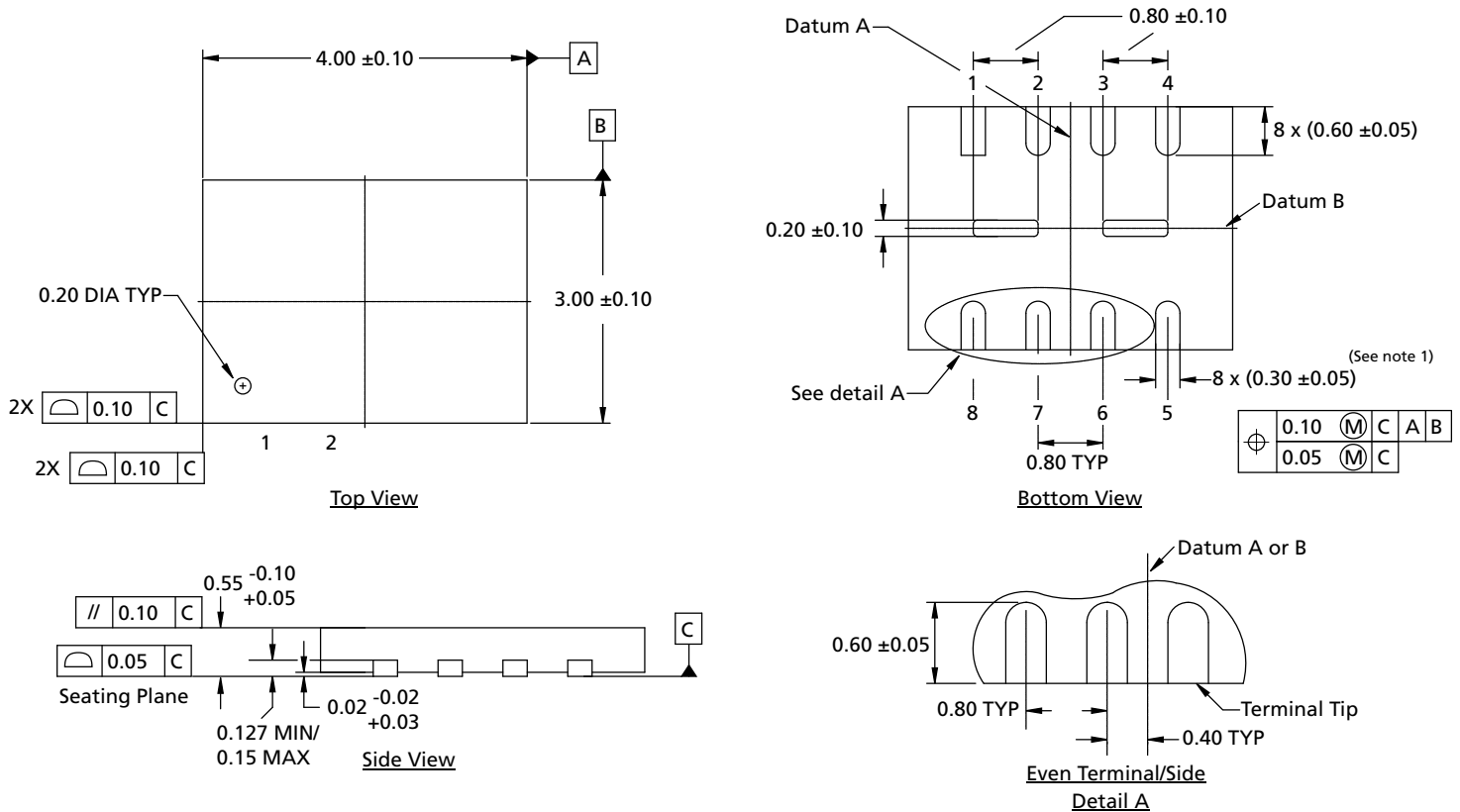
Note: 1. Drawing is not to scale.

Figure 34: VFDFPN8 (MLP8) 8mm x 6mm



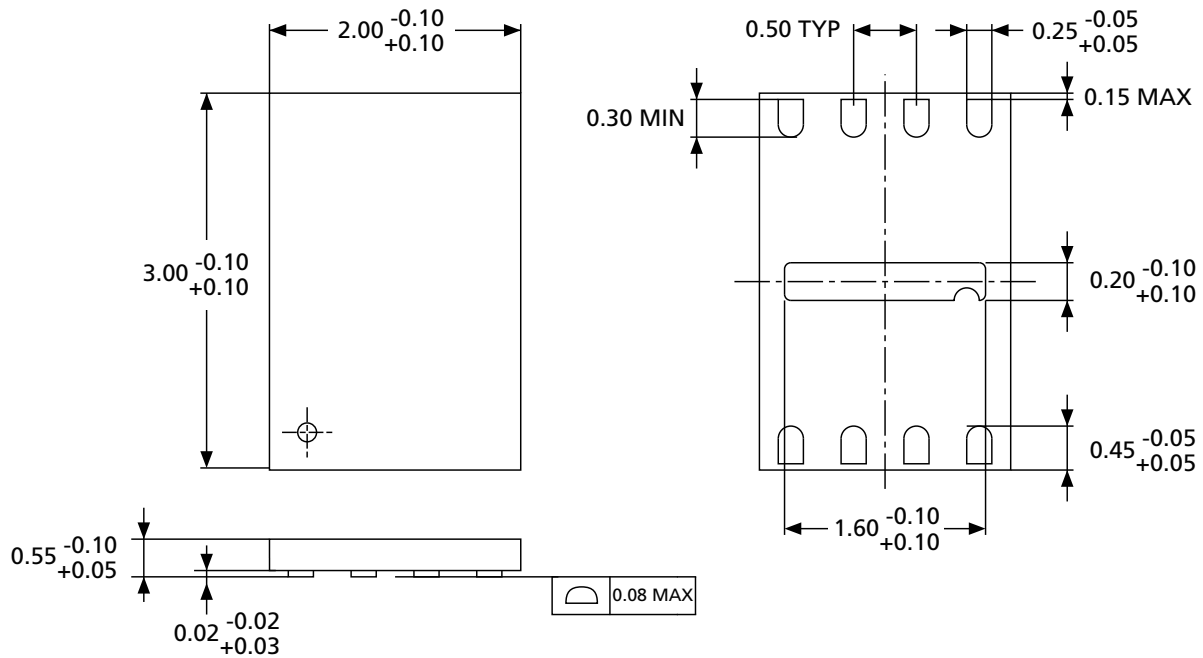
Note: 1. Drawing is not to scale.

Figure 35: UDFFPN8 (MLP8) 4mm x 3mm



- Notes:
1. The dimension 0.30 ± 0.05 applies to the metallic terminal and is measured between 0.15mm and 0.30mm from terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimensions should not be measured in that radius area.
 2. Maximum package warping is 0.05mm; maximum allowable burrs is 0.076mm in all directions; bilateral coplanarity zone applies to the exposed heat sink slug as well as to the terminals.
 3. Drawing is not to scale.

Figure 36: UFDFPN8 (MLP8) 2mm x 3mm



Note: 1. Drawing is not to scale.

Device Ordering Information

Standard Parts

Micron Serial NOR Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at micron.com. To compare features and specifications by device type, visit micron.com/products. Contact the factory for devices not found.

For more information on how to identify products and top-side marking by the process identification letter, refer to technical note TN-12-24, "Serial Flash Memory Device Marking for the M25P, M25PE, M25PX, and N25Q Product Families."

Table 25: Part Number Example

| Part Number Category | | | | | | | | | |
|----------------------|---------|-------------------|-------------------|---------|--------------|----------------|--------------------|-------------|------------------|
| Device Type | Density | Security Features | Operating Voltage | Package | Device Grade | Packing Option | Plating Technology | Lithography | Automotive Grade |
| M25P | 16 | – | V | MN | 6 | T | P | B | A |

Table 26: Part Number Information Scheme

| Part Number Category | Category Details | Notes |
|----------------------|---|--------------------|
| Device type | M25P = Serial Flash memory for code storage | |
| Density | 16 = 16Mb (2 Meg x 8) | |
| Security features | – = no extra security S = CFD programmed with UID | 1 |
| Operating voltage | V = V _{CC} = 2.7V to 3.6V | |
| Package | MN = SO8N (150 mils width) MW = SO8W (208 mils width) MF = SO16W (300 mils width) MP = VFDFPN8 6mm x 5mm (MLP8) ME = VFDFPN8 8mm x 6mm (MLP8) MC = UFDFPN8 4mm x 3mm (MLP8) | 2 3 |
| Device Grade | 6 = Industrial temperature range: –40°C to 85°C. Device tested with standard test flow. 3 = Automotive temperature range: –40°C to 125°C. Device tested with high reliability test flow. | 4, 5 |
| Packing Option | – = Standard packing (tube for SO8N, SO8W, and SO16W packages; tray for MLP packages) T = Tape and reel packing | |
| Plating technology | P or G = RoHS compliant | |
| Lithography | B = 110nm technology, Fab 13 diffusion plant | |

Table 26: Part Number Information Scheme (Continued)

| Part Number Category | Category Details | Notes |
|----------------------|--|-------|
| Automotive Grade | A = Automotive: –40°C to 85°C part. Device tested with high reliability test flow. | |
| | – = Standard: –40°C to 125°C. | |

- Notes:
1. Secure options are available upon customer request.
 2. Package is available only for products in the 110nm process technology.
 3. Not for new designs. Use the MP package for new designs.
 4. Micron recommends the use of the automotive grade device in the automotive environment, autograde 6 and grade 3.
 5. Device grade 3 is available in an SO8 RoHS compliant package.

Note: The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Automotive Parts

Table 27: Part Number Example

| Part Number Category | | | | | | | | | |
|----------------------|---------|-------------------|-------------------|---------|--------------|----------------|--------------------|-------------|------------------|
| Device Type | Density | Security Features | Operating Voltage | Package | Device Grade | Packing Option | Plating Technology | Lithography | Automotive Grade |
| M25P | 16 | – | V | MN | 6 | T | P | B | A |

Table 28: Part Number Information Scheme

| Part Number Category | Category Details | Notes |
|----------------------|--|-------|
| Device type | M25P = Serial Flash memory for code storage | |
| Density | 16 = 8Mb (2 Meg x 8) | |
| Security features | – = no extra security | |
| Operating voltage | V = V _{CC} = 2.7V to 3.6V | |
| Package | MN = SO8N (150 mils width) | |
| | MF = SO16W (300 mils width) | |
| Device Grade | 6 = Industrial temperature range: –40°C to 85°C. Device tested with high reliability test flow. | 1 |
| | 3 = Automotive temperature range: –40°C to 125°C. Device tested with high reliability test flow. | |
| Packing Option | – = Tube | |
| | T = Tape and reel packing | |
| | Y = Tray | |
| Plating technology | P = RoHS compliant | |

Table 28: Part Number Information Scheme (Continued)

| Part Number Category | Category Details | Notes |
|----------------------|---|-------|
| Lithography | B = 110nm technology, Fab 13 diffusion plant | |
| Automotive Grade | A = Automotive: –40°C to 85°C part. Only with temperature grade 6. Device tested with high reliability test flow. | 1 |
| | – = Automotive: –40°C to 125°C. | |

Note: 1. Micron recommends the use of the automotive grade device in the automotive environment, autograde 6 and grade 3.

Revision History

Rev. J – 1/18

- Added Important Notes and Warnings section for further clarification aligning to industry standards

Rev. I – 4/15

- UID programmed for package UFDFPN8 4 x 3
- Updated note 1 in the Read Identification Data Out Sequence table

Rev. H – 1/14

- In standard and automotive ordering information, revised package option and changed Fab 2 to Fab 13

Rev. G – 1/13

- Removed part numbers from page 1
- Updated READ Identification in the Command Set Codes table to include 9Eh information
- Updated SO8W 208 mils Body Width drawing
- Updated Device Ordering Information section

Rev. F – 10/12

- Updated ordering information and package options
- Deleted old, extraneous pre-Micron revision history changes

Rev. E – 8/12

- Updated Command Set to include RELEASE FROM DEEP POWER-DOWN
- Updated Memory Map to eliminate the 64KB block box

Rev. D – 5/12

- In Signal Names table, changed direction column for DQ0 and DQ1 to input and output respectively
- Changed the Write Disable Command Sequenced graphic
- Revised Write Status Register topic
- Revised Power-Up/Down and Supply Line Decoupling topic

Rev. C – 3/12

- Updated address range in Memory Map

Rev. B – 3/12

- Corrected error in SO8N package drawing.
- Updated packing options in the Part Number Information Scheme table in Device Ordering Information



Micron M25P16 Serial Flash Embedded Memory Revision History

Rev. A – 9/2011

- Applied Micron brand

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.