

LTM4650A

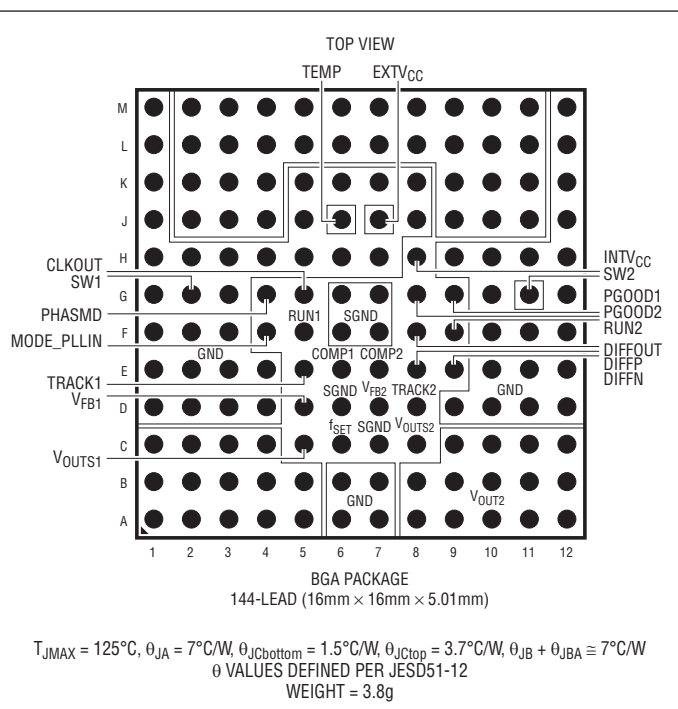
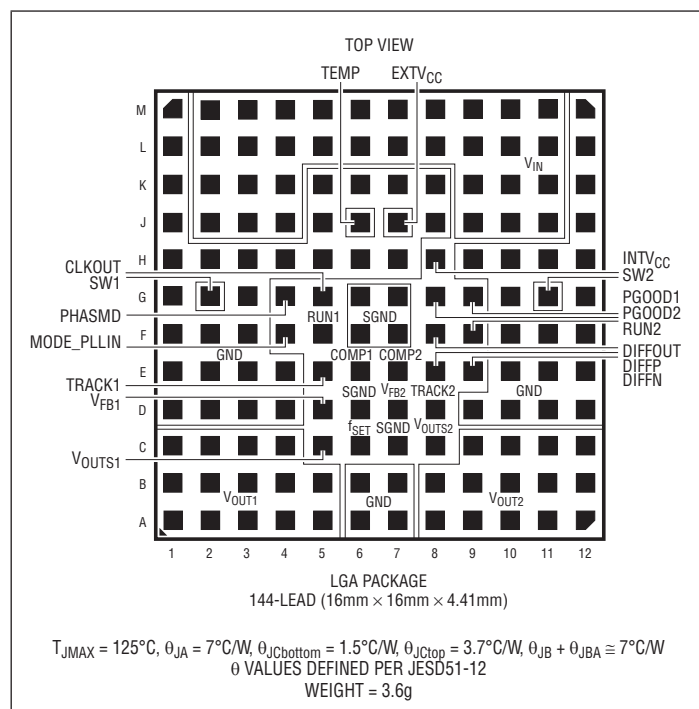
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} (Note 8)	–0.3V to 18V
V_{SW1} , V_{SW2}	–1V to 18V
PGOOD1, PGOOD2, RUN1, RUN2,	
INTV _{CC} , EXTV _{CC}	–0.3V to 6V
MODE_PLLIN, f_{SET} , TRACK1, TRACK2,	
DIFFOUT, PHASMD	–0.3V to INTV _{CC}
V_{OUT1} , V_{OUT2} , V_{OUTS1} , V_{OUTS2} (Note 6)	–0.3V to 6V

PIN CONFIGURATION

DIFFP, DIFFN	–0.3V to INTV _{CC}
COMP1, COMP2, V_{FB1} , V_{FB2} (Note 6)	–0.3V to 2.7V
INTV _{CC} Peak Output Current	50mA
Internal Operating Temperature Range	
(Note 2)	–40°C to 125°C
Storage Temperature Range	–55°C to 125°C
Peak Package Body Temperature	245°C



ORDER INFORMATION

<http://www.linear.com/product/LTM4650A#orderinfo>

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TOTAL DC ACCURACY	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE				
LTM4650AEV#PBF	Au (RoHS)	LTM4650AV	e4	LGA	3	±1%	–40°C to 125°C
LTM4650AIV#PBF	Au (RoHS)	LTM4650AV	e4	LGA	3	±1%	–40°C to 125°C
LTM4650AEY#PBF	SAC305 (RoHS)	LTM4650AY	e1	BGA	3	±1%	–40°C to 125°C
LTM4650AIY#PBF	SAC305 (RoHS)	LTM4650AY	e1	BGA	3	±1%	–40°C to 125°C
LTM4650AIY	SnPb (63/37)	LTM4650AY	e0	BGA	3	±1%	–40°C to 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

• Terminal Finish Part Marking:
www.linear.com/leadfree

• Recommended LGA and BGA PCB Assembly and Manufacturing Procedures:

www.linear.com/umodule/pcbassembly

• LGA and BGA Package and Tray Drawings:
www.linear.com/packaging

4650afb

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel. $T_A = 25^\circ\text{C}$ (Note 2), $V_{IN} = 12\text{V}$ and V_{RUN1} , V_{RUN2} at 5V unless otherwise noted. Per the typical application in Figure 34.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V _{IN}	Input DC Voltage		●	4.5		16	V
V _{OUT}	Output Voltage		●	0.6		5.5	V
V _{OUT1(DC)} , V _{OUT2(DC)}	Output Voltage, Total DC Variation with Line and Load (Note 8)	C _{IN} = 22μF × 3, C _{OUT} = 100μF × 1 Ceramic, 470μF POSCAP V _{IN} = 4.5V to 16V, V _{OUT} = 1.2V, I _{OUT} = 0A to 25A	●	1.188	1.2	1.212	V

Input Specifications

V_{RUN1} , V_{RUN2}	RUN Pin On/Off Threshold	RUN Rising		1.1	1.25	1.40	V
$V_{RUN1HYS}$, $V_{RUN2HYS}$	RUN Pin On Hysteresis				150		mV
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	$I_{OUT} = 0\text{A}$, $C_{IN} = 22\mu\text{F} \times 3$, $C_{SS} = 0.01\mu\text{F}$, $C_{OUT} = 100\mu\text{F} \times 3$, $V_{OUT1} = 1.2\text{V}$, $V_{OUT2} = 1.2\text{V}$, $V_{IN} = 12\text{V}$			1		A
$I_Q(VIN)$	Input Supply Bias Current (Both Channels On)	$V_{IN} = 12\text{V}$, $V_{OUT} = 1.2\text{V}$, Burst Mode Operation $V_{IN} = 12\text{V}$, $V_{OUT} = 1.2\text{V}$, Pulse-Skipping Mode $V_{IN} = 12\text{V}$, $V_{OUT} = 1.2\text{V}$, Switching Continuous Shutdown, RUN = 0, $V_{IN} = 12\text{V}$			4.5 19 115 35		mA mA mA μA
$I_S(VIN)$	Input Supply Current	$V_{IN} = 5\text{V}$, $V_{OUT} = 1.2\text{V}$, $I_{OUT} = 25\text{A}$ $V_{IN} = 12\text{V}$, $V_{OUT} = 1.2\text{V}$, $I_{OUT} = 25\text{A}$			8.2 3.1		A A

Output Specifications

$I_{OUT1(DC)}$, $I_{OUT2(DC)}$	Output Continuous Current Range	$V_{IN} = 12\text{V}$, $V_{OUT} = 1.2\text{V}$ (Note 7)		0		25	A
$\Delta V_{OUT1(LINE)}/V_{OUT1}$ $\Delta V_{OUT2(LINE)}/V_{OUT2}$	Line Regulation Accuracy	For Each Output, $V_{OUT} = 1.2\text{V}$, $I_{OUT} = 0\text{A}$, V_{IN} from 4.5V to 16V	●		0.02	0.1	%/V
$\Delta V_{OUT1}/V_{OUT1}$ $\Delta V_{OUT2}/V_{OUT2}$	Load Regulation Accuracy	For Each Output, $V_{IN} = 12\text{V}$, $V_{OUT} = 1.2\text{V}$, I_{OUT} from 0A to 25A (Note 7)	●		0.1	0.4	%
$V_{OUT1(AC)}$, $V_{OUT2(AC)}$	Output Ripple Voltage	For Each Output, $V_{IN} = 12\text{V}$, $V_{OUT} = 1.2\text{V}$, Frequency = 450kHz, $I_{OUT} = 0\text{A}$, $C_{OUT} =$ 100 $\mu\text{F} \times 3$ Ceramic, 470 μF POSCAP			15		mV _{P-P}
f_S (Each Channel)	Output Ripple Voltage Frequency	$V_{IN} = 12\text{V}$, $V_{OUT} = 1.2\text{V}$, $f_{SET} = 1.25\text{V}$ (Note 4)			500		kHz
f_{SYNC} (Each Channel)	SYNC Capture Range			250		780	kHz
$\Delta V_{OUTSTART}$ (Each Channel)	Turn-On Overshoot	$C_{OUT} = 100\mu\text{F} \times 3$ Ceramic, 470 μF POSCAP, $V_{IN} = 12\text{V}$, $V_{OUT} = 1.2\text{V}$, $I_{OUT} = 0\text{A}$			10		mV
t_{START} (Each Channel)	Turn-On Time	$C_{OUT} = 100\mu\text{F} \times 3$ Ceramic, 470 μF POSCAP, $V_{IN} = 12\text{V}$, No Load, TRACK/SS with 0.01 μF to GND			5		ms
$\Delta V_{OUT(LS)}$ (Each Channel)	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load $C_{OUT} = 100\mu\text{F} \times 3$ Ceramic, 470 μF POSCAP, $V_{IN} = 12\text{V}$, $V_{OUT} = 1.2\text{V}$			30		mV
t_{SETTLE} (Each Channel)	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, $V_{IN} = 12\text{V}$, $C_{OUT} = 100\mu\text{F} \times 3$ Ceramic, 470 μF POSCAP			20		μs
$I_{OUT(PK)}$ (Each Channel)	Output Current Limit	$V_{IN} = 12\text{V}$, $V_{OUT} = 1.2\text{V}$			30		A

Control Section

V_{FB1} , V_{FB2}	Voltage at V_{FB} Pins	$I_{OUT} = 0\text{A}$, $V_{OUT} = 1.2\text{V}$	●	0.595	0.600	0.605	V
I_{FB}		(Note 6)			-5	-20	nA
V_{OVL}	Feedback Overvoltage Lockout		●	0.64	0.66	0.68	V

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel. $T_A = 25^\circ\text{C}$ (Note 2), $V_{IN} = 12\text{V}$ and V_{RUN1} , V_{RUN2} at 5V unless otherwise noted. Per the typical application in Figure 34.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{TRACK1} , I_{TRACK2}	Track Pin Soft-Start Pull-Up Current	TRACK1, TRACK2 Start at 0V	1	1.25	1.5	μA
UVLO	Undervoltage Lockout (Falling)			3.3		V
UVLO Hysteresis				0.6		V
$t_{\text{ON(MIN)}}$	Minimum On-Time	(Note 6)		90		ns
R_{FBH1} , R_{FBH2}	Resistor Between V_{OUTS1} , V_{OUTS2} and V_{FB1} , V_{FB2} Pins for Each Output		60.05	60.4	60.75	$\text{k}\Omega$
V_{PGOOD1} , V_{PGOOD2} Low	PGOOD Voltage Low	$I_{\text{PGOOD}} = 2\text{mA}$		0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	$V_{\text{PGOOD}} = 5\text{V}$			± 5	μA
V_{PGOOD}	PGOOD Trip Level	V_{FB} with Respect to Set Output Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive		-10 10		% %

INTV_{CC} Linear Regulator

V_{INTVCC}	Internal V_{CC} Voltage	$6\text{V} < V_{\text{IN}} < 16\text{V}$	4.8	5	5.2	V
V_{INTVCC} Load Regulation	INTV _{CC} Load Regulation	$I_{\text{CC}} = 0\text{mA}$ to 50mA		0.5	2	%
V_{EXTVCC}	EXTV _{CC} Switchover Voltage	EXTV _{CC} Ramping Positive	4.5	4.7		V
$V_{\text{EXTVCC(DROP)}}$	EXTV _{CC} Dropout	$I_{\text{CC}} = 20\text{mA}$, $V_{\text{EXTVCC}} = 5\text{V}$		50	100	mV
$V_{\text{EXTVCC(HYST)}}$	EXTV _{CC} Hysteresis			220		mV

Oscillator and Phase-Locked Loop

Frequency Nominal	Nominal Frequency	$f_{\text{SET}} = 1.2\text{V}$	450	500	550	kHz
Frequency Low	Lowest Frequency	$f_{\text{SET}} = 0\text{V}$ (Note 5)	210	250	290	kHz
Frequency High	Highest Frequency	$f_{\text{SET}} > 2.4\text{V}$, Up to INTV _{CC}	700	780	860	kHz
f_{SET}	Frequency Set Current		9	10	11	μA
$R_{\text{MODE_PLLIN}}$	MODE_PLLIN Input Resistance			250		$\text{k}\Omega$
CLKOUT	Phase (Relative to V_{OUT1})	PHASMD = GND PHASMD = Float PHASMD = INTV _{CC}		60 90 120		Deg Deg Deg
CLK High CLK Low	Clock High Output Voltage Clock Low Output Voltage		2		0.2	V V

Differential Amplifier

A_V Differential Amplifier	Gain			1		V/V
R_{IN}	Input Resistance	Measured at DIFFP Input		80		$\text{k}\Omega$
V_{OS}	Input Offset Voltage	$V_{\text{DIFFP}} = V_{\text{DIFFOUT}} = 1.2\text{V}$, $I_{\text{DIFFOUT}} = 100\mu\text{A}$			3	mV
PSRR Differential Amplifier	Power Supply Rejection Ratio	$4.5\text{V} < V_{\text{IN}} < 16\text{V}$		90		dB
I_{CL}	Maximum Output Current			3		mA
$V_{\text{OUT(MAX)}}$	Maximum Output Voltage	$I_{\text{DIFFOUT}} = 300\mu\text{A}$	INTV _{CC} - 1.4			V
GBW	Gain Bandwidth Product			3		MHz
V_{TEMP}	Diode Connected PNP	$I = 100\mu\text{A}$		0.6		V
TC	Temperature Coefficient	●		-2.2		mV/C

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4650A is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4650AE is guaranteed to meet specifications from 0°C to 125°C internal temperature. Specifications over the -40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4650AI is guaranteed over the full -40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: Two outputs are tested separately and the same testing condition is applied to each output.

Note 4: The switching frequency is programmable from 250kHz to 780kHz.

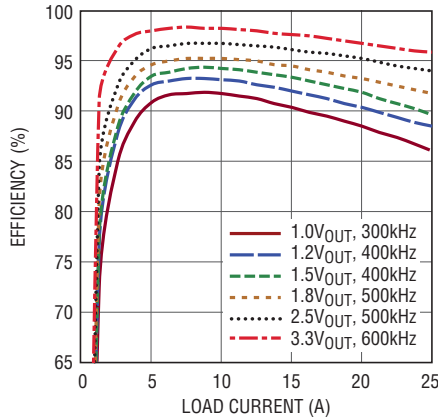
Note 5: LTM4650A device is designed to operate from 250kHz to 780kHz

Note 6: These parameters are tested at wafer sort.

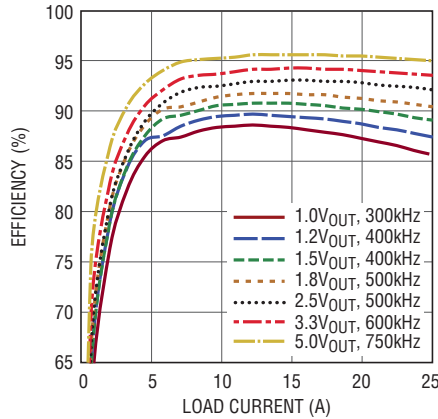
Note 7: See output current derating curve for different ambient temperature.

Note 8: Total DC output voltage error includes all errors over temperature – reference, line and load regulation as well as the tolerance of the integrated top feedback resistor.

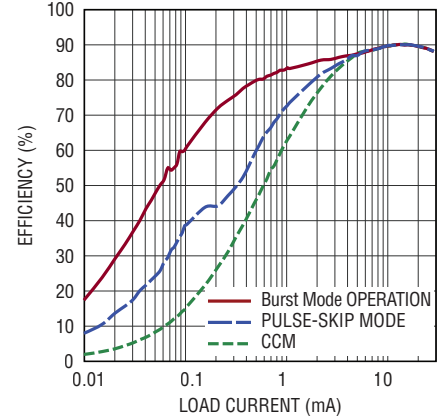
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Output Current,
 $V_{IN} = 5V$ 

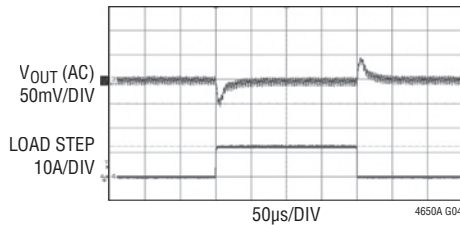
4650A G01

Efficiency vs Output Current,
 $V_{IN} = 12V$ 

4650A G02

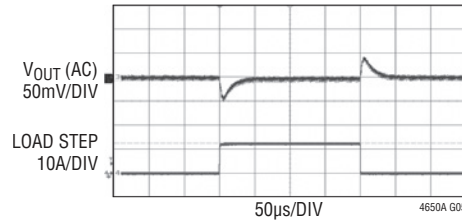
Burst Mode and Pulse-Skip Mode
Efficiency $V_{IN}=12V$, $V_{OUT} = 1.2V$,
 $f_s = 300kHz$ 

4650A G03

1V Dual Phase Single Output
Load Transient Response
(Ceramic Cap)

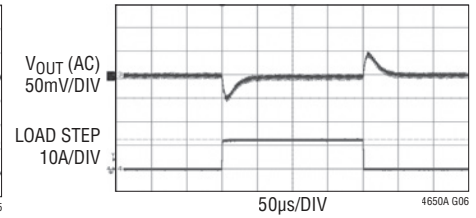
4650A G04

12VIN, 1VOUT, 300kHz,
DUAL PHASE SINGLE OUTPUT
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/μs SLEW RATE
COUT = 16× 100μF CERAMIC CAP
CFF = 47pF

1.2V Dual Phase Single Output
Load Transient Response
(Ceramic Cap)

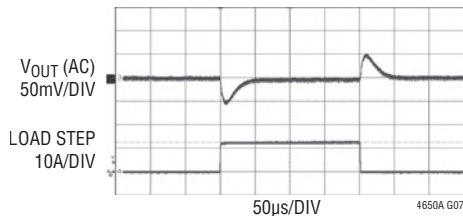
4650A G05

12VIN, 1.2VOUT, 400kHz,
DUAL PHASE SINGLE OUTPUT
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/μs SLEW RATE
COUT = 16× 100μF CERAMIC CAP
CFF = 47pF

1.5V Dual Phase Single Output
Load Transient Response
(Ceramic Cap)

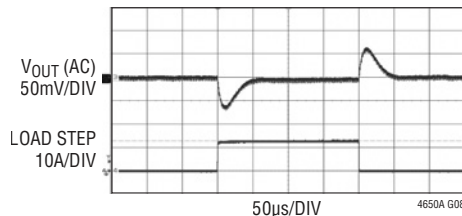
4650A G06

12VIN, 1.5VOUT, 400kHz,
DUAL PHASE SINGLE OUTPUT
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/μs SLEW RATE
COUT = 16× 100μF CERAMIC CAP
CFF = 47pF

1.8V Dual Phase Single Output
Load Transient Response
(Ceramic Cap)

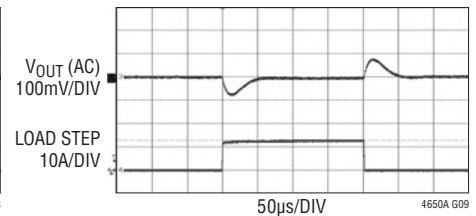
4650A G07

12VIN, 1.8VOUT, 500kHz,
DUAL PHASE SINGLE OUTPUT
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/μs SLEW RATE
COUT = 16× 100μF CERAMIC CAP
CFF = 47pF

2.5V Dual Phase Single Output
Load Transient Response
(Ceramic Cap)

4650A G08

12VIN, 2.5VOUT, 500kHz,
DUAL PHASE SINGLE OUTPUT
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/μs SLEW RATE
COUT = 16× 100μF CERAMIC CAP
CFF = 47pF

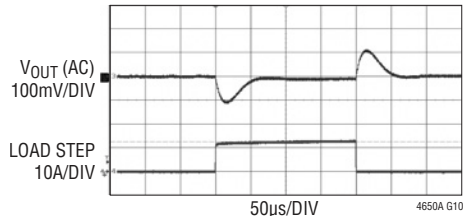
3.3V Dual Phase Single Output
Load Transient Response
(Ceramic Cap)

4650A G09

12VIN, 3.3VOUT, 600kHz,
DUAL PHASE SINGLE OUTPUT
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/μs SLEW RATE
COUT = 16× 100μF CERAMIC CAP
CFF = 47pF

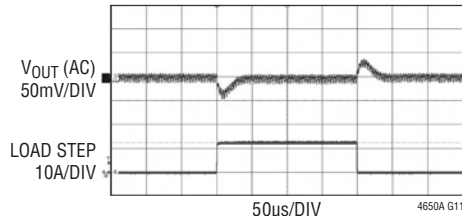
TYPICAL PERFORMANCE CHARACTERISTICS

**5V Dual Phase Single Output
Load Transient Response
(Ceramic Cap)**



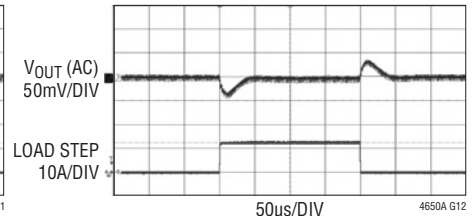
12VIN, 5VOUT, 750kHz,
DUAL PHASE SINGLE OUTPUT
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
COUT = 16 × 100µF CERAMIC CAP
CFF = 47pF

**1V Dual Phase Single Output
Load Transient Response
(POSCAP)**



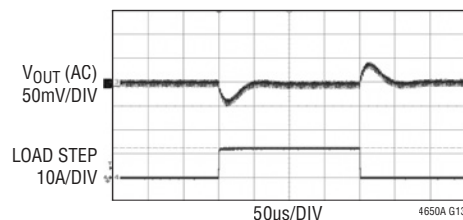
12VIN, 1VOUT, 300kHz,
DUAL PHASE SINGLE OUTPUT
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
COUT = 4 × 470µF POSCAP + 8 × 100µF CERAMIC
NO CFF

**1.2V Dual Phase Single Output
Load Transient Response
(POSCAP)**



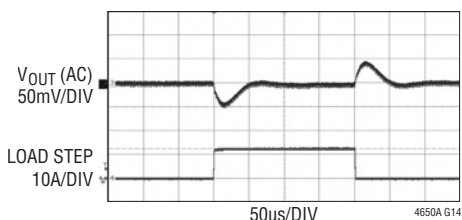
12VIN, 1.2VOUT, 400kHz,
DUAL PHASE SINGLE OUTPUT
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
COUT = 4 × 470µF POSCAP + 8 × 100µF CERAMIC
NO CFF

**1.5V Dual Phase Single Output
Load Transient Response
(POSCAP)**



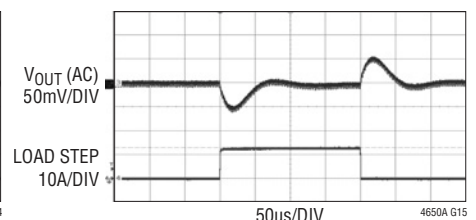
12VIN, 1.5VOUT, 400kHz,
DUAL PHASE SINGLE OUTPUT
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
COUT = 4 × 470µF POSCAP + 8 × 100µF CERAMIC
NO CFF

**1.8V Dual Phase Single Output
Load Transient Response
(POSCAP)**



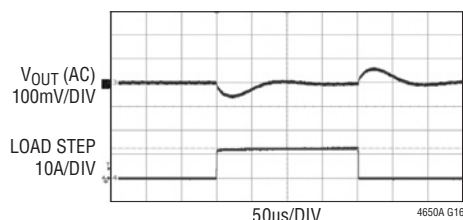
12VIN, 1.8VOUT, 500kHz,
DUAL PHASE SINGLE OUTPUT
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
COUT = 4 × 470µF POSCAP + 8 × 100µF CERAMIC
NO CFF

**2.5V Dual Phase Single Output
Load Transient Response
(POSCAP)**



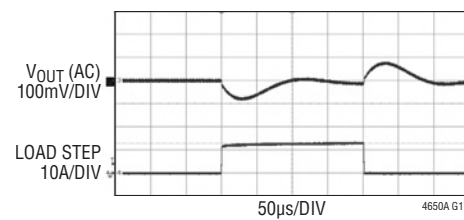
12VIN, 2.5VOUT, 500kHz,
DUAL PHASE SINGLE OUTPUT
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
COUT = 4 × 470µF POSCAP + 8 × 100µF CERAMIC
NO CFF

**3.3V Dual Phase Single Output
Load Transient Response
(POSCAP)**



12VIN, 3.3VOUT, 600kHz,
DUAL PHASE SINGLE OUTPUT
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
COUT = 4 × 470µF POSCAP + 8 × 100µF CERAMIC
NO CFF

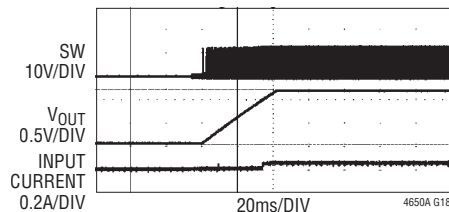
**5V Dual Phase Single Output
Load Transient Response
(POSCAP)**



12VIN, 5VOUT, 750kHz,
DUAL PHASE SINGLE OUTPUT
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
COUT = 4 × 470µF POSCAP + 8 × 100µF CERAMIC
NO CFF

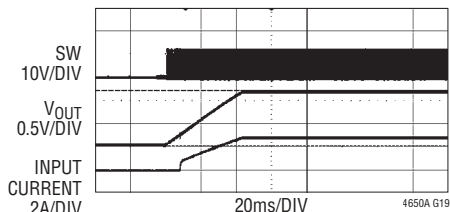
TYPICAL PERFORMANCE CHARACTERISTICS

Single Phase Start-Up with No load



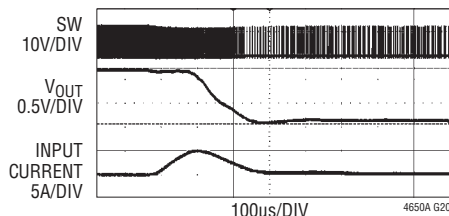
12VIN, 1.2VOUT, 400kHz
COUT = 2× 470µF
SPCAP + 4× 100µF CERAMIC CAP
CSS = 0.1µF

Single Phase Start-Up with 25A Load



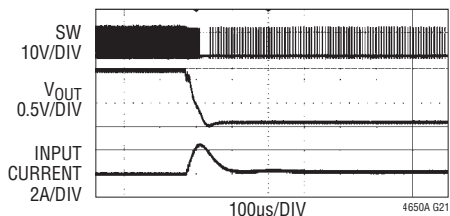
12VIN, 1.2VOUT, 400kHz
COUT = 2× 470µF
SPCAP + 4× 100µF CERAMIC CAP
CSS = 0.1µF

Single Phase Short-Circuit Protection with No load



12VIN, 1.2VOUT, 400kHz
COUT = 2× 470µF
SPCAP + 4× 100µF CERAMIC CAP

Single Phase Short-Circuit Protection with 25A Load



12VIN, 1.2VOUT, 400kHz
COUT = 2× 470µF
SPCAP + 4× 100µF CERAMIC CAP

PIN FUNCTIONS (Recommended to Use Test Points to Monitor Signal Pin Connections.)



PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG μ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{OUT1} (A1–A5, B1–B5, C1–C4): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 6.

GND (A6–A7, B6–B7, D1–D4, D9–D12, E1–E4, E10–E12, F1–F3, F10–F12, G1, G3, G10, G12, H1–H7, H9–H12, J1, J5, J8, J12, K1, K5–K8, K12, L1, L12, M1, M12): Power Ground Pins for Both Input and Output Returns.

V_{OUT2} (A8–A12, B8–B12, C9–C12): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 6.

V_{OUTS1}, V_{OUTS2} (C5, C8): This pin is connected to the top of the internal top feedback resistor for each output. The pin can be directly connected to its specific output, or connected to DIFFOUT when the remote sense amplifier is used. In paralleling modules, one of the V_{OUTS} pins is connected to the DIFFOUT pin in remote sensing or directly to V_{OUT} with no remote sensing. It is very important to connect these pins to either the DIFFOUT or V_{OUT} since this is the feedback path, and cannot be left open. See the Applications Information section.

f_{SET} (C6): Frequency Set Pin. A 10 μ A current is sourced from this pin. A resistor from this pin to ground sets a voltage that in turn programs the operating frequency. Alternatively, this pin can be driven with a DC voltage that can set the operating frequency. See the Applications Information section.

SGND (C7, D6, G6–G7, F6–F7): Signal Ground Pin. Return ground path for all analog and low power circuitry. Tie a single connection to the output capacitor GND in the application. See layout guidelines in Figure 14.

V_{FB1}, V_{FB2} (D5, D7): The Negative Input of the Error Amplifier for Each Channel. Internally, this pin is connected to V_{OUTS1} or V_{OUTS2} with a 60.4k Ω precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and GND pins. In PolyPhase[®] operation, tying the V_{FB} pins together allows for parallel operation. See the Applications Information section for details. Do not drive this pin.

TRACK1, TRACK2 (E5, D8): Output Voltage Tracking Pin and Soft-Start Inputs. Each channel has a 1.3 μ A pull-up current source. When one channel is configured to be master of the two channels, then a capacitor from this pin to ground will set a soft-start ramp rate. The remaining channel can be set up as the slave, and have the master's output applied through a voltage divider to the slave output's track pin. This voltage divider is equal to the slave output's feedback divider for coincidental tracking. See the Applications Information section.

COMP1, COMP2 (E6, E7): Current control threshold and error amplifier compensation point for each channel. The current comparator threshold increases with this control voltage. This device is internal compensated. See Applications Information section. Tie the COMP pins together for parallel operation. Do not drive this pin.

DIFFP (E8): Positive input of the remote sense amplifier. This pin is connected to the remote sense point of the output voltage. Diffamp can be used for ≤ 3.3 V outputs. See the Applications Information section.

DIFFN (E9): Negative input of the remote sense amplifier. This pin is connected to the remote sense point of the output GND. Diffamp can be used for ≤ 3.3 V outputs. See the Applications Information section.

MODE_PLLIN (F4): Force Continuous Mode, Burst Mode Operation, or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to SGND to force both channels into force continuous mode of operation. Connect to INTV_{CC} to enable pulse-skipping mode of operation. Leaving the pin floating will enable Burst Mode operation. A clock on the pin will force both channels into continuous mode of operation and synchronized to the external clock applied to this pin.

RUN1, RUN2 (F5, F9): Run Control Pin. A voltage above 1.25V will turn on each channel in the module. A voltage below 1.25V on the RUN pin will turn off the related channel. Each RUN pin has a 1 μ A pull-up current, once the RUN pin reaches 1.2V an additional 4.5 μ A pull-up current is added to this pin.

PIN FUNCTIONS (Recommended to Use Test Points to Monitor Signal Pin Connections.)

DIFFOUT (F8): Internal Remote Sense Amplifier Output. Connect this pin to V_{OUTS1} or V_{OUTS2} depending on which output is using remote sense. In parallel operation connect one of the V_{OUTS} pin to DIFFOUT for remote sensing.

SW1, SW2 (G2, G11): Switching node of each channel that is used for testing purposes. Also an R-C snubber network can be applied to reduce or eliminate switch node ringing, or otherwise leave floating. See the Applications Information section.

PHASMD (G4): Connect this pin to SGND, $INTV_{CC}$, or floating this pin to select the phase of CLKOUT to 60 degrees, 120 degrees, and 90 degrees respectively.

CLKOUT (G5): Clock output with phase control using the PHASMD pin to enable multiphase operation between devices. See the Applications Information section.

PGOOD1, PGOOD2 (G9, G8): Output Voltage Power Good Indicator. Open drain logic output that is pulled to ground when the output voltage is not within $\pm 10\%$ of the regulation point.

$INTV_{CC}$ (H8): Internal 5V Regulator Output. The control circuits and internal gate drivers are powered from this voltage. Decouple this pin to PGND with a $4.7\mu F$ low ESR tantalum or ceramic. $INTV_{CC}$ is activated when either RUN1 or RUN2 is activated.

TEMP (J6): Temperature Monitor. An internal diode connected NPN transistor connected between TEMP and SGND pins. See the Applications Information section.

$EXTV_{CC}$ (J7): External power input that is enabled through a switch to $INTV_{CC}$ whenever $EXTV_{CC}$ is greater than 4.7V. Do not exceed 6V on this input, and connect this pin to V_{IN} when operating V_{IN} on 5V. An efficiency increase will occur that is a function of the $(V_{IN} - INTV_{CC})$ multiplied by power MOSFET driver current. Typical current requirement is 30mA. V_{IN} must be applied before $EXTV_{CC}$, and $EXTV_{CC}$ must be removed before V_{IN} .

V_{IN} (M2–M11, L2–L11, J2–J4, J9–J11, K2–K4, K9–K11): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

Heat Sink (Top Exposed Metal): The top exposed metal is electrically unconnected.

SIMPLIFIED BLOCK DIAGRAM

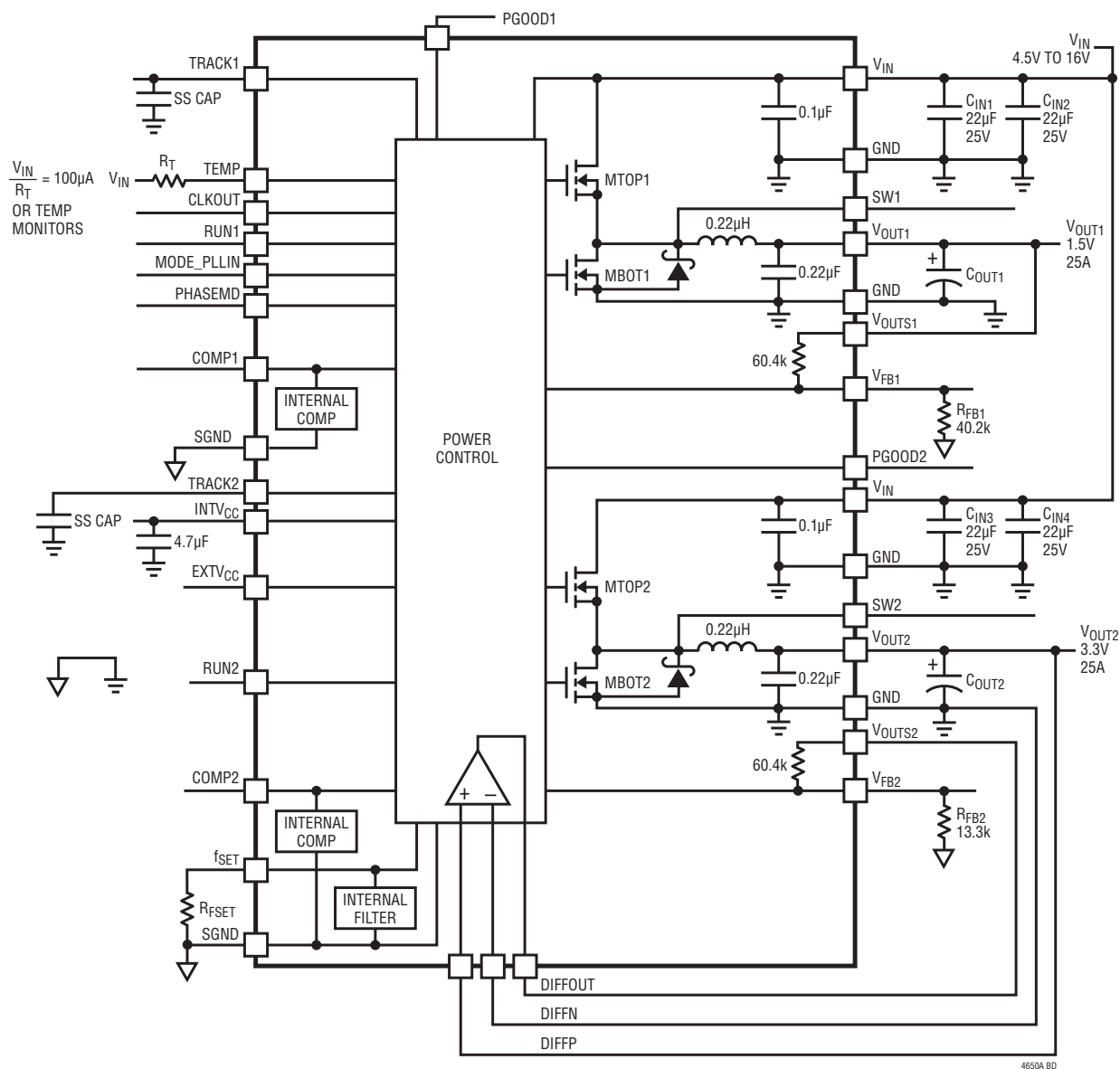


Figure 1. Simplified LTM4650A Block Diagram

DECOUPLING REQUIREMENTS $T_A = 25^\circ\text{C}$. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN1}, C_{IN2} C_{IN3}, C_{IN4}	External Input Capacitor Requirement ($V_{IN1} = 4.5\text{V to } 16\text{V}$, $V_{OUT1} = 1.2\text{V}$) ($V_{IN2} = 4.5\text{V to } 16\text{V}$, $V_{OUT2} = 3.3\text{V}$)	$I_{OUT1} = 25\text{A}$ $I_{OUT2} = 25\text{A}$	22	66		μF
C_{OUT1} C_{OUT2}	External Output Capacitor Requirement ($V_{IN1} = 4.5\text{V to } 16\text{V}$, $V_{OUT1} = 1.2\text{V}$) ($V_{IN2} = 4.5\text{V to } 16\text{V}$, $V_{OUT2} = 3.3\text{V}$)	$I_{OUT1} = 25\text{A}$ $I_{OUT2} = 25\text{A}$	300	600		μF

OPERATION

Power Module Description

The LTM4650A is a dual-output standalone nonisolated switching mode DC/DC power supply with $\pm 1\%$ total DC output error over line, load and temperature variation. It can provide two 25A outputs or single 50A output with few external input and output capacitors and setup components. This module provides precisely regulated output voltages programmable via external resistors from $0.6V_{DC}$ to $5.5V_{DC}$ over 4.5V to 16V input voltages. The typical application schematic is shown in Figure 32.

The LTM4650A has dual integrated constant-frequency current mode regulators and built-in power MOSFET devices with fast switching speed. The typical switching frequency is 300kHz to 750kHz depending on different input and output conditions. For switching-noise sensitive applications, it can be externally synchronized from 250kHz to 780kHz. A resistor can be used to program a free run frequency on the f_{SET} pin. See the Applications Information section.

With current mode control, multi LTM4650As can be easily paralleled to provide up to 300A current with guaranteed perfect current sharing. Also, with current mode control, the LTM4650A module is able to achieve sufficient stability margins and a fast transient response with a minimum number of output capacitors, even with all ceramic output capacitors. See Applications Information section.

Current mode control provides cycle-by-cycle fast current limit and foldback current limit in an overcurrent condition. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD outputs low if the output feedback voltage exits a $\pm 10\%$ window around the regulation point. As the output voltage exceeds 10% above regulation, the bottom MOSFET will turn on to clamp the output voltage. The top MOSFET will be turned off. This overvoltage protect is feedback voltage referred.

Pulling the RUN pins below 1.1V forces the regulators into a shutdown state, by turning off both MOSFETs. The TRACK pins are used for programming the output voltage ramp and voltage tracking during start-up or used for soft-starting the regulator. See the Applications Information section.

The LTM4650A is internally compensated to be stable over all operating conditions. Table 6 provides a guideline for input and output capacitances for several operating conditions. The LTpowerCAD™ will be provided for transient and stability analysis. The V_{FB} pin is used to program the output voltage with a single external resistor to ground. A differential remote sense amplifier is available for sensing the output voltage accurately on one of the outputs at the load point, or in parallel operation sensing the output voltage at the load point.

High efficiency at light loads can be accomplished with selectable Burst Mode operation or pulse-skipping operation using the MODE_PLLIN pin. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section. See the Applications Information section for details.

A general purpose temperature diode is included inside the module to monitor the temperature of the module. See the Applications Information section for details.

The switch pins are available for functional operation monitoring and a resistor-capacitor snubber circuit can be carefully placed on the switch pin to ground to dampen any high frequency ringing on the transition edges. See the Applications Information section for details.

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The typical LTM4650A application circuit is shown in Figure 32. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 6 for specific external capacitor requirements for particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio that can be achieved for a given input voltage. Each output of the LTM4650A is capable of 98% duty cycle, but the V_{IN} to V_{OUT} minimum dropout is still shown as a function of its load current and will limit output current capability related to high duty cycle on the top side switch. Minimum on-time $t_{ON(MIN)}$ is another consideration in operating at a specified duty cycle while operating at a certain frequency due to the fact that $t_{ON(MIN)} < D/f_{SW}$, where D is duty cycle and f_{SW} is the switching frequency. $t_{ON(MIN)}$ is specified in the electrical parameters as 90ns.

Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4kΩ internal feedback resistor connects between the V_{OUTS1} to V_{FB1} and V_{OUTS2} to V_{FB2} . It is very important that these pins be connected to their respective outputs for proper feedback regulation. Overvoltage can occur if these V_{OUTS1} and V_{OUTS2} pins are left floating when used as individual regulators, or at least one of them is used in paralleled regulators. The output voltage will default to 0.6V with no feedback resistor on either V_{FB1} or V_{FB2} . Adding a resistor R_{FB} from V_{FB} pin to GND programs the output voltage:

$$V_{OUT} = 0.6V \cdot \frac{60.4k + R_{FB}}{R_{FB}}$$

Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT}	0.6V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5V
R_{FB}	Open	90.9k	60.4k	40.2k	30.2k	19.1k	13.3k	8.25k

For parallel operation of multiple channels the same feedback setting resistor can be used for the parallel design. This is done by connecting the V_{OUTS1} to the output as shown in Figure 2, thus tying one of the internal 60.4k

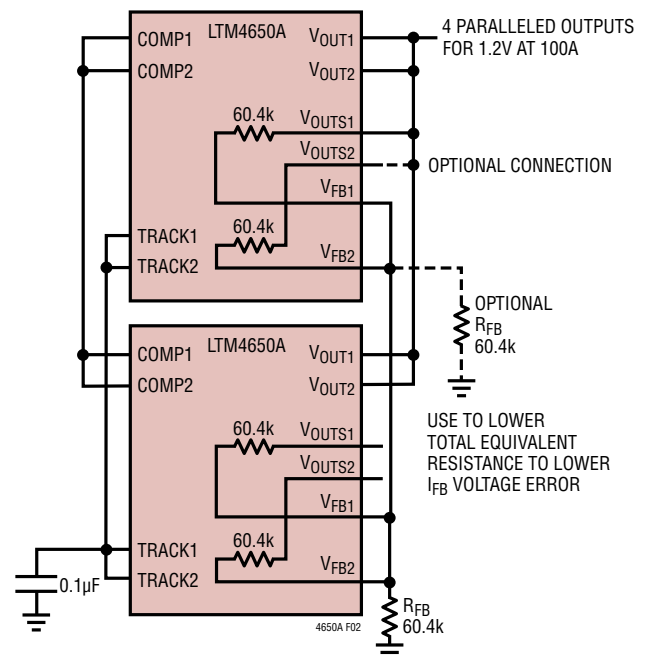


Figure 2. 4-Phase Parallel Configurations

resistors to the output. All of the V_{FB} pins tie together with one programming resistor as shown in Figure 2.

In parallel operation, the V_{FB} pins have an I_{FB} current of 20nA maximum each channel. To reduce output voltage error due to this current, an additional V_{OUTS} pin can be tied to V_{OUT} , and an additional R_{FB} resistor can be used to lower the total Thevenin equivalent resistance seen by this current. For example in Figure 2, the total Thevenin equivalent resistance of the V_{FB} pin is $(60.4k // R_{FB})$, which is 30.2k where R_{FB} is equal to 60.4k for a 1.2V output. Four phases connected in parallel equates to a worst case feedback current of $4 \cdot I_{FB} = 80nA$ maximum. The voltage error is $80nA \cdot 30.2k = 2.4mV$. If V_{OUTS2} is connected, as shown in Figure 2, to V_{OUT} , and another 60.4k resistor is connected from V_{FB2} to ground, then the voltage error is reduced to 1.2mV. If the voltage error is acceptable then no additional connections are necessary. The onboard 60.4k resistor is 0.5% accurate and the V_{FB} resistor can be chosen by the user to be as accurate as needed. All COMP pins are tied together for current sharing between the phases. The TRACK/SS pins can be tied together and a single soft-start capacitor can be used to soft-start the regulator. The soft-start equation will need to have the soft-start current parameter increased by the number of paralleled channels. See Output Voltage Tracking section.

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Input Capacitors

The LTM4650A module should be connected to a low AC-impedance DC source. For the regulator input, two 22μF input ceramic capacitors per channel are used for RMS ripple current. A 47μF to 100μF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty-cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \cdot \sqrt{D \cdot (1 - D)}$$

In the above equation, $\eta\%$ is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor, Polymer capacitor.

Output Capacitors

The LTM4650A is designed for low output voltage ripple noise and good transient response. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, the low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range for each output is from 300μF to 800μF per output channel. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 6 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 25% load step. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 6 matrix,

and the Analog Devices LTpowerCAD Design Tool will be provided for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. The Analog Devices μModule Power Design Tool can calculate the output ripple reduction as the number of implemented phases increases by N times. A small value 10Ω to 50Ω resistor can be placed in series from V_{OUT} to the V_{OUTS} pin to allow for a bode plot analyzer to inject a signal into the control loop and validate the regulator stability. The same resistor could be placed in series from V_{OUT} to $DIFFP$ and a bode plot analyzer could inject a signal into the control loop and validate the regulator stability.

Burst Mode Operation

The LTM4650A is capable of Burst Mode operation on each regulator in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. Burst Mode operation is enabled with the $MODE_PLLIN$ pin floating. During this operation, the peak current of the inductor is set to approximately one third of the maximum peak current value in normal operation even though the voltage at the $COMP$ pin indicates a lower value. The voltage at the $COMP$ pin drops when the inductor's average current is greater than the load requirement. As the $COMP$ voltage drops below 0.5V, the BURST comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off. The load current is now being supplied from the output capacitors. When the output voltage drops, causing $COMP$ to rise above 0.5V, the internal sleep line goes low, and the LTM4650A resumes normal operation. The next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats.

Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping

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mode should be used. Pulse-skipping operation allows the LTM4650A to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Tying the MODE_PLLIN pin to INTV_{CC} enables pulse-skipping operation. At light loads the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode. This mode will maintain higher effective frequencies thus lower output ripple and lower noise than Burst Mode operation.

Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE_PLLIN pin to GND. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4650A's output

voltage is in regulation. Either regulator can be configured for force continuous mode.

Multiphase Operation

For output loads that demand more than 25A of current, two outputs in LTM4650A or even multiple LTM4650As can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripples. The MODE_PLLIN pin allows the LTM4650A to synchronize to an external clock (between 250kHz and 780kHz) and the internal phase-locked-loop allows the LTM4650A to lock onto incoming clock phase as well. The CLKOUT signal can be connected to the MODE_PLLIN pin of the following stage to line up both the frequency and the phase of the entire system. Tying the PHASMD pin to INTV_{CC}, SGND, or (floating) generates a phase difference (between MODE_PLLIN and CLKOUT) of 120 degrees, 60 degrees, or 90 degrees respectively. A total of 12 phases can be cascaded to run simultaneously with respect to each other by programming the PHASMD pin of each LTM4650A channel to different levels. Figure 3 shows a 2-phase design, 4-phase design and a 6-phase design example for clock phasing with the PHASMD table.

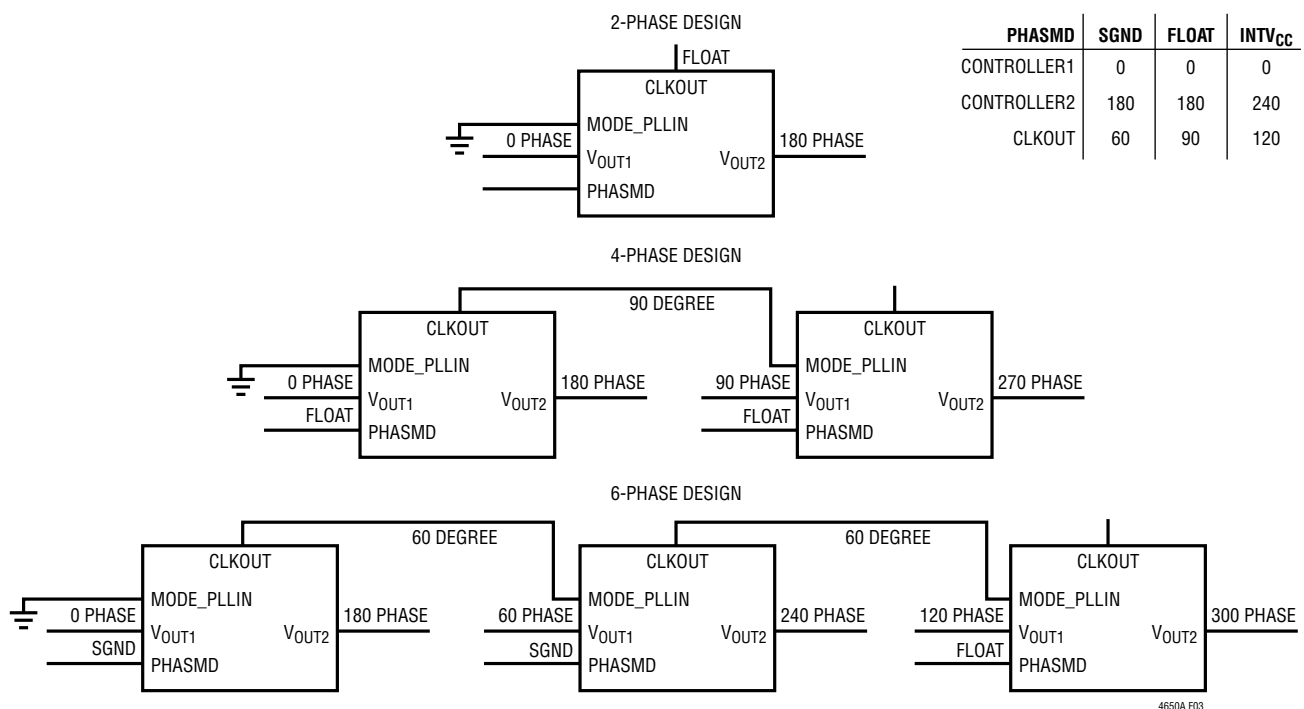


Figure 3. Examples of 2-Phase, 4-Phase, and 6-Phase Operation with PHASMD Table

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A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design.

The LTM4650A device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design.

Connect the COMP pins, FB pins, TRACK/SS pin and V_{OUT} pins from different modules together. See Figure 33 and 35 for examples of parallel operation.

Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 4 shows this graph.

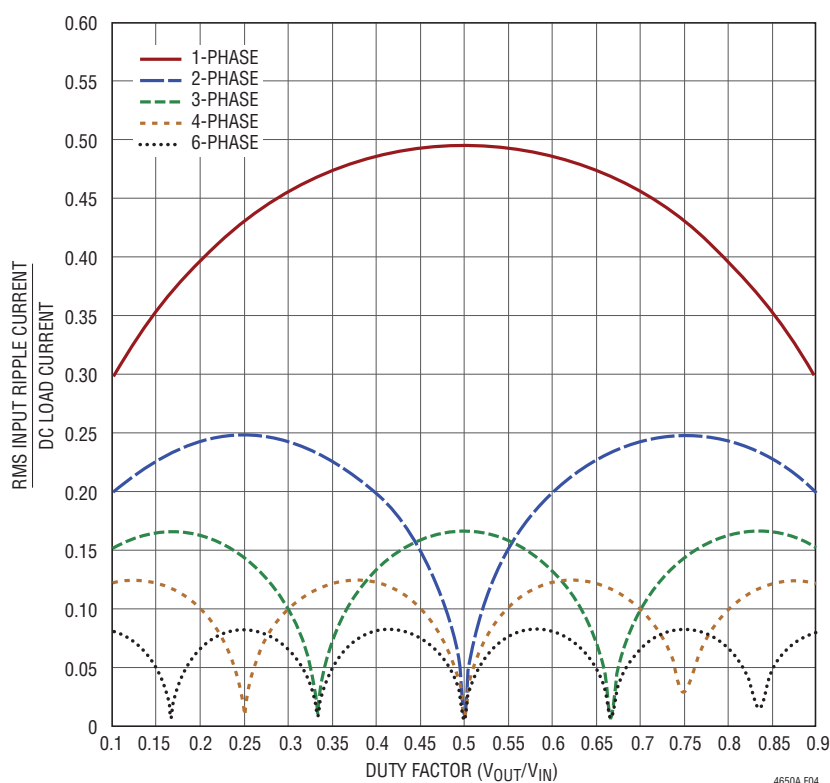


Figure 4. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

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Frequency Selection and Phase-Lock Loop (MODE_PLLIN and f_{SET} Pins)

The LTM4650A device is operated over a range of frequencies to improve power conversion efficiency. It is recommended to operate the module at 300kHz to 750kHz over different input and output range for the best efficiency and inductor current ripple.

The LTM4650A switching frequency can be set with an external resistor from the f_{SET} pin to SGND. An accurate 10 μ A current source into the resistor will set a voltage that programs the frequency or a DC voltage can be applied. Figure 5 shows a graph of frequency setting versus programming voltage. An external clock can be applied to the MODE_PLLIN pin from 0V to INTV_{CC} over a frequency range of 250kHz to 780kHz. The clock input high threshold is 1.6V and the clock input low threshold is 1V. The LTM4650A has the PLL loop filter components on board. The frequency setting resistor should always be present to set the initial switching frequency before locking to an external clock. Both regulators will operate in continuous mode while being externally clock.

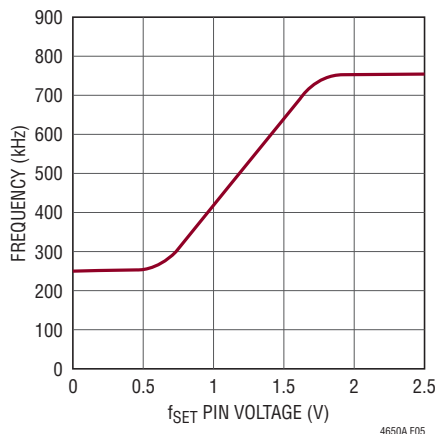


Figure 5. Operating Frequency vs f_{SET} Pin Voltage

The output of the PLL phase detector has a pair of complementary current sources that charge and discharge the internal filter network. When the external clock is applied then the f_{SET} frequency resistor is disconnected with an internal switch, and the current sources control the frequency adjustment to lock to the incoming external clock. When no external clock is applied, then the internal switch is on, thus connecting the external f_{SET} frequency set resistor for free run operation.

Minimum On-Time

Minimum on-time t_{ON} is the smallest time duration that the LTM4650A is capable of turning on the top MOSFET on either channel. It is determined by internal timing delays, and the gate charge required turning on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$\frac{V_{OUT}}{V_{IN} \cdot \text{FREQ}} > t_{ON(MIN)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the output ripple and current will increase. The on-time can be increased by lowering the switching frequency. A good rule of thumb is to keep on-time longer than 110ns.

Soft-Start And Output Voltage Tracking

The TRACK/SS pin provides a means to either soft-start the regulator or track it to a different power supply. A capacitor on the TRACK/SS pin will program the ramp rate of the output voltage. An internal 1.3 μ A current source will charge up the external soft-start capacitor towards INTV_{CC} voltage. When the TRACK/SS voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage. The total soft-start time can be calculated as:

$$t_{SS} = 0.6 \cdot \frac{C_{SS}}{1.3\mu A}$$

where C_{SS} is the capacitance on the TRACK/SS pin. Current foldback and forced continuous mode are disabled during the soft-start process.

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Output voltage tracking can also be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. Figure 6 shows an example waveform where the slave regulator's output slew rate is proportional to the master's.

Since the slave regulator's TRACK/SS is connected to the master's output through a $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider and its voltage used to regulate the slave output voltage when TRACK/SS voltage is below 0.6V, the slave output voltage and the master output voltage should satisfy the following equation during start-up:

$$V_{OUT(SL)} \cdot \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} =$$

$$V_{OUT(MA)} \cdot \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

The $R_{FB(SL)}$ is the feedback resistor and the $R_{TR(TOP)}/R_{TR(BOT)}$ is the resistor divider on the TRACK/SS pin of the slave regulator, as shown in Figure 7.

Following the previous equation, the ratio of the master's output slew rate (MR) to the slave's output slew rate (SR) is determined by:

$$\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}}$$

For example, $V_{OUT(MA)} = 1.5V$, $MR = 1.5V/1ms$ and $V_{OUT(SL)} = 3.3V$, $SR = 3.3V/1ms$. From the equation, we could solve that $R_{TR(TOP)} = 60.4k$ and $R_{TR(BOT)} = 40.2k$ are a good combination for the ratiometric tracking.

The TRACK/SS pin will have the $2\mu A$ current source on when a resistive divider is used to implement tracking on the slave regulator. This will impose an offset on the TRACK/SS pin input. Smaller value resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the $60.4k$ is used then a $6.04k$ can be used to reduce the TRACK/SS pin offset to a negligible value.

Coincident output tracking can be recognized as a special ratiometric output tracking in which the master's output slew rate (MR) is the same as the slave's output slew rate (SR), waveform as shown in Figure 8.

From the equation, we could easily find that, in coincident tracking, the slave regulator's TRACK/SS pin resistor divider is always the same as its feedback divider:

$$\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

For example, $R_{TR(TOP)} = 60.4k$ and $R_{TR(BOT)} = 13.3k$ is a good combination for coincident tracking for a $V_{OUT(MA)} = 1.5V$ and $V_{OUT(SL)} = 3.3V$ application.

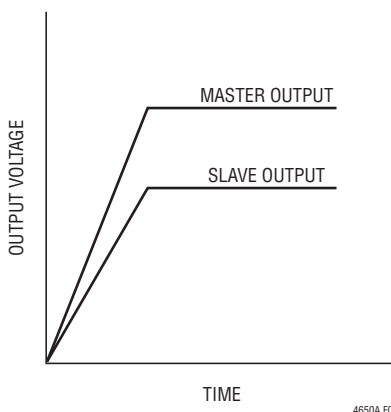


Figure 6. Output Ratiometric Tracking Waveform

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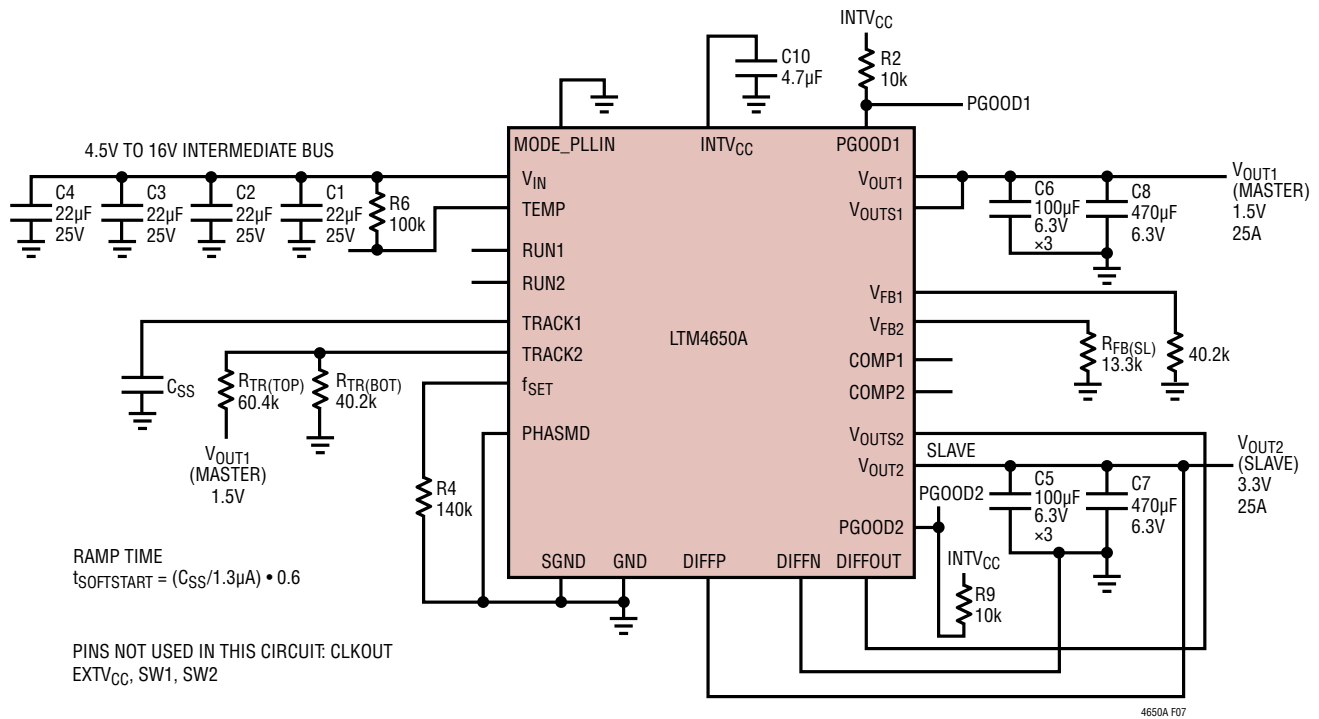


Figure 7. Example of Output Tracking Application Circuit

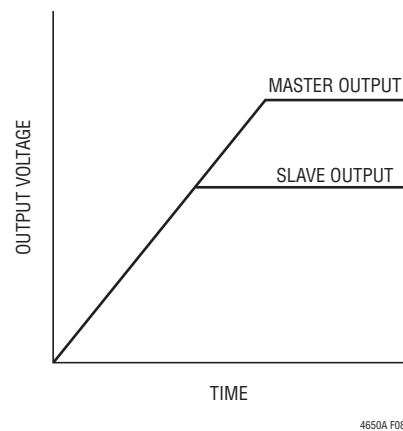


Figure 8. Output Coincident Tracking Waveform

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Power Good

The PGOOD pins are open drain pins that can be used to monitor valid output voltage regulation. This pin monitors a 10% window around the regulation point. A resistor can be pulled up to a particular supply voltage no greater than 6V maximum for monitoring.

Stability Compensation

The module has already been internally compensated for all output voltages. Table 6 is provided for most application requirements. LTpowerCAD will be provided for other control loop optimization.

Run Enable

The RUN pins have an enable threshold of 1.4V maximum, typically 1.25V with 150mV of hysteresis. They control the turn on each of the channels and INTV_{CC}. These pins can be pulled up to V_{IN} for 5V operation, or a 5V Zener diode can be placed on the pins and a 10k to 100k resistor can be placed up to higher than 5V input for enabling the channels. There is 1μA pull-up current for each RUN pin. The LTM4650A will turn on with RUN floating. Please note RUN has a 6V Abs Max voltage rating. The RUN pins can also be used for output voltage sequencing. In parallel operation the RUN pins can be tie together and controlled from a single control. See the Typical Application circuits in Figure 32.

INTV_{CC} and EXTV_{CC}

The LTM4650A module has an internal 5V low dropout regulator that is derived from the input voltage. This regulator is used to power the control circuitry and the power MOSFET drivers. This regulator can source up to 70mA, and typically uses ~30mA for powering the device at the maximum frequency. This internal 5V supply is enabled by either RUN1 or RUN2.

EXTV_{CC} allows an external 5V supply to power the LTM4650A and reduce power dissipation from the internal low dropout 5V regulator. The power loss savings can be calculated by:

$$(V_{IN} - 5V) \cdot 30mA = P_{LOSS}$$

EXTV_{CC} has a threshold of 4.7V for activation, and a maximum rating of 6V. When using a 5V input, connect this 5V input to EXTV_{CC} also to maintain a 5V gate drive level. EXTV_{CC} must sequence on after V_{IN}, and EXTV_{CC} must sequence off before V_{IN}.

Differential Remote Sense Amplifier

An accurate differential remote sense amplifier is provided to sense low output voltages accurately at the remote load points. This is especially true for high current loads. The amplifier can be used on one of the two channels, or on a single parallel output. It is very important that the DIFFP and DIFFN are connected properly at the output, and DIFFOUT is connected to either V_{OUTS1} or V_{OUTS2}. In parallel operation, the DIFFP and DIFFN are connected properly at the output, and DIFFOUT is connected to one of the V_{OUTS} pins. Review the parallel schematics in Figure 33 and review Figure 2. Please note Diffamp can be used for ≤3.3V outputs.

SW Pins

The SW pins are generally for testing purposes by monitoring these pins. These pins can also be used to dampen out switch node ringing caused by LC parasitic in the switched current paths. Usually a series R-C combination is used called a snubber circuit. The resistor will dampen the resonance and the capacitor is chosen to only affect the high frequency ringing across the resistor. If the stray inductance or capacitance can be measured or approximated then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to predict. It combines the power path board inductance in combination with the MOSFET interconnect bond wire inductance.

First the SW pin can be monitored with a wide bandwidth scope with a high frequency scope probe. The ring frequency can be measured for its value. The impedance Z can be calculated:

$$Z_{(L)} = 2\pi fL,$$

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where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z , then the ringing should be dampened. The snubber capacitor value is chosen so that its impedance is equal to the resistor at the ring frequency. Calculated by: $Z_C = 1/(2\pi fC)$. These values are a good place to start with. Modification to these components should be made to attenuate the ringing with the least amount of power loss.

Temperature Monitoring

A diode connected PNP transistor is used for the TEMP monitor function by monitoring its voltage over temperature. The temperature dependence of this diode voltage can be understood in the equation:

$$V_D = nV_T \ln\left(\frac{I_D}{I_S}\right)$$

where V_T is the thermal voltage (kT/q), and n , the ideality factor, is 1 for the diode connected PNP transistor being used in the LTM4650A. I_S is expressed by the typical empirical equation:

$$I_S = I_0 \exp\left(\frac{-V_{G0}}{V_T}\right)$$

where I_0 is a process and geometry dependent current, (I_0 is typically around 20k orders of magnitude larger than I_S at room temperature) and V_{G0} is the band gap voltage of 1.2V extrapolated to absolute zero or -273°C .

If we take the I_S equation and substitute into the V_D equation, then we get:

$$V_D = V_{G0} - \left(\frac{kT}{q}\right) \ln\left(\frac{I_0}{I_D}\right), \quad V_T = \frac{kT}{q}$$

The expression shows that the diode voltage decreases (linearly if I_0 were constant) with increasing temperature and constant diode current. Figure 9 shows a plot of V_D vs Temperature over the operating temperature range of the LTM4650A.

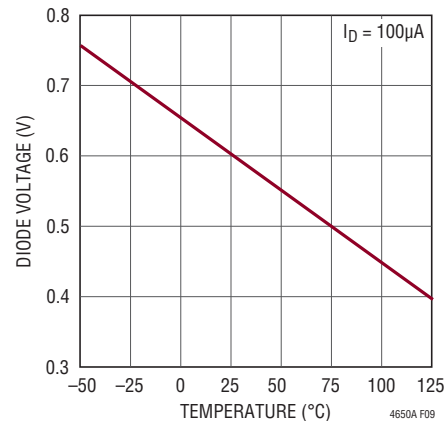


Figure 9. Diode Voltage V_D vs Temperature $T(K)$ for Different Bias Currents

If we take this equation and differentiate it with respect to temperature T , then:

$$\frac{dV_D}{dT} = -\frac{V_{G0} - V_D}{T}$$

This dV_D/dT term is the temperature coefficient equal to about -2mV/K or $-2\text{mV}/^\circ\text{C}$. The equation is simplified for the first order derivation.

Solving for T , $T = -(V_{G0} - V_D)/(dV_D/dT)$ provides the temperature.

1st Example: Figure 9 for 27°C , or 300K the diode voltage is 0.598V, thus, $300\text{K} = -(1200\text{mV} - 598\text{mV})/(-2.0\text{mV/K})$

2nd Example: Figure 9 for 75°C , or 350K the diode voltage is 0.50V, thus, $350\text{K} = -(1200\text{mV} - 500\text{mV})/(-2.0\text{mV/K})$

Converting the Kelvin scale to Celsius is simply taking the Kelvin temp and subtracting 273 from it.

A typical forward voltage is given in the electrical characteristics section of the data sheet, and Figure 9 is the plot of this forward voltage. Measure this forward voltage at 27°C to establish a reference point. Then using the above expression while measuring the forward voltage over temperature will provide a general temperature monitor. Connect a resistor between TEMP and V_{IN} to set the current to $100\mu\text{A}$. See Figure 33 for an example.

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Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a μ Module package mounted to a hardware test board—also defined by JESD51-9 (“Test Boards for Area Array Surface Mount Package Thermal Measurements”). The motivation for providing these thermal coefficients is found in JESD 51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the μ Module regulator’s thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one’s application-usage, and can be adapted to correlate thermal performance to one’s own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA} , the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as “still air” although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical μ Module, the bulk of the heat flows out

the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don’t generally match the user’s application.

3. θ_{JCTOP} , the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical μ Module are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don’t generally match the user’s application.
4. θ_{JB} , the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the μ Module and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 10; blue resistances are contained within the μ Module regulator, whereas green resistances are external to the μ Module.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a μ Module. For example, in normal board-mounted applications, never does 100% of the device’s total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the μ Module—as the standard defines for θ_{JCTop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

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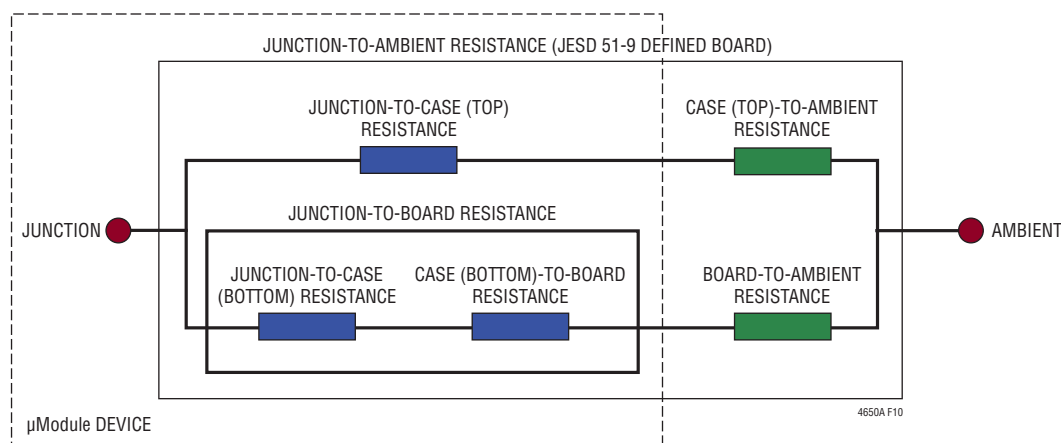


Figure 10. Graphical Representation of JESD51-12 Thermal Coefficients

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the μ Module and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the μ Module with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process

and due-diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory test have been performed and correlated to the μ Module model, then the θ_{JB} and θ_{BA} are summed together to correlate quite well with the μ Module model with no airflow or heat sinking in a properly define chamber. This $\theta_{JB} + \theta_{BA}$ value is shown in the Pin Configuration section and should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink. Each system has its own thermal characteristics, therefore thermal analysis must be performed by the user in a particular system.

The LTM4650A module has been designed to effectively remove heat from both the top and bottom of the package. The bottom substrate material has very low thermal resistance to the printed circuit board. An external heat sink can be applied to the top of the device for excellent heat sinking with airflow.

Figure 11 shows the thermal image of the LTM4650A, without airflow, without heat sink, running paralleled from 12V to 1V at 50A with around 87.3% efficiency and 7.2W power loss. Figure 12 shows the thermal image of the LTM4650A, with 200LFM airflow and external heat sink, running paralleled form 12V to 5V at 50A with around 95% efficiency and 13W power loss.

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Safety Considerations

The LTM4650A modules do not provide isolation from V_{IN} to V_{OUT} . There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support over current protection. A temperature diode is provided for monitoring internal temperature, and can be used to detect the need for thermal shutdown that can be done by controlling the RUN pin.

Power Derating

The 1V, 1.8V, 3.3V and 5V power loss curves in Figures 14 to 17 can be used in coordination with the load current derating curves in Figures 18 to 31 for calculating an approximate θ_{JA} thermal resistance for the LTM4650A with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with a 1.2 multiplicative factor at 125°C.

The derating curves are plotted with CH1 and CH2 in parallel single output operation starting at 50A of load with low ambient temperature. The output voltages are 1V to 5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis.

The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at ~120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased.

The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 22, the load current is derated to ~25A at ~90°C with no air or heat sink and the power loss for the 12V to 1.8V at 25A output is a ~4.4W loss. The 4.4W loss is calculated with the ~3.7W room temperature loss from the 12V to 1.8V power loss curve at 25A, and the 1.2 multiplying factor at 120°C ambient. If the 90°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 30°C divided 4.4W equals a 6.8°C/W θ_{JA} thermal resistance. Table 2 specifies a 7°C/W value which is pretty close. The airflow graphs are more accurate due to the fact that the ambient temperature environment is controlled better with airflow. Tables 2 to 5 provide equivalent thermal resistances for 1V to 5V outputs with and without airflow and heat sinking.

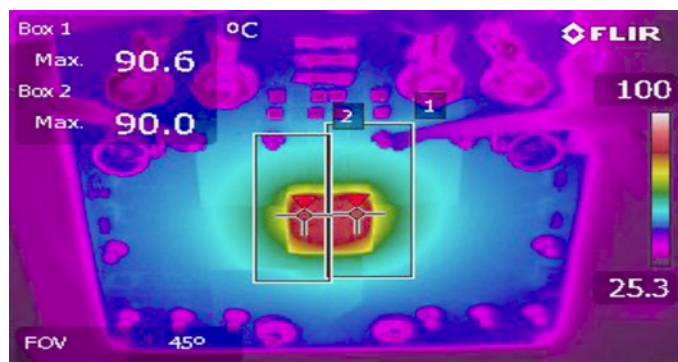


Figure 11. Thermal Image 12V to 1V, 50A with No Airflow without Heat Sink

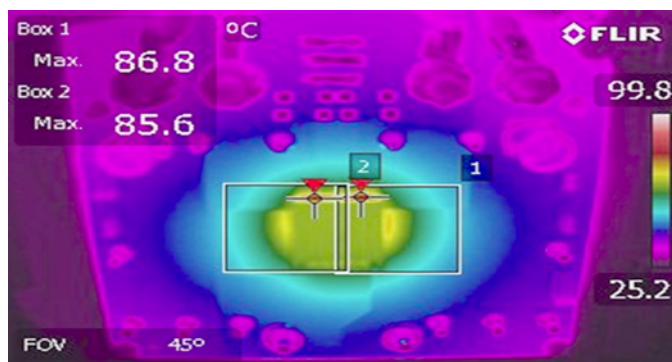


Figure 12. Thermal Image 12V to 5V, 50A with 200LFM Airflow without Heat Sink

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The derived thermal resistances in Tables 2 and 3 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for all four layers. The PCB dimensions are 101mm × 114mm. The BGA heat sinks are listed in Table 3.

Layout Checklist/Example

The high integration of LTM4650A makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN} , GND, V_{OUT1} and V_{OUT2} . It helps to minimize the PCB conduction loss and thermal stress.

- Place high frequency ceramic input and output capacitors next to the V_{IN} , PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the V_{OUT} , V_{FB} , and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 13 gives a good example of the recommended layout.

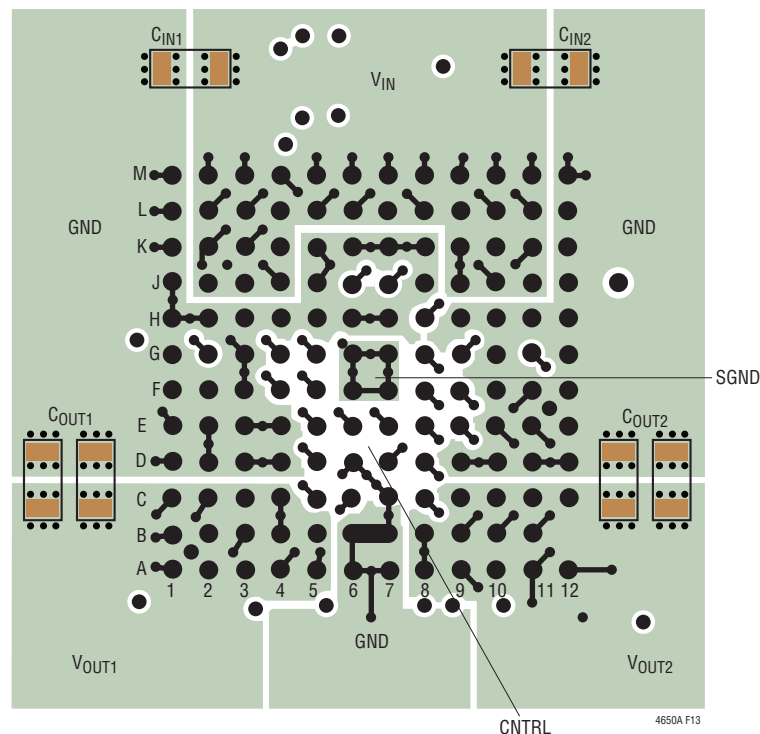


Figure 13. Recommended PCB Layout

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Table 2. 1.0V Output

DERATING CURVE	V _{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ _{JA} (°C/W)
Figures 18, 19	5, 12	Figure 14	0	None	7
Figures 18, 19	5, 12	Figure 14	200	None	6
Figures 18, 19	5, 12	Figure 14	400	None	5.5
Figures 20, 21	5, 12	Figure 14	0	BGA Heat Sink	6.5
Figures 20, 21	5, 12	Figure 14	200	BGA Heat Sink	5
Figures 20, 21	5, 12	Figure 14	400	BGA Heat Sink	4

Table 3. 1.8V Output

DERATING CURVE	V _{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ _{JA} (°C/W)
Figures 22, 23	5, 12	Figure 15	0	None	7
Figures 22, 23	5, 12	Figure 15	200	None	6
Figures 22, 23	5, 12	Figure 15	400	None	5.5
Figures 24, 25	5, 12	Figure 15	0	BGA Heat Sink	6.5
Figures 24, 25	5, 12	Figure 15	200	BGA Heat Sink	4
Figures 24, 25	5, 12	Figure 15	400	BGA Heat Sink	3.5

Table 4. 3.3V Output

DERATING CURVE	V _{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ _{JA} (°C/W)
Figures 26, 27	5, 12	Figure 16	0	None	7
Figures 26, 27	5, 12	Figure 16	200	None	6
Figures 26, 27	5, 12	Figure 16	400	None	5.5
Figures 28, 29	5, 12	Figure 16	0	BGA Heat Sink	6.5
Figures 28, 29	5, 12	Figure 16	200	BGA Heat Sink	5
Figures 28, 29	5, 12	Figure 16	400	BGA Heat Sink	4

Table 5. 5V Output

DERATING CURVE	V _{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ _{JA} (°C/W)
Figures 30	12	Figure 17	0	None	7
Figures 30	12	Figure 17	200	None	6
Figures 30	12	Figure 17	400	None	5.5
Figures 31	12	Figure 17	0	BGA Heat Sink	6.5
Figures 31	12	Figure 17	200	BGA Heat Sink	4
Figures 31	12	Figure 17	400	BGA Heat Sink	3.5

HEAT SINK MANUFACTURER

PART NUMBER

WEBSITE

Aavid Thermalloy

375424B00034G

www.aavid.com

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Table 6. Output Voltage Response vs Component Matrix (Refer to Figure 33) Load Step Typical Measured Values

2-Phase Single Output Solution

C _{IN} (CERAMIC)			C _{OUT} (CERAMIC)			C _{OUT} (BULK)		
VENDORS	VALUE	PART NUMBER	VENDORS	VALUE	PART NUMBER	VENDORS	VALUE	PART NUMBER
MURATA	22μF, 16V, X5R, 1210	GRM32ER61C226KE20L	MURATA	100μF, 6.3V, X5R, 1210	GRM32ER60J107ME20L	Panasonic	470μF, 6.3V 10mΩ	6TPF470MAH ¹
MURATA	22μF, 16V, X5R, 1206	GRM31CR61C226KE15K	MURATA	220μF, 4V, X5R, 1206	GRM31CR60G227M	Panasonic	470μF, 2.5V 3mΩ	EEFGX0E4TIR ²
TDK	22μF, 16V, X5R, 1210	C3225X5R1C226M250AA	Taiyo Yuden	100μF, 6.3V, X5R, 1210	JMK325BJ107MM-T			
			Taiyo Yuden	220μF, 4V, X5R, 1210	AMK325ABJ227MM-T			

25% Load Step (0A to 12.5A), Ceramic Output Cap Only Solutions

V _{IN}	V _{OUT}	C _{IN3} (BULK)	C _{IN} (CERAMIC)	C _{OUT} (BULK)	C _{OUT} (CERAMIC)	FEED-FORWARD CAPACITOR (C _{FF})	PEAK-PEAK DEVIATION (V _{PK-PK})	SETTLING TIME (t _{SETTLE})	LOAD STEP	LOAD STEP SLEW RATE	R _{FB} (kΩ)	FREQ (kHz)
12V	1V	150μF	22μF ×4	None	100μF×16	47pF	102mV	50μs	12.5A	10A/μs	90.9	300kHz
12V	1.2V	150μF	22μF ×4	None	100μF×16	47pF	92mV	50μs	12.5A	10A/μs	60.4	400kHz
12V	1.5V	150μF	22μF ×4	None	100μF×16	47pF	105mV	50μs	12.5A	10A/μs	40.2	400kHz
12V	1.8V	150μF	22μF ×4	None	100μF×16	47pF	109mV	50μs	12.5A	10A/μs	30.2	500kHz
12V	2.5V	150μF	22μF ×4	None	100μF×16	47pF	134mV	60μs	12.5A	10A/μs	19.1	500kHz
12V	3.3V	150μF	22μF ×4	None	100μF×16	47pF	161mV	60μs	12.5A	10A/μs	13.3	600kHz
12V	5V	Suggest to Use POSCAP + Ceramic Cap										

25% Load Step (0A to 12.5A), POSCAP+Ceramic Output Cap Solutions

V _{IN}	V _{OUT}	C _{IN3} (BULK)	C _{IN} (CERAMIC)	C _{OUT} (BULK)	C _{OUT} (CERAMIC)	FEED-FORWARD CAPACITOR (C _{FF})	PEAK-PEAK DEVIATION (V _{PK-PK})	SETTLING TIME (t _{SETTLE})	LOAD STEP	LOAD STEP SLEW RATE	R _{FB} (kΩ)	FREQ (kHz)
12V	1V	150μF	22μF ×4	470μF×4 ²	100μF×8	None	82mV	50μs	12.5A	10A/μs	90.9	300kHz
12V	1.2V	150μF	22μF ×4	470μF×4 ²	100μF×8	None	80mV	50μs	12.5A	10A/μs	60.4	400kHz
12V	1.5V	150μF	22μF ×4	470μF×4 ²	100μF×8	None	92mV	60μs	12.5A	10A/μs	40.2	400kHz
12V	1.8V	150μF	22μF ×4	470μF×4 ²	100μF×8	None	97mV	70μs	12.5A	10A/μs	30.2	500kHz
12V	2.5V	150μF	22μF ×4	470μF×4 ²	100μF×8	None	117mV	70μs	12.5A	10A/μs	19.1	500kHz
12V	3.3V	150μF	22μF ×4	470μF×4 ¹	100μF×8	None	127mV	80μs	12.5A	10A/μs	13.3	600kHz
12V	5V	150μF	22μF ×4	470μF×4 ¹	100μF×8	None	167mV	100μs	12.5A	10A/μs	8.25	700kHz

Notes 1 and 2. Different (BULK) C_{OUT} are used. See part number in Table 6.

Note 3. C_{IN} (BULK) may be required with long PCB traces.

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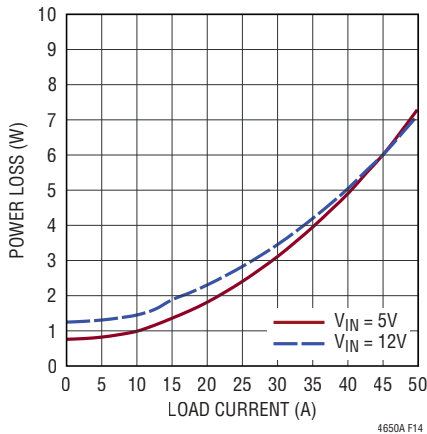


Figure 14. 1.0V_{OUT} Power Loss Curve

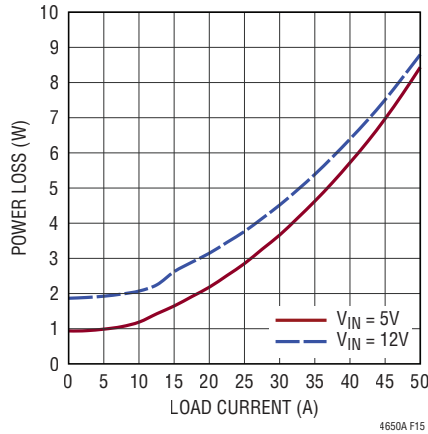


Figure 15. 1.8V_{OUT} Power Loss Curve

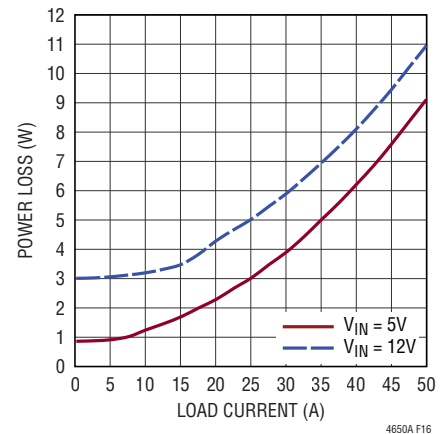


Figure 16. 3.3V_{OUT} Power Loss Curve

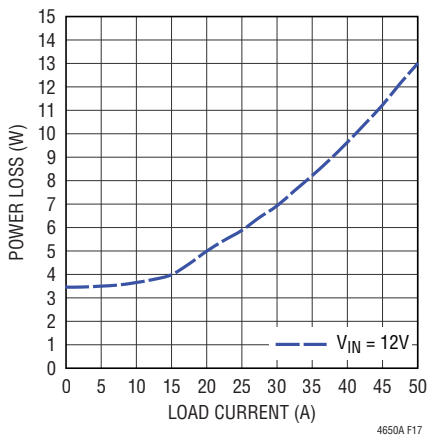


Figure 17. 5V_{OUT} Power Loss Curve

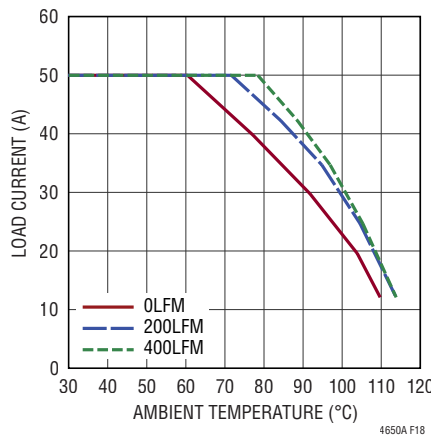


Figure 18. 12V to 1V Derating Curve, No Heat Sink

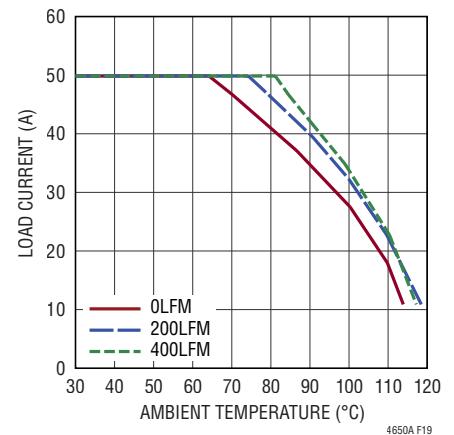


Figure 19. 5V to 1V Derating Curve, No Heat Sink

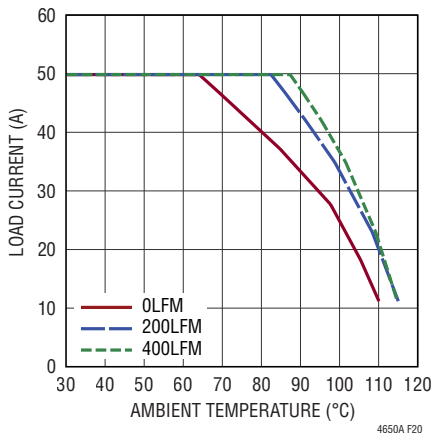


Figure 20. 12V to 1V Derating Curve, BGA Heat Sink

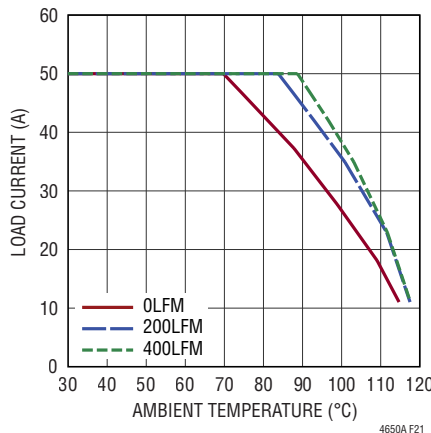


Figure 21. 5V to 1V Derating Curve, BGA Heat Sink

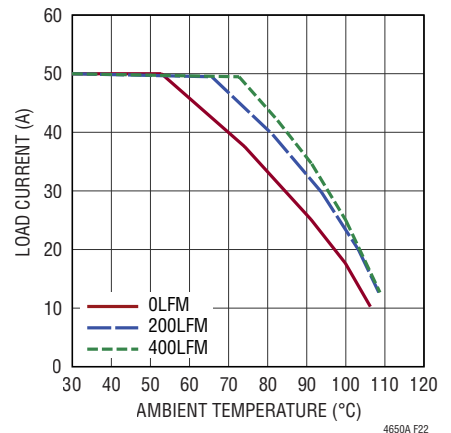


Figure 22. 12V to 1.8V Derating Curve, No Heat Sink

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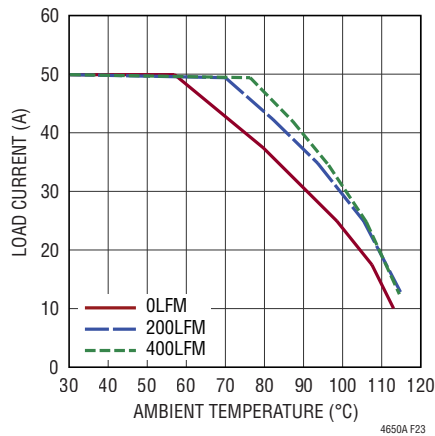


Figure 23. 5V to 1.8V Derating Curve, No Heat Sink

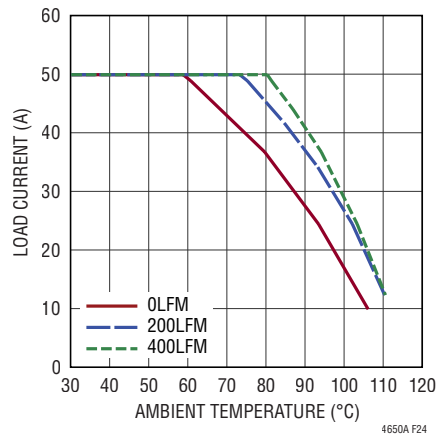


Figure 24. 12V to 1.8V Derating Curve, BGA Heat Sink

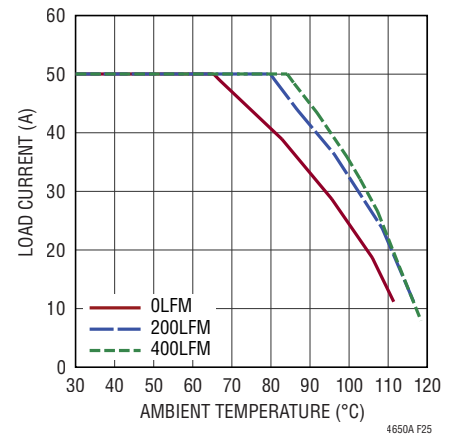


Figure 25. 5V to 1.8V Derating Curve, BGA Heat Sink

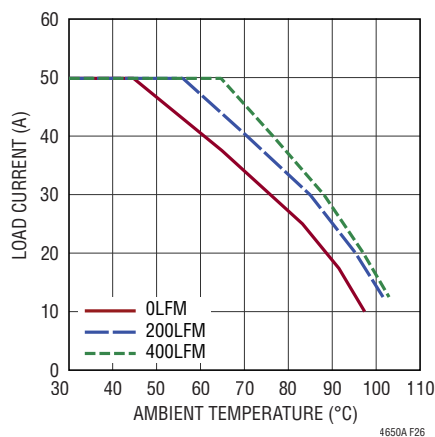


Figure 26. 12V to 3.3V Derating Curve, No Heat Sink

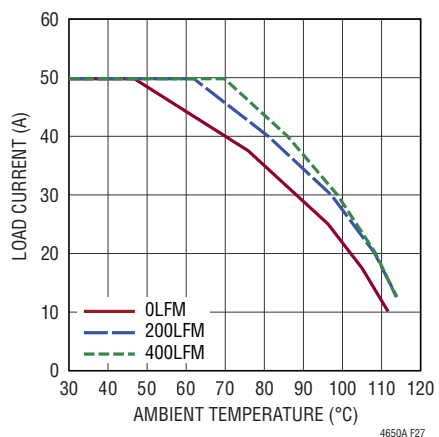


Figure 27. 5V to 3.3V Derating Curve, No Heat Sink

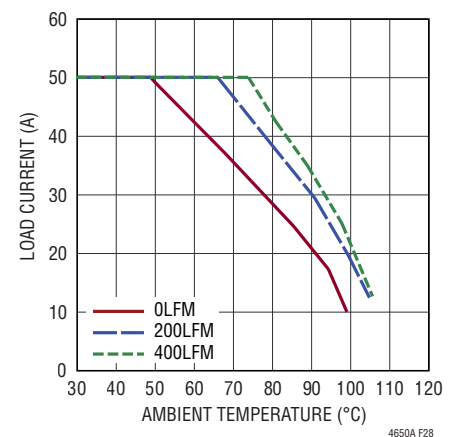


Figure 28. 12V to 3.3V Derating Curve, BGA Heat Sink

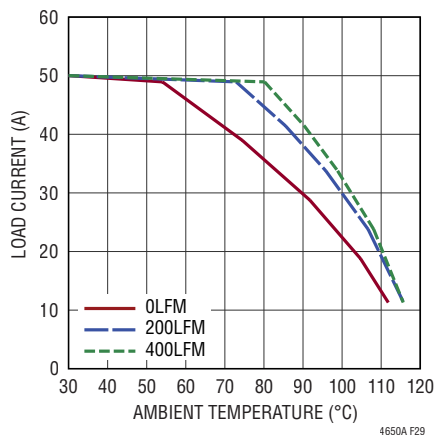


Figure 29. 5V to 3.3V Derating Curve, BGA Heat Sink

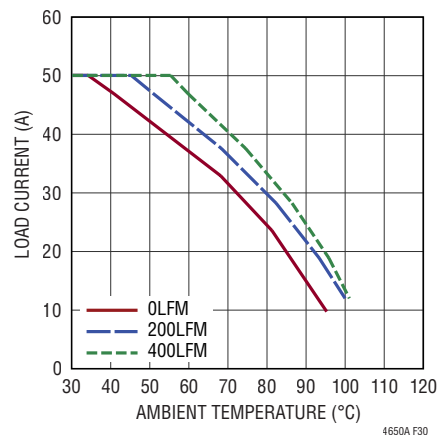


Figure 30. 12V to 5V Derating Curve, No Heat Sink

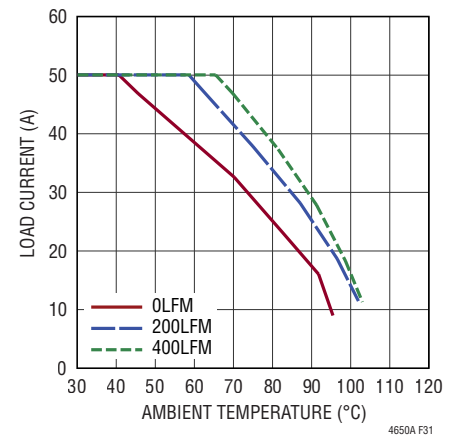


Figure 31. 12V to 5V Derating Curve, BGA Heat Sink

TYPICAL APPLICATIONS

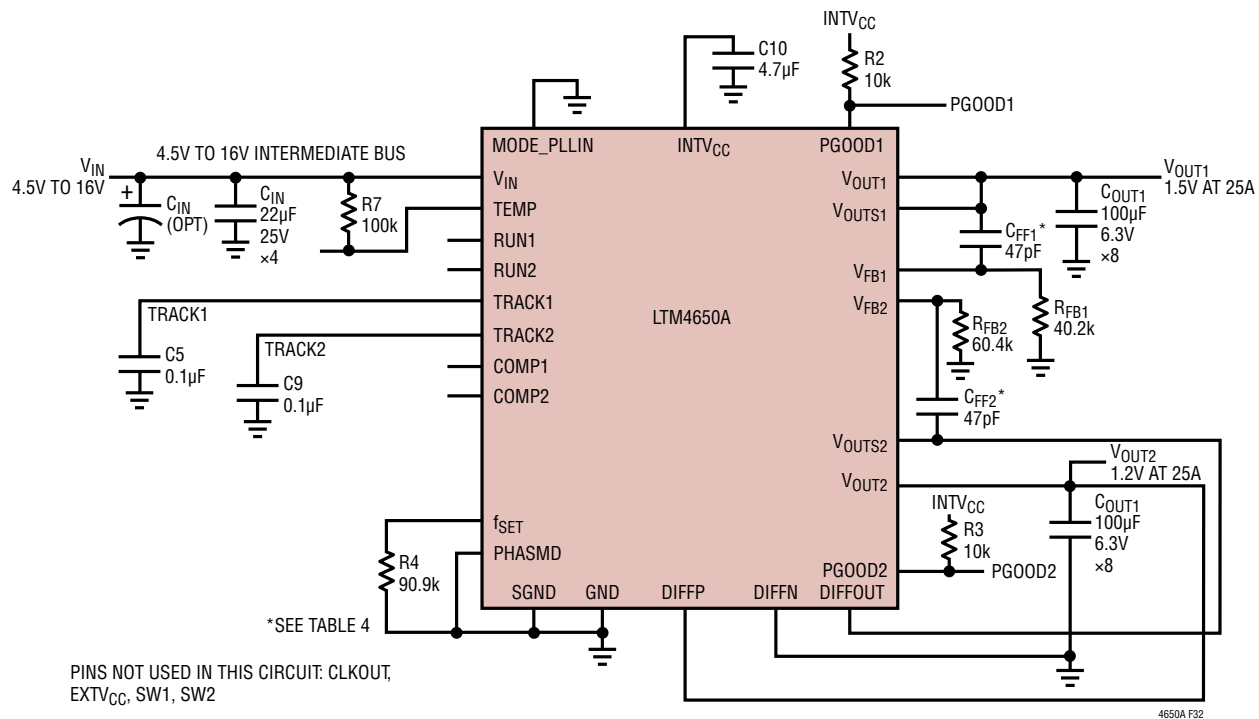


Figure 32. Typical 4.5V_{IN} to 16V_{IN}, 1.5V and 1.2V at 25A Outputs

TYPICAL APPLICATIONS

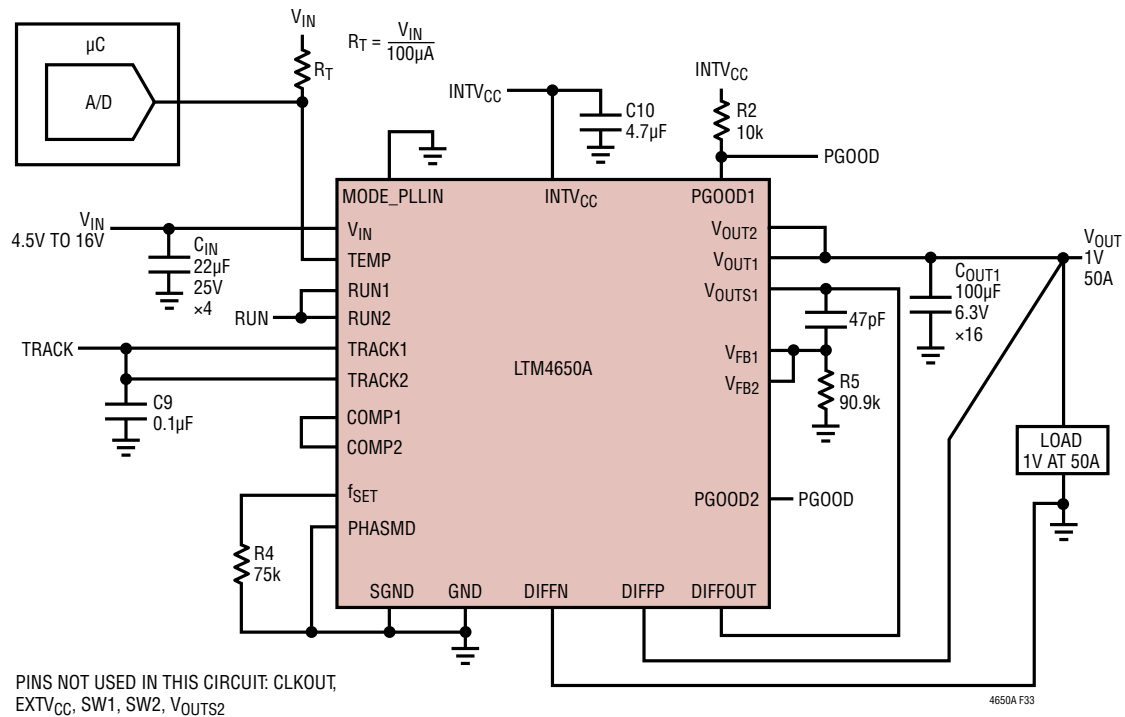


Figure 33. LTM4650A 2-Phase, 1V at 50A Design

TYPICAL APPLICATIONS

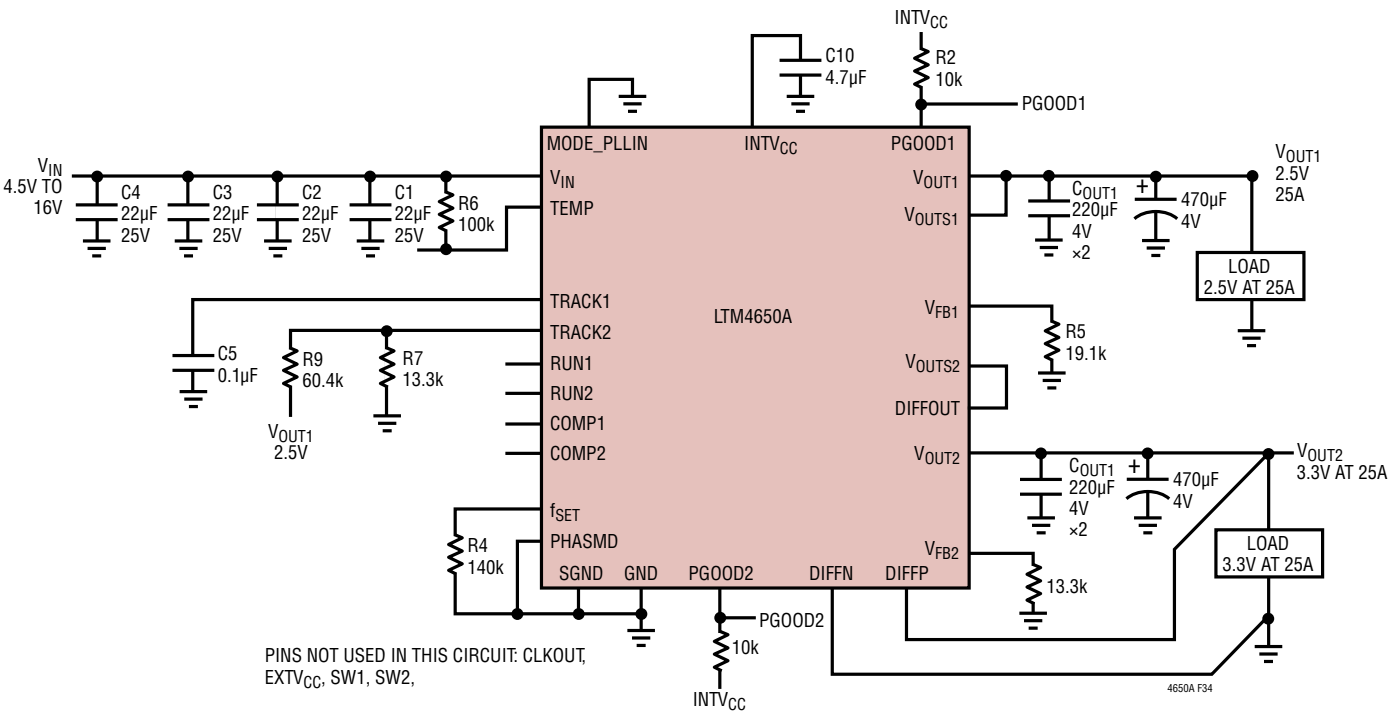


Figure 34. LTM4650A 2.5V and 3.3V Output with Tracking Function

TYPICAL APPLICATIONS

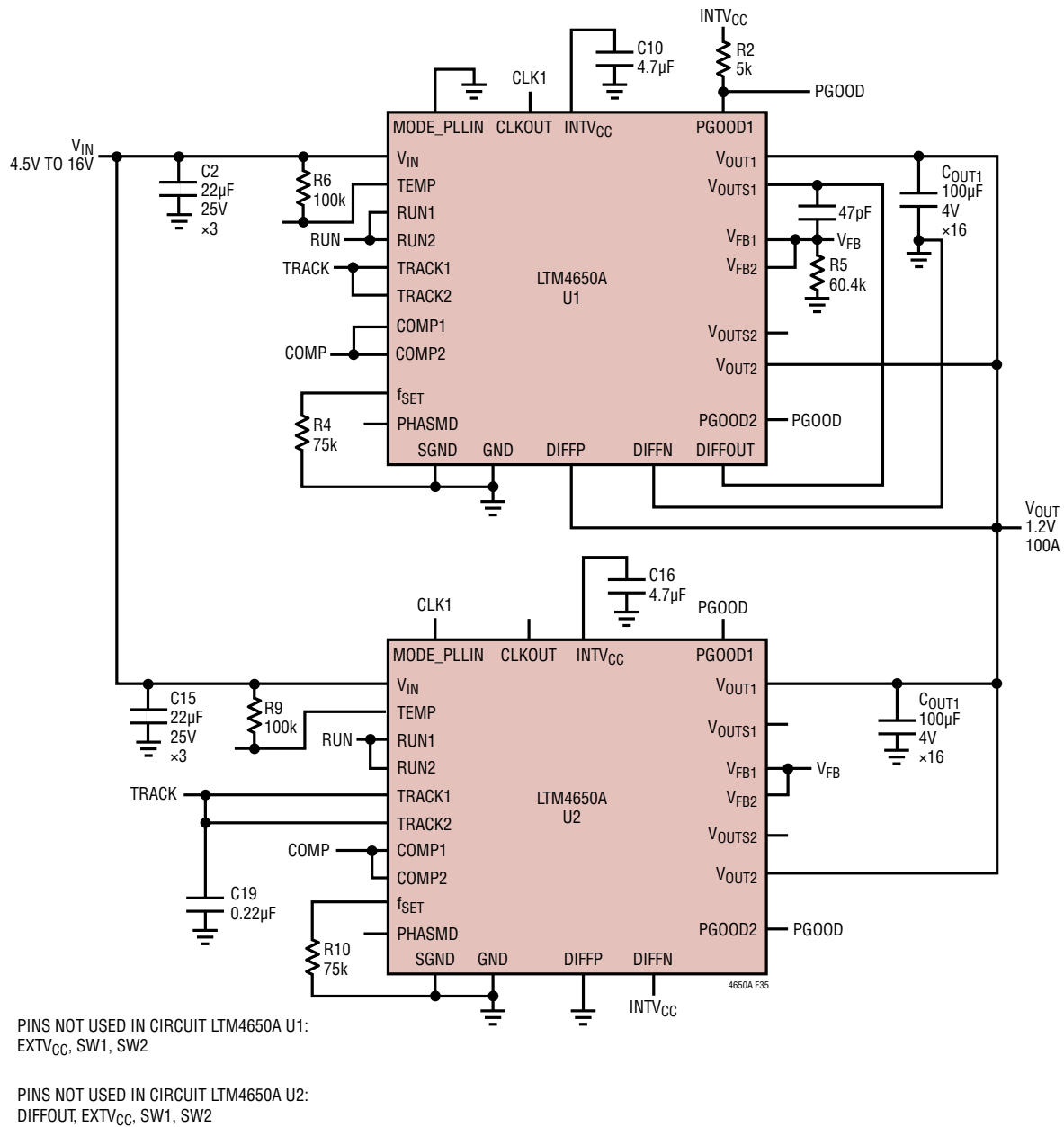


Figure 35. LTM4650A 4-Phase, 1.2V at 100A

PACKAGE DESCRIPTION

LTM4650A Component LGA and BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V _{OUT1}	B1	V _{OUT1}	C1	V _{OUT1}	D1	GND	E1	GND	F1	GND
A2	V _{OUT1}	B2	V _{OUT1}	C2	V _{OUT1}	D2	GND	E2	GND	F2	GND
A3	V _{OUT1}	B3	V _{OUT1}	C3	V _{OUT1}	D3	GND	E3	GND	F3	GND
A4	V _{OUT1}	B4	V _{OUT1}	C4	V _{OUT1}	D4	GND	E4	GND	F4	MODE_PLLIN
A5	V _{OUT1}	B5	V _{OUT1}	C5	V _{OUT1S}	D5	VFB1	E5	TRACK1	F5	RUN1
A6	GND	B6	GND	C6	f _{SET}	D6	SGND	E6	COMP1	F6	SGND
A7	GND	B7	GND	C7	SGND	D7	VFB2	E7	COMP2	F7	SGND
A8	V _{OUT2}	B8	V _{OUT2}	C8	V _{OUT2S}	D8	TRACK2	E8	DIFFP	F8	DIFFOUT
A9	V _{OUT2}	B9	V _{OUT2}	C9	V _{OUT2}	D9	GND	E9	DIFFN	F9	RUN2
A10	V _{OUT2}	B10	V _{OUT2}	C10	V _{OUT2}	D10	GND	E10	GND	F10	GND
A11	V _{OUT2}	B11	V _{OUT2}	C11	V _{OUT2}	D11	GND	E11	GND	F11	GND
A12	V _{OUT2}	B12	V _{OUT2}	C12	V _{OUT2}	D12	GND	E12	GND	F12	GND

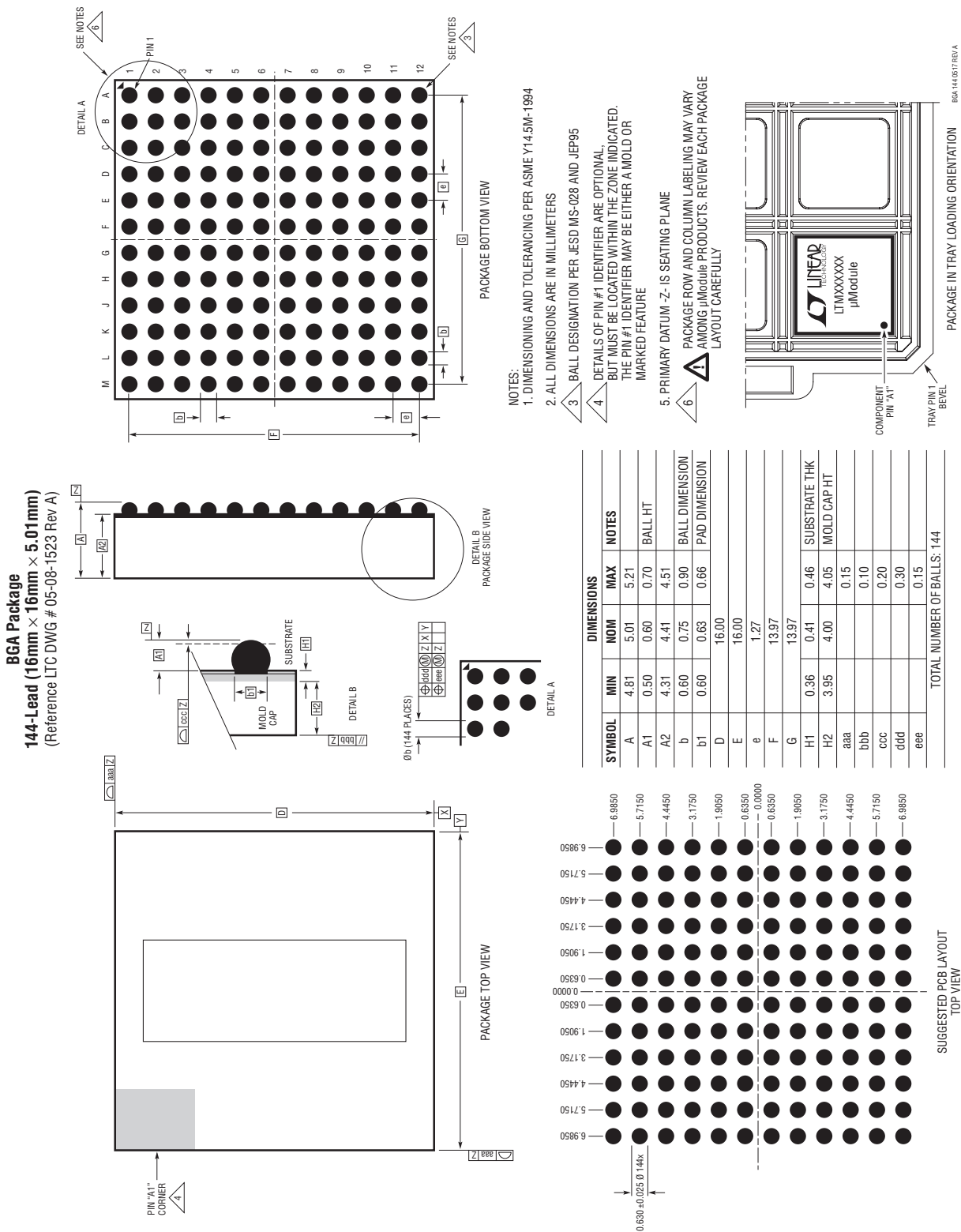
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	GND	J1	GND	K1	GND	L1	GND	M1	GND
G2	SW1	H2	GND	J2	V _{IN}	K2	V _{IN}	L2	V _{IN}	M2	V _{IN}
G3	GND	H3	GND	J3	V _{IN}	K3	V _{IN}	L3	V _{IN}	M3	V _{IN}
G4	PHASEMD	H4	GND	J4	V _{IN}	K4	V _{IN}	L4	V _{IN}	M4	V _{IN}
G5	CLKOUT	H5	GND	J5	GND	K5	GND	L5	V _{IN}	M5	V _{IN}
G6	SGND	H6	GND	J6	TEMP	K6	GND	L6	V _{IN}	M6	V _{IN}
G7	SGND	H7	GND	J7	EXTV _{CC}	K7	GND	L7	V _{IN}	M7	V _{IN}
G8	PGOOD2	H8	INTV _{CC}	J8	GND	K8	GND	L8	V _{IN}	M8	V _{IN}
G9	PGOOD1	H9	GND	J9	V _{IN}	K9	V _{IN}	L9	V _{IN}	M9	V _{IN}
G10	GND	H10	GND	J10	V _{IN}	K10	V _{IN}	L10	V _{IN}	M10	V _{IN}
G11	SW2	H11	GND	J11	V _{IN}	K11	V _{IN}	L11	V _{IN}	M11	V _{IN}
G12	GND	H12	GND	J12	GND	K12	GND	L12	GND	M12	GND

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTM4650A#packaging> for the most recent package drawings.

PACKAGE DESCRIPTION

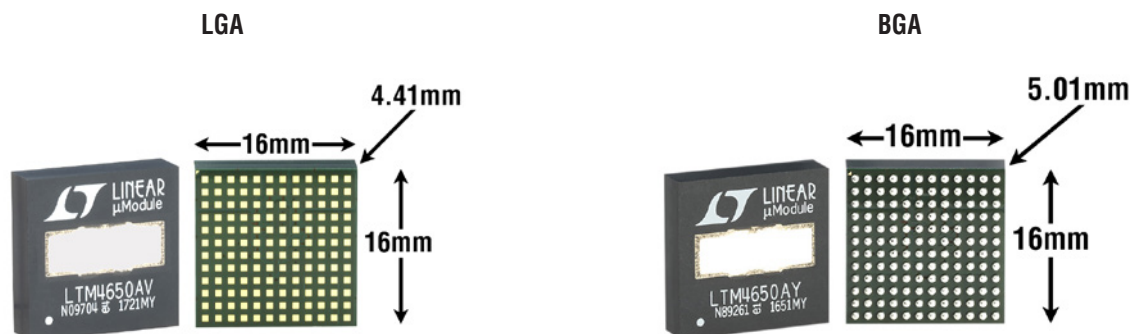
Please refer to <http://www.linear.com/product/LTM4650A#packaging> for the most recent package drawings.



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/17	Added Pin Compatible feature	1
B	10/17	Added LGA Package	1, 2, 35, 38

PACKAGE PHOTO



DESIGN RESOURCES

SUBJECT	DESCRIPTION
μModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
μModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search Input V_{in} (Min) V V_{in} (Max) V Output V_{out} V I_{out} A Search
TechClip Videos	Quick videos detailing how to bench test electrical and thermal performance of μModule products.
Digital Power System Management	Analog Devices's family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4630A	Lower Current than LTM4650A; Up to 5.3V _{OUT} , Dual 18A or Single 36A	Pin Compatible with LTM4650A; 4.5V ≤ V _{IN} ≤ 15V, 0.6V ≤ V _{OUT} ≤ 5.3V, 16mm × 16mm × 4.41mm (LGA)
LTM4630-1	Lower Current and lower V _{OUT(MAX)} than LTM4650A with External Compensation. Dual 18A or Single 36A. ±0.8% (–1A) or ±1.5% (–1B) V _{OUT} accuracy	4.5V ≤ V _{IN} ≤ 15V, 0.6V ≤ V _{OUT} ≤ 1.8V, 16mm × 16mm × 5.01mm (BGA)
LTM4630	Lower Current, Lower V _{OUT(MAX)} than LTM4650A; Dual 18A or Single 36A	Pin Compatible with LTM4650A; 4.5V ≤ V _{IN} ≤ 15V, 0.6V ≤ V _{OUT} ≤ 1.8V, 16mm × 16mm × 4.41mm (LGA), 16mm × 16mm × 5.01mm (BGA)
LTM4620A	Lower Current than LTM4650A; Up to 5.3V _{OUT} , Dual 13A or Single 26A.	Pin Compatible with LTM4650A. 4.5V ≤ V _{IN} ≤ 16V, 0.6V ≤ V _{OUT} ≤ 5.3V, 15mm × 15mm × 4.41mm (LGA), 15mm × 15mm × 5.01mm (BGA)
LTM4636	Single 40A μModule Regulator	4.7V ≤ V _{IN} ≤ 15V. 0.6V ≤ V _{OUT} ≤ 3.3V. 16mm × 16mm × 7.07mm (BGA)
LTM4677	Dual 18A or Single 36A with PSM	4.5V ≤ V _{IN} ≤ 16V, 0.5V ≤ V _{OUT} ≤ 1.8V. 16mm × 16mm × 5.01mm (BGA)
LTM4644	Quad 4A	4V ≤ V _{IN} ≤ 14V, 0.6V ≤ V _{OUT} ≤ 5.5V. 9mm × 15mm × 5.01mm (BGA)
LTM4639	Lower V _{IN} (2.375V ≤ V _{IN} ≤ 7V), 20A	0.6V ≤ V _{OUT} ≤ 5.5V. 15mm × 15mm × 4.92mm (BGA)

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