

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC} = 5\text{V}$, $V_{BUS} = 5\text{V}$, $\text{GND} = \text{GND2} = 0\text{V}$, $\text{ON} = V_{LO}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	Operating Supply Range (Isolated Power Input)	●		4.4	12	16.5	V
V_{BUS}	Operating Supply Range (USB Bus Power Input)	●		4.4	5	16.5	V
	V_{CC} Supply Current Power Off	$\text{ON} = 0\text{V}$, $V_{CC} = 4.4\text{V}$ to 16.5V	●		100	500	μA
I_{CC}	V_{CC} Supply Current Power On	$I_{CC2} = 0\text{mA}$, Figure 1	●		50	100	mA
	V_{BUS} Supply Current Power Off	$\text{ON} = 0\text{V}$	●		10	100	μA
I_{BUS}	V_{BUS} Supply Current Power On	$I_{VLO} = 0\text{mA}$, Figure 1	●		6	9	mA
	V_{BUS} Supply Current Suspend Mode	$\text{SPNDPWR} = 3.3\text{V}$ USB Suspend Timeout $\text{SPNDPWR} = 0$, USB Suspend Timeout	● ●			500	μA mA
V_{CC2}	Regulated V_{CC2} Output Voltage, Loaded	$V_{CC} = 4.4\text{V}$, $I_{CC2} = 200\text{mA}$, Figure 1	●	4.75	5	5.25	V
		$V_{CC} = 8.6\text{V}$, $I_{CC2} = 500\text{mA}$, Figure 1	●	4.75	5	5.25	V
	V_{CC2} Source Current High Power Mode	$V_{CC} = 8.6\text{V}$, Figure 1	●	500			mA
	V_{CC2} Source Current Bus Power Mode	$V_{CC} = V_{BUS} = 4.4\text{V}$, Figure 1	●	200			mA
V_{LO}	V_{LO} Regulated Output Voltage	$I_{VLO} = 0\text{mA}$ to 10mA , Figure 1	●	3.15	3.3	3.45	V
	V_{LO} Output Voltage Maximum Current	Figure 1	●			10	mA
V_{LO2}	V_{LO2} Regulated Output Voltage	$I_{VLO2} = 0\text{mA}$ to 10mA , Figure 1	●	3.15	3.3	3.45	V
	V_{LO2} Output Voltage Maximum Current	Figure 1	●			10	mA
USB Input Levels ($D1^+$, $D1^-$, $D2^+$, $D2^-$)							
V_{IH}	Single-Ended Input High Voltage	●		2.0			V
V_{IL}	Single-Ended Input Low Voltage	●				0.8	V
V_{HYS}	Single-Ended Input Hysteresis				200		mV
V_{DIFF}	Differential Input Sensitivity	$ (D1^+ - D1^-) $ or $ (D2^+ - D2^-) $	●	0.2			V
V_{CM}	Common Mode Voltage Range	$ (D1^+ + D1^-) /2$ or $ (D2^+ + D2^-) /2$	●	0.8		2.5	V
Logic Input Levels (ON, SPNDPWR)							
V_{IHL}	Logic Input High Voltage	●		2.0			V
V_{ILL}	Logic Input Low Voltage	●				0.8	V
I_{INL}	Logic Input Current	●				± 1	μA
V_{HYSL}	Logic Input Hysteresis				200		mV
USB Output Levels ($D1^+$, $D1^-$, $D2^+$, $D2^-$)							
V_{OL}	Output Low Voltage	$R_{PU} = 1.5\text{k}$ to 3.6V , Figure 4	●	0		0.3	V
V_{OH}	Output High Voltage	$R_{PD} = 15\text{k}$ to 0V , Figure 4	●	2.8		3.6	V
V_{CRS}	Differential Output Signal Cross-Point Voltage		●	1.3		2.0	V
Terminations							
R_{PU}	Bus Pull-Up Resistance on Upstream Facing Port	$D2^+$ or $D2^-$ Pull-Up to 3.3V		1.425		1.575	$\text{k}\Omega$
R_{PD}	Bus Pull-Down Resistance on Downstream Facing Port	$D2^+$ and $D2^-$ Pull-Down to GND2		14.25		15.75	$\text{k}\Omega$
Z_{DRV}	USB Driver Output Resistance	●		28		44	Ω
C_{INUSB}	USB Transceiver Pad Capacitance to GND	(Note 2)			10		pF

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC} = 5\text{V}$, $V_{BUS} = 5\text{V}$, $\text{GND} = \text{GND2} = 0\text{V}$, $\text{ON} = V_{LO}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Low Speed USB							
t _{LDR}	Low Speed Data Rate	C _L = 50pF to 450pF (Note 4)			1.5		Mbps
t _{LR}	Rise Time	Figure 2, C _L = 50pF to 600pF	●	75		300	ns
t _{LF}	Fall Time	Figure 2, C _L = 50pF to 600pF	●	75		300	ns
t _{LPRR} , t _{LPFF}	Propagation Delay	Figure 2, C _L = 50pF to 600pF	●		200	300	ns
t _{LDJ1}	Differential Jitter	To Next Transition (Note 2)				±45	ns
t _{LDJ2}	Differential Jitter	To Paired Transitions (Note 2)				± 15	ns
Full Speed USB							
t _{FDR}	Full Speed Data Rate	C _L = 50pF (Note 4)			12		Mbps
t _{FR}	Rise Time	Figure 3, C _L = 50pF	●	4		20	ns
t _{FF}	Fall Time	Figure 3, C _L = 50pF	●	4		20	ns
t _{FPRR} , t _{FPFF}	Propagation Delay	Figure 3, C _L = 50pF	●	60	80	115	ns
t _{FDJ1}	Differential Jitter	To Next Transition (Note 2)			2		ns
t _{FDJ2}	Differential Jitter	To Paired Transitions (Note 2)			1		ns
Power Supply Generator							
	V _{CC2} – GND2 Supply Start-Up Time (ON → V _{LO} , V _{CC2} to 4.5V)	R _{LOAD} = 50Ω, C _{LOAD} = 100μF R _{LOAD} = 10Ω, C _{LOAD} = 100μF, V _{CC} = 12V	● ●		2 3	5 10	ms ms
t _{WUSPND}	Wake Up from Suspend Mode	Resume Signal, SPNDPWR = 0	●		0.25	10	μs
ESD (HBM) (Note 2)	Isolation Barrier	GND to GND2			±15		kV
	D1 ⁺ , D1 [–] , D2 ⁺ , D2 [–]	D1 ⁺ /D1 [–] to GND, V _{CC} , V _{BUS} , or V _{LO} and D2 ⁺ /D2 [–] to GND2, V _{CC2} , or V _{LO2}			±15		kV
	ON, SPNDPWR				±3		kV

ISOLATION CHARACTERISTICS

$T_A = 25^\circ\text{C}$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Isolation Barrier: GND to GND2						
V_{ISO}	Rated Dielectric Insulation Voltage (Notes 6, 7)	1 Minute (Derived from 1 Second Test)	2500			V_{RMS}
		1 Second (Note 5)	3000			V_{RMS}
	Common Mode Transient Immunity	$V_{BUS} = V_{CC} = 5\text{V}$, $\text{ON} = 3.3\text{V}$, 1000V in 33ns Transient Between GND and GND2 (Note 2)	± 30			$\text{kV}/\mu\text{s}$
V_{IORM}	Maximum Working Insulation Voltage	(Notes 2, 5)	560 400			V_{PEAK} V_{RMS}
	Partial Discharge	$V_{PR} = 750V_{RMS}$ (Note 5)			<5	pC
CTI	Comparative Tracking Index	IEC 60112 (Note 2)	600			V_{RMS}
	Depth of Erosion	IEC 60112 (Note 2)		0.017		mm
DTI	Distance Through Insulation	(Note 2)		0.1		mm
	Input to Output Resistance	(Notes 2, 5)	10^{12}			Ω
	Input to Output Capacitance	(Notes 2, 5)		13		pF
	Creepage Distance	(Notes 2, 5)		9.48		mm

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design and not production tested.

Note 3: This μ Module transceiver includes over temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when over temperature protection is active. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

Note 4: Maximum data rate is guaranteed by other measured parameters and is not directly tested.

Note 5: Device considered a 2-terminal device. Measurement between groups of pins A1 through B11 shorted together and pins K1 through L11 shorted together.

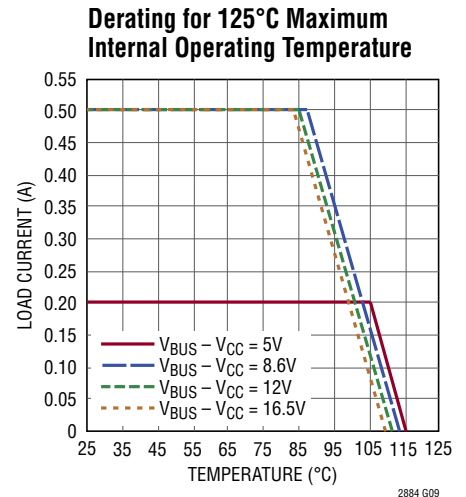
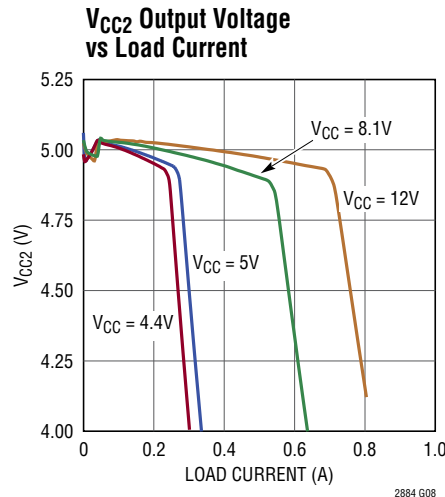
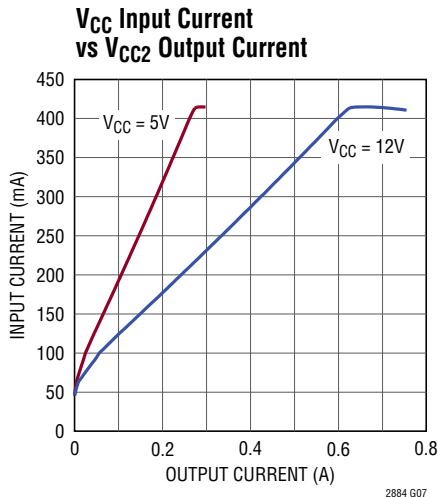
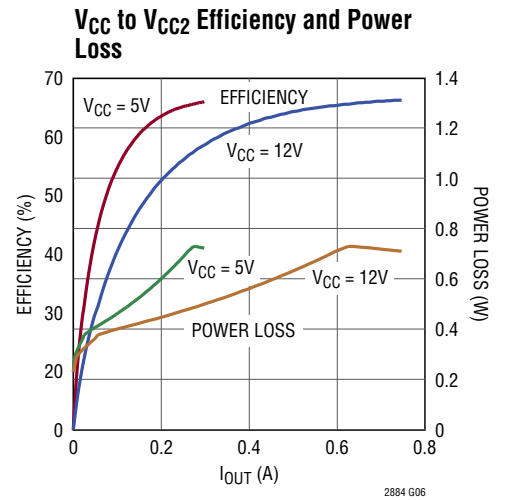
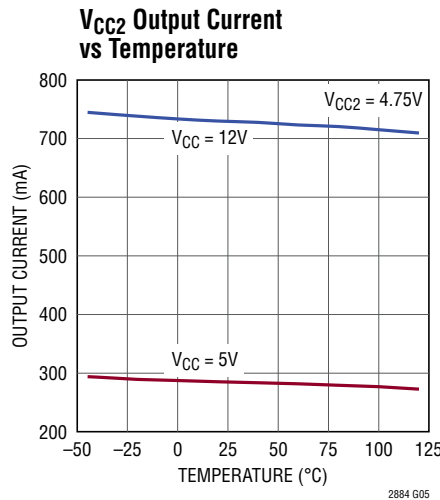
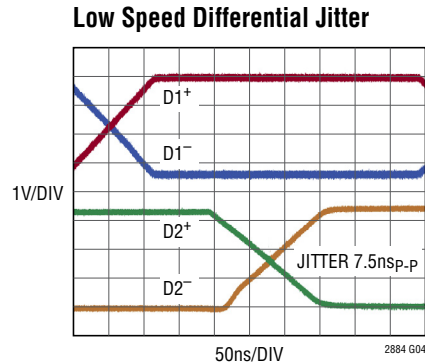
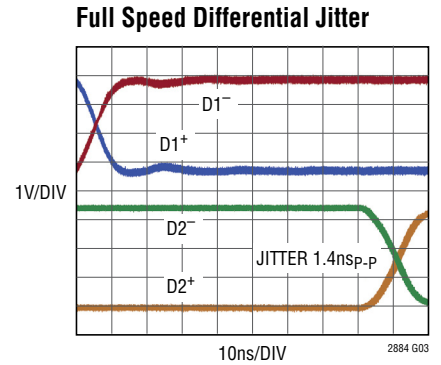
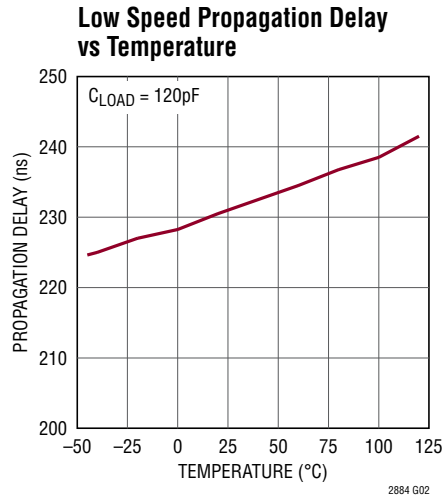
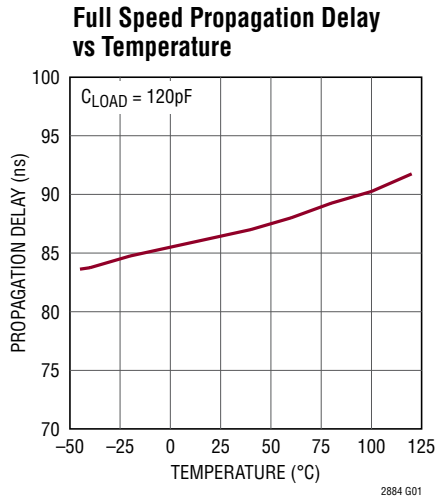
Note 6: The rated dielectric insulation voltage should not be interpreted as a continuous voltage rating.

Note 7: In accordance with UL1577, each device is proof tested for the 2500V_{RMS} rating by applying the equivalent positive and negative peak voltage multiplied by an acceleration factor of 1.2 for one second.

TYPICAL PERFORMANCE CHARACTERISTICS

ON = 3.3V, unless otherwise noted.

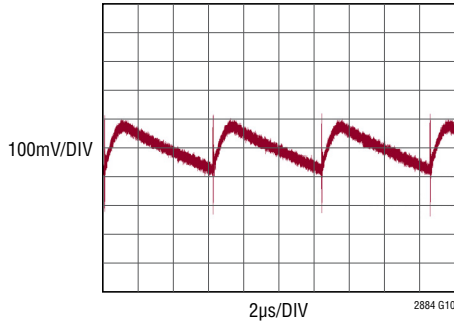
$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $V_{BUS} = 5\text{V}$, $\text{GND} = \text{GND2} = 0\text{V}$,



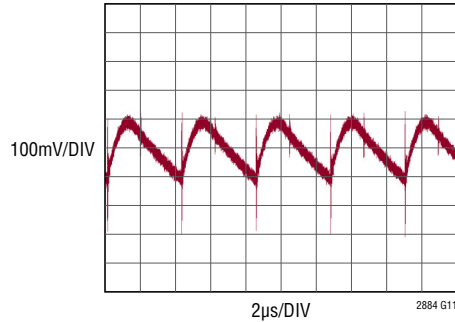
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $V_{BUS} = 5\text{V}$, $\text{GND} = \text{GND2} = 0\text{V}$,
 $\text{ON} = 3.3\text{V}$, unless otherwise noted.

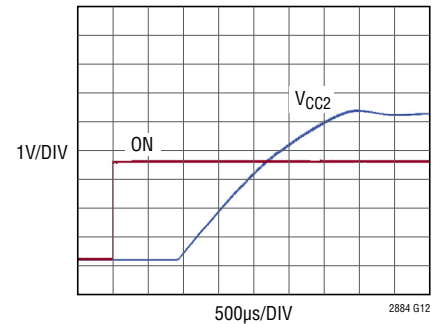
**V_{CC2} Ripple, $V_{CC} = 5\text{V}$,
 $I_{CC2} = 200\text{mA}$**



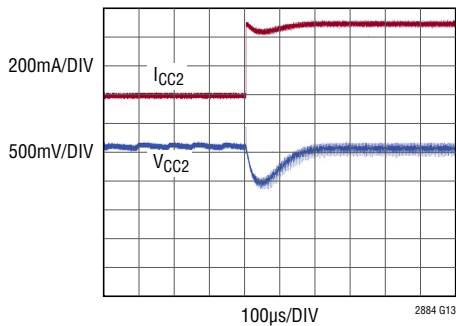
**V_{CC2} Ripple, $V_{CC} = 12\text{V}$,
 $I_{CC2} = 500\text{mA}$**



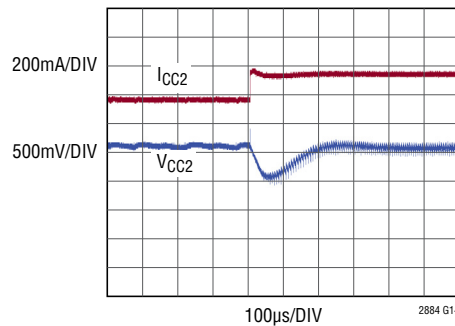
V_{CC2} Start-Up Ramp



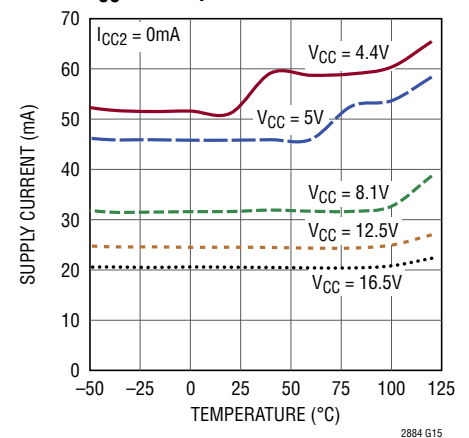
**V_{CC2} = Load Step Response,
 0mA to 500mA ($V_{CC} = 12\text{V}$)**



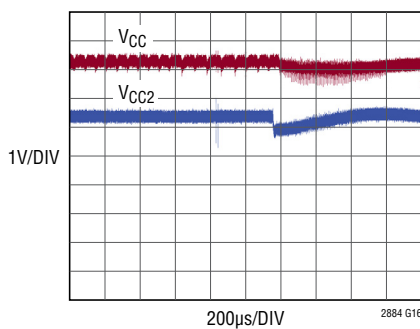
**V_{CC2} = Load Step Response,
 0mA to 200mA ($V_{CC} = 5\text{V}$)**



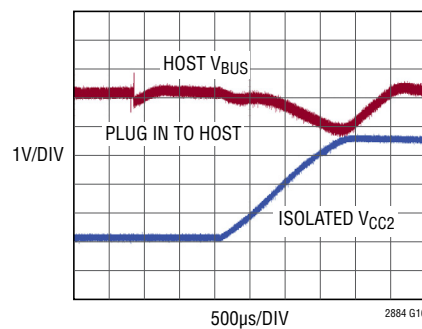
I_{CC} vs Temperature



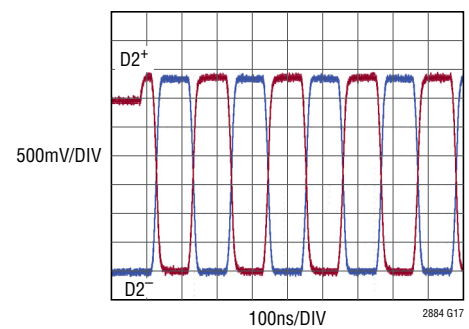
V_{CC2} Droop/Plug-In Response



**Upstream V_{BUS} Droop During
 Plug-In with $C_{LOAD} = 100\mu\text{F}$**



Full Speed Data Start of Packet



PIN FUNCTIONS

Upstream Side (V_{CC} , V_{BUS} , V_{LO} , GND)

D1⁻ (A1): USB Data Bus Upstream Facing Negative Transceiver Pin. A 1.5k pull-up resistor is automatically configured to indicate the idle condition of the D2⁻ pin.

D1⁺ (A2): USB Data Bus Upstream Facing Positive Transceiver Pin. A 1.5k pull-up resistor is automatically configured to indicate the idle condition of the D2⁺ pin.

SPNDPWR (A3): Suspend Power Control. A high input enables the DC/DC converter shutdown control if the USB bus is suspended. A low input (GND) disables the shutdown control to the DC/DC converter maintaining power to the isolated downstream side during suspend mode. The recovery time from suspend mode may be equivalent to the power supply start-up time if the DC/DC converter was shut down. The SPNDPWR pin is referenced to V_{LO} and GND.

ON (A4): Enable for Power and Data Communication Through the Isolation Barrier. If ON is high, the part is enabled. If ON is low, the upstream side is held in reset and the isolated side is unpowered by the DC/DC converter. The ON pin is referenced between V_{LO} and GND.

V_{LO} (A5): Internally Regulated 3.3V Logic Voltage Output. The V_{LO} pin is used as a positive reference for the ON and SPNDPWR pins and can source up to 10mA of surplus current. Internally bypassed to GND with 2.2 μ F. Output supply, no external connection necessary.

GND (A6, B1-B11): Upstream Circuit Ground.

V_{BUS} (A7): Voltage Supply Input to USB Transceiver. The operating range is 4.4V to 16.5V. Connect to the USB V_{BUS} supply or an external source. Internally bypassed to GND with 2.2 μ F.

V_{CC} (A8-A11): Voltage Supply Input to DC/DC Converter. The operating range is 4.4V to 16.5V. Connect to an external supply greater than 8.6V for 500mA on V_{CC2} , V_{BUS} must be connected to the external supply or USB power. Connect to the USB V_{BUS} for up to 200mA on V_{CC2} . Connect V_{CC} to V_{BUS} when the peripheral device has an external power source. Internally bypassed to GND with 4.7 μ F.

Isolated Downstream Side (V_{CC2} , V_{LO2} , GND2)

GND2 (K1-K11, L3, L4, L6, L7): Downstream Circuit Ground.

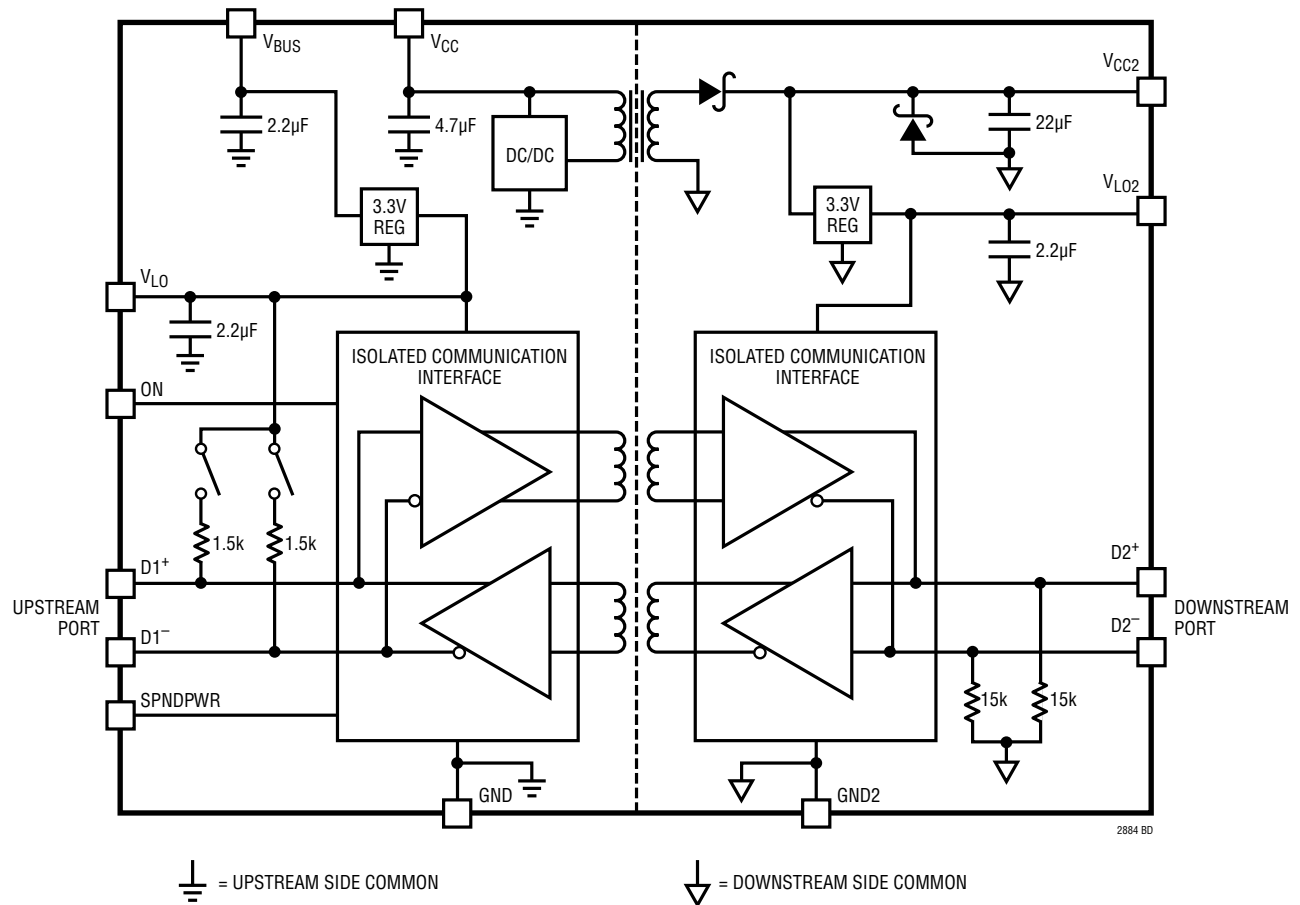
D2⁻ (L1): USB Data Bus Downstream Facing Negative Transceiver Pin. The pin has a 15k pull-down resistor to GND2.

D2⁺ (L2): USB Data Bus Downstream Facing Positive Transceiver Pin. The pin has a 15k pull-down resistor to GND2.

V_{LO2} (L5): Internally Regulated 3.3V Logic Voltage Output. The V_{LO2} pin can source up to 10mA of surplus current. Internally bypassed to GND2 with 2.2 μ F. Output supply, no external connection necessary.

V_{CC2} (L8-L11): Isolated Voltage Supply Output from DC/DC Converter. Output voltage is 5V and can support up to 500mA of peripheral device current referenced to GND2. Output current is dependant on input supply voltage and current limit. Internally bypassed to GND2 with 22 μ F. Output supply, no external connection necessary.

BLOCK DIAGRAM



TEST CIRCUITS

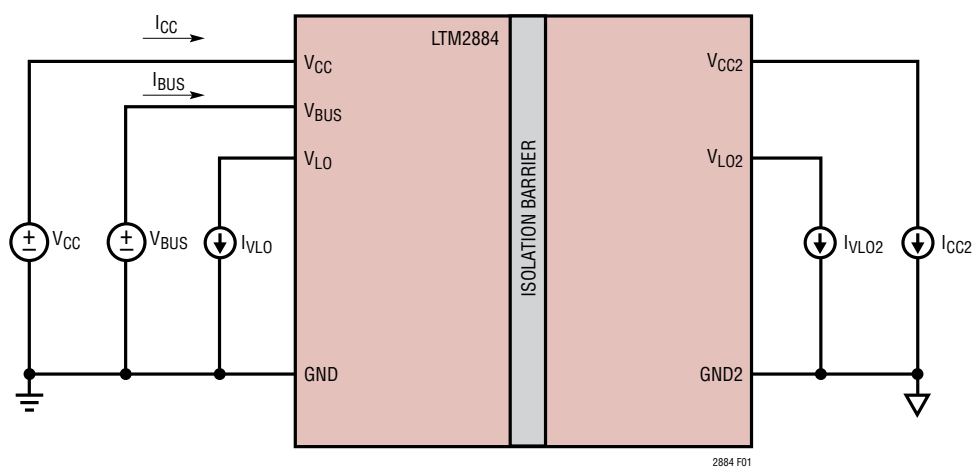


Figure 1. Power Supply Loads

TEST CIRCUITS

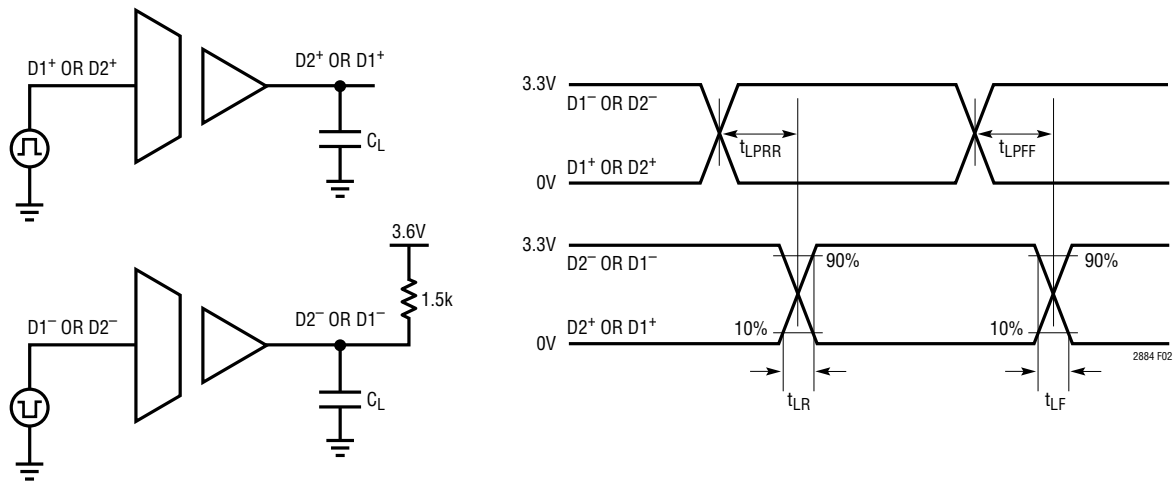


Figure 2. Low Speed Timing Measurements

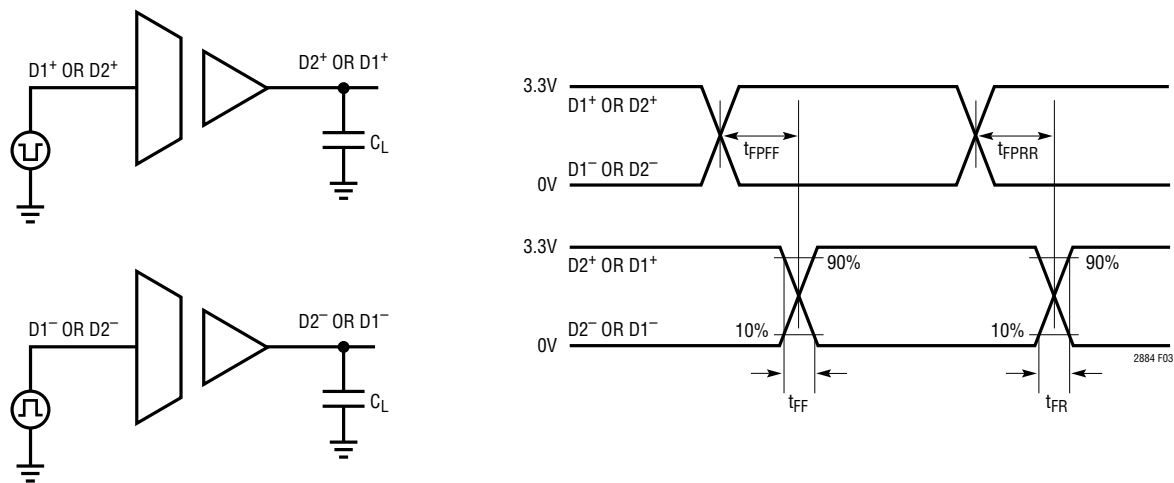


Figure 3. Full Speed Timing Measurements

FUNCTIONAL TABLE

USB Transceiver Functional Table

MODE	D1 ⁺	D1 ⁻	AUTOMATIC PULL-UP CONNECTION	D2 ⁺	D2 ⁻	SPNDPWR
Full Speed (Idle)	1.5k Pull-Up	Host Pull-Down	D1 ⁺	Peripheral Pull-Up	15k Pull-Down	X
Low Speed (Idle)	Host Pull-Down	1.5k Pull-Up	D1 ⁻	15k Pull-Down	Peripheral Pull-Up	X
Disconnected (Idle)	Host Pull-Down	Host Pull-Down	None	15k Pull-Down	15k Pull-Down	X
Suspend (Idle >3ms)	Set at Device Connect	Set at Device Connect	Set at Device Connect	Peripheral or 15k	Peripheral or 15k	0
Suspend No Power (Idle >3ms)	Set at Device Connect	Set at Device Connect	Set at Device Connect	15k Pull-Down	15k Pull-Down	3.3V
D1 to D2 Data	IN ⁺	IN ⁻	Set at Device Connect	OUT ⁺	OUT ⁻	X
D2 to D1 Data	OUT ⁺	OUT ⁻	Set at Device Connect	IN ⁺	IN ⁻	X

Power Functional Table

MODE	ON	SPNDPWR	V _{CC}	V _{BUS}	DC/DC CONVERTER
Off	0	X	X	X	OFF
On	3.3V	X	>4.4V	>4.4V	ON
On, Suspend (Idle >3ms)	3.3V	0	>4.4V	>4.4V	ON
On, Suspend (Idle >3ms), Power Off	3.3V	3.3V	>4.4V	>4.4V	OFF
On, USB Transceiver Only Power Off	3.3V	X	0	>4.4V	OFF

OPERATION

The LTM2884 μ Module transceiver provides a galvanically isolated robust USB interface, powered by an integrated, regulated DC/DC converter, complete with decoupling capacitors. This flexible device can support a variety of USB configurations, either bus powered or externally powered. Applications include isolation in hosts, hubs, peripherals, or standalone inline bus splitters. Automatically configured pull-up resistors are included to represent the condition of the isolated downstream USB bus to the upstream USB bus. The LTM2884 is ideal for use in USB connections where grounds between upstream hub/host and downstream devices can take on different voltages. Isolation in the LTM2884 blocks high voltage differences and eliminates ground loops and is extremely tolerant of common mode transients between ground potentials. Error free operation is maintained through common mode events exceeding 30kV/ μ s providing excellent noise isolation.

The LTM2884 contains a fully integrated DC/DC converter including the transformer, so that no external components are necessary in many configurations. The upstream side contains a flyback converter that regulates the downstream output voltage through primary sensing techniques. The internal power solution is sufficient to support the transceiver interface and supply up to 500mA at 5V through V_{CC2} to an attached device dependent on the supply voltage and available current on V_{CC} .

The integrated USB transceivers on both sides of the isolation barrier support full and low speed modes defined in the USB 2.0 specification. The communication through the isolation barrier for USB is bidirectional and as such the LTM2884 determines data flow direction based on which side a start of packet (SOP) begins first. The direction of data is maintained until an end of packet (EOP) pattern is observed or a timeout occurs due to a lack of activity. The USB interface maintains a consistent propagation delay representative of a hub delay and transfers all data.

Pull-up resistors integrated in the upstream interface automatically indicate device connections and disconnections. A downstream device connection automatically selects the proper pull-up resistor at the upstream facing port after sensing the idle state of the downstream device at connection time. Disconnection of a downstream device automatically releases the pull-up resistor on the upstream facing port allowing the upstream 15k pull-down resistors to pull the bus signals to a disconnect condition. This function makes the LTM2884 ideal for host, hub, bus splitter, or peripheral device integration.

Isolator μ Module Technology

The LTM2884 utilizes isolator μ Module technology to translate signals and power across an isolation barrier. Signals on either side of the barrier are encoded into pulses and translated across the isolation boundary using differential signaling through coreless transformers formed in the μ Module substrate. This system, complete with data refresh, error checking, safe shutdown on fail, and extremely high common mode immunity, provides a robust solution for bidirectional signal isolation. The μ Module technology provides the means to combine the isolated signaling with a USB transceiver and powerful isolated DC/DC converter in one small package.

USB Transceiver Pin Protection

The LTM2884 USB transceiver pins D1⁺, D1⁻, D2⁺, and D2⁻ have protection from ESD and short-circuit faults. The transceiver pins withstand ± 15 KV HBM ESD events. Overcurrent circuitry on the transceiver pins monitor fault conditions from D1⁺ and D1⁻ to GND, V_{LO} , or V_{BUS} and from D2⁺ and D2⁻ to GND2, V_{LO2} , or V_{CC2} . A current detection circuit disables the transceiver pin if the pin sinks about 40mA for greater than 600ns. The V_{LO} and V_{LO2} output supplies protect the USB transceiver pins from shorts to GND or GND2 respectively with a 40mA current limit.

APPLICATIONS INFORMATION

USB Connectivity

The LTM2884 μ Module transceiver connects directly to USB ports on the upstream side and the downstream side without the addition of external components. The transceiver passes through all data and does not act as a hub or intelligent device. The bus lines are monitored for idle conditions, start of packet, and end of packet conditions to properly maintain bus speed and data direction. The series resistance, pull-up, and pull-down resistors are built into the LTM2884. The upstream facing USB port contains automatically configured 1.5k pull-up resistors which are switched in or out based on the downstream side peripheral device configuration. This implementation allows upstream reporting of the downstream bus speed and connection/disconnection conditions. Built-in 15k pull-down resistors are included from the D2⁺ and D2⁻ signals to GND2 supporting the downstream bus configuration.

Monitoring the USB data pins, the LTM2884 detects a K-state to begin a data packet and set the data direction. The data is monitored for an end of packet signature and a finishing J-state before the bus is released. The data payload between the K-state and J-state is transferred through the LTM2884 isolator with a delay of approximately 80ns.

Idle State Communication and Automatic Speed Selection

The LTM2884 μ Module transceiver maintains the conditions of the USB bus idle state by monitoring the downstream side bus idle condition and refreshing the state across the isolation barrier at a consistent rate. Furthermore, the LTM2884 monitors the speed of the downstream peripheral once connected and sets its own operation to match. Figure 4 shows the abbreviated circuitry of the automatic monitoring and reporting of the bus speeds. The D2⁺ or D2⁻ signals are monitored for a connection to pull-ups on D2⁺ or D2⁻ and the result is processed as full speed or low speed, otherwise disconnect. The idle state is communicated to the upstream side through a refresh transmission. The switches SW1 or SW2 are controlled based on the received information. SW1 is closed if D2⁺ is detected to have a pull-up and D2⁻ was open. SW2 is closed if D2⁻ is detected to have a pull-up and D2⁺ was open. Both SW1 and SW2 are opened if the downstream USB bus is disconnected. During a USB suspend, the pull-up resistor will maintain the condition prior to detecting the suspend command.

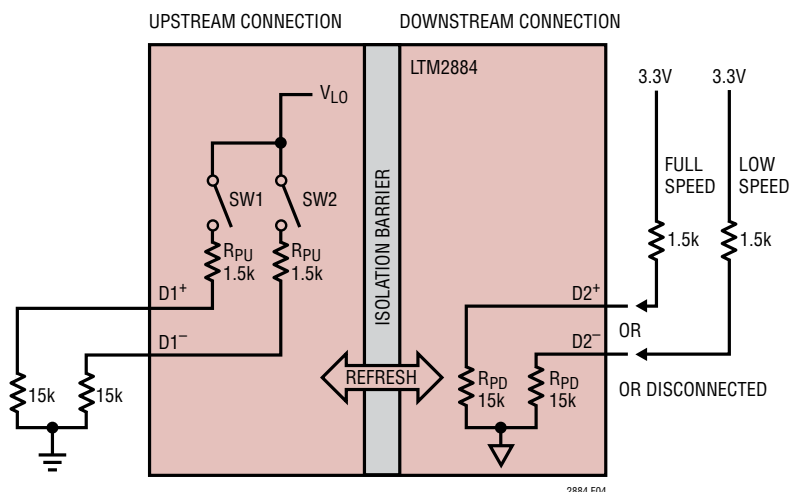


Figure 4. Idle State Automatic Resistor Setting

APPLICATIONS INFORMATION

Suspend Mode

When the upstream USB bus is idle for greater than 3ms, the LTM2884 enters suspend mode. The power savings and behavior in suspend mode depend on the state of the SPNDPWR pin, as summarized in Table 1.

Table 1. Suspend Mode Operation

SPNDPWR	V _{CC2}	I _{BUS}	I _{CC}	WAKE-UP	WAKE-UP TIME
High	Off	< 500μA	V _{CC} /45k	Resume	3ms
Low	On	1.5mA	50mA	Resume or Remote Wake-Up	10μs

The biggest power savings in suspend mode comes when SPNDPWR is high. In this case, the DC/DC converter is disabled, shutting down power to the isolated side, while the current draw on V_{CC} and V_{BUS} are minimized. However, in this mode, if a downstream device is connected or disconnected from the bus or remote wake-up functionality is configured, it will not be recognized by the LTM2884 and will not be relayed to the host. A resume command at the upstream side will wake up the LTM2884 and a re-numeration by the host will be required. Recovery time is about 3ms from the start of the resume command on the upstream side.

If SPNDPWR is low in suspend mode, the LTM2884 operates in a low power mode but maintains a higher functional state with the DC/DC converter on and the downstream transceiver powered. The V_{BUS} current is reduced to 1.5mA and V_{CC} current is about 50mA when there is no external draw on V_{CC2}. Wake-up is initiated with disconnects, reconnects, or a remote wake-up command from a downstream device or a resume command from the host. Recovery time from suspend mode is about 10μs from when the first state change is detected.

During suspend mode DC current drawn from V_{L0} into external circuits will be supplied from V_{BUS} and may exceed the limits set in the USB specification.

DC/DC Power Supply

The internal DC/DC converter converts the input power from the V_{CC} pin to the V_{CC2} output. The power delivered to the V_{CC2} pin is regulated and current limited to protect against overcurrent conditions. The voltage supply, V_{CC}, is sensed to limit the maximum current that can be delivered before USB specifications are exceeded. Connecting the V_{CC} and V_{BUS} supply pins to the USB V_{BUS} pin (4.4V to 5.5V) limits the maximum downstream side supply current to 200mA before V_{CC2} supply degradation. When V_{CC} is connected to a high voltage external DC source (8.6V to 16.5V) the current limit is increased so that 500mA is sourced from V_{CC2}. If a downstream device sinking current from V_{CC2} draws more than 25mA, the input current on V_{CC} may exceed 100mA, the USB single unit load specification for low power devices. The LTM2884 does not enforce a 100mA current limit for low power peripherals.

V_{CC2} is internally decoupled to GND2 with a 22μF capacitor. Add an additional low ESR 100μF capacitor to V_{CC2} to meet the V_{BUS} downstream supply decoupling minimum specification of 120μF when supporting device plug in. Locate the additional 100μF capacitor adjacent to the downstream USB connector. Additional capacitance may not be necessary when the LTM2884 is used in a peripheral device, or upstream hub application.

V_{L0} and V_{L02} Supplies

The V_{L0} and V_{L02} output supply pins are available for use as low current 3.3V supplies on both sides of the isolation barrier. They also serve as supplies for the USB interface circuitry. An internal linear regulator maintains 3.3V on V_{L0} from the V_{BUS} input supply. A separate linear regulator maintains 3.3V on V_{L02} from V_{CC2}. The current is limited to 10mA for external applications. Exceeding this limit may cause degradation in the V_{L0} or V_{L02} supplies and undesirable operation from the USB isolator. Connection of signals ON or SPNDPWR to V_{L0} will not cause a significant change in the available V_{L0} current. These supplies are available to support interface logic to the isolated USB port. In order to meet the suspend mode current limit, minimize the DC current of external applications on the V_{L0} output supply. V_{L0} and V_{L02} are protected from overcurrent and overtemperature conditions.

APPLICATIONS INFORMATION

Supply Current

Loading the multiple output supply pins of the LTM2884 affects the supply current on V_{BUS} and V_{CC} . The V_{BUS} input supplies current to the upstream side of the transceiver and to the V_{LO} pin. The V_{CC} input supplies power to V_{CC2} and V_{LO2} through an isolated DC/DC converter. The efficiency (η) of the DC/DC converter is shown in the Typical Performance Characteristics section for 5V and 12V inputs from V_{CC} to V_{CC2} .

Supply Current Equations

Operating:

$$I_{BUS} = 6mA + I_{VLO}$$

$$I_{CC} = \frac{V_{CC2} \cdot (6mA + I_{CC2} + I_{VLO2})}{\eta \cdot V_{CC}}$$

Suspend: SPNDPWR = 0

$$I_{BUS} = 1.5mA + I_{VLO}$$

$$I_{CC} = \frac{V_{CC2} \cdot (6mA + I_{CC2} + I_{VLO2})}{\eta \cdot V_{CC}}$$

Suspend: SPNDPWR = V_{LO}

$$I_{BUS} = 0.45mA + I_{VLO}$$

$$I_{CC} = \frac{V_{CC}}{45k}$$

Off:

$$I_{BUS} = 10\mu A$$

$$I_{CC} = \frac{V_{CC}}{45k}$$

USB 2.0 Compatibility

The LTM2884 μ Module transceiver is compatible with the USB 2.0 specification of full and low speed operation. Some characteristics and implementations may not support full compliance with the USB 2.0 specification. Three specific

cases exist within the LTM2884 μ Module transceiver and the integrated DC/DC power converter.

First, the propagation delay for full speed data of 80ns exceeds the specification for a single hub of 44ns plus the attached cable delay of 26ns. This is due to driving the signal to the 3.3V rail prior to a K-state transition to maintain balanced crossover voltages equivalent to the cross over voltages of the successive data transitions. USB ports commonly drive the idle state bus to the 3.3V rail prior to the k-state start of packet transition.

Second, setting SPNDPWR = V_{LO} will cause the DC/DC power converter to turn off during a bus suspend. V_{CC2} will lose power causing the downstream device to lose enumeration. Remote wake-up, disconnect, and reconnect events are ignored. A resume command from the host or upstream hub will start the DC/DC converter and wake up the downstream device. The downstream device will require re-enumeration, which causes a failure in USB compliance testing. After a resume command initiates, a delay of 3ms will elapse before the isolated device is fully powered. When SPNDPWR = 0V, the DC/DC power converter remains on during suspend, therefore power and enumeration information is retained. The V_{CC} supply consumes 50mA to support the isolated power during suspend. Separate the V_{BUS} and V_{CC} supplies to comply with the 2.5mA USB 2.0 V_{BUS} suspend current specification.

Third, when connecting a low power device to the downstream side of the LTM2884 and V_{BUS} and V_{CC} are connected together, the input current is higher due to the operating current and the efficiency of the DC/DC converter. The operating current of the DC/DC converter and the USB transceiver function is 46mA. The efficiency of the converter is approximately 55%, resulting in a 1/0.55 increase in the input current due to the load current on V_{CC2} . A 100mA load on V_{CC2} appears as a 181mA load + operating current at V_{BUS} and V_{CC} . In order to meet a 100mA input current, the V_{CC2} load current must be less than 25mA. This characteristic of an isolated supply may limit the use of the LTM2884 in bus powered hub applications or downstream connection to a bus powered hub. Connect V_{CC} to an external supply to mitigate this concern.

APPLICATIONS INFORMATION

Hot Plug Protection

The V_{CC} and V_{BUS} inputs are bypassed with low ESR ceramic capacitors. During a hot plug event, the supply inputs can overshoot the supplied voltage due to cable inductance. When using external power supply sources greater than 10V that can be hot plugged, add an additional 2.2 μ F tantalum capacitor with greater than 1 Ω of ESR, or a ceramic capacitor with a series 1 Ω resistor to the V_{CC} input to reduce the possibility of exceeding absolute maximum ratings. Refer to Application Note 88, "Ceramic Capacitors Can Cause Overvoltage Transients," for a detailed discussion of this problem.

PC Board Layout

The high integration of the LTM2884 makes PCB layout simple. However, to optimize its electrical isolation characteristics, EMI, and thermal performance, some layout considerations are necessary. The PCB layout in Figure 5 is a recommended configuration for a low EMI USB application. The following considerations optimize the performance of the LTM2884:

- Under loaded conditions, V_{CC} and GND current exceed 700mA, V_{CC2} and GND2 current is up to 500mA. Use sufficient copper on the PCB to ensure resistive losses do not cause the supply voltage to drop below the minimum allowed level. The heavy copper traces will also help to reduce thermal stress and improve thermal conductivity.
- Input and output decoupling is not required on peripheral or hub inputs. Add additional low ESR capacitance to reduce noise induction on the power supply connections. Hub/bus splitter outputs require an additional 100 μ F of low ESR capacitance.
- Do not place copper between the inner columns of pads on the top or bottom of the PCB. This area must remain open to withstand the rated isolation voltage and maintain the creepage distance.

RF, Magnetic Field Immunity

The isolator μ Module technology used within the LTM2884 has been independently evaluated, and successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3	Radiated, Radio-Frequency, Electromagnetic Field Immunity
EN 61000-4-8	Power Frequency Magnetic Field Immunity
EN 61000-4-9	Pulsed Magnetic Field Immunity

Tests were performed using an unshielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 2.

Table 2. Test Frequency Field Strength

EN 61000-4-3, Annex D, 80MHz to 1GHz	10V/m
1.4MHz to 2GHz	3V/m
2GHz to 2.7GHz	1V/m
EN 61000-4-8, Level 4 50Hz and 60Hz	30A/m
EN 61000-4-8, Level 5 60Hz	100A/m*
EN 61000-4-9, Level 5 Pulse	1000A/m

*Non IEC Method

EMI

Radiated emissions have been measured for the LTM2884 using a gigahertz transverse electromagnetic (GTEM) cell with and without a USB cable attached. The performance shown in Figure 6 was achieved with the layout structure in Figure 5. Results are corrected per IEC 61000-4-20.

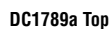


Figure 5. PC Board Layout

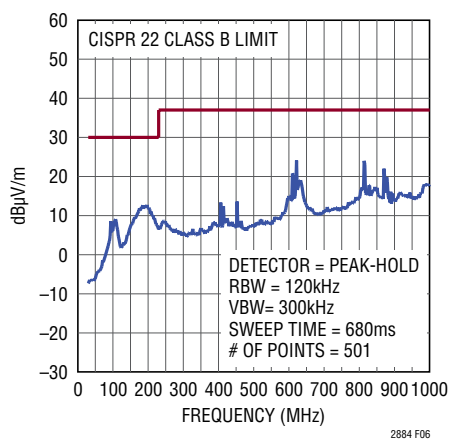


Figure 6. EMI Plot

TYPICAL APPLICATIONS

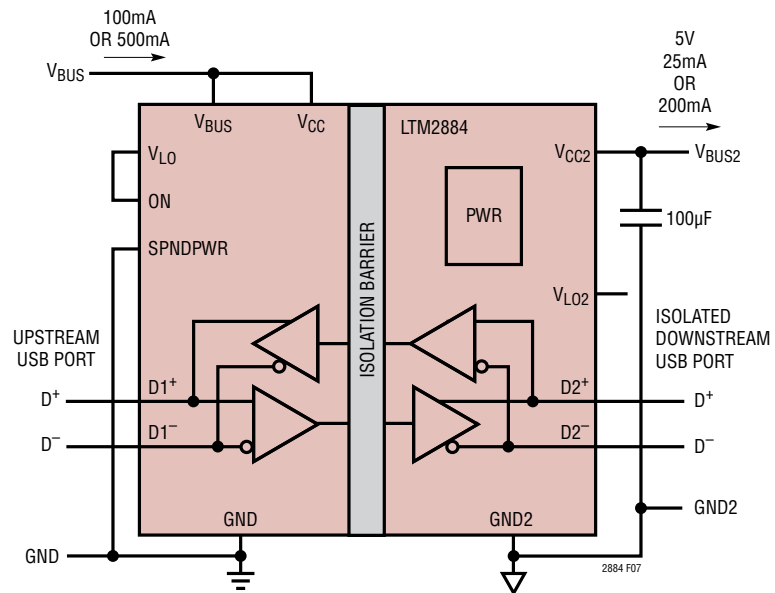


Figure 7. Bus Powered Inline Bus Splitter

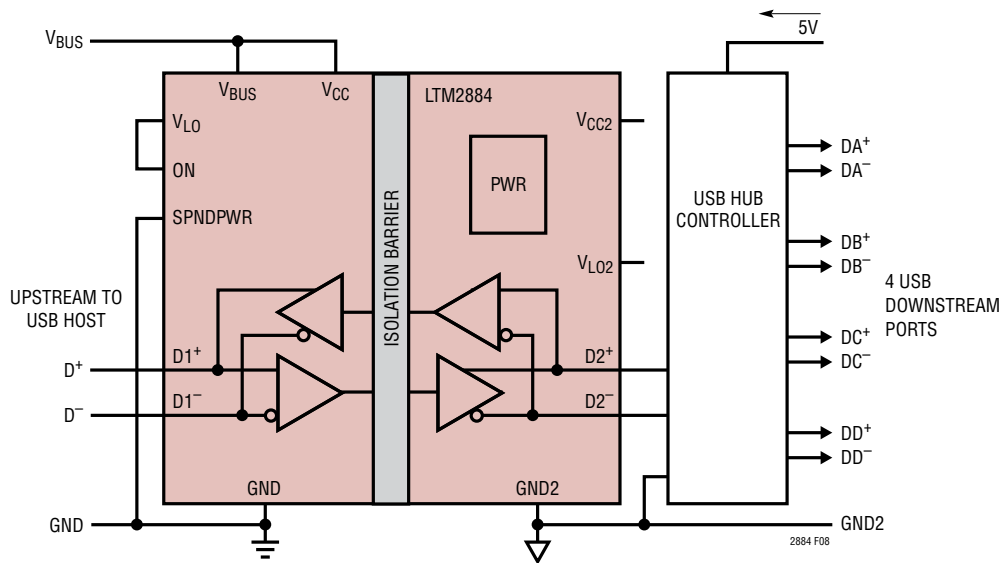


Figure 8. USB Hub Upstream Isolator

TYPICAL APPLICATIONS

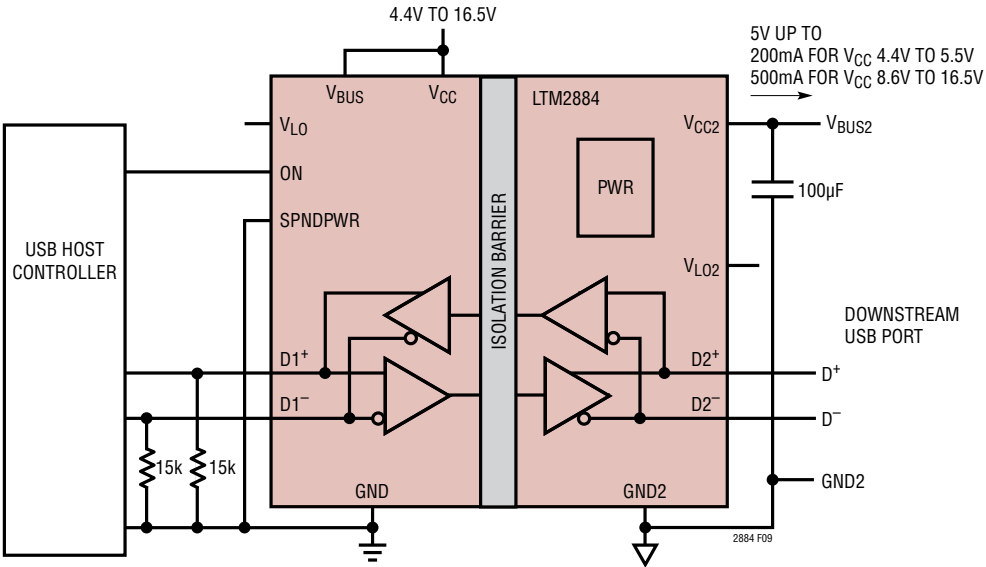


Figure 9. USB Host Integration

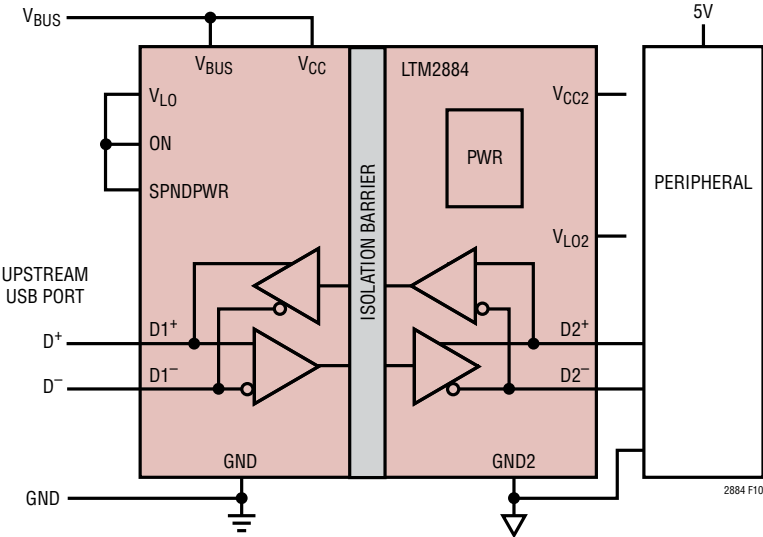


Figure 10. Powered Peripheral Device with USB Isolation and Low Current Suspend



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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/16	Added UL-CSA logo in Features list	1
B	11/16	Lowered Storage Temperature to -55°C	2



RELATED PARTS

2884fb