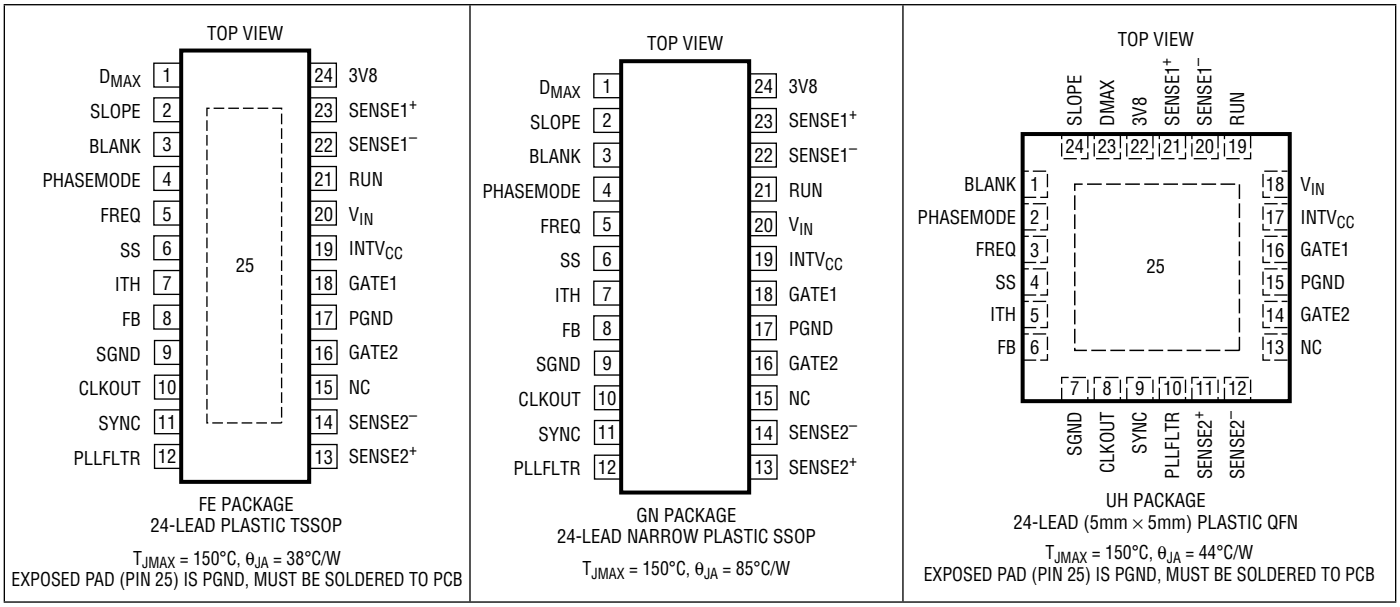
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Input Supply Voltage (V_{IN}) ..... –0.3V to 40V
$INTV_{CC}$ Voltage ..... –0.3V to 6V
$INTV_{CC}$ LDO RMS Output Current 50mA
RUN Voltage ..... –0.3V to 8V
SYNC Voltage..... –0.3V to 6V
SLOPE, PHASEMODE, D_{MAX},
BLANK Voltage..... –0.3V to V_{3V8}
$SENSE1^+$, $SENSE1^-$, $SENSE2^+$,
$SENSE2^-$ Voltage ..... –0.3V to V_{3V8}
SS, PLLFLTR Voltage ..... –0.3V to V_{3V8}
ITH Voltage ..... –0.3V to 2.7V
FB Voltage..... –0.3V to V_{3V8}
FREQ Voltage ..... –0.3V to 1.5V
Operating Junction Temperature Range (Notes 3, 4)
LTC3862E..... –40°C to 85°C
LTC3862I..... –40°C to 125°C
LTC3862H ..... –40°C to 150°C
Storage Temperature Range..... –65°C to 150°C
Reflow Peak Body Temperature ..... 260°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3862EFE#PBF	LTC3862EFE#TRPBF	3862FE	24-Lead Plastic TSSOP	–40°C to 85°C
LTC3862IFE#PBF	LTC3862IFE#TRPBF	3862FE	24-Lead Plastic TSSOP	–40°C to 125°C
LTC3862HFE#PBF	LTC3862HFE#TRPBF	3862FE	24-Lead Plastic TSSOP	–40°C to 150°C
LTC3862EGN#PBF	LTC3862EGN#TRPBF	LTC3862GN	24-Lead Plastic SSOP	–40°C to 85°C
LTC3862IGN#PBF	LTC3862IGN#TRPBF	LTC3862GN	24-Lead Plastic SSOP	–40°C to 125°C
LTC3862HGN#PBF	LTC3862HGN#TRPBF	LTC3862GN	24-Lead Plastic SSOP	–40°C to 150°C
LTC3862EUH#PBF	LTC3862EUH#TRPBF	3862	24-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C
LTC3862IUH#PBF	LTC3862IUH#TRPBF	3862	24-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3862HUH#PBF	LTC3862HUH#TRPBF	3862	24-Lead (5mm × 5mm) Plastic QFN	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

(Notes 2, 3) The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, RUN = 2V and SS = open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Input and $INTV_{CC}$ Linear Regulator							
V_{IN}	V_{IN} Supply Voltage Range			4		36	V
I_{VIN}	V_{IN} Supply Current Normal Mode, No Switching Shutdown	 (Note 5) V_{RUN} = 0V	 ● ●		 1.8 30	 3.0 80	 mA µA
$INTV_{CC}$	LDO Regulator Output Voltage			4.8	5.0	5.2	V
$dV_{INTVCC(LINE)}$	Line Regulation	6V < V_{IN} < 36V			0.002	0.02	%/V
$dV_{INTVCC(LOAD)}$	Load Regulation	Load = 0mA to 20mA		–2			%
V_{UVLO}	$INTV_{CC}$ UV^+ Voltage	Rising $INTV_{CC}$			3.3		V
	$INTV_{CC}$ UV^- Voltage	Falling $INTV_{CC}$			2.9		V
3V8	LDO Regulator Output Voltage				3.8		V
Switcher Control Loop							
V_{FB}	Reference Voltage	V_{ITH} = 0.8V (Note 6) E-Grade (Note 3) I-Grade and H-Grade (Note 3)	● ●	1.210 1.199	1.223 1.223	1.235 1.248	V V
dV_{FB}/dV_{IN}	Feedback Voltage V_{IN} Line Regulation	V_{IN} = 4V to 36V (Note 6)			±0.002	0.01	%/V
dV_{FB}/dV_{ITH}	Feedback Voltage Load Regulation	V_{ITH} = 0.5V to 1.2V (Note 6)			0.01	0.1	%
g_m	Transconductance Amplifier Gain	V_{ITH} = 0.8V (Note 6), ITH Pin Load = ±5µA			660		µMho
f_{0dB}	Error Amplifier Unity-Gain Crossover Frequency	(Note 7)			1.8		MHz
V_{ITH}	Error Amplifier Maximum Output Voltage (Internally Clamped)	V_{FB} = 1V, No Load			2.7		V
	Error Amplifier Minimum Output Voltage	V_{FB} = 1.5V, No Load			50		mV
I_{ITH}	Error Amplifier Output Source Current				–30		µA
	Error Amplifier Output Sink Current				30		µA
I_{FB}	Error Amplifier Input Bias Currents	(Note 6)			–50	–200	nA
$V_{ITH(PSKIP)}$	Pulse Skip Mode Operation ITH Pin Voltage	Rising ITH Voltage (Note 6) Hysteresis			0.275 25		V mV
$I_{SENSE(ON)}$	SENSE Pin Current				0.01	2	µA
$V_{SENSE(MAX)}$	Maximum Current Sense Input Threshold	V_{SLOPE} = Float, Low Duty Cycle (Note 3)	 ●	65 60	75 75	85 90	mV mV
$V_{SENSE(MATCH)}$	CH1 to CH2 Maximum Current Sense Threshold Matching	V_{SLOPE} = Float, Low Duty Cycle (Note 3) (V_{SENSE1} – V_{SENSE2})	●	–10		10	mV
RUN/Soft-Start							
I_{RUN}	RUN Source Current	V_{RUN} = 0V V_{RUN} = 1.5V			–0.5 –5		µA µA
V_{RUN}	High Level RUN Channel Enable Threshold				1.22		V
V_{RUNHYS}	RUN Threshold Hysteresis				80		mV
I_{SS}	SS Pull-Up Current	V_{SS} = 0V			–5		µA
R_{SS}	SS Pull-Down Resistance	V_{RUN} = 0V			10		kΩ
Oscillator							
f_{OSC}	Oscillator Frequency	R_{FREQ} = 45.6k R_{FREQ} = 45.6k	 ●	280 260	300 300	320 340	kHz kHz
	Oscillator Frequency Range		●	75		500	kHz
V_{FREQ}	Nominal FREQ Pin Voltage	R_{FREQ} = 45.6k			1.223		V

ELECTRICAL CHARACTERISTICS

(Notes 2, 3) The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, RUN = 2V and SS = open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SYNC}	SYNC Minimum Input Frequency	V_{SYNC} = External Clock	●			50	kHz
	SYNC Maximum Input Frequency	V_{SYNC} = External Clock	●	650			kHz
V_{SYNC}	SYNC Input Threshold	Rising Threshold			1.5		V
$I_{PLLFLTR}$	Phase Detector Sourcing Output Current	$f_{SYNC} > f_{OSC}$			–15		µA
	Phase Detector Sinking Output Current	$f_{SYNC} < f_{OSC}$			15		µA
CH1-CH2	Channel 1 to Channel 2 Phase Relationship	$V_{PHASEMODE}$ = 0V $V_{PHASEMODE}$ = Float $V_{PHASEMODE}$ = 3V8			180 180 120		Deg Deg Deg
CH1-CLKOUT	Channel 1 to CLKOUT Phase Relationship	$V_{PHASEMODE}$ = 0V $V_{PHASEMODE}$ = Float $V_{PHASEMODE}$ = 3V8			90 60 240		Deg Deg Deg
D_{MAX}	Maximum Duty Cycle	V_{DMAX} = 0V (Note 9) V_{DMAX} = Float V_{DMAX} = 3V8			96 84 75		% % %
$t_{ON(MIN)1}$	Minimum On-Time	V_{BLANK} = 0V (Note 8)			180		ns
$t_{ON(MIN)2}$	Minimum On-Time	V_{BLANK} = Float (Note 8)			260		ns
$t_{ON(MIN)3}$	Minimum On-Time	V_{BLANK} = 3V8 (Note 8)			340		ns
Gate Driver							
$R_{DS(ON)}$	Driver Pull-Up $R_{DS(ON)}$				2.1		Ω
	Driver Pull-Down $R_{DS(ON)}$				0.7		Ω
Overvoltage							
$V_{FB(OV)}$	V_{FB}, Overvoltage Lockout Threshold	$V_{FB(OV)} – V_{FB(NOM)}$ in Percent		8	10	12	%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: The LTC3862E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3862I is guaranteed over the full –40°C to 125°C operating junction temperature range and the LTC3862H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: Supply current in normal operation is dominated by the current needed to charge the external MOSFET gates. This current will vary with supply voltage and the external MOSFETs used.

Note 6: The IC is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage.

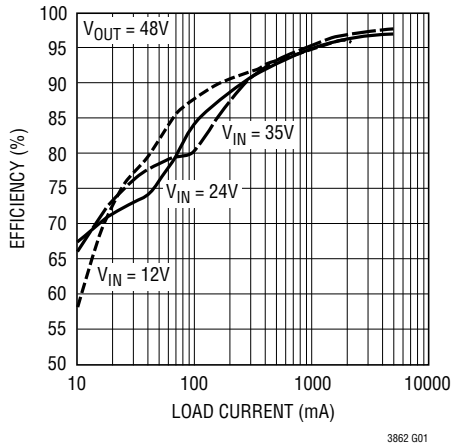
Note 7: Guaranteed by design, not subject to test.

Note 8: The minimum on-time condition is specified for an inductor peak-to-peak ripple current = 30% (see Minimum On-Time Considerations in the Applications Information section).

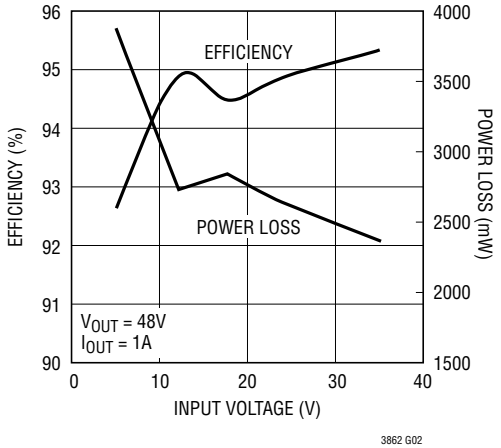
Note 9: The maximum duty cycle limit is derived from an internal clock that runs at 12x the programmed switching frequency. See the Applications Information for additional information.

TYPICAL PERFORMANCE CHARACTERISTICS

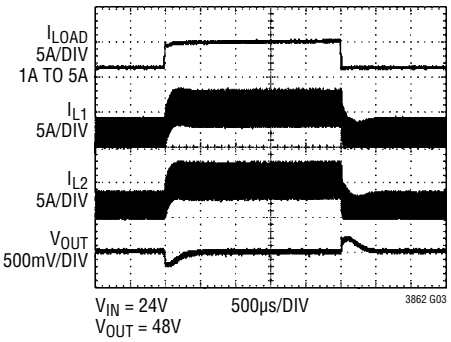
Efficiency vs Output Current



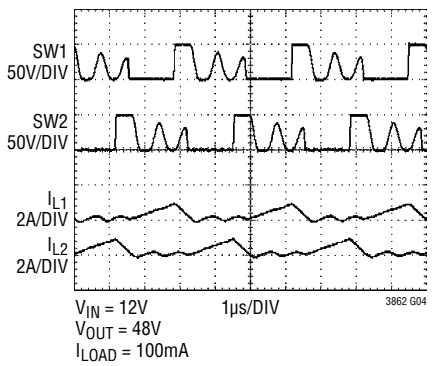
Efficiency and Power Loss vs Input Voltage



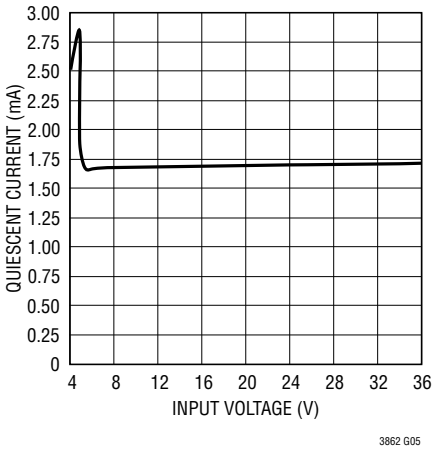
Load Step



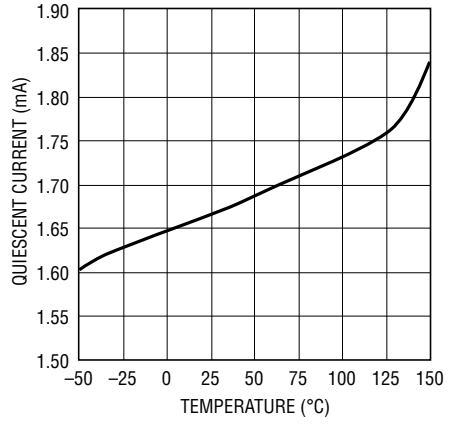
Inductor Current at Light Load



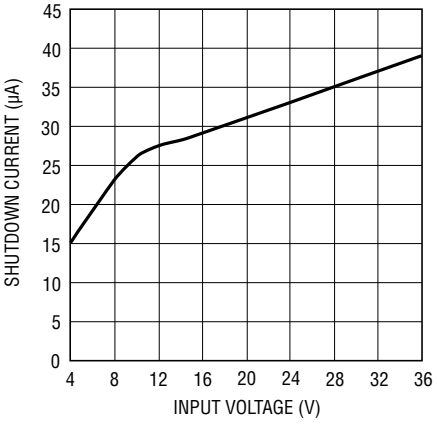
Quiescent Current vs Input Voltage



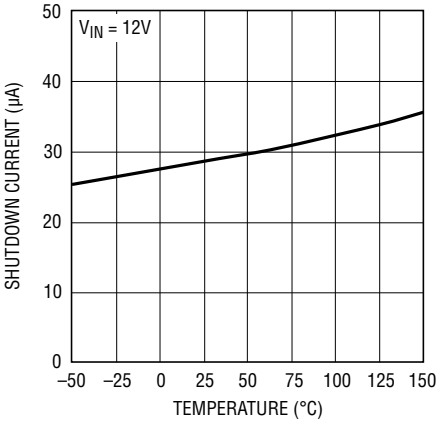
Quiescent Current vs Temperature



Shutdown Quiescent Current vs Input Voltage

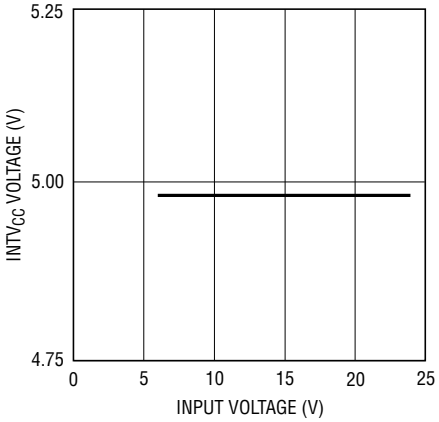


Shutdown Quiescent Current vs Temperature

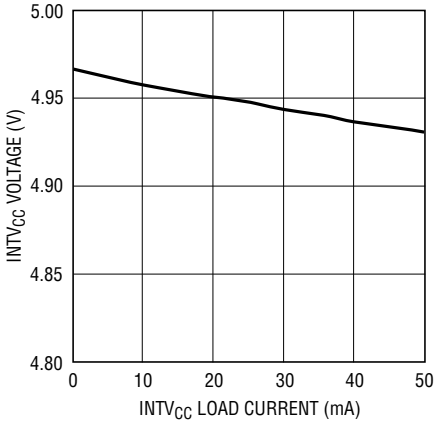


TYPICAL PERFORMANCE CHARACTERISTICS

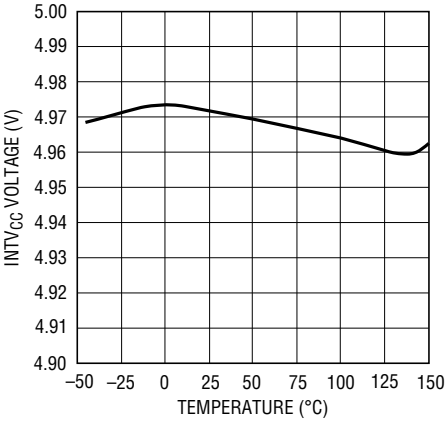
$INTV_{CC}$ Line Regulation



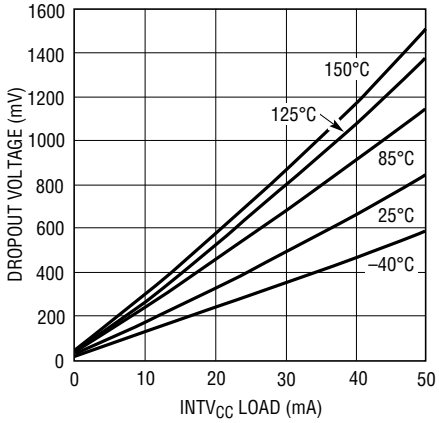
$INTV_{CC}$ Load Regulation



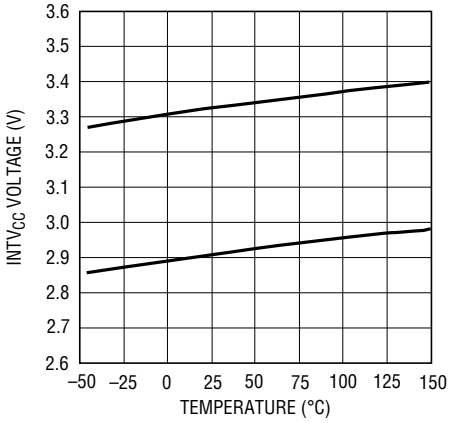
$INTV_{CC}$ vs Temperature



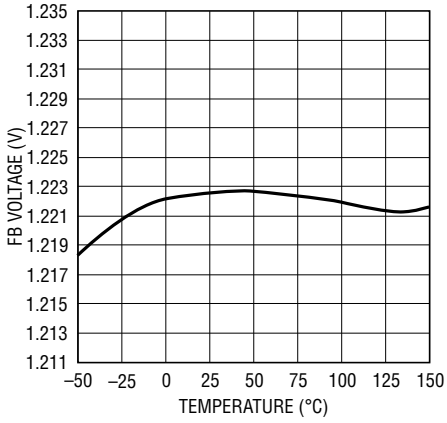
$INTV_{CC}$ LDO Dropout vs Load Current, Temperature



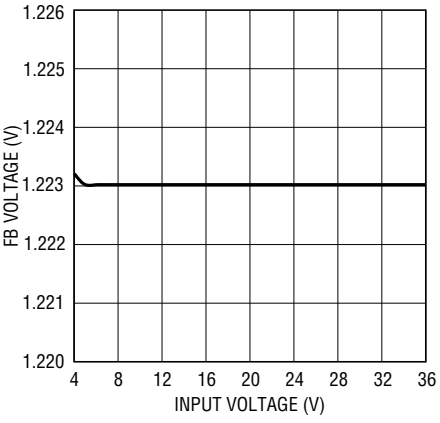
$INTV_{CC}$ UVLO Threshold vs Temperature



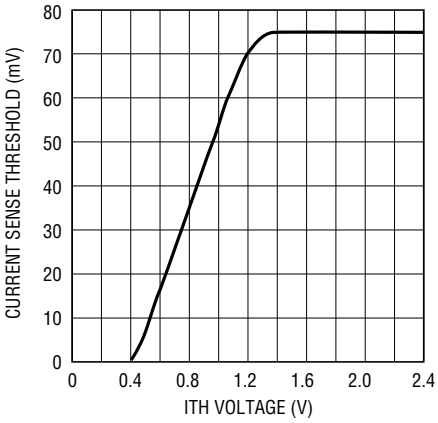
Feedback Voltage vs Temperature



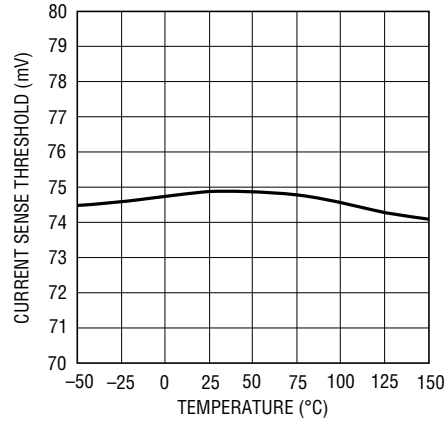
Feedback Voltage Line Regulation



Current Sense Threshold vs ITH Voltage

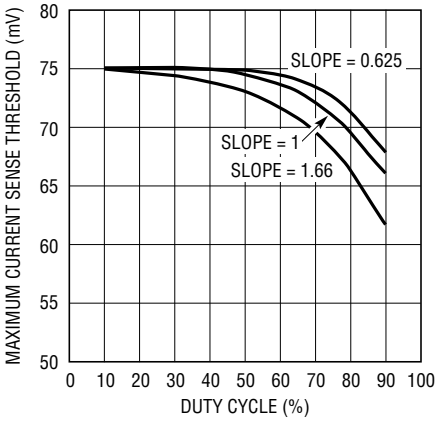


Current Sense Threshold vs Temperature



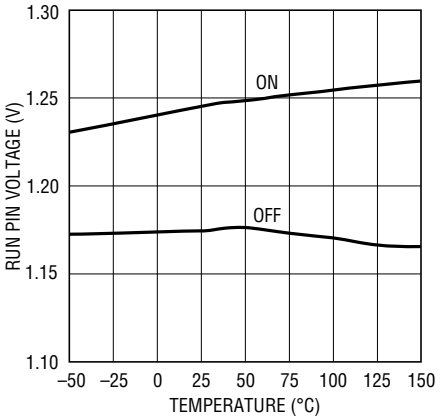
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Current Sense Threshold vs Duty Cycle



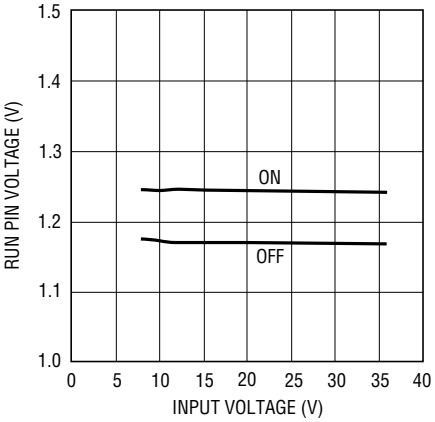
3862 G18

RUN Threshold vs Temperature



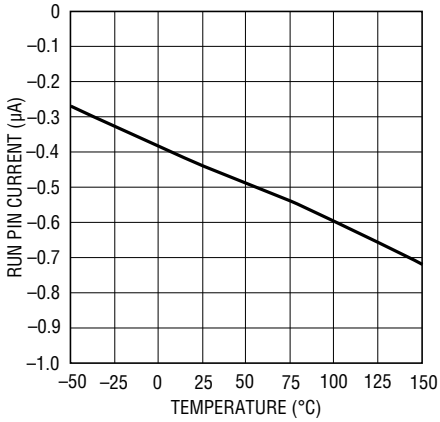
3862 G09

RUN Threshold vs Input Voltage



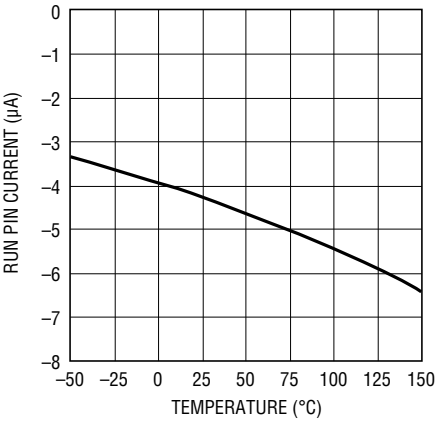
3862 G20

RUN (Off) Source Current vs Temperature



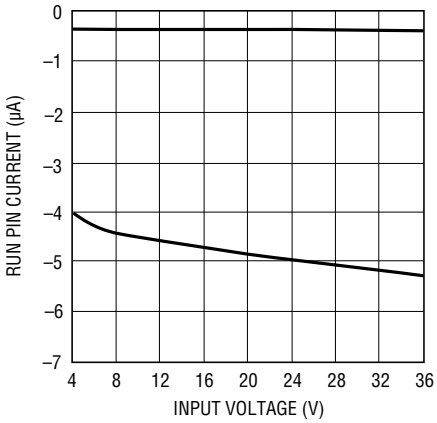
3862 G21vv

RUN (On) Source Current vs Temperature



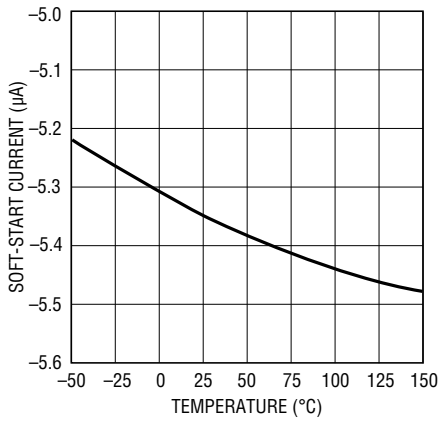
1344 G06

RUN Source Current vs Input Voltage



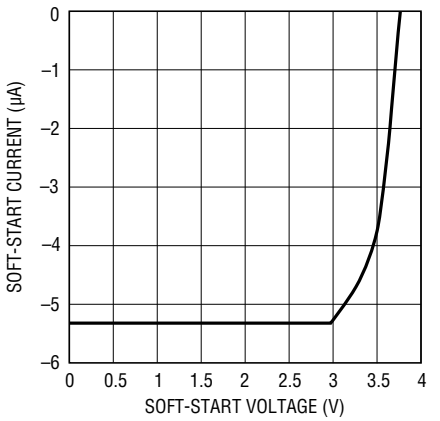
3862 G23

Soft-Start Current vs Temperature



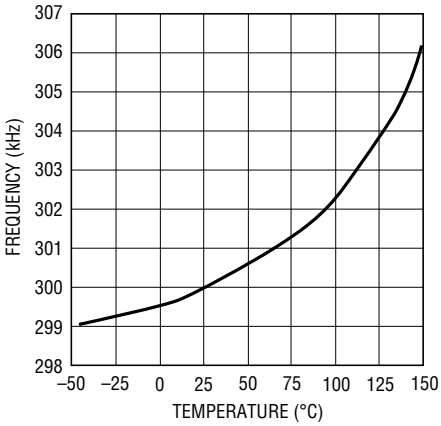
3862 G24

Soft-Start Current vs Soft-Start Voltage



3862 G25

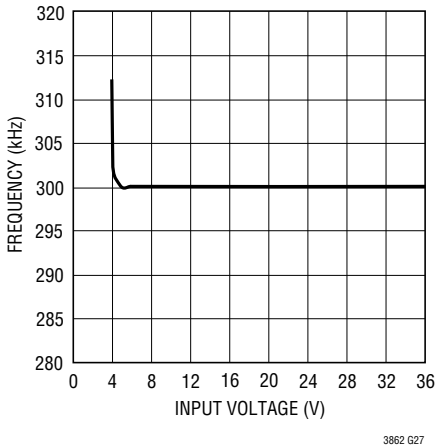
Oscillator Frequency vs Temperature



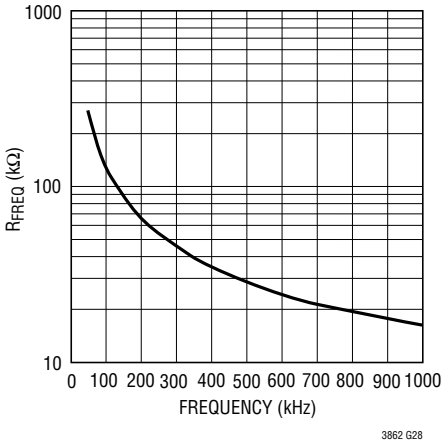
3862 G26

TYPICAL PERFORMANCE CHARACTERISTICS

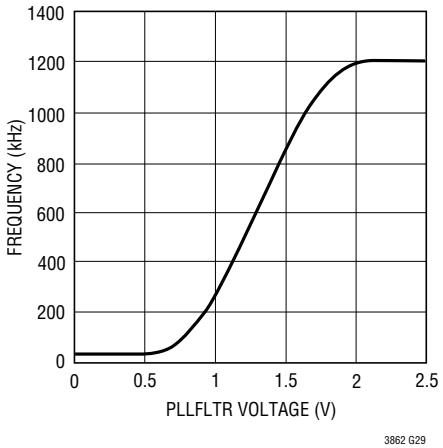
Oscillator Frequency vs Input Voltage



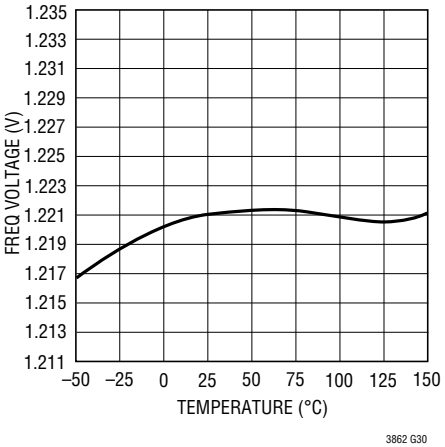
R_{FREQ} vs Frequency



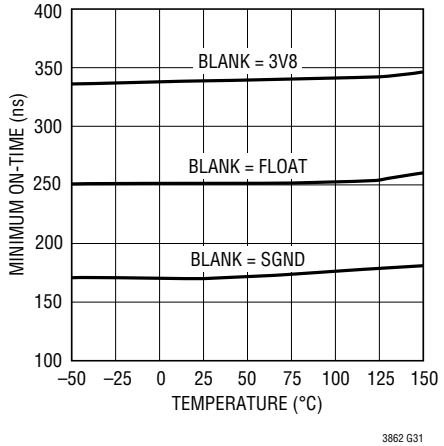
Frequency vs PLLFLTR Voltage



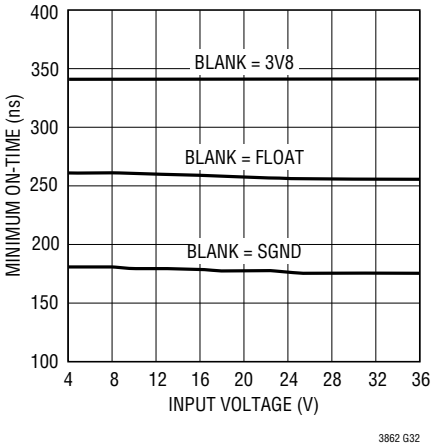
Frequency Voltage vs Temperature



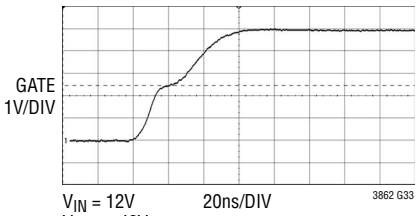
Minimum On-Time vs Temperature



Minimum On-Time vs Input Voltage

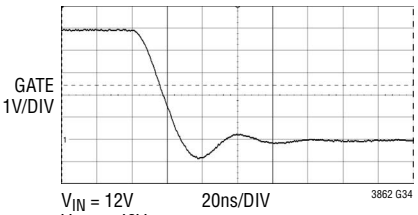


Gate Turn-On Waveform Driving Renesas HAT2266



V_{IN} = 12V 20ns/DIV
V_{OUT} = 48V
I_{OUT} = 1A
MOSFET RENESAS HAT2266

Gate Turn-Off Waveform Driving Renesas HAT2266



V_{IN} = 12V 20ns/DIV
V_{OUT} = 48V
I_{OUT} = 1A
MOSFET RENESAS HAT2266

PIN FUNCTIONS (SSOP/QFN/TSSOP)

3V8 (Pin 24/Pin 22/Pin 24): Output of the Internal 3.8V LDO from $INTV_{CC}$. Supply pin for the low voltage analog and digital circuits. A low ESR 1nF ceramic bypass capacitor should be connected between 3V8 and SGND, as close as possible to the IC.

BLANK (Pin 3/Pin 1/Pin 3): Blanking Time. Floating this pin provides a nominal minimum on-time of 260ns. Connecting this pin to 3V8 provides a minimum on-time of 340ns, while connecting it to SGND provides a minimum on-time of 180ns.

CLKOUT (Pin 10/Pin 8/Pin 10): Digital Output Used for Daisy-Chaining Multiple LTC3862 ICs in Multi-Phase Systems. The PHASEMODE pin voltage controls the relationship between CH1 and CH2 as well as between CH1 and CLKOUT.

D_{MAX} (Pin 1/Pin 23/Pin 1): Maximum Duty Cycle. This pin programs the maximum duty cycle. Floating this pin provides 84% duty cycle. Connecting this pin to 3V8 provides 75% duty cycle, while connecting it to SGND provides 96% duty cycle. The maximum duty cycle is derived from an internal clock that runs at 12x the programmed switching frequency. As a result, the maximum duty cycle limit D_{MAX} is extremely precise.

FB (Pin 8/Pin 6/Pin 8): Error Amplifier Input. The FB pin should be connected through a resistive divider network to V_{OUT} to set the output voltage.

FREQ (Pin 5/Pin 3/Pin 5): A resistor from FREQ to SGND sets the operating frequency.

GATE1 (Pin 18/Pin 16/Pin 18): Gate Drive Output. The LTC3862 provides a 5V gate drive referenced to PGND to drive a logic-level threshold MOSFET. The gate pin is rated for an absolute maximum voltage of –0.3V minimum and 6V maximum.

GATE2 (Pin 16/Pin 14/Pin 16): Gate Drive Output. The LTC3862 provides a 5V gate drive referenced to PGND to drive a logic-level threshold MOSFET. The gate pin is rated for an absolute maximum voltage of –0.3V minimum and 6V maximum.

$INTV_{CC}$ (Pin 19/Pin 17/Pin 19): Output of the Internal 5V Low Dropout Regulator (LDO). A low ESR 4.7µF (X5R or better) ceramic bypass capacitor should be connected between $INTV_{CC}$ and PGND, as close as possible to the IC.

ITH (Pin 7/Pin 5/Pin 7): Error Amplifier Output. The current comparator trip threshold increases with the ITH control voltage. The ITH pin is also used for compensating the control loop of the converter.

PGND (Pin 17/Pin 15, Exposed Pad Pin 25/Pin 17, Exposed Pad Pin 25): Power Ground. Connect this pin close to the sources of the power MOSFETs. PGND should also be connected to the negative terminals of V_{IN} and $INTV_{CC}$ bypass capacitors. PGND is electrically isolated from the SGND pin. The Exposed Pad of the FE and QFN packages is connected to PGND and must be soldered to PCB ground for electrical contact and rated thermal performance.

PHASEMODE (Pin 4/Pin 2/Pin 4): The PHASEMODE pin voltage programs the phase relationship between CH1 and CH2 rising gate signals, as well as the phase relationship between CH1 gate signal and CLKOUT. Floating this pin or connecting it to either 3V8, or SGND changes the phase relationship between CH1, CH2 and CLKOUT.

PLLFLTR (Pin 12/Pin 10/Pin 12): PLL Lowpass Filter Input. When synchronizing to an external clock, this pin serves as the lowpass filter input for the PLL. A series resistor and capacitor connected from PLLFLTR to SGND compensate the PLL feedback loop.

RUN (Pin 21/Pin 19/Pin 21): Run Control Input. A voltage above 1.22V on the pin turns on the IC. Forcing the pin below 1.22V causes the IC to shut down. There is a 0.5µA pull-up current for this pin. Once the RUN pin raises above 1.22V, an additional 4.5µA pull-up current is added to the pin for programmable hysteresis.

$SENSE1^+$ (Pin 23/Pin 21/Pin 23): Positive Inputs to the Current Comparators. The ITH pin voltage programs the current comparator offset in order to set the peak current trip threshold. This pin is normally connected to a sense resistor in the source of the power MOSFET.

PIN FUNCTIONS (SSOP/QFN/TSSOP)

SENSE2$^+$ (Pin 13/Pin 11/Pin 13): Positive Inputs to the Current Comparators. The ITH pin voltage programs the current comparator offset in order to set the peak current trip threshold. This pin is normally connected to a sense resistor in the source of the power MOSFET.

SENSE1$^-$ (Pin 22/Pin 20/Pin 22): Negative Inputs to the Current Comparators. This pin is normally connected to the bottom of the sense resistor.

SENSE2$^-$ (Pin 14/Pin 12/Pin 14): Negative Inputs to the Current Comparators. This pin is normally connected to the bottom of the sense resistor.

SGND (Pin 9/Pin 7/Pin 9): Signal Ground. All feedback and soft-start connections should return to SGND. For optimum load regulation, the SGND pin should be kelvin connected to the PCB location between the negative terminals of the output capacitors.

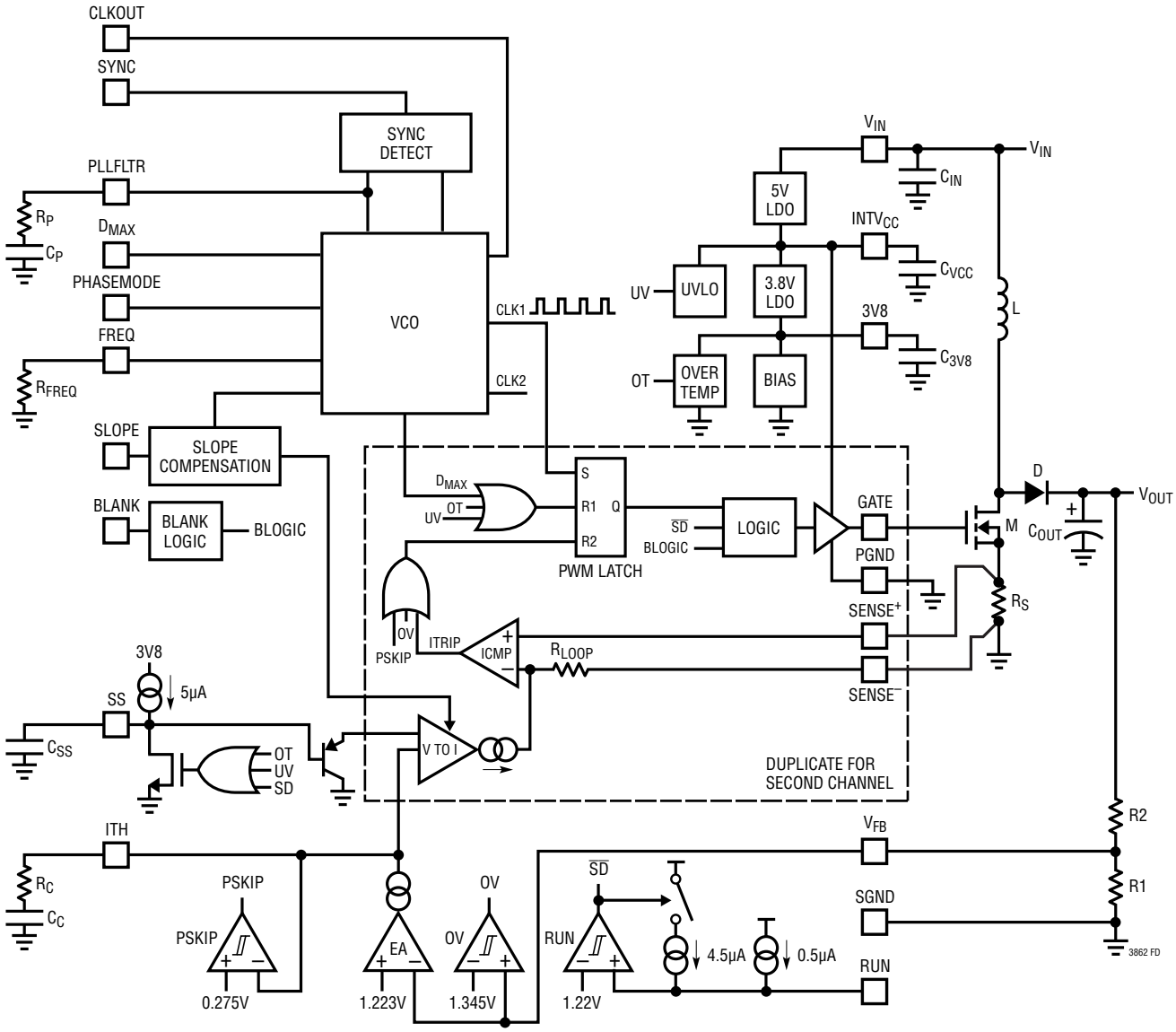
SLOPE (Pin 2/Pin 24/Pin 2): This pin programs the gain of the internal slope compensation. Floating this pin provides a normalized slope compensation gain of 1.00. Connecting this pin to 3V8 increases the normalized slope compensation by 66%, and connecting it to SGND decreases the normalized slope compensation by 37.5%. See Applications Information for more details.

SS (Pin 6/Pin 4/Pin 6): Soft-Start Input. For soft-start operation, connecting a capacitor from this pin to SGND will clamp the output of the error amp. An internal 5µA current source will charge the capacitor and set the rate of increase of the peak switch current of the converter.

SYNC (Pin 11/Pin 9/Pin 11): PLL Synchronization Input. Applying an external clock between 50kHz and 650kHz will cause the operating frequency to synchronize to the clock. SYNC is pulled down by a 50k internal resistor. The rising edge of the SYNC input waveform will align with the rising edge of GATE1 in closed-loop operation. A SYNC signal with an amplitude greater than 1.6V is considered an active high, while any signal below 0.9V is considered an active low.

V_{IN} (Pin 20/Pin 18/Pin 20): Main Supply Input. A low ESR ceramic capacitor should be connected between this pin and SGND.

FUNCTIONAL DIAGRAM



OPERATION

The Control Loop

The LTC3862 uses a constant frequency, peak current mode step-up architecture with its two channels operating 180 degrees out of phase. During normal operation, each external MOSFET is turned on when the clock for that channel sets the PWM latch, and is turned off when the main current comparator, ICMP, resets the latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier compares the output feedback signal at the V_{FB} pin to the internal 1.223V reference and generates an error signal at the ITH pin. When the load current increases it causes a slight decrease in V_{FB} relative to the reference voltage, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current. After the MOSFET is turned off, the inductor current flows through the boost diode into the output capacitor and load, until the beginning of the next clock cycle.

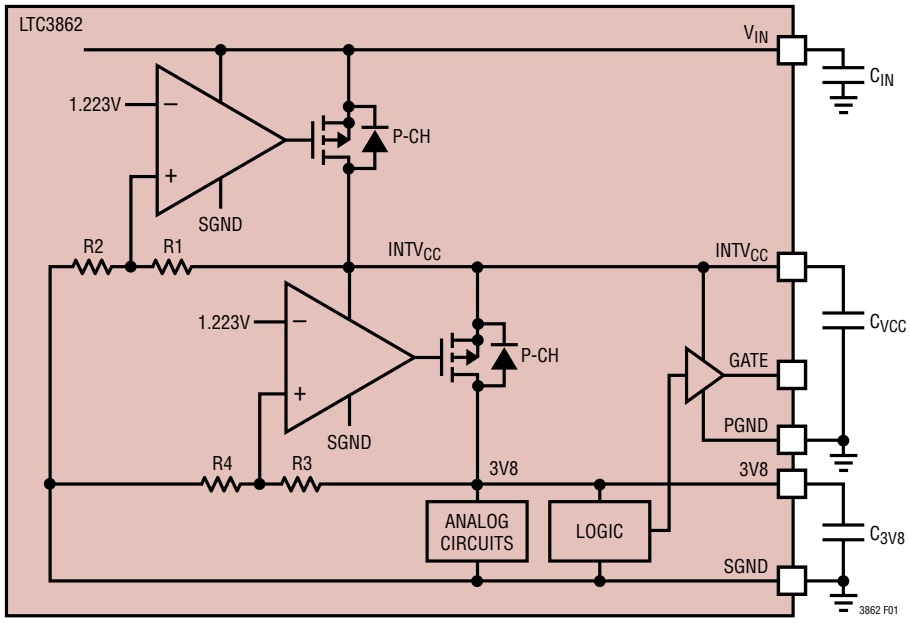
Cascaded LDOs Supply Power to the Gate Driver and Control Circuitry

The LTC3862 contains two cascaded PMOS output stage low dropout voltage regulators (LDOs), one for the gate drive supply ($INTV_{CC}$) and one for the low voltage analog and digital control circuitry (3V8). A block diagram of this power supply arrangement is shown in Figure 1.

The Gate Driver Supply LDO ($INTV_{CC}$)

The 5V output ($INTV_{CC}$) of the first LDO is powered from V_{IN} and supplies power to the power MOSFET gate drivers. The $INTV_{CC}$ pin should be bypassed to PGND with a minimum of 4.7µF of ceramic capacitance (X5R or better), placed as close as possible to the IC pins. If two power MOSFETs are connected in parallel for each channel in order to increase the output power level, or if a single MOSFET with a Q_G greater than 50nC is used, then it is recommended that the bypass capacitance be increased to a minimum of 10µF.

An undervoltage lockout (UVLO) circuit senses the $INTV_{CC}$ regulator output in order to protect the power MOSFETs from operating with inadequate gate drive. For the LTC3862 the rising UVLO threshold is typically 3.3V and the hysteresis is typically 400mV. The LTC3862 was optimized for logic-level power MOSFETs and applications where the output voltage is less than 50V to 60V. For applications requiring standard threshold power MOSFETs, please refer to the LTC3862-1 data sheet.



NOTE: PLACE C_{VCC} AND C_{3V8} CAPACITORS AS CLOSE AS POSSIBLE TO DEVICE PINS

Figure 1. Cascaded LDOs Provide Gate Drive and Control Circuitry Power

OPERATION

In multi-phase applications, all of the FB pins are connected together and all of the error amplifier output pins (ITH) are connected together. **The $INTV_{CC}$ pins, however, should not be connected together.** The $INTV_{CC}$ regulator is capable of sourcing current but is not capable of sinking current. As a result, when two or more $INTV_{CC}$ regulator outputs are connected together, the highest voltage regulator supplies all of the gate drive and control circuit current, and the other regulators are off. This would place a thermal burden on the highest output voltage LDO and could cause the maximum die temperature to be exceeded. In multi-phase LTC3862 applications, each $INTV_{CC}$ regulator output should be independently bypassed to its respective PGND pin as close as possible to each IC.

The Low Voltage Analog and Digital Supply LDO (3V8)

The second LDO within the LTC3862 is powered off of $INTV_{CC}$ and serves as the supply to the low voltage analog and digital control circuitry, as shown in Figure 1. The output voltage of this LDO (which also has a PMOS output device) is 3.8V. Most of the analog and digital control circuitry is powered from the internal 3V8 LDO. The 3V8 pin should be bypassed to SGND with a 1nF ceramic capacitor (X5R or better), placed as close as possible to the IC pins. This LDO is not intended to be used as a supply for external circuitry.

Thermal Considerations and Package Options

The LTC3862 is offered in two package options. The 5mm × 5mm QFN package (UH24) has a thermal resistance $R_{TH(JA)}$ of 34°C/W, the 24-pin TSSOP (FE24) package has a thermal resistance of 38°C/W, and the 24-pin SSOP (GN24) package has a thermal resistance of 85°C/W. The QFN and TSSOP package options have a lead pitch of 0.65mm, and the GN24 option has a lead pitch of 0.025in.

The $INTV_{CC}$ regulator can supply up to 50mA of total current. As a result, care must be taken to ensure that the maximum junction temperature of the IC is never exceeded. The junction temperature can be estimated using the following equations:

$$I_{Q(TOT)} = I_Q + Q_{G(TOT)} \bullet f$$

$$P_{DISS} = V_{IN} \bullet (I_Q + Q_{G(TOT)} \bullet f)$$

$$T_J = T_A + P_{DISS} \bullet R_{TH(JA)}$$

The total quiescent current ($I_{Q(TOT)}$) consists of the static supply current (I_Q) and the current required to charge the gate capacitance of the power MOSFETs. The value of $Q_{G(TOT)}$ should come from the plot of V_{GS} vs Q_G in the Typical Performance Characteristics section of the MOSFET data sheet. The value listed in the electrical specifications may be measured at a higher V_{GS}, such as 10V, whereas the value of interest is at the 5V $INTV_{CC}$ gate drive voltage.

As an example of the required thermal analysis, consider a 2-phase boost converter with a 9V to 24V input voltage range and an output voltage of 48V at 2A. The switching frequency is 150kHz and the maximum ambient temperature is 70°C. The power MOSFET used for this application is the Vishay Si7478DP, which has a typical $R_{DS(ON)}$ of 8.8mΩ at V_{GS} = 4.5V and 7.5mΩ at V_{GS} = 10V. From the plot of V_{GS} vs Q_G, the total gate charge at V_{GS} = 5V is 50nC (the temperature coefficient of the gate charge is low). One power MOSFET is used for each phase. For the QFN package option:

$$I_{Q(TOT)} = 3mA + 2 \bullet 50nC \bullet 150kHz = 18mA$$

$$P_{DISS} = 24V \bullet 18mA = 432mW$$

$$T_J = 70°C + 432mW \bullet 34°C/W = 84.7°C$$

In this example, the junction temperature rise is only 14.7°C. These equations demonstrate how the gate charge current typically dominates the quiescent current of the IC, and how the choice of package option and board heat sinking can have a significant effect on the thermal performance of the solution.

OPERATION

To prevent the maximum junction temperature from being exceeded, the input supply current to the IC should be checked when operating in continuous mode (heavy load) at maximum V_{IN}. A tradeoff between the operating frequency and the size of the power MOSFETs may need to be made in order to maintain a reliable junction temperature. Finally, it is important to verify the calculations by performing a thermal analysis of the final PCB using an infrared camera or thermal probe. As an option, an external regulator shown in Figure 3 can be used to reduce the total power dissipation on the IC.

Thermal Shutdown Protection

In the event of an overtemperature condition (external or internal), an internal thermal monitor will shut down the gate drivers and reset the soft-start capacitor if the die temperature exceeds 170°C. This thermal sensor has a hysteresis of 10°C to prevent erratic behavior at hot temperatures. The LTC3862's internal thermal sensor is intended to protect the device during momentary overtemperature conditions. Continuous operation above the specified maximum operating junction temperature, however, may result in device degradation.

Operation at Low Supply Voltage

The LTC3862 has a minimum input voltage of 4V, making it a good choice for applications that experience low supply conditions. The gate driver for the LTC3862 consists of PMOS pull-up and NMOS pull-down devices, allowing the full $INTV_{CC}$ voltage to be applied to the gates during power MOSFET switching. Nonetheless, care should be taken to determine the minimum gate drive supply voltage ($INTV_{CC}$) in order to choose the optimum power MOSFETs. Important parameters that can affect the minimum gate drive voltage are the minimum input voltage ($V_{IN(MIN)}$), the LDO dropout voltage, the Q_G of the power MOSFETs, and the operating frequency.

If the input voltage V_{IN} is low enough for the $INTV_{CC}$ LDO to be in dropout, then the minimum gate drive supply voltage is:

$$V_{INTVCC} = V_{IN(MIN)} - V_{DROPOUT}$$

The LDO dropout voltage is a function of the total gate drive current and the quiescent current of the IC (typically 3mA). A curve of dropout voltage vs output current for the LDO is shown in Figure 2. The temperature coefficient of the LDO dropout voltage is approximately 6000ppm/°C.

The total Q-current ($I_{Q(TOT)}$) flowing in the LDO is the sum of the controller quiescent current (3mA) and the total gate charge drive current.

$$I_{Q(TOT)} = I_Q + Q_{G(TOT)} \bullet f$$

After the calculations have been completed, it is important to measure the gate drive waveforms and the gate driver supply voltage ($INTV_{CC}$ to PGND) over all operating conditions (low V_{IN}, nominal V_{IN} and high V_{IN}, as well as from light load to full load) to ensure adequate power MOSFET enhancement. Consult the power MOSFET data sheet to determine the actual $R_{DS(ON)}$ for the measured V_{GS}, and verify your thermal calculations by measuring the component temperatures using an infrared camera or thermal probe.

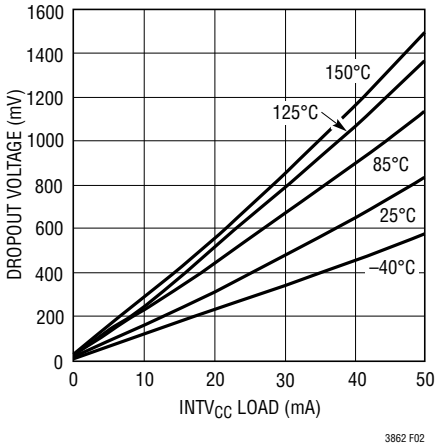


Figure 2. $INTV_{CC}$ LDO Dropout Voltage vs Current

OPERATION

Operation at High Supply Voltage

At high input voltages, the LTC3862's internal LDO can dissipate a significant amount of power, which could cause the maximum junction temperature to be exceeded. Conditions such as a high operating frequency, or the use of more than one power MOSFET per channel, could push the junction temperature rise to high levels. If the thermal equations above indicate too high a rise in the junction temperature, an external bias supply can always be used to reduce the power dissipation on the IC, as shown in Figure 3.

For example, a 5V or 12V system rail that is available would be more suitable than the 24V main input power rail to power the LTC3862. Also, the bias power can be generated with a separate switching or LDO regulator. An example of an LDO regulator is shown in Figure 3. The output voltage of the LDO regulator can be set by selecting an appropriate Zener diode to be higher than 5V but low enough to divide the power dissipation between LTC3862 and Q1 in Figure 3. The absolute maximum voltage rating of the $INTV_{CC}$ pin is 6V.

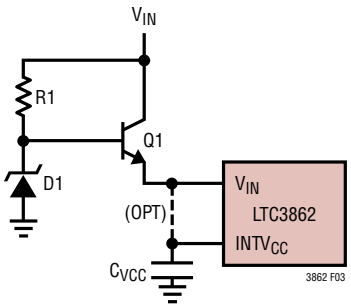


Figure 3. Using the LTC3862 with an External Bias Supply

Power Supply Sequencing

As shown in Figure 1, there are body diodes in parallel with the PMOS output transistors in the two LDO regulators in the LTC3862. As a result, it is not possible to bias the $INTV_{CC}$ and V_{IN} pins of the chip from separate power supplies. Independently biasing the $INTV_{CC}$ pin from a separate power supply can cause one of two possible failure modes during supply sequencing. If the $INTV_{CC}$ supply comes up before the V_{IN} supply, high current will flow from the external $INTV_{CC}$ supply, through the body diode of the LDO PMOS device, to the input capacitor and V_{IN} pin. This high current flow could trigger a latchup condition and cause catastrophic failure of the IC.

If, however, the V_{IN} supply to the IC comes up before the $INTV_{CC}$ supply, the external $INTV_{CC}$ supply will act as a load to the internal LDO in the LTC3862, and the LDO will attempt to charge the $INTV_{CC}$ output with its short-circuit current. This will result in excessive power dissipation and possible thermal overload of the LTC3862.

If an independent 5V supply exists in the system, it may be possible to short $INTV_{CC}$ and V_{IN} together to 5V in order to reduce gate drive power dissipation. With V_{IN} and $INTV_{CC}$ shorted together, the LDO output PMOS transistor is biased at V_{DS} = 0V, and the current demand of the internal analog and digital control circuitry, as well as the gate drive current, will be supplied by the external 5V supply.

Programming the Output Voltage

The output voltage is set by a resistor divider according to the following formula:

$$V_{OUT} = 1.223V\left(1+\frac{R2}{R1}\right)$$

The external resistor divider is connected to the output as shown in Figure 4. Resistor R1 is normally chosen so that the output voltage error caused by the current flowing out of the V_{FB} pin during normal operation is negligible compared to the current in the divider. For an output voltage error due to the error amp input bias current of less than 0.5%, this translates to a maximum value of R1 of about 30k.

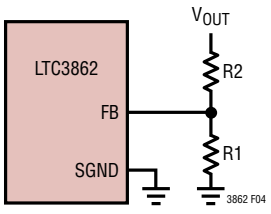


Figure 4. Programming the Output Voltage with a Resistor Divider

OPERATION

Operation of the RUN Pin

The control circuitry in the LTC3862 is turned on and off using the RUN pin. Pulling the RUN pin below 1.22V forces shutdown mode and releasing it allows a 0.5µA current source to pull this pin up, allowing a "normally on" converter to be designed. Alternatively, the RUN pin can be externally pulled up or driven directly by logic. Care must be taken not to exceed the absolute maximum rating of 8V for this pin.

The comparator on the RUN pin can also be used to sense the input voltage, allowing an undervoltage detection circuit to be designed. This is helpful in boost converter applications where the input current can reach very high levels at low input voltage:

$$I_{IN} = \frac{I_{OUT} \bullet V_{OUT}}{V_{IN} \bullet \eta}$$

The 1.22V input threshold of the RUN comparator is derived from a precise bandgap reference, in order to maximize the accuracy of the undervoltage-sensing function. The RUN comparator has 80mV built-in hysteresis. When the voltage on the RUN pin exceeds 1.22V, the current sourced into the RUN pin is switched from 0.5µA to 5µA current. The user can therefore program both the rising threshold and the amount of hysteresis using the values of the resistors in the external divider, as shown in the following equations:

$$V_{IN(ON)} = 1.22V\left(1+\frac{R_A}{R_B}\right) - 0.5\mu \bullet R_A$$

$$V_{IN(OFF)} = 1.22V\left(1+\frac{R_A}{R_B}\right) - 5\mu \bullet R_A$$

Several of the possible RUN pin control techniques are illustrated in Figure 5.

Frequency Selection and the Phase Lock Loop

The selection of the switching frequency is a tradeoff between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires a larger inductor and output capacitor to maintain low output ripple.

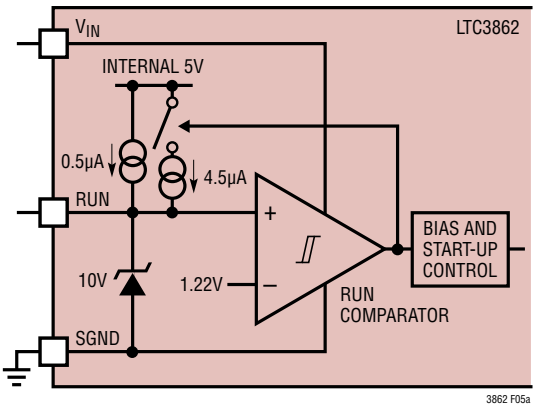


Figure 5a. Using the RUN Pin for a "Normally On" Converter

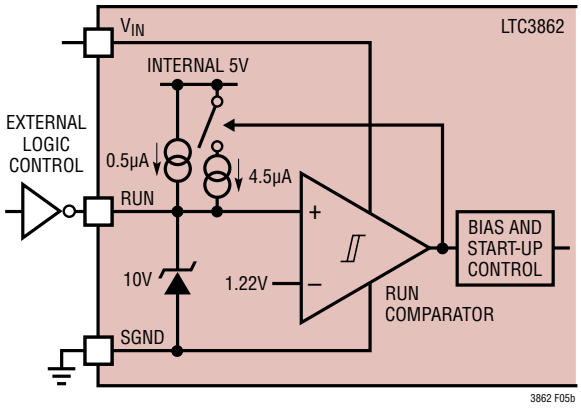


Figure 5b. On/Off Control Using External Logic

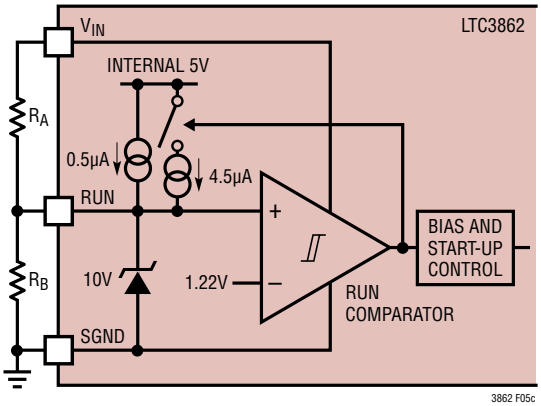


Figure 5c. Programming the Input Voltage Turn-On and Turn-Off Thresholds Using the RUN Pin

OPERATION

The LTC3862 uses a constant frequency architecture that can be programmed over a 75kHz to 500kHz range using a single resistor from the FREQ pin to ground. Figure 6 illustrates the relationship between the FREQ pin resistance and the operating frequency.

The operating frequency of the LTC3862 can be approximated using the following formula:

$$R_{FREQ} = 5.5096E9(f_{OSC})^{-0.9255}$$

A phase-lock loop is available on the LTC3862 to synchronize the internal oscillator to an external clock source connected to the SYNC pin. Connect a series RC network from the PLLFLTR pin to SGND to compensate PLL's feedback loop. Typical compensation components are a 0.01µF capacitor in series with a 10k resistor. The PLLFLTR pin is both the output of the phase detector and the input to the voltage controlled oscillator (VCO). The LTC3862 phase detector adjusts the voltage on the PLLFLTR pin to align the rising edge of GATE1 to the leading edge of the external clock signal, as shown in Figure 7. The rising edge of GATE2 will depend upon the voltage on the PHASEMODE pin. The capture range of the LTC3862's PLL is 50kHz to 650kHz.

Because the operating frequency of the LTC3862 can be programmed using an external resistor, in synchronized applications, it is recommended that the free-running frequency (as defined by the external resistor) be set to the same value as the synchronized frequency. This results in a start-up of the IC at approximately the same frequency as the external clock, so that when the sync signal comes alive, no discontinuity at the output will be observed. It also ensures that the operating frequency remains essentially constant in the event the sync signal is lost. The SYNC pin has an internal 50k resistor to ground.

Using the CLKOUT and PHASEMODE Pins in Multi-Phase Applications

The LTC3862 features two pins (CLKOUT and PHASEMODE) that allow multiple ICs to be daisy-chained together for higher current multi-phase applications. For a 3- or 4-phase

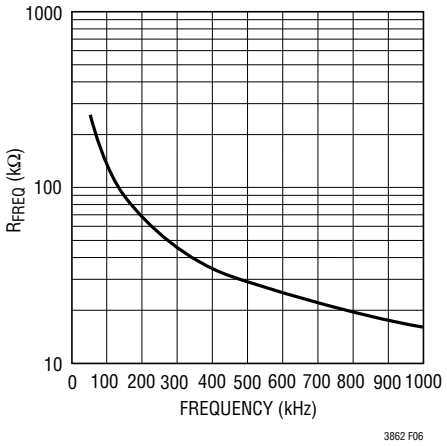


Figure 6. FREQ Pin Resistor Value vs Frequency

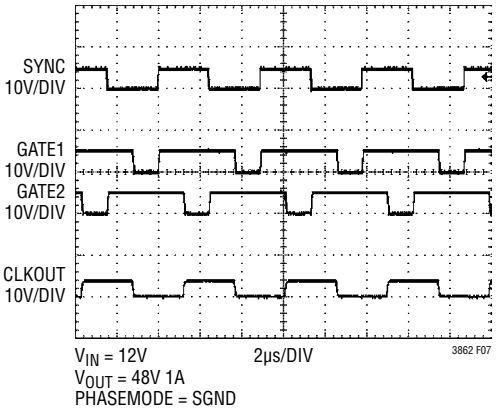


Figure 7. Synchronization of the LTC3862 to an External Clock Using the PLL

design, the CLKOUT signal of the master controller is connected to the SYNC input of the slave controller in order to synchronize additional power stages for a single high current output. The PHASEMODE pin is used to adjust the phase relationship between channel 1 and channel 2, as well as the phase relationship between channel 1 and CLKOUT, as summarized in Table 1. The phases are calculated relative to the zero degrees, defined as the rising edge of the GATE1 output. In a 6-phase application the CLKOUT pin of the master controller connects to the SYNC input of the 2nd controller and the CLKOUT pin of the 2nd controller connects to the SYNC pin of the 3rd controller.

OPERATION

Table 1

PHASEMODE	CH-1 to CH-2 PHASE	CH-1 to CLKOUT PHASE	APPLICATION
SGND	180°	90°	2-Phase, 4-Phase
Float	180°	60°	6-Phase
3V8	120°	240°	3-Phase

Using the LTC3862 Transconductance (g_m) Error Amplifier in Multi-Phase Applications

The LTC3862 error amplifier is a transconductance, or g_m amplifier, meaning that it has high DC gain but high output impedance (the output of the error amplifier is a current proportional to the differential input voltage). This style of error amplifier greatly eases the task of implementing a multi-phase solution, because the amplifiers from two or more chips can be connected in parallel. In this case the FB pins of multiple LTC3862s can be connected together, as well as the ITH pins, as shown in Figure 8. The g_m of the composite error amplifier is simply n times the transconductance of one amplifier, or $g_{m(TOT)} = n \bullet 660\mu S$, where n is the number of amplifiers connected in parallel. The transfer function from the ITH pin to the current comparator inputs was carefully designed to be accurate, both from channel-to-channel and chip-to-chip. This way the peak inductor current matching is kept accurate.

A buffered version of the output of the error amplifier determines the threshold at the input of the current comparator. The ITH voltage that represents zero peak current is 0.4V and the voltage that represents current limit is 1.2V (at low duty cycle). During an overload condition, the output of the error amplifier is clamped to 2.6V at low duty cycle, in order to reduce the latency when the overload condition terminates. A patented circuit in the LTC3862 is used to recover the slope compensation signal, so that the maximum peak inductor current is not a strong function of the duty cycle.

In multiphase applications that use more than one LTC3862 controller, it is possible for ground currents on the PCB to disturb the control lines between the ICs, resulting in erratic behavior. In these applications the FB pins should be connected to each other through 100Ω resistors and each slave FB pin should be decoupled locally with a 100pF capacitor to ground, as shown in Figure 8.

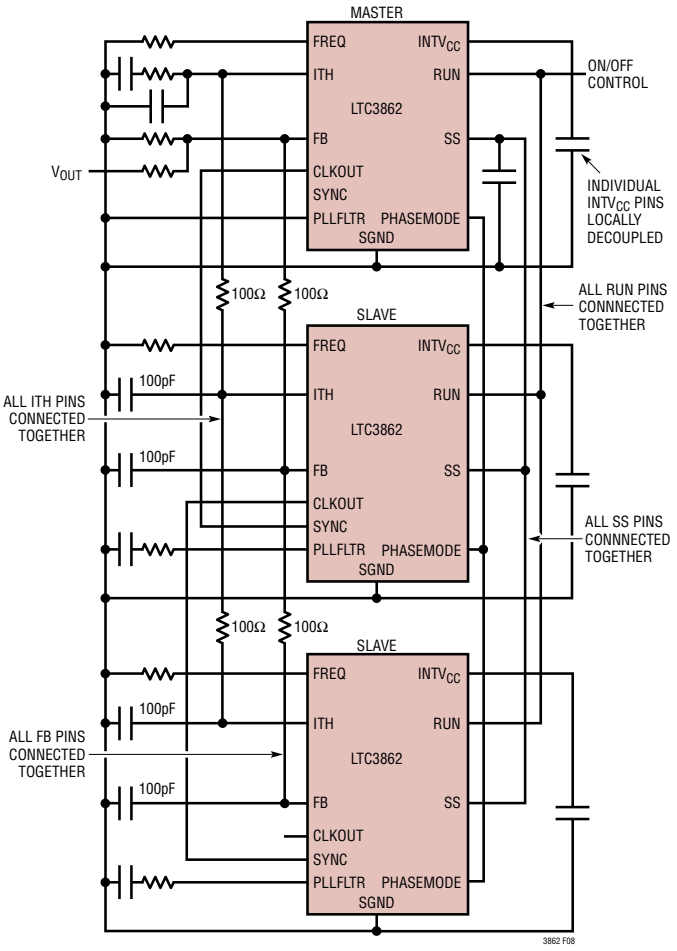


Figure 8. LTC3862 Error Amplifier Configuration for Multi-Phase Operation

Soft-Start

The start-up of the LTC3862 is controlled by the voltage on the SS pin. An internal PNP transistor clamps the current comparator sense threshold during soft-start, thereby limiting the peak switch current. The base of the PNP is connected to the SS pin and the emitter to an internal, buffered ITH node (please note that the ITH pin voltage may not track the soft-start voltage during this time period). An internal 5µA current source charges the SS capacitor, and clamps the peak sense threshold until the voltage on the soft-start capacitor reaches approximately 0.6V. The required amount of soft-start capacitance can be estimated using the following equation:

$$C_{SS} = 5\mu A\left(\frac{t_{SS}}{0.6V}\right)$$

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The SS pin has an internal open-drain NMOS pull-down transistor that turns on when the RUN pin is pulled low, when the voltage on the $INTV_{CC}$ pin is below its undervoltage lockout threshold, or during an overtemperature condition. In multi-phase applications that use more than one LTC3862 chip, connect all of the SS pins together and use one external capacitor to program the soft-start time. In this case, the current into the soft-start capacitor will be $I_{SS} = n \bullet 5\mu A$, where n is the number of SS pins connected together. Figure 9 illustrates the start-up waveforms for a 2-phase LTC3862 application.

Pulse Skip Operation at Light Load

As the load current is decreased, the controller enters discontinuous mode (DCM). The peak inductor current can be reduced until the minimum on-time of the controller is reached. Any further decrease in the load current will cause pulse skipping to occur, in order to maintain output regulation, which is normal. The minimum on-time of the controller in this mode is approximately 180ns (with the blanking time set to its minimum value), the majority of which is leading edge blanking. Figure 10 illustrates the LTC3862 switching waveforms at the onset of pulse skipping.

Programmable Slope Compensation

For a current mode boost regulator operating in CCM, slope compensation must be added for duty cycles above 50%, in order to avoid sub-harmonic oscillation. For the LTC3862, this ramp compensation is internal and user adjustable. Having an internally fixed ramp compensation waveform normally places some constraints on the value of the inductor and the operating frequency. For example, with a fixed amount of internal slope compensation, using an excessively large inductor would result in too much effective slope compensation, and the converter could become unstable. Likewise, if too small an inductor were used, the internal ramp compensation could be inadequate to prevent sub-harmonic oscillation.

The LTC3862 contains a pin that allows the user to program the slope compensation gain in order to optimize performance for a wider range of inductance. With the SLOPE pin left floating, the normalized slope gain is 1.00. Connecting the SLOPE pin to ground reduces the normalized gain to 0.625 and connecting this pin to the 3V8 supply increases the normalized slope gain to 1.66.

With the normalized slope compensation gain set to 1.00, the design equations assume an inductor ripple current of 20% to 40%, as with previous designs. Depending upon the application circuit, however, a normalized gain of 1.00 may not be optimum for the inductor chosen. If the ripple current in the inductor is greater than 40%, the normalized slope gain can be increased to 1.66 (an increase of 66%) by connecting the SLOPE pin to the 3V8 supply. If the inductor ripple current is less than 20%, the normalized slope gain can be reduced to 0.625 (a decrease of 37.5%) by connecting the SLOPE pin to SGND.

To check the effectiveness of the slope compensation, apply a load step to the output and monitor the cycle-by-cycle

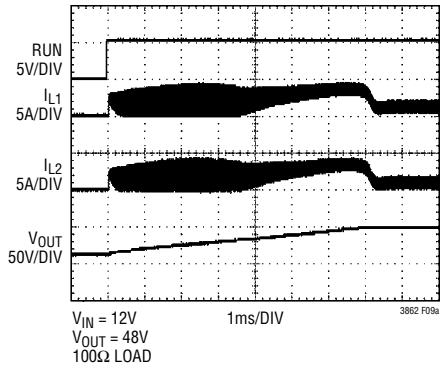

Figure 9. Typical Start-Up Waveforms for a Boost Converter Using the LTC3862

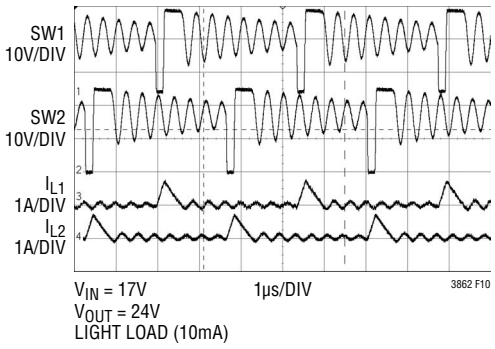

Figure 10. Light Load Switching Waveforms for the LTC3862 at the Onset of Pulse Skipping

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behavior of the inductor current during the leading and trailing edges of the load current. Vary the input voltage over its full range and check for signs of cycle-by-cycle SW node instability or sub-harmonic oscillation. When the slope compensation is too low the converter can suffer from excessive jitter or, worst case, sub-harmonic oscillation. When excess slope compensation is applied to the internal current sense signal, the phase margin of the control loop suffers. Figure 11 illustrates inductor current waveforms for a properly compensated loop.

The LTC3862 contains a patented circuit whereby most of the applied slope compensation is recovered, in order to provide a $SENSE^+$ to $SENSE^-$ threshold which is not a strong function of the duty cycle. This sense threshold is, however, a function of the programmed slope gain, as shown in Figure 12. The data sheet typical specification of 75mV for $SENSE^+$ minus $SENSE^-$ is measured at a normalized slope gain of 1.00 at low duty cycle. For applications where the normalized slope gain is not 1.00, use Figure 12 to determine the correct value of the sense resistor.

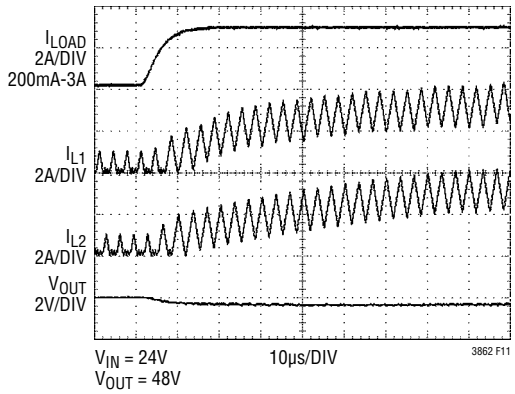

Figure 11. Inductor Current Waveforms for a Properly Compensated Control Loop

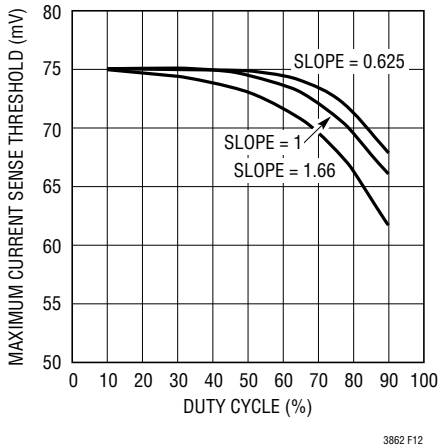

Figure 12. Effect of Slope Gain on the Peak SENSE Threshold

Programmable Blanking and the Minimum On-Time

The BLANK pin on the LTC3862 allows the user to program the amount of leading edge blanking at the SENSE pins. Connecting the BLANK pin to SGND results in a minimum on-time of 180ns, floating the pin increases this time to 260ns, and connecting the BLANK pin to the 3V8 supply results in a minimum on-time of 340ns. The majority of the minimum on-time consists of this leading edge blanking, due to the inherently low propagation delay of the current comparator (25ns typ) and logic circuitry (10ns to 15ns).

The purpose of leading edge blanking is to filter out noise on the SENSE pins at the leading edge of the power MOSFET turn-on. During the turn-on of the power MOSFET the gate drive current, the discharge of any parasitic capacitance on the SW node, the recovery of the boost diode charge, and parasitic series inductance in the high di/dt path all contribute to overshoot and high frequency noise that could cause false-tripping of the current comparator. Due to the wide range of applications the LTC3862 is well-suited to, fixing one value of the internal leading edge blanking time would have required the longest delay time to have been used. Providing a means to program the blank time allows users to optimize the SENSE pin filtering for each application. Figure 13 illustrates the effect of the programmable leading edge blank time on the minimum on-time of a boost converter.

Programmable Maximum Duty Cycle

In order to maintain constant frequency and a low output ripple voltage, a single-ended boost (or flyback or SEPIC) converter is required to turn off the switch every cycle for some minimum amount of time. This off-time allows the transfer of energy from the inductor to the output capacitor and load, and prevents excessive ripple current and voltage. For inductor-based topologies like boost and SEPIC converters, having a maximum duty cycle as close as possible to 100% may be desirable, especially in low V_{IN} to high V_{OUT} applications. However, for transformer-based solutions, having a maximum duty cycle near 100% is

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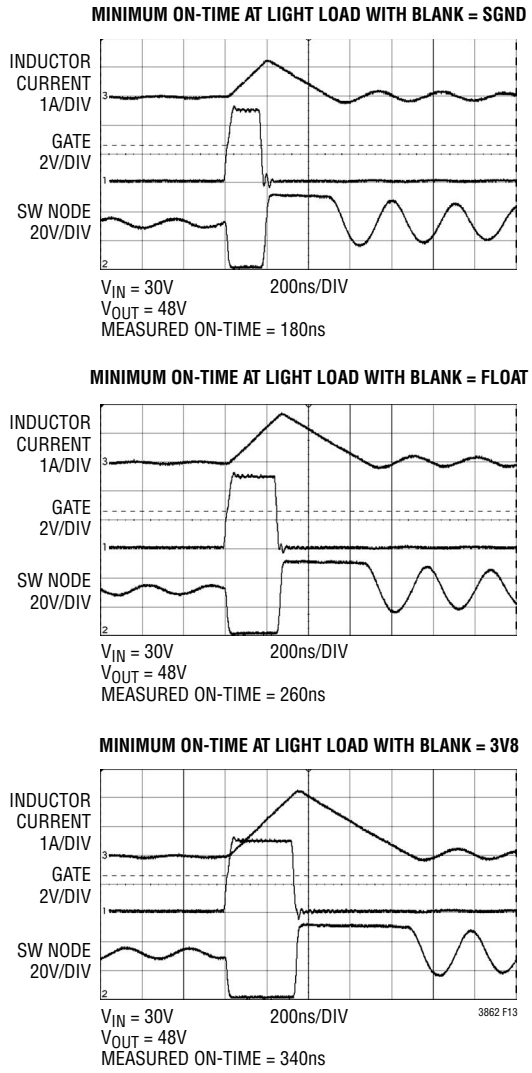

Figure 13. Leading Edge Blanking Effects on the Minimum On-Time

undesirable, due to the need for V • sec reset during the primary switch off-time.

In order to satisfy these different applications requirements, the LTC3862 has a simple way to program the maximum duty cycle. Connecting the D_{MAX} pin to SGND limits the maximum duty cycle to 96%. Floating this pin limits the duty cycle to 84% and connecting the D_{MAX} pin to the 3V8 supply limits it to 75%. Figure 14 illustrates the effect of limiting the maximum duty cycle on the SW node waveform of a boost converter.

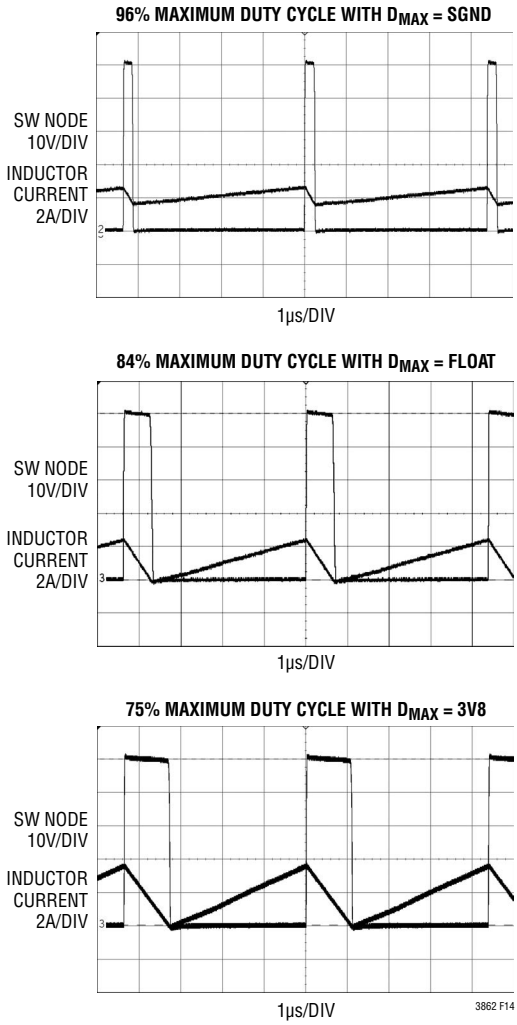

Figure 14. SW Node Waveforms with Different Duty Cycle Limits

The LTC3862 contains an oscillator that runs at 12x the programmed switching frequency, in order to provide for 2-, 3-, 4-, 6- and 12-phase operation. A digital counter is used to divide down the fundamental oscillator frequency in order to obtain the operating frequency of the gate drivers. **Since the maximum duty cycle limit is obtained from this digital counter, the percentage maximum duty cycle does not vary with process tolerances or temperature**.

The SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are high impedance inputs to the CMOS current comparators for each channel. Nominally, there is no DC current into or out of these

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pins. There are ESD protection diodes connected from these pins to SGND, although even at hot temperature the leakage current into the SENSE+ and SENSE– pins should be less than 1µA.

Since the LTC3862 contains leading edge blanking, an external RC filter is not required for proper operation. However, if an external filter is used, the filter components should be placed close to the SENSE+ and SENSE– pins on the IC, as shown in Figure 15. The positive and negative sense node traces should then run parallel to each other to a Kelvin connection underneath the sense resistor, as shown in Figure 16. Sensing current elsewhere on the board can add parasitic inductance and capacitance to the current sense element, degrading the information at the sense pins and making the programmed current limit unpredictable. Avoid the temptation to connect the SENSE– line to the ground plane using a PCB via; this could result in unpredictable behavior.

The sense resistor should be connected to the source of the power MOSFET and the ground node using short, wide PCB traces, as shown in Figure 16. Ideally, the bottom terminal of the sense resistors will be immediately adjacent to the negative terminal of the output capacitor, since this path is a part of the high di/dt loop formed by the switch, boost diode, output capacitor and sense resistor. Placement of the inductors is less critical, since the current in the inductors is a triangle waveform.

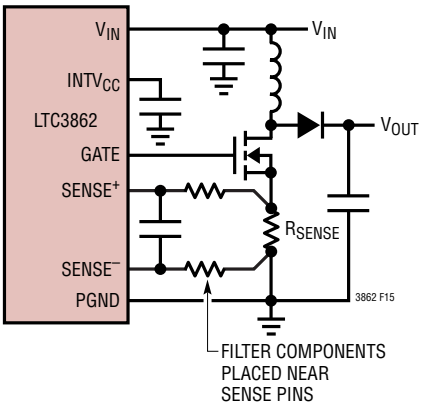

Figure 15. Proper Current Sense Filter Component Placement

Checking the Load Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem.

The availability of the ITH pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin.

The ITH series R_C • C_C filter sets the dominant pole-zero loop compensation. The transfer function for boost and flyback converters contains a right half plane zero that normally requires the loop crossover frequency to be reduced significantly in order to maintain good phase

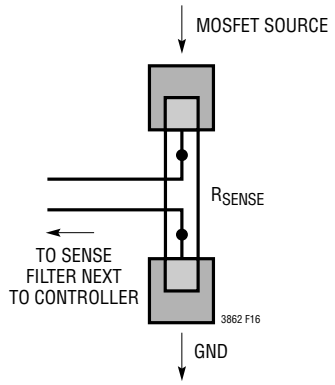

Figure 16. Connecting the SENSE+ and SENSE– Traces to the Sense Resistor Using a Kelvin Connection

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margin. The R_C • C_C filter values can typically be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type(s) and value(s) have been determined. The output capacitor configuration needs to be selected in advance because the effective ESR and bulk capacitance have a significant effect on the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET and load resistor directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a fast load step condition. The initial output voltage step resulting from the step change in the output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. Figure 17 illustrates the load step response of a properly compensated boost converter.

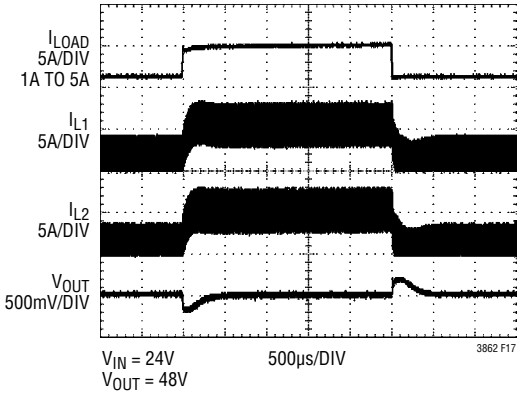

Figure 17. Load Step Response of a Properly Compensated Boost Converter

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Typical Boost Applications Circuit

A basic 2-phase, single output LTC3862 application circuit is shown in Figure 18. External component selection is driven by the characteristics of the load and the input supply.

Duty Cycle Considerations

For a boost converter operating in a continuous conduction mode (CCM), the duty cycle of the main switch is:

$$D = \left(\frac{V_O + V_F - V_{IN}}{V_O + V_F} \right) = t_{ON} \bullet f$$

where V_F is the forward voltage of the boost diode. The minimum on-time for a given application operating in CCM is:

$$t_{ON(MIN)} = \frac{1}{f} \left(\frac{V_O + V_F - V_{IN(MAX)}}{V_O + V_F} \right)$$

For a given input voltage range and output voltage, it is important to know how close the minimum on-time of the application comes to the minimum on-time of the control IC. The LTC3862 minimum on-time can be programmed from 180ns to 340ns using the BLANK pin.

Minimum On-Time Limitations

In a single-ended boost converter, two steady-state conditions can result in operation at the minimum on-time of the controller. The first condition is when the input voltage is close to the output voltage. When V_{IN} approaches V_{OUT} the voltage across the inductor approaches zero during the switch off-time. Under this operating condition the converter can become unstable and the output can experience high ripple voltage oscillation at audible frequencies. For applications where the input voltage can approach or exceed the output voltage, consider using a SEPIC or buck-boost topology instead of a boost converter.

The second condition that can result in operation at the minimum on-time of the controller is at light load, in deep discontinuous mode. As the load current is decreased, the on-time of the switch decreases, until the minimum on-time limit of the controller is reached. Any further decrease in the output current will result in pulse skipping, a typically benign condition where cycles are skipped in order to maintain output regulation.

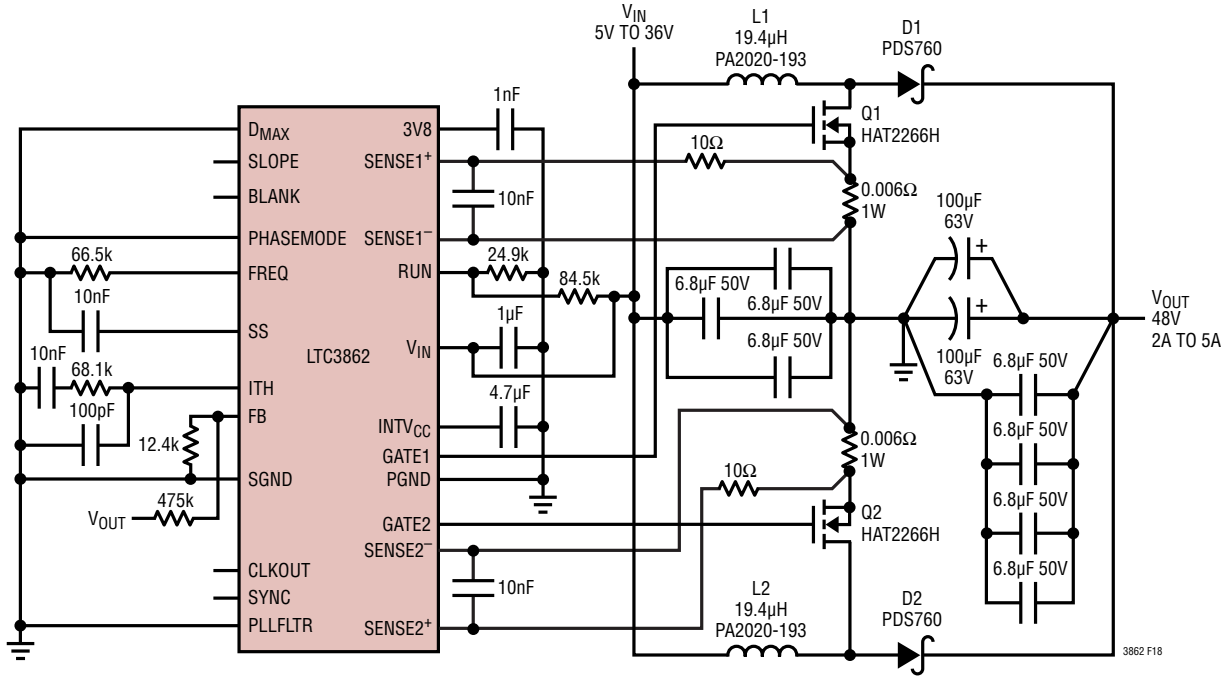

Figure 18. A Typical 2-Phase, Single Output Boost Converter Application Circuit

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Maximum Duty Cycle Limitations

Another operating extreme occurs at high duty cycle, when the input voltage is low and the output voltage is high. In this case:

$$D_{MAX} = \left(\frac{V_O + V_F - V_{IN(MIN)}}{V_O + V_F} \right)$$

A single-ended boost converter needs a minimum off-time every cycle in order to allow energy transfer from the input inductor to the output capacitor. This minimum off-time translates to a maximum duty cycle for the converter. The equation above can be rearranged to obtain the maximum output voltage for a given minimum input or maximum duty cycle.

$$V_{O(MAX)} = \frac{V_{IN}}{1 - D_{MAX}} - V_F$$

The equation for D_{MAX} above can be used as an initial guideline for determining the maximum duty cycle of the application circuit. However, losses in the inductor, input and output capacitors, the power MOSFETs, the sense resistors and the controller (gate drive losses) all contribute to an increasing of the duty cycle. The effect of these losses will be to *decrease* the maximum output voltage for a given minimum input voltage.

After the initial calculations have been completed for an application circuit, it is important to build a prototype of the circuit and measure it over the entire input voltage range, from light load to full load, and over temperature, in order to verify proper operation of the circuit.

Peak and Average Input Currents

The control circuit in the LTC3862 measures the input current (by means of resistors in the sources of the power MOSFETs), so the output current needs to be reflected back to the input in order to dimension the power MOSFETs properly. Based on the fact that, ideally, the output power is equal to the input power, the maximum average input current is:

$$I_{IN(MAX)} = \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

The peak current in each inductor is:

$$I_{IN(PK)} = \frac{1}{n} \bullet \left(1 + \frac{\chi}{2} \right) \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

where n represents the number of phases and χ represents the percentage peak-to-peak ripple current in the inductor. For example, if the design goal is to have 30% ripple current in the inductor, then $\chi = 0.30$, and the peak current is 15% greater than the average.

Inductor Selection

Given an input voltage range, operating frequency and ripple current, the inductor value can be determined using the following equation:

$$L = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX}$$

where:

$$\Delta I_L = \frac{\chi}{n} \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

Choosing a larger value of ΔI_L allows the use of a lower value inductor but results in higher output voltage ripple, greater core losses, and higher ripple current ratings for the input and output capacitors. A reasonable starting point is 30% ripple current in the inductor ($\chi = 0.3$), or:

$$\Delta I_L = \frac{0.3}{n} \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

The inductor saturation current rating needs to be higher than the worst-case peak inductor current during an overload condition. If $I_{O(MAX)}$ is the maximum rated load current, then the maximum current limit value ($I_{O(CL)}$) would normally be chosen to be some factor (e.g., 30%) greater than $I_{O(MAX)}$.

$$I_{O(CL)} = 1.3 \bullet I_{O(MAX)}$$

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Reflecting this back to the input, where the current is being measured, and accounting for the ripple current, gives a minimum saturation current rating for the inductor of:

$$I_{L(SAT)} \geq \frac{1}{n} \bullet \left(1+\frac{\chi}{2}\right) \bullet \frac{1.3 \bullet I_{O(MAX)}}{1-D_{MAX}}$$

The saturation current rating for the inductor should be determined at the minimum input voltage (which results in the highest duty cycle and maximum input current), maximum output current and the maximum expected core temperature. The saturation current ratings for most commercially available inductors drop at high temperature. To verify safe operation, it is a good idea to characterize the inductor's core/winding temperature under the following conditions: 1) worst-case operating conditions, 2) maximum allowable ambient temperature and 3) with the power supply mounted in the final enclosure. Thermal characterization can be done by placing a thermocouple in intimate contact with the winding/core structure, or by burying the thermocouple within the windings themselves.

Remember that a single-ended boost converter is **not** short-circuit protected, and that under a shorted output condition, the output current is limited only by the input supply capability. For applications requiring a step-up converter that is short-circuit protected, consider using a SEPIC or forward converter topology.

Power MOSFET Selection

The peak-to-peak gate drive level is set by the $INTV_{CC}$ voltage is 5V for the LTC3862 under normal operating conditions. Selection criteria for the power MOSFETs include the $R_{DS(ON)}$, gate charge Q_G, drain-to-source breakdown voltage BV_{DSS}, maximum continuous drain current $I_{D(MAX)}$, and thermal resistances $R_{TH(JA)}$ and $R_{TH(JC)}$—both junction-to-ambient and junction-to-case.

The gate driver for the LTC3862 consists of PMOS pull-up and NMOS pull-down devices, allowing the full $INTV_{CC}$ voltage to be applied to the gates during power MOSFET switching. Nonetheless, care must be taken to ensure that the minimum gate drive voltage is still sufficient to full enhance the power MOSFET. Check the MOSFET data sheet carefully to verify that the $R_{DS(ON)}$ of the MOSFET is specified for a voltage less than or equal to the nominal $INTV_{CC}$ voltage of 5V. For applications that require a power MOSFET rated at 6V or 10V, please refer to the LTC3862-1 data sheet.

Also pay close attention to the BV_{DSS} specifications for the MOSFETs relative to the maximum actual switch voltage in the application. Check the switching waveforms of the MOSFET directly on the drain terminal using a single probe and a high bandwidth oscilloscope. Ensure that the drain voltage ringing does not approach the BV_{DSS} of the MOSFET. Excessive ringing at high frequency is normally an indicator of too much series inductance in the high di/dt current path that includes the MOSFET, the boost diode, the output capacitor, the sense resistor and the PCB traces connecting these components.

The GATE of MOSFET Q1 could experience transient voltage spikes during turn-on and turn-off of the MOSFET, due to parasitic lead inductance and improper PCB layout. These voltage spikes could exceed the absolute maximum voltage rating of LTC3862's GATE pin. The GATE pins are rated for an absolute maximum voltage of –0.3V minimum and 6V maximum. Hence it is recommended to add an external buffer close to the GATE of the MOSFET as shown in Figure 19.

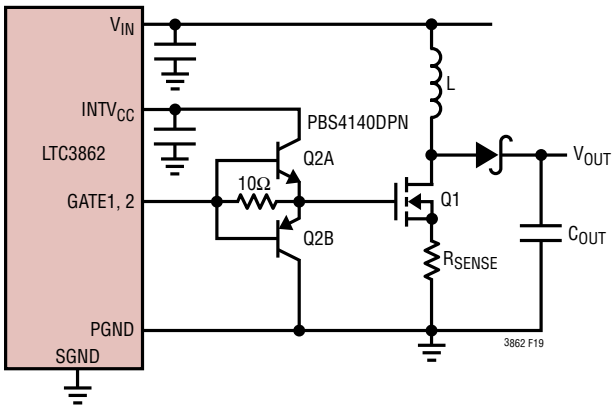

Figure 19. External Buffer Circuit

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Finally, check the MOSFET manufacturer's data sheet for an avalanche energy rating (EAS). Some MOSFETs are not rated for body diode avalanche and will fail catastrophically if the V_{DS} exceeds the device BV_{DSS}, even if only by a fraction of a volt. Avalanche-rated MOSFETs are better able to sustain high frequency drain-to-source ringing near the device BV_{DSS} during the turn-off transition.

Calculating Power MOSFET Switching and Conduction Losses and Junction Temperatures

In order to calculate the junction temperature of the power MOSFET, the power dissipated by the device must be known. This power dissipation is a function of the duty cycle, the load current and the junction temperature itself (due to the positive temperature coefficient of its $R_{DS(ON)}$). As a result, some iterative calculation is normally required to determine a reasonably accurate value.

The power dissipated by the MOSFET in a multi-phase boost converter with n phases is:

$$P_{FET} = \left(\frac{I_{O(MAX)}}{n \bullet \left(1 - D_{MAX}\right)} \right)^2 \bullet R_{DS(ON)} \bullet D_{MAX} \bullet \rho_T$$

$$+ k \bullet V_{OUT}{}^2 \bullet \frac{I_{O(MAX)}}{n \bullet \left(1 - D_{MAX}\right)} \bullet C_{RSS} \bullet f$$

The first term in the equation above represents the I^2R losses in the device, and the second term, the switching losses. The constant, k = 1.7, is an empirical factor inversely related to the gate drive current and has the dimension of 1/current.

The ρ_T term accounts for the temperature coefficient of the $R_{DS(ON)}$ of the MOSFET, which is typically 0.4%/°C. Figure 20 illustrates the variation of normalized $R_{DS(ON)}$ over temperature for a typical power MOSFET.

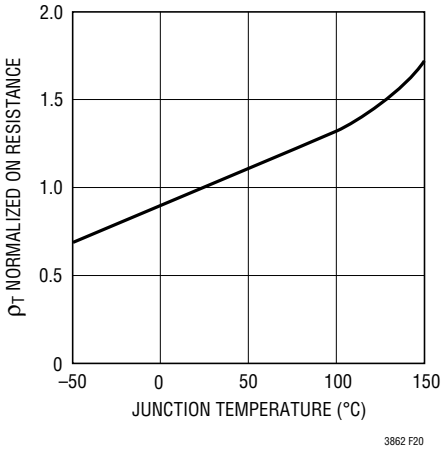

Figure 20. Normalized Power MOSFET $R_{DS(ON)}$ vs Temperature

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P_{FET} \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(CA)}$). This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

It is tempting to choose a power MOSFET with a very low $R_{DS(ON)}$ in order to reduce conduction losses. In doing so, however, the gate charge Q_G is usually significantly higher, which increases switching and gate drive losses. Since the switching losses increase with the square of the output voltage, applications with a low output voltage generally have higher MOSFET conduction losses, and high output voltage applications generally have higher MOSFET switching losses. At high output voltages, the highest efficiency is usually obtained by using a MOSFET with a higher $R_{DS(ON)}$ and lower Q_G. The equation above can easily be split into two components (conduction and switching) and entered into a spreadsheet, in order to compare the performance of different MOSFETs.

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Programming the Current Limit

The peak sense voltage threshold for the LTC3862 is 75mV at low duty cycle and with a normalized slope gain of 1.00, and is measured from SENSE+ to SENSE–. Figure 21 illustrates the change in the sense threshold with varying duty cycle and slope gain.

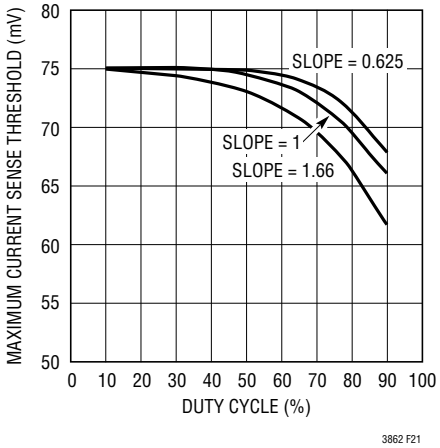

Figure 21. Maximum Sense Voltage Variation with Duty Cycle and Slope Gain

For a boost converter where the current limit value is chosen to be 30% higher than the maximum load current, the peak current in the MOSFET and sense resistor is:

$$I_{SW(MAX)} = I_{R(SENSE)} = \frac{1}{n} \bullet \left(1 + \frac{\chi}{2}\right) \bullet \frac{1.3 \bullet I_{O(MAX)}}{1 - D_{MAX}}$$

The sense resistor value is then:

$$R_{SENSE} = \frac{V_{SENSE(MAX)} \bullet n \bullet \left(1 - D_{MAX}\right)}{1.3 \bullet \left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)}}$$

Again, the factor n is the number of phases used, and χ represents the percentage ripple current in the inductor. The number 1.3 represents the factor by which the current limit exceeds the maximum load current, $I_{O(MAX)}$. For example, if the current limit needs to exceed the maximum load current by 50%, then the 1.3 factor should be replaced with 1.5.

The average power dissipated in the sense resistor can easily be calculated as:

$$P_{R(SENSE)} = \left(\frac{1.3 \bullet I_{O(MAX)}}{n \bullet \left(1 - D_{MAX}\right)}\right)^2 \bullet R_{SENSE} \bullet D_{MAX}$$

This equation assumes no temperature coefficient for the sense resistor. If the resistor chosen has a significant temperature coefficient, then substitute the worst-case high resistance value into the equation.

The resistor temperature can be calculated using the equation:

$$T_D = T_A + P_{R(SENSE)} \bullet R_{TH(JA)}$$

Selecting the Output Diodes

To maximize efficiency, a fast switching diode with low forward drop and low reverse leakage is required. The output diode in a boost converter conducts current during the switch off-time. The peak reverse voltage that the diode must withstand is equal to the regulator output voltage. The average forward current in normal operation is equal to the output current, and the peak current is equal to the peak inductor current:

$$I_{D(PEAK)} = \frac{1}{n} \bullet \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

Although the average diode current is equal to the output current, in very high duty cycle applications (low V_{IN} to high V_{OUT}) the peak diode current can be several times higher than the average, as shown in Figure 22. In this

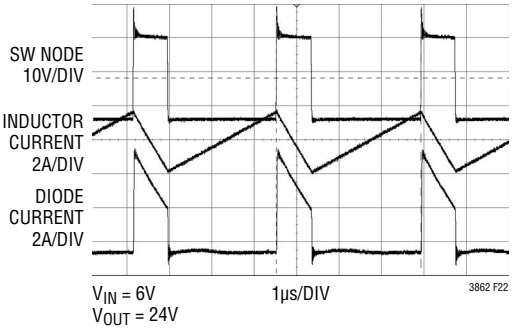

Figure 22. Diode Current Waveform for a High Duty Cycle Application

APPLICATIONS INFORMATION

case check the diode manufacturer's data sheet to ensure that its peak current rating exceeds the peak current in the equation above. In addition, when calculating the power dissipation in the diode, use the value of the forward voltage (V_F) measured at the peak current, not the average output current. Excess power will be dissipated in the series resistance of the diode, which would not be accounted for if the average output current and forward voltage were used in the equations. Finally, this additional power dissipation is important when deciding on a diode current rating, package type, and method of heat sinking.

To a close approximation, the power dissipated by the diode is:

$$P_D = I_{D(PEAK)} \bullet V_{F(PEAK)} \bullet (1 - D_{MAX})$$

The diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure. Once the proper diode has been selected and the circuit performance has been verified, measure the temperature of the power components using a thermal probe or infrared camera over all operating conditions to ensure a good thermal design.

Finally, remember to keep the diode lead lengths short and to observe proper switch-node layout (see Board Layout Checklist) to avoid excessive ringing and increased dissipation.

Output Capacitor Selection

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct combination of output capacitors for a boost converter application. The effects of these three parameters on the output voltage ripple waveform are illustrated in Figure 23 for a typical boost converter.

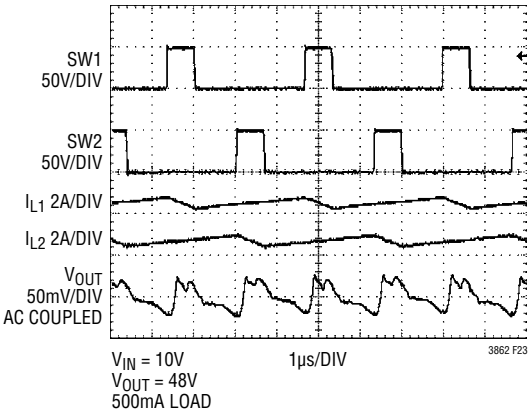

Figure 23. Switching Waveforms for a Boost Converter

The choice of component(s) begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step and the charging/discharging ΔV. For the purpose of simplicity we will choose 2% for the maximum output ripple, to be divided equally between the ESR step and the charging/discharging ΔV. This percentage ripple will change, depending on the requirements of the application, and the equations provided below can easily be modified.

One of the key benefits of multi-phase operation is a reduction in the peak current supplied to the output capacitor by the boost diodes. As a result, the ESR requirement of the capacitor is relaxed. For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} \leq \frac{0.01 \bullet V_{OUT}}{I_{D(PEAK)}}$$

where:

$$I_{D(PEAK)} = \frac{1}{n} \bullet \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

The factor n represents the number of phases and the factor χ represents the percentage inductor ripple current.

APPLICATIONS INFORMATION

For the bulk capacitance, which we assume contributes 1% to the total output ripple, the minimum required capacitance is approximately:

$$C_{OUT} \geq \frac{I_{O(MAX)}}{0.01 \bullet n \bullet V_{OUT} \bullet f}$$

For many designs it will be necessary to use one type of capacitor to obtain the required ESR, and another type to satisfy the bulk capacitance. For example, using a low ESR ceramic capacitor can minimize the ESR step, while an electrolytic capacitor can be used to supply the required bulk C.

The voltage rating of the output capacitor must be greater than the maximum output voltage, with sufficient derating to account for the maximum capacitor temperature.

Because the ripple current in the output capacitor is a square wave, the ripple current requirements for this capacitor depend on the duty cycle, the number of phases and the maximum output current. Figure 24 illustrates the normalized output capacitor ripple current as a function of duty cycle. In order to choose a ripple current rating for the output capacitor, first establish the duty cycle range, based on the output voltage and range of input voltage. Referring to Figure 24, choose the worst-case high normalized ripple current, as a percentage of the maximum load current.

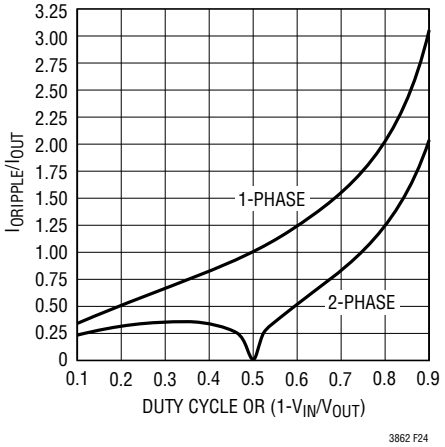

Figure 24. Normalized Output Capacitor Ripple Current (RMS) for a Boost Converter

The output ripple current is divided between the various capacitors connected in parallel at the output voltage. Although ceramic capacitors are generally known for low ESR (especially X5R and X7R), these capacitors suffer from a relatively high voltage coefficient. Therefore, it is not safe to assume that the entire ripple current flows in the ceramic capacitor. Aluminum electrolytic capacitors are generally chosen because of their high bulk capacitance, but they have a relatively high ESR. As a result, some amount of ripple current will flow in this capacitor. If the ripple current flowing into a capacitor exceeds its RMS rating, the capacitor will heat up, reducing its effective capacitance and adversely affecting its reliability. After the output capacitor configuration has been determined using the equations provided, measure the individual capacitor case temperatures in order to verify good thermal performance.

Input Capacitor Selection

The input capacitor voltage rating in a boost converter should comfortably exceed the maximum input voltage. Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of the input capacitor is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

The input ripple current in a multi-phase boost converter is relatively low (compared with the output ripple current), because this current is continuous and is being divided between two or more inductors. Nonetheless, significant stress can be placed on the input capacitor, especially

APPLICATIONS INFORMATION

in high duty cycle applications. Figure 25 illustrates the normalized input ripple current, where:

$$I_{NORM} = \frac{V_{IN}}{L \bullet f}$$

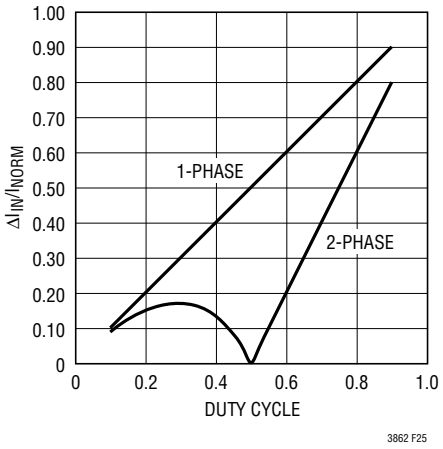

Figure 25. Normalized Input Peak-to-Peak Ripple Current

A Design Example

Consider the LTC3862 application circuit is shown in Figure 26a. The output voltage is 48V and the input voltage range is 5V to 36V. The maximum output current is 5A when the input voltage is 24V to 36V. Below 24V, current limit will linearly reduce the maximum load to 1A at 5V in (see Figure 26b).

1. The duty cycle range (where 5A is available at the output) is:

$$D_{MAX} = \left(\frac{V_O + V_F - V_{IN}}{V_O + V_F}\right)$$

$$= \left(\frac{48V + 0.5V - 24V}{48V + 0.5V}\right) = 50.5\%$$

$$D_{MIN} = \left(\frac{48V + 0.5V - 36V}{48V + 0.5V}\right) = 25.8\%$$

2. The operating frequency is chosen to be 300kHz so the period is 3.33µs. From Figure 6, the resistor from the FREQ pin to ground is 45.3k.

3. The minimum on-time for this application operating in CCM is:

$$t_{ON(MIN)} = \frac{1}{f} \bullet \left(\frac{V_O + V_F - V_{IN(MAX)}}{V_O + V_F}\right) = \frac{1}{300kHz} \bullet$$

$$\left(\frac{48V + 0.5V - 36V}{48V + 0.5V}\right) = 859ns$$

The maximum DC input current is:

$$I_{IN(MAX)} = \frac{I_{O(MAX)}}{1 - D_{MAX}} = \frac{5A}{1 - 0.505} = 10.1A$$

4. A ripple current of 40% is chosen so the peak current in each inductor is:

$$I_{IN(PK)} = \frac{1}{n} \bullet \left(1 - \frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

$$= \frac{1}{2} \bullet \left(1 + \frac{0.4}{2}\right) \bullet \frac{5A}{1 - 0.505} = 6.06A$$

5. The inductor ripple current is:

$$\Delta I_L = \frac{\chi}{n} \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}} = \frac{0.4}{2} \bullet \frac{5A}{1 - 0.505} = 2.02A$$

6. The inductor value is therefore:

$$L = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX} = \frac{24V}{2.02A \bullet 300kHz} \bullet 0.505$$

$$= 20\mu H$$

7. For a current limit value 30% higher than the maximum load current:

$$I_{O(CL)} = 1.3 \bullet I_{O(MAX)} = 1.3 \bullet 5A = 6.5A$$

APPLICATIONS INFORMATION

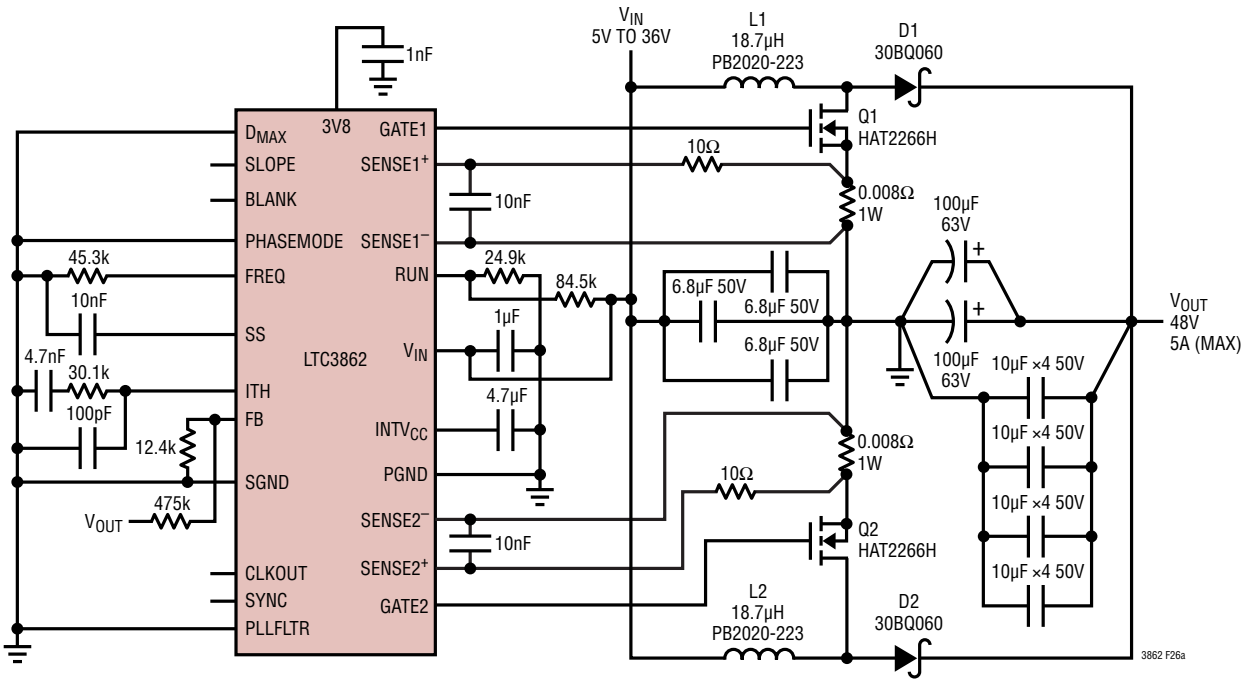

Figure 26a. A 5V to 36V Input, 48V/5A Output 2-Phase Boost Converter Application Circuit

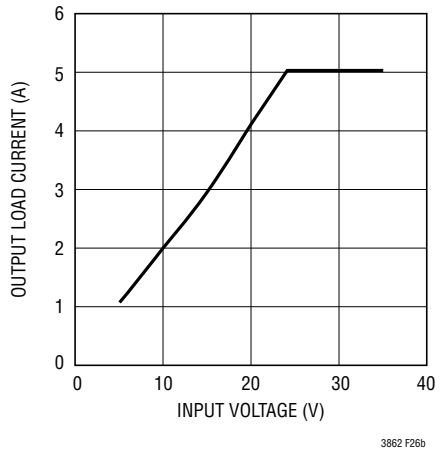

Figure 26b. Output Current vs Input Voltage

The saturation current rating of the inductors must therefore exceed:

$$I_{L(SAT)} \geq \frac{1}{n} \bullet \left(1+\frac{\chi}{2}\right) \bullet \frac{1.3 \bullet I_{O(MAX)}}{1-D_{MAX}}$$

$$= \frac{1}{2} \bullet \left(1+\frac{0.4}{2}\right) \bullet \frac{1.3 \bullet 5A}{1-0.505} = 7.9A$$

The inductor value chosen was 18.7µH and the part number is PB2020-223, manufactured by Pulse Engineering. This inductor has a saturation current rating of 20A.

8. The power MOSFET chosen for this application is a Renesas HAT2266H. This MOSFET has a typical $R_{DS(ON)}$ of 11mΩ at V_{GS} = 4.5V and 9.2mΩ at V_{GS} = 10V. The BV_{DSS} is rated at a minimum of 60V and the maximum continuous drain current is 30A. The typical gate charge is 25nC for a V_{GS} = 4.5V. Last but not least, this MOSFET has an absolute maximum avalanche energy rating EAS of 34mJ, indicating that it is capable of avalanche without catastrophic failure.

9. The total IC quiescent current, IC power dissipation and maximum junction temperature are approximately:

$$I_{Q(TOT)} = I_Q + 2 \bullet Q_{G(TOT)} \bullet f$$
$$= 3mA + 2 \bullet 25nC \bullet 300kHz = 18mA$$

$$P_{DISS} = 24V \bullet 18mA = 432mW$$

$$T_J = 70°C + 432mW \bullet 34°C/W = 84.7°C$$

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10. The inductor ripple current was chosen to be 40% and the maximum load current is 5A. For a current limit set at 30% above the maximum load current, the maximum switch and sense resistor currents are:

$$I_{SW(MAX)} = I_{R(SENSE)} = \frac{1}{n} \bullet \left(1 + \frac{\chi}{2}\right) \bullet \frac{1.3 \bullet I_{O(MAX)}}{1 - D_{MAX}}$$

$$= \frac{1}{2} \bullet \left(1 + \frac{0.4}{2}\right) \bullet \frac{1.3 \bullet 5A}{1 - 0.505} = 7.9A$$

11. The maximum current sense threshold for the LTC3862 is 75mV at low duty cycle and a normalized slope gain of 1.0. Using Figure 21, the maximum sense voltage drops to 73mV at a duty cycle of 51% with a normalized slope gain of 1, so the sense resistor is calculated to be:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{SW(MAX)}} = \frac{73mV}{7.9A} = 9.2m\Omega$$

For this application a 8mΩ, 1W surface mount resistor was used for each phase.

12. The power dissipated in the sense resistors in current limit is:

$$P_{R(SENSE)} = \left(\frac{1.3 \bullet I_{O(MAX)}}{n \bullet \left(1 - D_{MAX}\right)}\right)^2 \bullet R_{SENSE} \bullet D_{MAX}$$

$$= \left(\frac{1.3 \bullet 5}{2 \bullet \left(1 - 0.505\right)}\right)^2 \bullet 0.009 \bullet 0.505$$

$$= 0.20W$$

13. The average current in the boost diodes is half the output current (5A/2 = 2.5A), but the peak current in each diode is:

$$I_{D(PEAK)} = \frac{1}{n} \bullet \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

$$= \frac{1}{2} \bullet \left(1 + \frac{0.4}{2}\right) \bullet \frac{5A}{1 - 0.505} = 6.06A$$

The diode chosen for this application is the 30BQ060, manufactured by International Rectifier. This surface mount diode has a maximum average forward current of 3A at 125°C and a maximum reverse voltage of 60V. The maximum forward voltage drop at 25°C is 0.65V and is 0.42V at 125°C (the positive TC of the series resistance is compensated by the negative TC of the diode forward voltage).

The power dissipated by the diode is approximately:

$$P_D = I_{D(PEAK)} \bullet V_{F(PEAK)} \bullet (1 - D_{MAX})$$

$$= 6.06A \bullet 0.42V \bullet (1 - 0.505) = 1.26W$$

14. Two types of output capacitors are connected in parallel for this application; a low ESR ceramic capacitor and an aluminum electrolytic for bulk storage. For a 1% contribution to the total ripple voltage, the maximum ESR of the composite output capacitance is approximately:

$$ESR_{COUT} \leq \frac{0.01 \bullet V_{OUT}}{I_{D(PEAK)}} = \frac{0.01 \bullet 48V}{4.4A} = 0.109\Omega$$

For the bulk capacitance, which we assume contributes 1% to the total output ripple, the minimum required capacitance is approximately:

$$C_{OUT} \geq \frac{I_{O(MAX)}}{0.01 \bullet n \bullet V_{OUT} \bullet f} = \frac{5A}{0.01 \bullet 2 \bullet 48V \bullet 300kHz} T$$

$$= 17.5\mu F$$

For this application, in order to obtain both low ESR and an adequate ripple current rating (see Figure 24), two 100µF, 63V aluminum electrolytic capacitors were connected in parallel with four 6.8µF, 50V ceramic capacitors. Figure 27 illustrates the switching waveforms for this application circuit.

APPLICATIONS INFORMATION

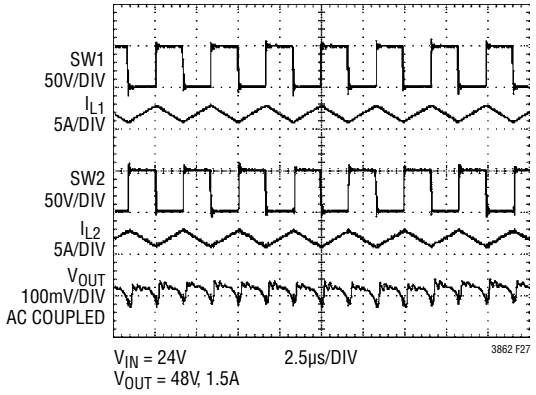


Figure 27. LTC3862 Switching Waveforms for Boost Converter

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the converter:

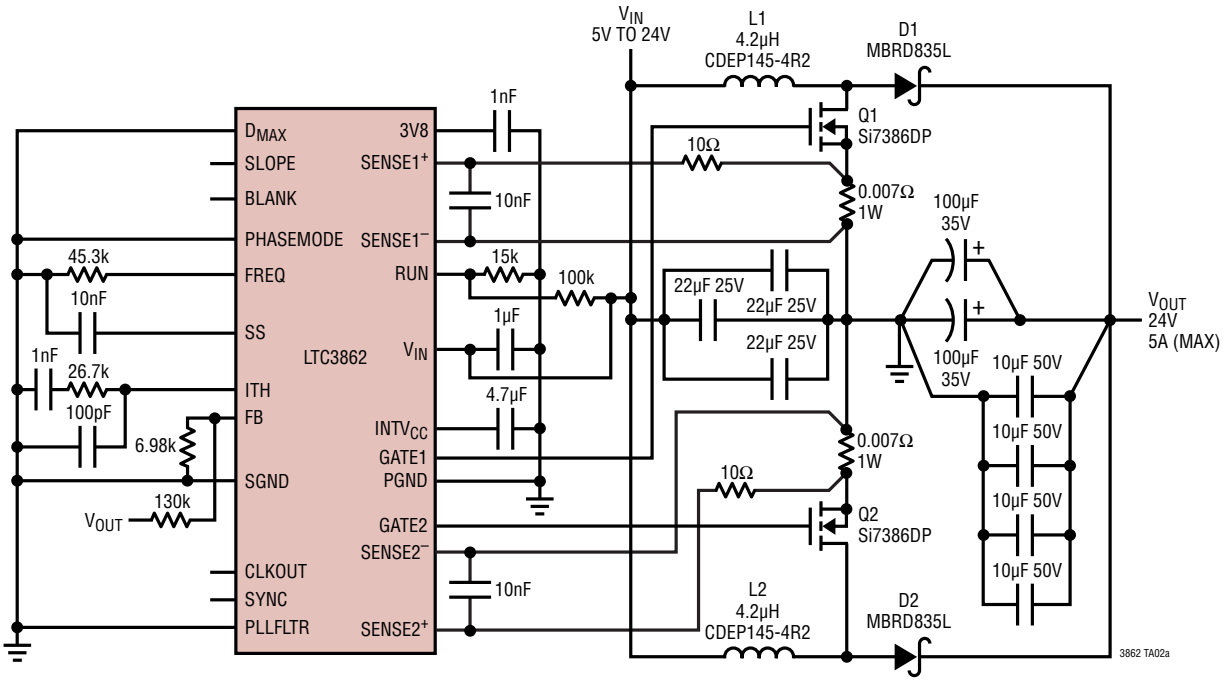
1. For lower power applications a 2-layer PC board is sufficient. However, for higher power levels, a multilayer PC board is recommended. Using a solid ground plane and proper component placement under the circuit is the easiest way to ensure that switching noise does not affect the operation.
2. In order to help dissipate the power from the MOSFETs and diodes, keep the ground plane on the layers closest to the power components. Use power planes for the MOSFETs and diodes in order to maximize the heat spreading from these components into the PCB.
3. Place all power components in a tight area. This will minimize the size of high current loops. The high di/dt loops formed by the sense resistor, power MOSFET, the boost diode and the output capacitor should be kept as small as possible to avoid EMI.
4. Orient the input and output capacitors and current sense resistors in a way that minimizes the distance between the pads connected to the ground plane. Keep the capacitors for $INTV_{CC}$, 3V8 and V_{IN} as close as possible to LTC3862.
5. Place the $INTV_{CC}$ decoupling capacitor as close as possible to the $INTV_{CC}$ and PGND pins, on the same layer as the IC. A low ESR (X5R or better) 4.7µF to 10µF ceramic capacitor should be used.
6. Use a local via to ground plane for all pads that connect to the ground. Use multiple vias for power components.
7. Place the small-signal components away from high frequency switching nodes on the board. The pinout of the LTC3862 was carefully designed in order to make component placement easy. All of the power components can be placed on one side of the IC, away from all of the small-signal components.
8. The exposed area on the bottom of the QFN package is internally connected to PGND; however it should not be used as the main path for high current flow.
9. The MOSFETs should also be placed on the same layer of the board as the sense resistors. The MOSFET source should connect to the sense resistor using a short, wide PCB trace.
10. The output resistor divider should be located as close as possible to the IC, with the bottom resistor connected between FB and SGND. The PCB trace connecting the top resistor to the upper terminal of the output capacitor should avoid any high frequency switching nodes.
11. Since the inductor acts like a current source in a peak current mode control topology, its placement on the board is less critical than the high di/dt components.
12. The $SENSE^+$ and $SENSE^-$ PCB traces should be routed parallel to one another with minimum spacing in between all the way to the sense resistor. These traces should avoid any high frequency switching nodes in the layout. These PCB traces should also be Kelvin-connected to the interior of the sense resistor pads, in order to avoid sensing errors due to parasitic PCB resistance IR drops.

APPLICATIONS INFORMATION

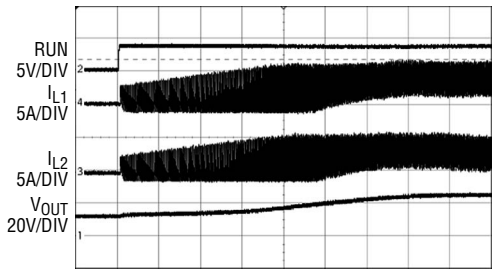
13. If an external RC filter is used between the sense resistor and the SENSE+ and SENSE– pins, these filter components should be placed as close as possible to the SENSE+ and SENSE– pins of the IC. Ensure that the SENSE– line is connected to the ground only at the point where the current sense resistor is grounded.
14. Keep the MOSFET drain nodes (SW1, SW2) away from sensitive small-signal nodes, especially from the opposite channel's current-sensing signals. The SW nodes can have slew rates in excess of 1V/ns relative to ground and should therefore be kept on the "output side" of the LTC3862.
15. Check the stress on the power MOSFETs by independently measuring the drain-to-source voltages directly across the devices terminals. Beware of inductive ringing that could exceed the maximum voltage rating of the MOSFET. If this ringing cannot be avoided and exceeds the maximum rating of the device, choose a higher voltage rated MOSFET or consider using a snubber.
16. When synchronizing the LTC3862 to an external clock, use a low impedance source such as a logic gate to drive the SYNC pin and keep the lead as short as possible.

TYPICAL APPLICATIONS

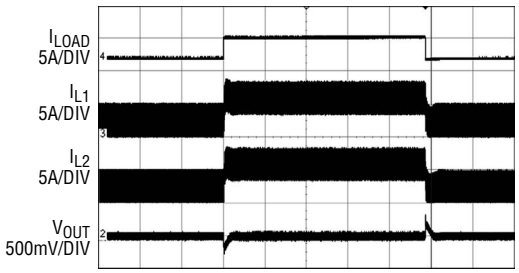
A 12V Input, 24V/5A Output 2-Phase Boost Converter Application Circuit



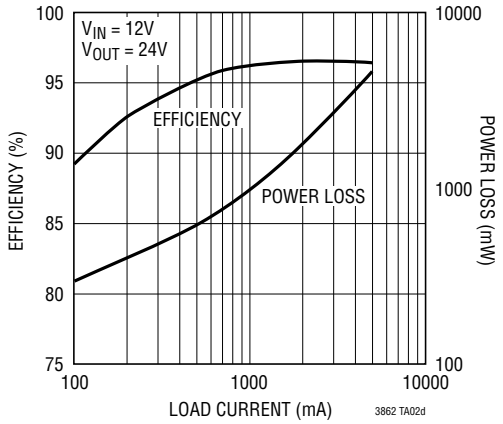
Start-Up



Load Step

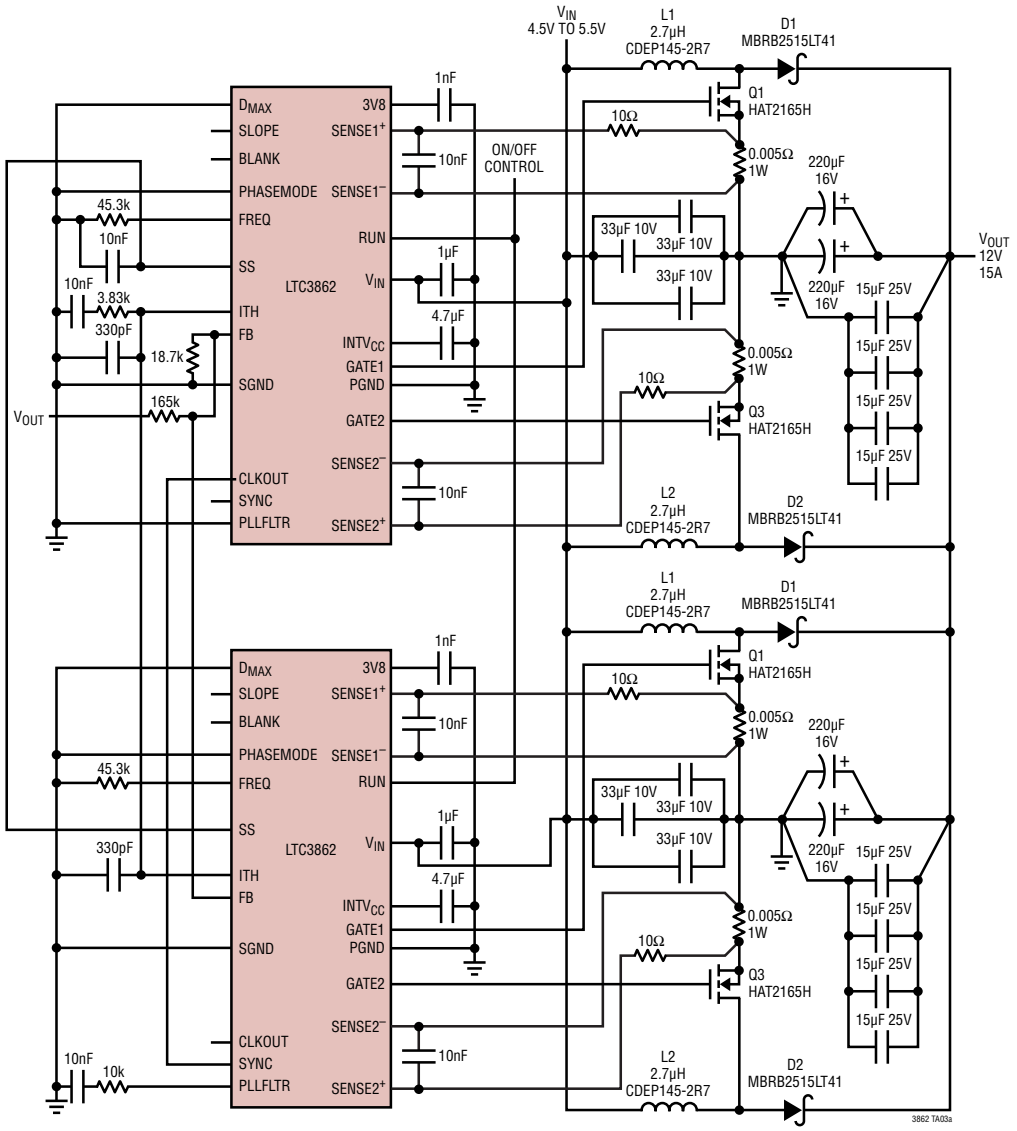


Efficiency

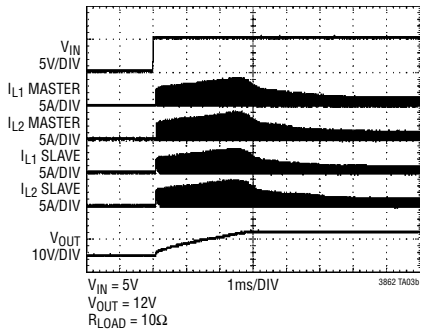


TYPICAL APPLICATIONS

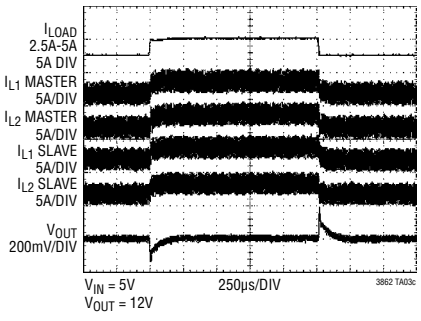
A 4.5V to 5.5V Input, 12V/15A Output 4-Phase Boost Converter Application Circuit



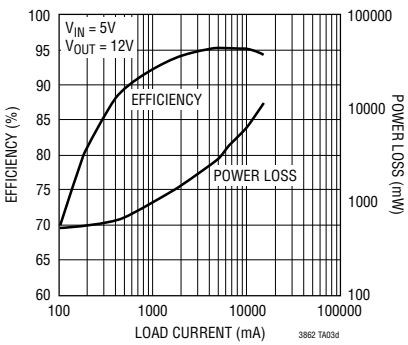
Start-Up



Load Step



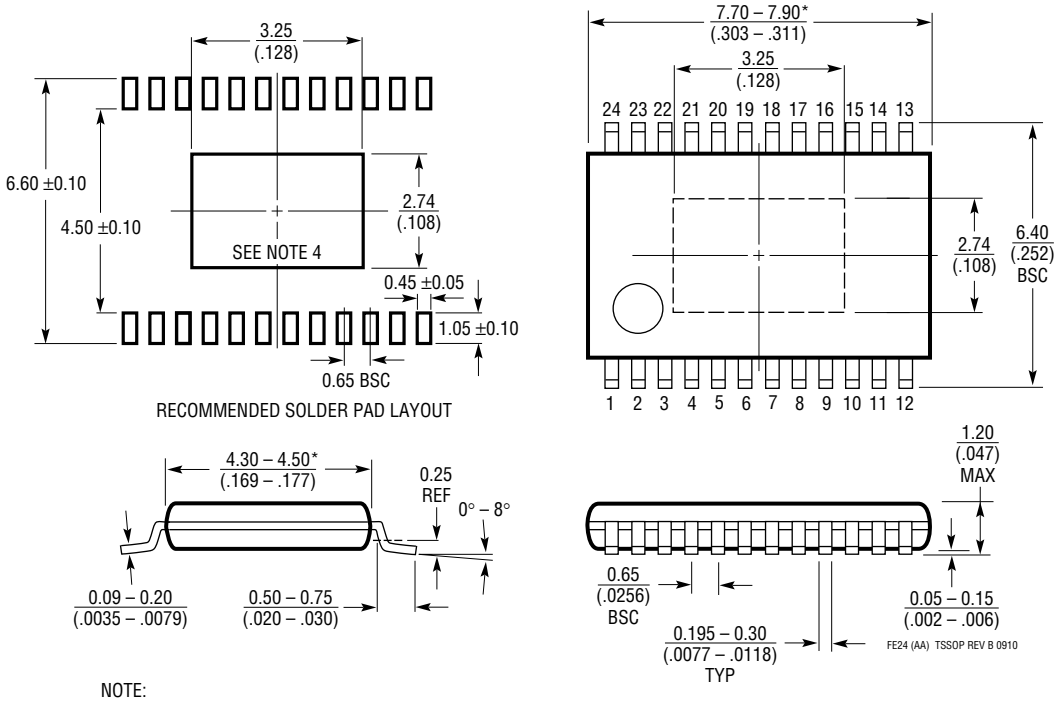
Efficiency



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
24-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1771 Rev B)
Exposed Pad Variation AA



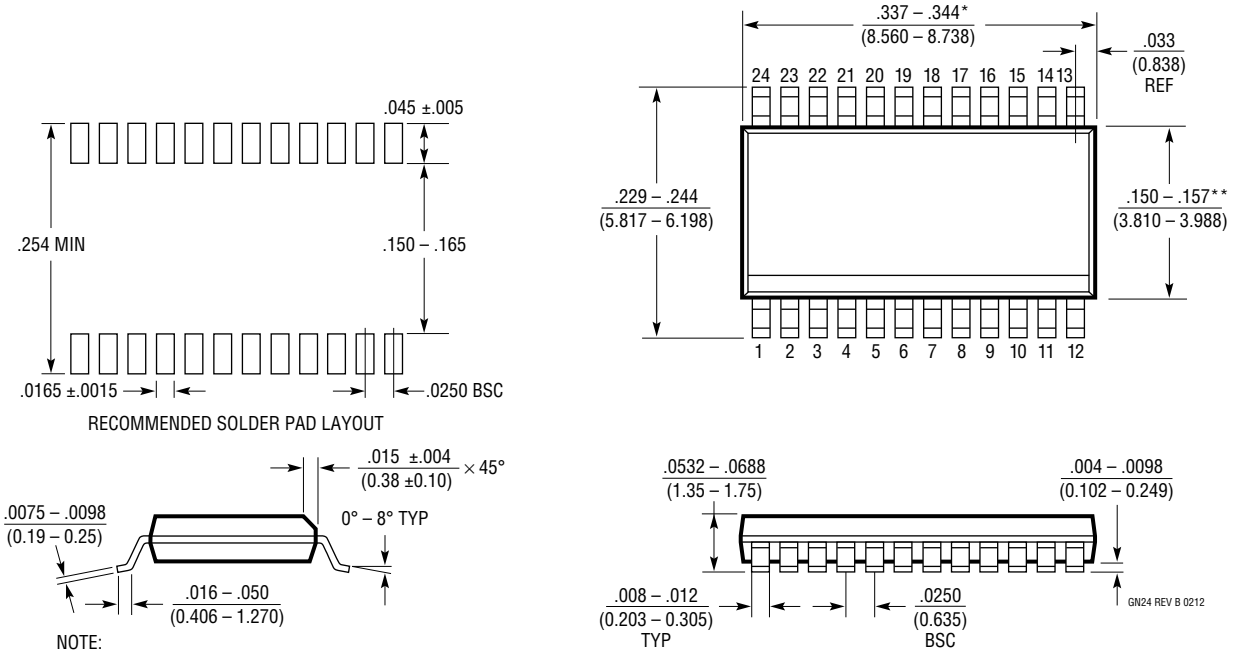
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

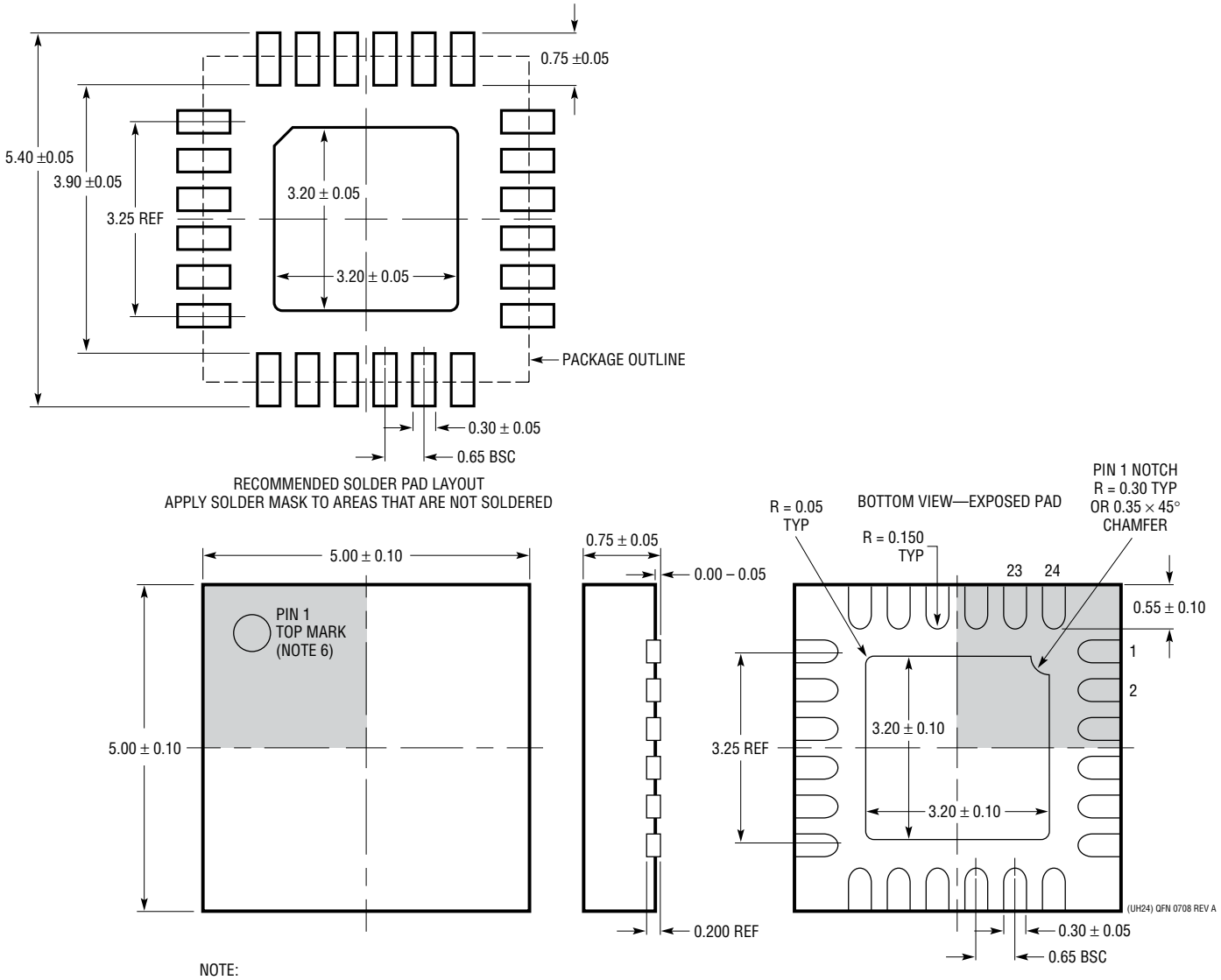
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UH Package
24-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1747 Rev A)



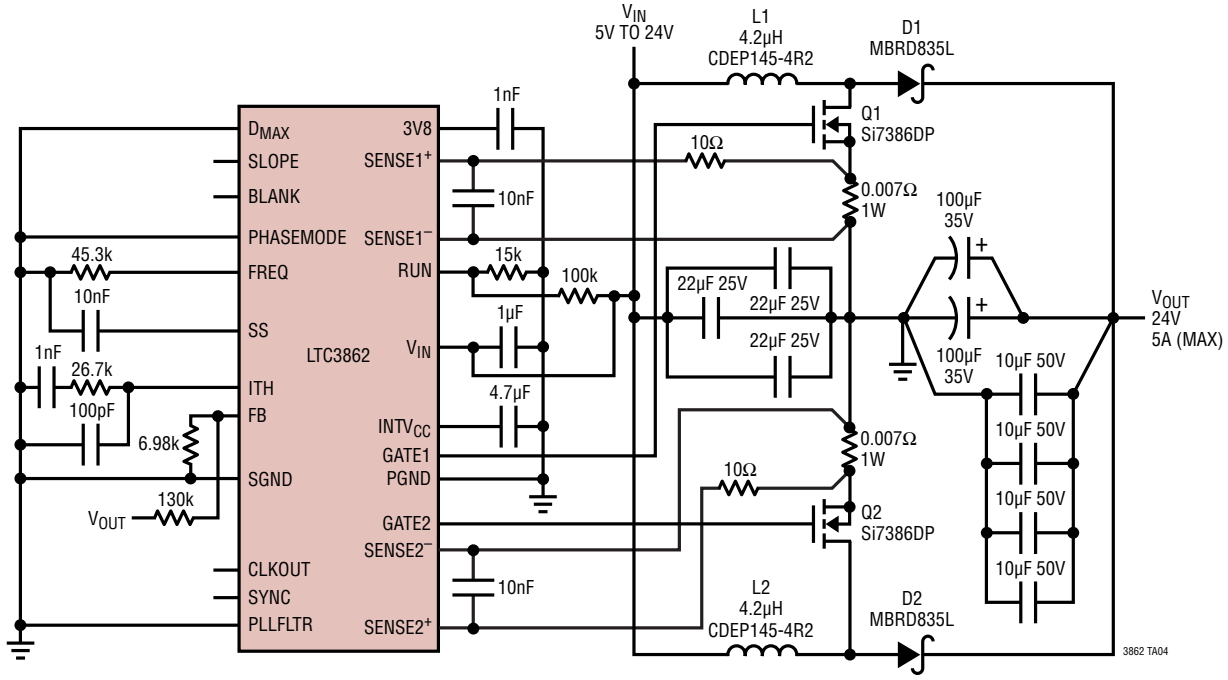
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	12/13	Added Comparison table	1
		Added Note 9	4
		Added pin number registers	9

TYPICAL APPLICATION

A 12V Input, 24V/5A Output 2-Phase Boost Converter Application Circuit



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3787/ LTC3787-1	Single Output, Dual Channel Multiphase Synchronous Step-Up Controller	4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHz to 900kHz Operating Frequency, 4mm × 5mm QFN-28, SSOP-28
LTC3788-1	Dual Output, Multiphase Synchronous Step-Up Controller	4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHz to 900kHz Fixed Frequency, 5mm × 5mm QFN-32, SSOP-28
LTC3786	Low IQ Synchronous Step-Up Controller	4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHz to 900kHz Fixed Operating Frequency, 3mm × 3mm QFN-16, MSOP-16E
LT3757A	Boost, Flyback, SEPIC and Inverting Controller	2.9V ≤ V_{IN} ≤ 40V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 3mm × 3mm DFN-10 and MSOP-10E Packages
LTC3859AL	Low I_Q, Triple Output Buck/Buck/Boost Synchronous DC/DC Controller	All Outputs Remain in Regulation Through Cold Crank, 4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 38V, $V_{OUT(BUCKS)}$ Up to 24V, $V_{OUT(BOOST)}$ Up to 60V, I_Q = 28µA
LTC3789	High Efficiency Synchronous 4-Switch Buck-Boost DC/DC Controller	4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 38V, 4mm × 5mm QFN-28, SSOP-28