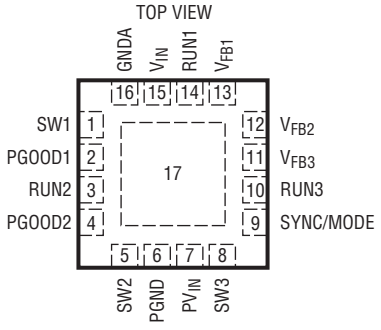
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage ..... –0.3V to 6V
RUNx, PGOODx ..... –0.3V to (V_{IN} + 0.3V)
V_{FBx}, SYNC/MODE ..... –0.3V to (V_{IN} + 0.3V)
SWx ..... –0.3V to (V_{IN} + 0.3V)
P-Switch Source Current (DC) (Note 8) 1.1A
N-Channel Sink Current (DC) (Note 8) 1.1A
Peak SW Sink and Source Current (Note 8) 1.3A
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION

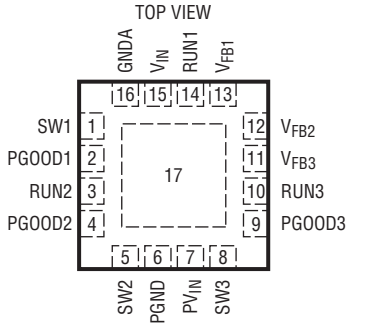
LTC3545



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 55°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

LTC3545-1



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 55°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3545EUD#PBF	LTC3545EUD#TRPBF	LCSR	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC3545IUD#PBF	LTC3545IUD#TRPBF	LCSR	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC3545EUD-1#PBF	LTC3545EUD-1#TRPBF	LDDP	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC3545IUD-1#PBF	LTC3545IUD-1#TRPBF	LDDP	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = PV_{IN} = 3.6V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
General Characteristics							
V_{IN}	Input Voltage Range		●	2.25		5.5	V
V_{FBx}	Regulated Feedback Voltage (Note 5)	T_A = 25°C		0.592	0.6	0.608	V
		0°C ≤ T_A ≤ 85°C	●	0.588	0.6	0.612	V
		LTC3545IUD; –40°C < T_A < 125°C	●	0.588	0.6	0.612	V
ΔV_{FBx}	Reference Voltage Line Regulation (Note 5)	V_{IN} = 2.25V to 5.5V	●		0.08	0.15	%/V

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = PV_{IN} = 3.6V unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{LOADREG}$	Output Voltage Load Regulation (Notes 5, 6)				0.5		%
I_{FBx}	Feedback Pin Leakage (Note 5)					80	nA
I_S	Input DC Bias Current (All Regulators Enabled) Pulse Skip (Active Mode) Burst Mode Operation (All Regulators Sleeping) Shutdown (RUN_X = 0V)	I_{LOAD} = 0A, 2.25MHz V_{FBx} = 0.5V V_{FBx} = 0.7V			 680 58 0.1	 750 70 2.0	 µA µA µA
f_{OSC}	Oscillator Frequency		●	1.8	2.25	2.7	MHz
f_{SYNC}	Synchronization Frequency	LTC3545 Only	●	1		3	MHz
$V_{RUN(HIGH)}$	RUNx Input High Voltage		●	1			V
$V_{RUN(LOW)}$	RUNx Input Low Voltage		●			0.3	V
I_{RUNx}	RUN Leakage Current				±0.1	±1	µA
I_{LSWx}	SWx Leakage	V_{RUNx} = 0V, V_{SWx} = 0V or 5.5V, V_{IN} = 5.5V			±0.1	±1	µA
I_{SYNC}	SYNC Leakage	V_{RUN} = 0V, V_{SYNC} = 0V or 5.5V, V_{IN} = 5.5V			±0.1	±1	µA
T_{PGOODx}	Power Good Threshold–Deviation From V_{FB} Steady State (0.6V)	V_{FBx} Ramping Up V_{FBx} Ramping Down			–7.5 –10		% %
R_{PGOODx}	Power Good Pull-Down On-Resistance	I_{PGD} = 50mA	●		14	50	Ω
MODE/SYNC	Thresholds				0.93		V
Individual Regulator Characteristics (One Regulator Enabled)							
t_{SS}	Soft-Start Period	V_{FBx} = 10% to 90% Fullscale			850	1100	µs
I_{PK}	Peak Switch Current Limit			1	1.3	1.6	A
I_Q	Input DC Bias Current Pulse Skip (Active Mode) Burst Mode Operation (Sleeping)	I_{LOAD} = 0A, 2.25MHz V_{FBx} = 0.5V V_{FBx} = 0.7V			 310 31		 µA µA
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET (Note 7)	I_{SWx} = 100mA			0.35		Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET (Note 7)	I_{SWx} = –100mA			0.35		Ω
V_{UVLO}	Undervoltage Lockout	(High V_{CC} to Low)	●		1.8	2.25	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3545E/LTC3545E-1 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3545I/LTC3545I-1 are guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D)(68°C/W)$$

This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: The LTC3545/LTC3545-1 are tested in a proprietary test mode that connects V_{FB} to the output of the error amplifier.

Note 6: Load regulation is inferred by measuring the regulation loop gain.

Note 7: The QFN switch-on resistance is guaranteed by correlation to water level measurements.

Note 8: Guaranteed by long-term current density limitations.

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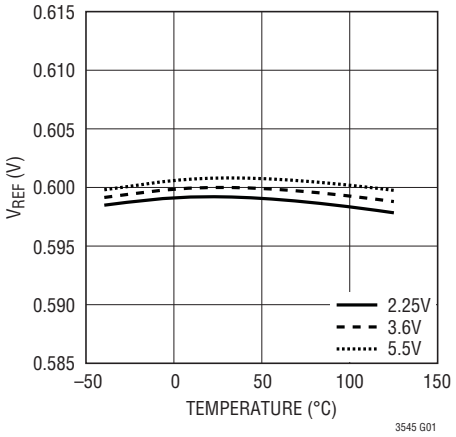
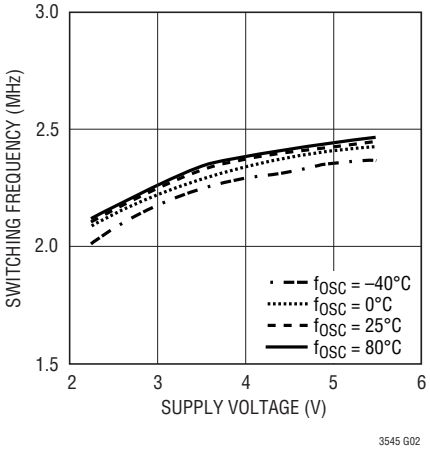
TYPICAL PERFORMANCE CHARACTERISTICS

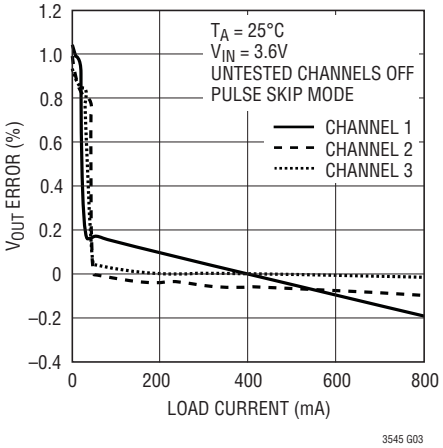
V_{REF} vs Temperature at 2.25V, 3.6V, 5.5V



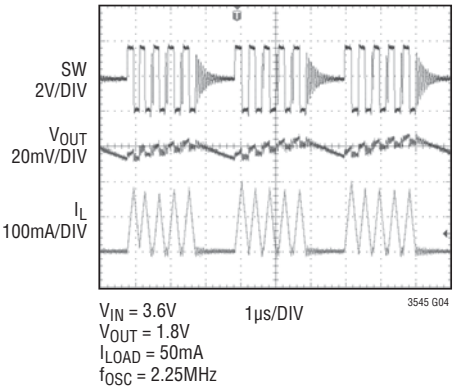
Switching Frequency vs Supply Voltage and Temperature



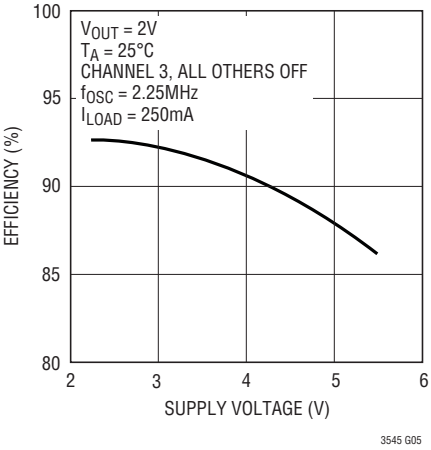
Load Regulation, All Channels



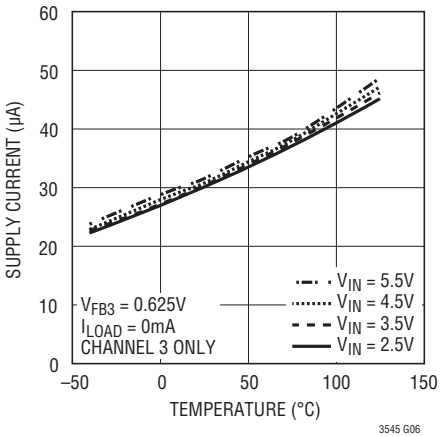
Burst Mode Operation



Efficiency vs Supply Voltage



Supply Current vs Temperature Burst Mode Operation



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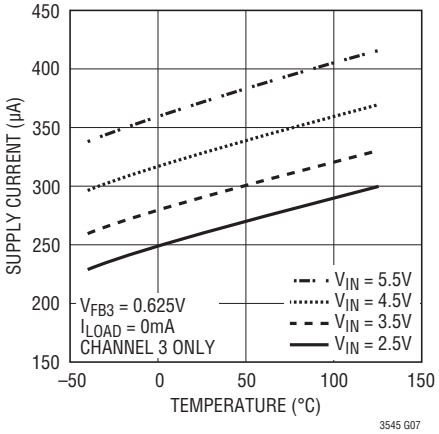
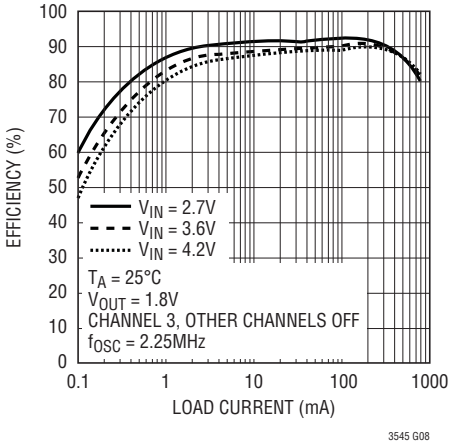
TYPICAL PERFORMANCE CHARACTERISTICS

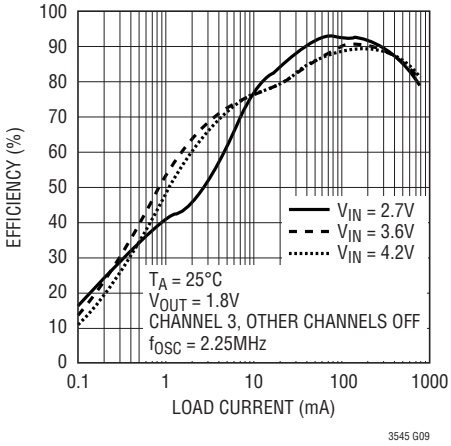
Supply Current vs Temperature, Pulse Skipping



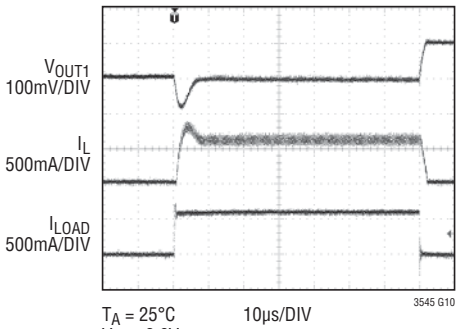
Efficiency vs Load Current, Burst Mode Operation



Efficiency vs Load Current, Pulse Skipping Operation

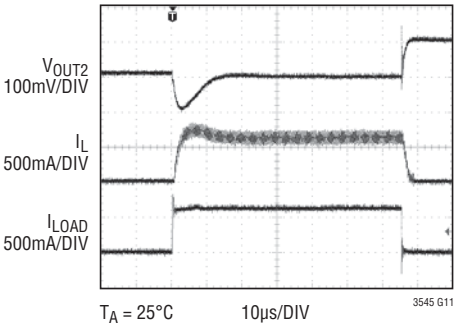


Channel 1 Load Step Response



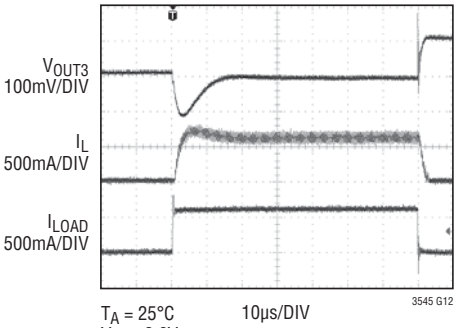
TA = 25°C 10µs/DIV
VIN = 3.6V
VOUT = 1.2V
LOAD STEP 0mA TO 600mA
Burst Mode OPERATION

Channel 2 Load Step Response



TA = 25°C 10µs/DIV
VIN = 3.6V
VOUT = 1.5V
LOAD STEP 0mA TO 600mA
Burst Mode OPERATION

Channel 3 Load Step Response



TA = 25°C 10µs/DIV
VIN = 3.6V
VOUT = 1.8V
LOAD STEP 0mA TO 600mA
Burst Mode OPERATION

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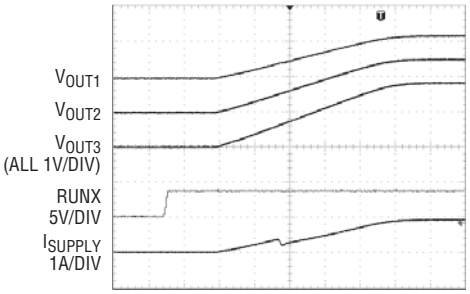
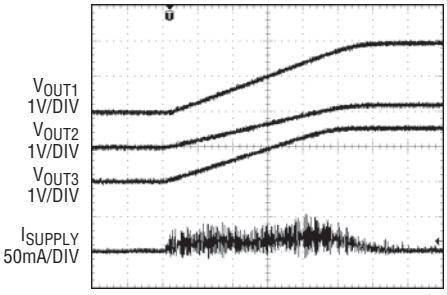
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up From Shutdown Loaded



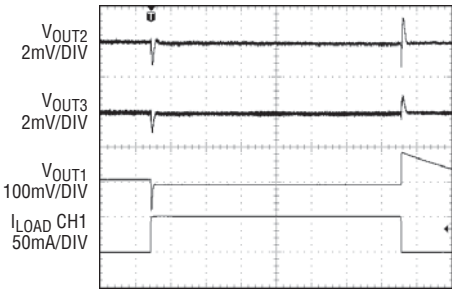
T_A = 25°C 200µs/DIV
V_{IN} = 3.6V
I_{LOAD} = 600mA, ALL CHANNELS

Start-Up From Shutdown No Load



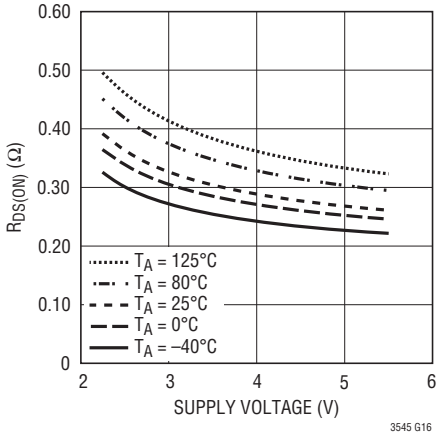
T_A = 25°C 200µs/DIV
V_{IN} = 3.6V
I_{LOAD} = 0, ALL CHANNELS

Load Step Crosstalk

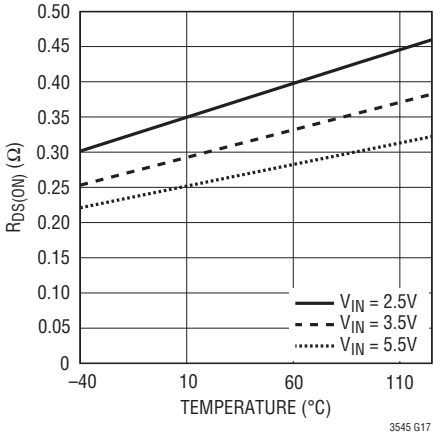


T_A = 25°C 200µs/DIV
V_{IN} = 3.6V
500mA LOAD STEP IN CHANNEL1
CHANNELS 2 AND 3 LOADED AT 400mA EACH

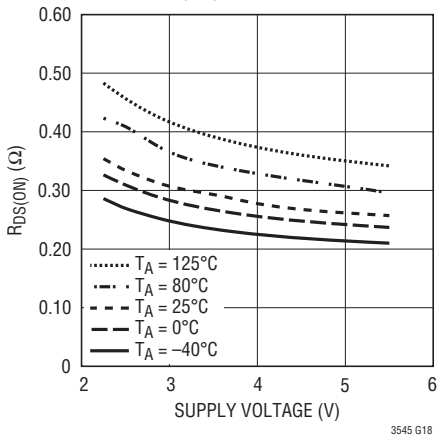
PFET $R_{DS(ON)}$ vs Supply Voltage



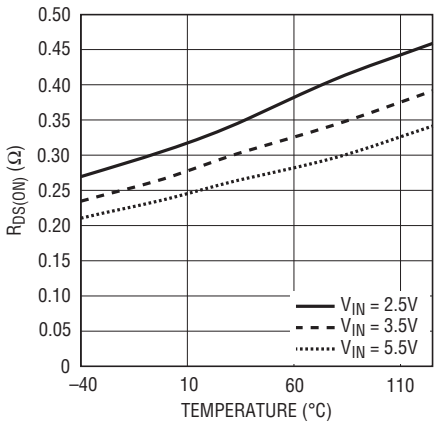
PFET $R_{DS(ON)}$ vs Temperature



NFET $R_{DS(ON)}$ vs Supply Voltage



NFET $R_{DS(ON)}$ vs Temperature



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PIN FUNCTIONS

SW1 (Pin 1): Switch Node Connection to Inductor for Regulator 1. This pin connects to the internal power MOSFET switches.

PGOOD1 (Pin 2): This open-drain output voltage is pulled to a logic low when V_{FB1} is below 0.54V (V_{OUT1} is below 90% of regulated level).

RUN2 (Pin 3): Regulator 2 Enable Pin. Apply a voltage greater than $V_{RUN(HIGH)}$ to enable this regulator.

PGOOD2 (Pin 4): This open-drain output voltage is pulled to a logic low when V_{FB2} is below 0.54V (V_{OUT2} is below 90% of regulated level).

SW2 (Pin 5): Switch Node Connection to Inductor for Regulator 2. This pin connects to the internal power MOSFET switches.

PGND (Pin 6): Regulators 2 and 3 Power Path Return.

PV_{IN} (Pin 7): Power Path Supply Pin for Regulators 2 and 3. This pin must be closely decoupled to PGND, with a 4.7µF or greater ceramic capacitor.

SW3 (Pin 8): Switch Node Connection to Inductor for Regulator 3. This pin connects to the internal power MOSFET switches.

SYNC/MODE (Pin 9, LTC3545 Only): Mode Select and External Clock Input. When pulled low, part operates in Burst Mode operation. When pulled high, part operates in pulse skipping mode. When driven by a 1MHz to 3MHz external clock, the part operates in pulse skipping mode with a switching frequency equal to the external clock.

PGOOD3 (Pin 9, LTC3545-1 Only): This open-drain output voltage is pulled to a logic low when V_{FB3} is below 0.54V (V_{OUT3} is below 90% of regulated level). The LTC3545-1 operates in Burst Mode operation only.

RUN3 (Pin 10): Regulator 3 Enable Pin. Apply a voltage greater than $V_{RUN(HIGH)}$ to enable this regulator.

V_{FB3} (Pin 11): Regulator 3 Feedback Pin. This pin receives the feedback voltage from an external resistive divider across the output.

V_{FB2} (Pin 12): Regulator 2 Feedback Pin. This pin receives the feedback voltage from an external resistive divider across the output.

V_{FB1} (Pin 13): Regulator 1 Feedback Pin. This pin receives the feedback voltage from an external resistive divider across the output.

RUN1 (Pin 14): Regulator 1 Enable Pin. Apply a voltage greater than $V_{RUN(HIGH)}$ to enable this regulator.

V_{IN} (Pin 15): Supply Pin for Internal Reference and Control Circuitry. Power path supply for regulator 1.

GNDA (Pin 16): Ground Pin for Internal Reference and Control Circuitry. Power path return for regulator 1.

Exposed Pad (Pin 17): GND. Must be soldered to the PCB.

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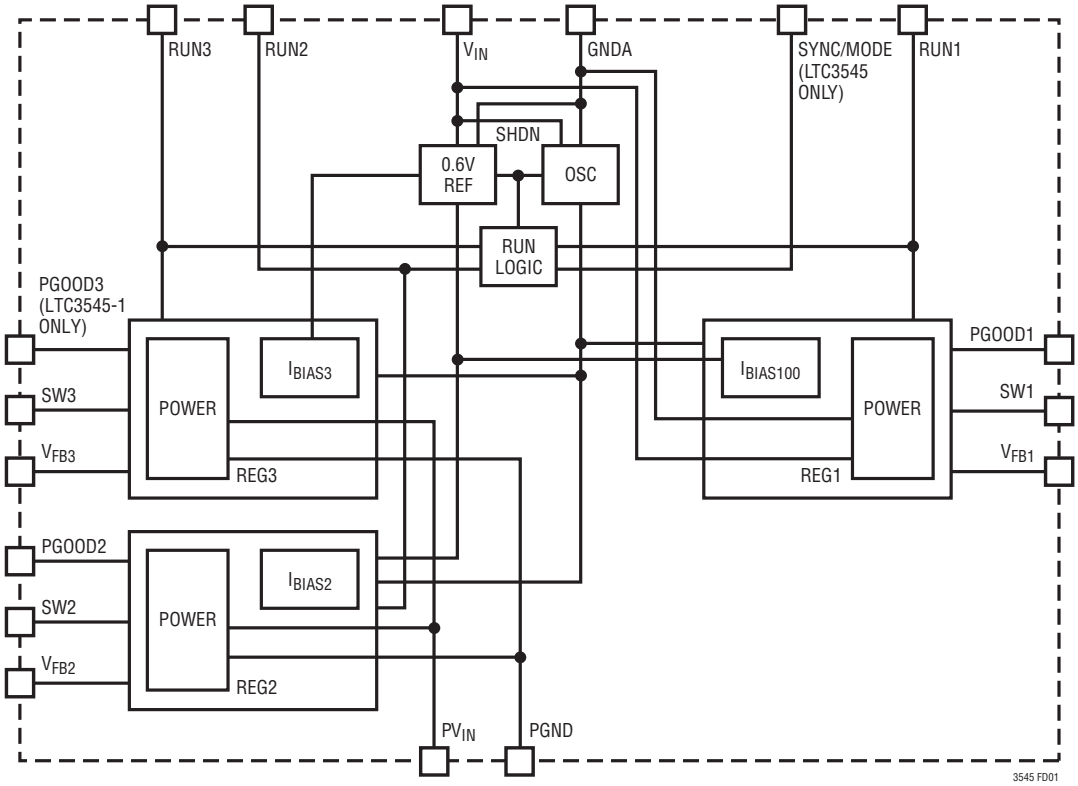
FUNCTIONAL DIAGRAMS



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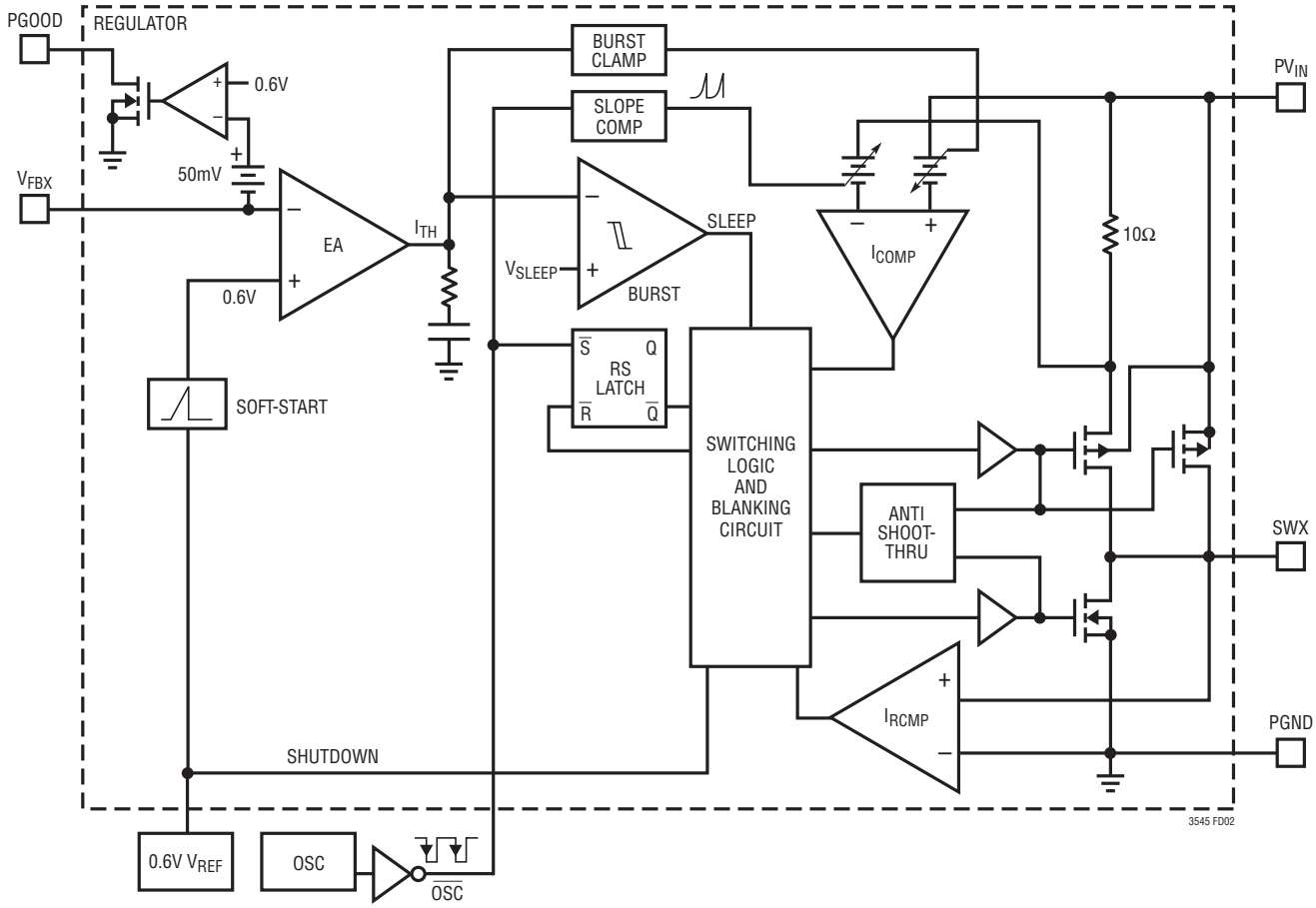
FUNCTIONAL DIAGRAMS



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OPERATION

MAIN CONTROL LOOP

The LTC3545/LTC3545-1 use a constant frequency, current mode step-down architecture. Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. During normal operation, the internal top power MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the current comparator, I_{COMP}, resets the RS latch. The peak inductor current at which I_{COMP} resets the RS latch, is controlled by the output of error amplifier EA. When the load current increases, it causes a slight decrease in the feedback voltage FB relative to the 0.6V reference, which in turn, causes the EA amplifier's output voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator, I_{RCMP}, or the beginning of the next clock cycle.

PULSE SKIPPING/Burst Mode OPERATION

At light loads, the inductor current may reach zero or reverse on each pulse. The bottom MOSFET is turned off by the current reversal comparator, I_{RCMP}, and the switch voltage will ring. This is discontinuous mode operation, and is normal behavior for the switching regulator.

At very light loads, the LTC3545/LTC3545-1 will automatically begin operating in either pulse skipping or Burst Mode operation depending on the state of the MODE/SYNC pin (LTC3545). In either case the part will begin to skip cycles in order to maintain regulation.

In pulse skip mode, the current pulses are smaller and more frequent, giving lower output ripple. In this mode, internal circuitry remains on and the pulses occur more frequently resulting in lower efficiency than in Burst Mode operation at light loads.

In Burst Mode operation, the part supplies fewer, larger current pulses, resulting in higher output ripple, but much higher light load efficiency than pulse skip mode. Efficiency is also improved by turning off much of the internal circuitry during the dead time between pulses.

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OPERATION

SOFT-START

Soft-start reduces surge currents on V_{IN} and output overshoot during start-up. Soft-start on the LTC3545/LTC3545-1 is implemented by internally ramping the reference signal fed to the error amplifier over approximately a 1ms period. Figure 1 shows the behavior of the regulator channels during start-up.

Short-Circuit Protection

Short-circuit protection is achieved by monitoring the inductor current. When the current exceeds a predetermined level, the main switch is turned off, and the synchronous switch is turned on long enough to allow the current in the inductor to decay below the fault threshold. This prevents a catastrophic inductor current run-away condition, but will still provide current to the output. Output voltage regulation in this condition is not achieved.

DROPOUT OPERATION

As the input supply voltage decreases to a value approaching the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor. An important detail to remember is that at low input supply voltages, the $R_{DS(ON)}$ of the P-channel switch increases (see Typical Performance Characteristics). Therefore, the user should calculate the power dissipation when the LTC3545/LTC3545-1 is used at 100% duty cycle with low input voltage (See Thermal Considerations in the Applications Information section).

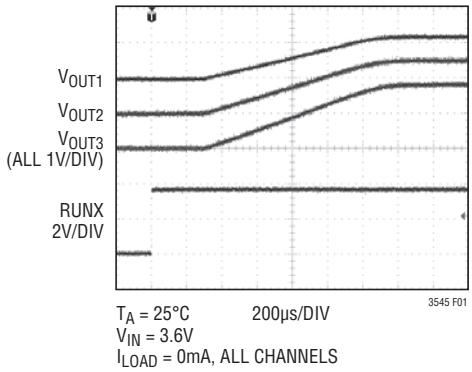

Figure 1. Start-Up from Shutdown, No Load

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APPLICATIONS INFORMATION

The basic LTC3545/LTC3545-1 application circuit is shown on the first page of this data sheet. External component selection is driven by the load requirement and begins with the selection of L followed by C_{IN} and C_{OUT}.

Inductor Selection

For most applications, the value of the inductor will fall in the range of 1µH to 10µH. Its value is chosen based on the desired ripple current. Large inductor values lower ripple current and small inductor values result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in Equation 1. A reasonable starting point for setting ripple current for an 800mA regulator is ΔI_L = 320mA (40% of 800mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 960mA rated inductor should be enough for most applications (800mA + 160mA). For better efficiency, choose a low DCR inductor.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the LTC3545/LTC3545-1 require to operate. Table 1 shows typical surface mount inductors that work well in LTC3545/LTC3545-1 applications.

Table 1. Representative Surface Mount Inductors

PART NUMBER	VALUE (µH)	DCR (Ω MAX)	MAX DC CURRENT (A)	W × L × H (mm³)
Wurth WE-TPC 744031	1.5 2.5 3.6	0.035 0.045 0.065	1.75 1.45 1.38	3.8 × 3.8 × 1.65
CoilCraft LPS4012	1 1.5 2.2 3.3	0.06 0.07 0.1 0.1	2.5 2.5 2.1 1.5	4.0 × 4.0 × 1.1
Sumida CDH38D11/SLD	1.4 2.4 3.6	0.055 0.094 0.13	1.8 1.3 1.1	4.0 × 4.0 × 1.2
Sumida CDRH3D16	1.5 2.2 3.3	0.043 0.075 0.11	1.55 1.2 1.1	3.8 × 3.8 × 1.8

C_{IN} and C_{OUT} Selection

In continuous mode, a worst-case estimate for the input current ripple can be determined by assuming that the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}, and amplitude $I_{OUT(MAX)}$. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \frac{\sqrt{V_{OUT}\left(V_{IN}-V_{OUT}\right)}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life (non-ceramic capacitors). This makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

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The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Using Ceramic Input and Output Capacitors

Higher value, lower cost, ceramic capacitors are now widely available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3545/LTC3545-1's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

However, care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN}, large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

The output voltage is set by tying V_{FB} to a resistive divider according to the following formula:

$$V_{OUT} = 0.6V \left(1 + \frac{R2}{R1} \right)$$

The external resistive divider is connected to the output allowing remote voltage sensing as shown in Figure 2.

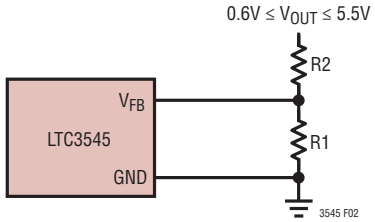

Figure 2. Setting the LTC3545 Output Voltage

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: Efficiency = 100% – (L1 + L2 + L3 + ...) where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses in LTC3545/LTC3545-1 circuits: V_{IN} quiescent current and I^2R losses. V_{IN} quiescent current loss dominates the efficiency loss at low load currents, whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of little consequence as illustrated on the front page of the data sheet.

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1. The quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, dQ, moves from PV_{IN} to ground. The resulting dQ/dt is the current out of PV_{IN} that is typically larger than the DC bias current and proportional to frequency. Both the DC bias and gate charge losses are proportional to PV_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses when in switching operation, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% total additional loss.

Thermal Considerations

The LTC3545/LTC3545-1 requires the package backplane metal to be well soldered to the PC board. This gives the QFN package exceptional thermal properties, making it difficult in normal operation to exceed the maximum junction temperature of the part. In most applications the LTC3545/LTC3545-1 do not dissipate much heat due to their high efficiency. In applications where the LTC3545/LTC3545-1 are running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part if it is not well thermally grounded. If the junction temperature reaches approximately 150°C, the power switches will be turned off and the SW nodes will become high impedance.

To prevent the LTC3545/LTC3545-1 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

As an example, consider one channel of the LTC3545/LTC3545-1 in dropout at an input voltage of 2.5V, a load current of 800mA, and an ambient temperature of 85°C. From the typical performance graph of switch resistance, the $R_{DS(ON)}$ of the P-channel switch at 85°C can be estimated as 0.42Ω. Therefore, power dissipated by the channel is:

$$P_D = I_{LOAD}^2 \bullet R_{DS(ON)} = 0.27W$$

The θ_{JA} for the 3mm × 3mm QFN package is 68°C/W. The temperature rise due to this power dissipation is:

$$T_R = \theta_{JA} \bullet P_D = 18°C$$

And a junction temperature of:

$$T_J = 85°C + 18°C = 103°C$$

which is below the maximum junction temperature of 125°C. This would not be the case if all three channels were operating at 800mA in dropout. Then T_R = 55°C, limiting the allowed ambient temperature in this scenario to less than 70°C.

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Similar situations can occur when all three channels are operating at maximum loads at high ambient temperature. As an example, consider a channel supplying 800mA at 1.8V output and 85% efficiency. The dissipated power can be calculated using

$$Loss = P_O\left(\frac{1-E}{E}\right) = 1.4W \bullet 0.17 = 0.25W$$

where P_O is the output power and E is the efficiency. In this case the temperature rise is 17°C, similar to the dropout scenario described above. Whereas one channel operating at these levels will safely fall within the temperature limitations of the part, three channels operating simultaneously at these levels will place limits on the peak ambient temperature.

Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance $R_{DS(ON)}$.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to (ΔI_{LOAD} • ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal. The regulator loop then acts to return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. For a detailed explanation of switching control loop theory, see Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25 • C_{LOAD}). Thus, a 10µF capacitor charging to 3.3V would require a 250µs rise time, limiting the charging current to about 130mA.

Design Example

As a design example, consider using the LTC3545/LTC3545-1 in a portable application with a Li-Ion battery. The battery provides V_{IN} ranging from 2.8V to 4.2V. The demand on one channel at 2.5V is 600mA. Using this channel as an example, first calculate the inductor value for 40% ripple current (240mA in this example) at maximum V_{IN}. Using a form of Equation 1:

$$L1 = \frac{2.5V}{(2.25MHz)(240mA)}\left(1-\frac{2.5V}{3.6V}\right) = 1.41\mu H$$

Use the closest standard value of 1.5µH. For low ripple applications, 10µF is a good choice for the output capacitor. A smaller output capacitor will shorten transient response settling time, but also increase the load transient ripple. A value for C5 = 4.7µF should suffice as the source impedance of a Li-Ion battery is very low. C5 and C1 both provide switching current to the output power switches. They should be placed as close a possible to the chip between V_{IN}/GNDA and PV_{IN}/PGND respectively. PV_{IN} and PGND are the supply and return power paths for both channels 2 and 3, so a value of 10µF for C1 is appropriate. The feedback resistors program the output voltage. Minimizing the current in these resistors will maximize efficiency at very light loads, but totals on the order of 200k are a good compromise between efficiency and immunity to any adverse effects of PCB parasitic capacitance on the feedback pins. Choosing 10µA as the feedback current with 0.6V feedback voltage makes R4 = 60k. A close standard 1% resistor is 60.4k. Using:

$$R3 = \left(\frac{2.5V}{0.6V}-1\right)\bullet R4 = 191.1k$$

The closest standard 1% resistor is 191k. A 20pF feedforward capacitor is recommended to improve transient response. The component values for the other channels are chosen in a similar fashion. Figure 4 shows the complete schematic for this example, along with the efficiency curve and burst mode ripple at an output current for the 2.5V output.

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PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3545/LTC3545-1. These items are also illustrated graphically in Figures 3 and 4. Figure 3 shows the power path components and traces. In this figure the feedback networks are not shown since they reside on the bottom side of the board. Check the following in your layout:

1. The power traces consisting of the PGND trace, the SW trace, the PV_{IN} trace, the V_{IN} and GNDA traces, should be kept short direct and wide.
2. Does each of the V_{FBx} pins connect directly to the respective feedback resistors? The resistive dividers must be connected between the (+) plate of the corresponding output filter capacitor (e.g. C2) and GNDA. If the circuit being powered is at such a distance from the part where voltage drops along circuit traces are large, consider a Kelvin connection from the powered circuit back to the resistive dividers.
3. Keep C1 and C5 as close to the part as possible.
4. Keep the switching nodes (SWx) away from the sensitive V_{FBx} nodes.
5. Keep the ground connected plates of the input and output capacitors as close as possible.
6. Care should be taken to provide enough space between unshielded inductors in order to minimize any transformer coupling.

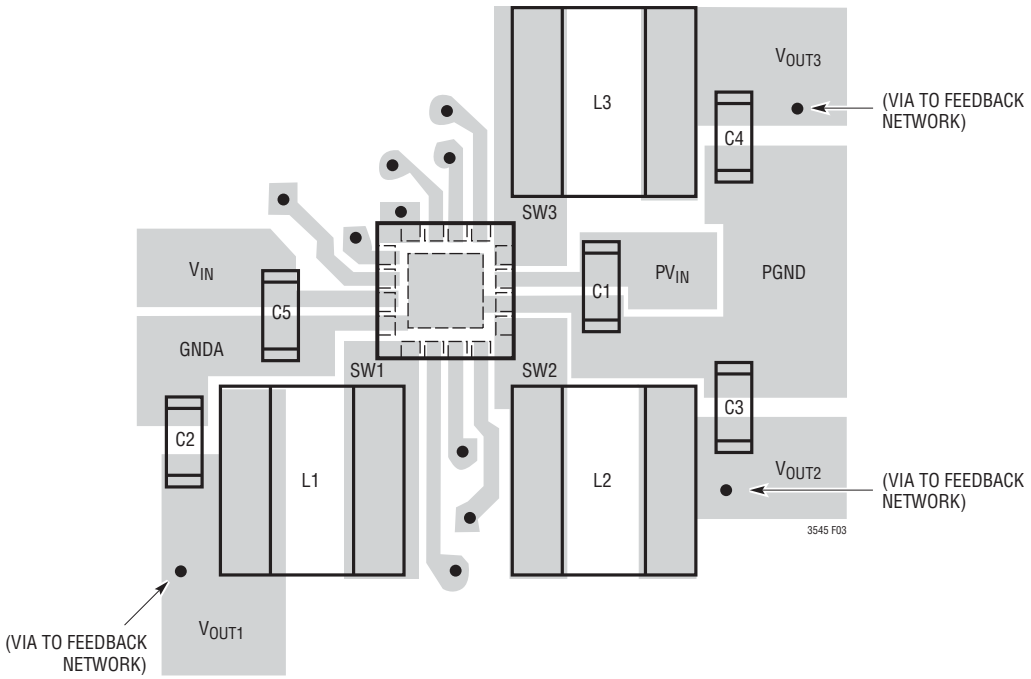

Figure 3. Layout Diagram

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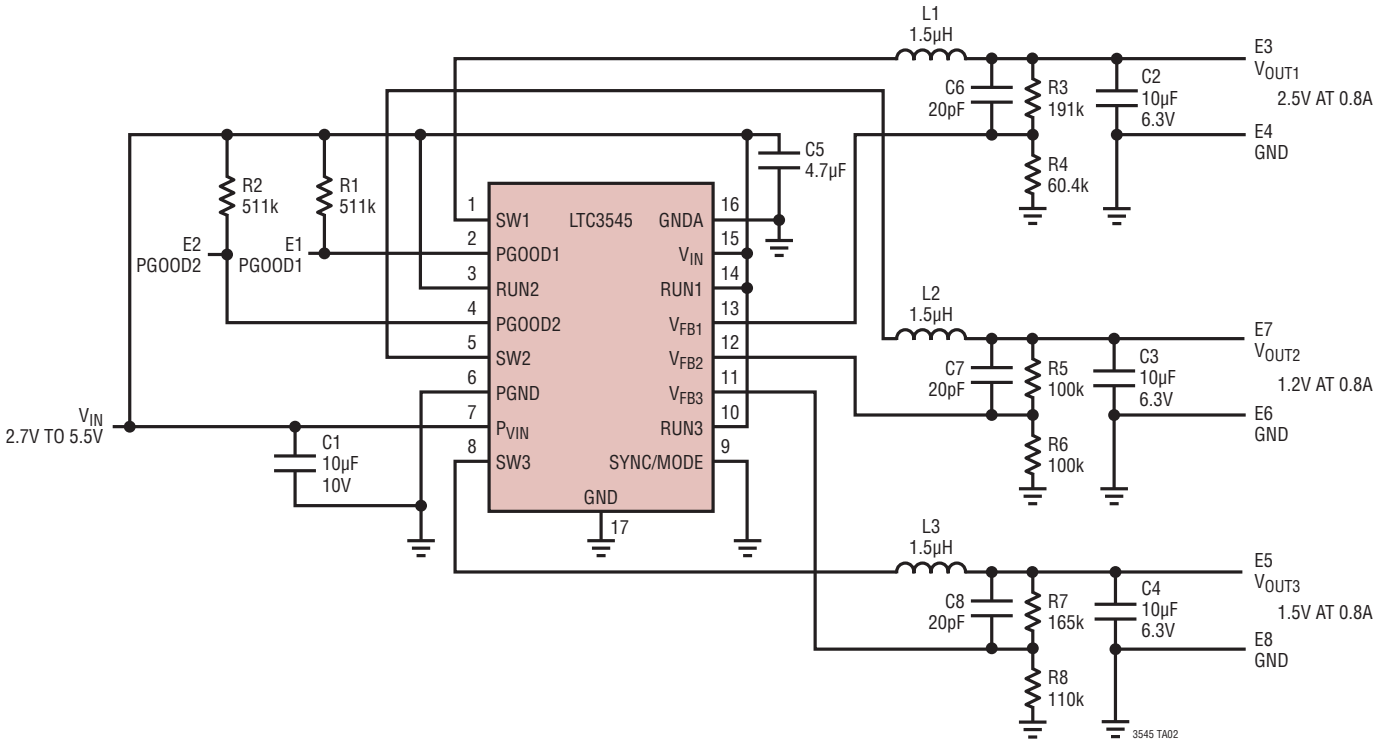
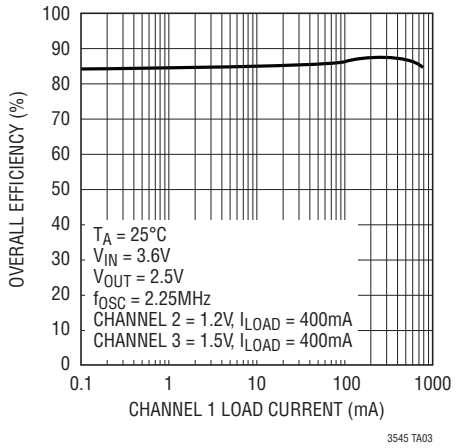
TYPICAL APPLICATIONS



Overall Efficiency vs Channel 1 Load Current



Burst Mode Ripple

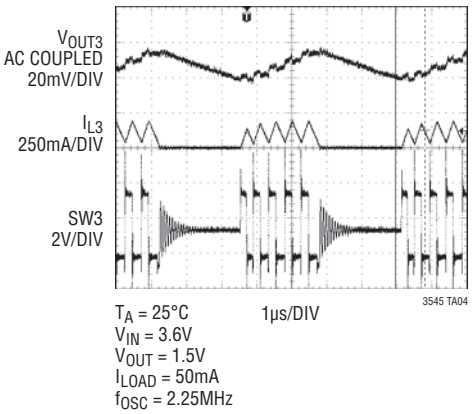


Figure 4. LTC3545 Low Ripple Burst Mode Operation

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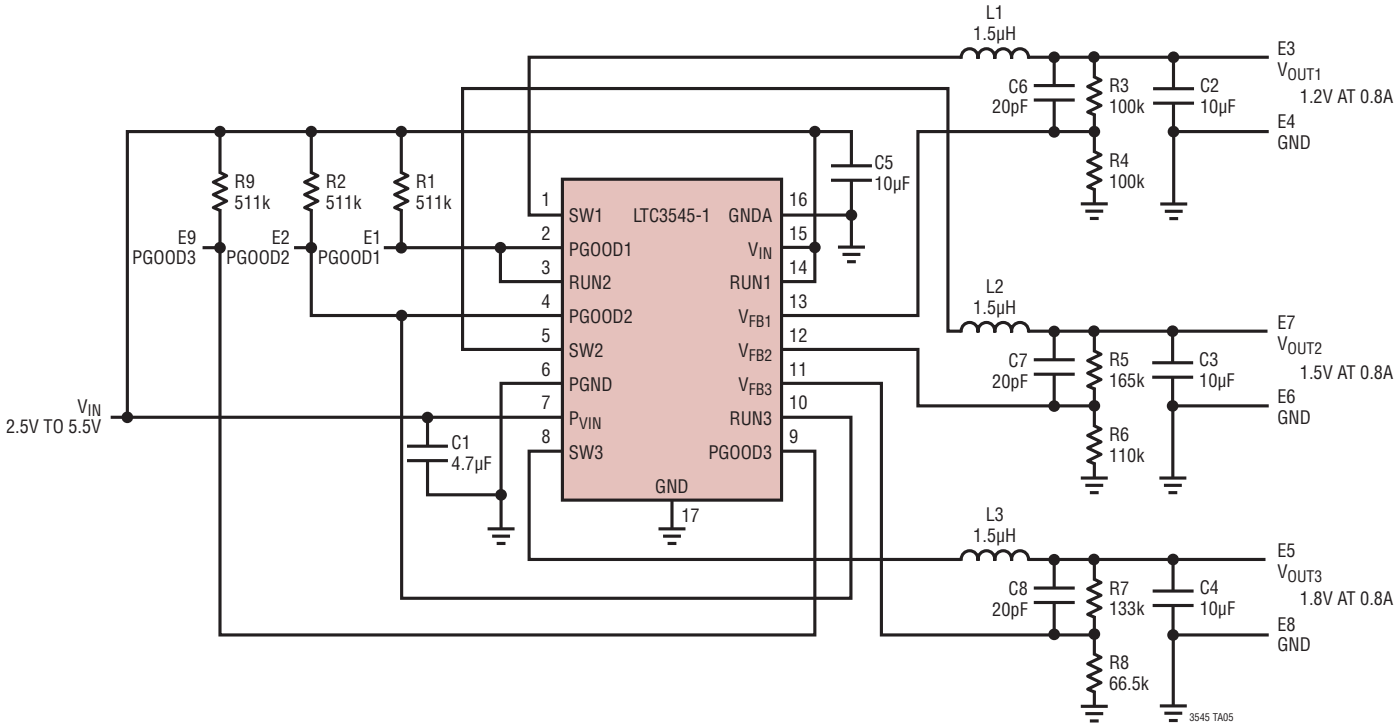

3-Channel Power Sequencing

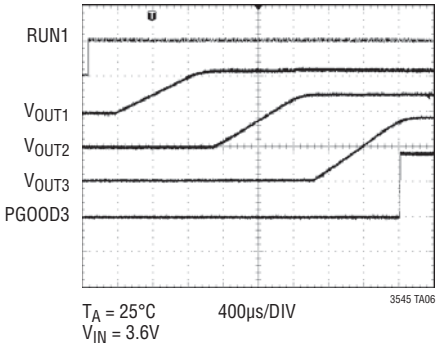

Figure 5. LTC3545-1 Three PGOODs and Power Sequencing

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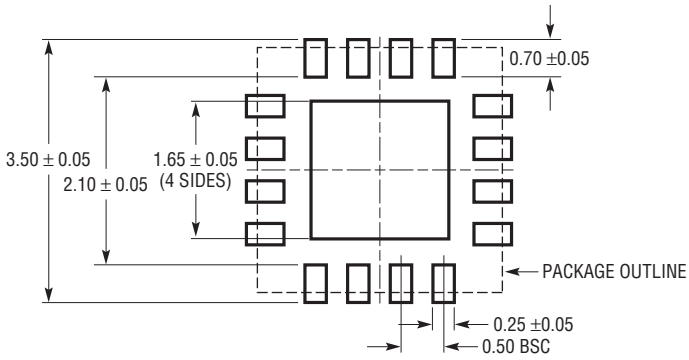
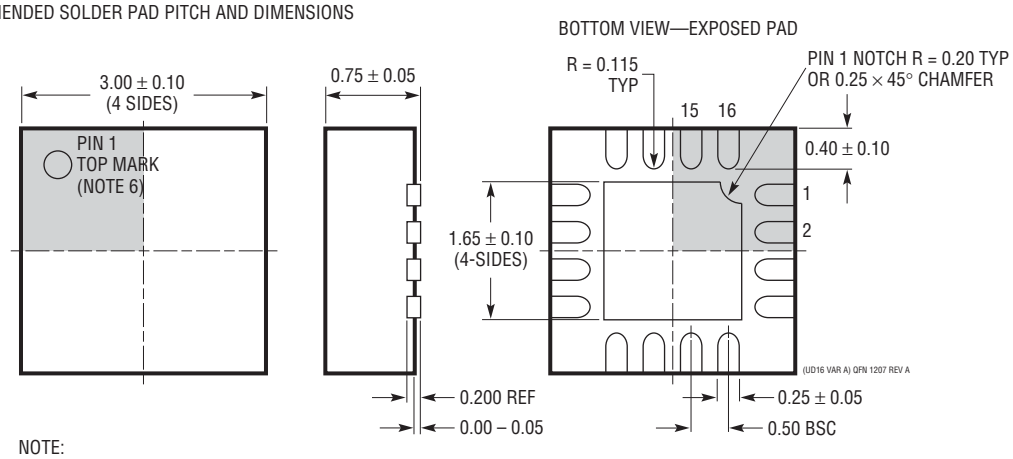
PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1700 Rev A)
Exposed Pad Variation AA



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-4)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3405/LTC3405A	300mA I_{OUT}, 1.5MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT™ Package
LTC3406/LTC3406B	600mA I_{OUT}, 1.5MHz, Synchronous Step-Down DC/DC Converters	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3407/LTC3407-2	Dual 600mA/800mA I_{OUT}, 1.5MHz/2.25MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, 10-Lead MSE, DFN Packages
LTC3409	600mA I_{OUT}, 1.7MHz/2.6MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 1.6V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 65µA, I_{SD} < 1µA, DFN Package
LTC3410/LTC3410B	300mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 26µA, I_{SD} < 1µA, SC70 Package
LTC3411	1.25A I_{OUT}, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, 10-Lead MSE, DFN Packages
LTC3412	2.5A I_{OUT}, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, 16-Lead TSSOPE Package
LTC3419	Dual 600mA, 2.25MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 35µA, I_{SD} < 1µA, MS10, 3mm × 3mm DFN Package
LTC3441/LTC3442 LTC3443	1.2A I_{OUT}, 2MHz, Synchronous Buck-Boost DC/DC Converters	95% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MIN)}$: 2.4V to 5.25V, I_Q = 50µA, I_{SD} < 1µA, DFN Package
LTC3531/LTC3531-3 LTC3531-3.3	200mA I_{OUT}, 1.5MHz, Synchronous Buck-Boost DC/DC Converters	95% Efficiency, V_{IN}: 1.8V to 5.5V, $V_{OUT(MIN)}$: 2V to 5V, I_Q = 16µA, I_{SD} < 1µA, ThinSOT, DFN Packages
LTC3532	500mA I_{OUT}, 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MIN)}$: 2.4V to 5.25V, I_Q = 35µA, I_{SD} < 1µA, 10-Lead MSE, DFN Packages
LTC3544/LTC3544B	300mA, 2 × 200mA, 100mA, 2.25MHz Quad Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, 3mm × 3mm QFN Package
LTC3547	Dual 300mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, 8-Lead DFN Package
LTC3548/LTC3548-1 LTC3548-2	Dual 400mA/800mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, 10-Lead MSE, DFN Packages
LTC3561	1.25A I_{OUT}, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 240µA, I_{SD} < 1µA, DFN Package

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