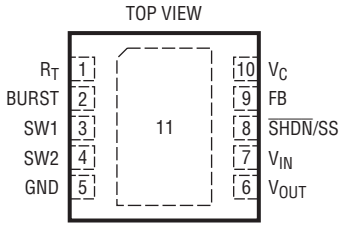
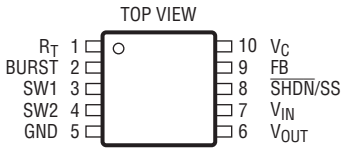
ABSOLUTE MAXIMUM RATINGS (Note 1)

BURST, V_{IN}, V_{OUT}, V_C, FB ..... –0.3V to 6V
R_T ..... 0V to 5V
$\overline{SHDN}$/SS ..... –0.3V to 6V
SW1, SW2
DC ..... –0.3V to 6V
Pulsed < 100ns ..... –0.3V to 7V
Operating Temperature Range (Note 2) .... –40°C to 85°C
Maximum Junction Temperature (Note 4) ..... 125°C
Storage Temperature Range
DD ..... –65°C to 125°C
MSOP ..... –65°C to 150°C
Lead Temperature (Soldering,10 sec)
MSOP ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE CONNECTED TO PCB



MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 125°C
θ_{JA} = 130°C/W 1 LAYER BOARD
θ_{JA} = 100°C/W 4 LAYER BOARD
θ_{JC} = 45°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3532EDD#PBF	LTC3532EDD#TRPBF	LBXR	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3532EMS#PBF	LTC3532EMS#TRPBF	LTBXS	10-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} = 3.6V, R_T = 64.9k, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Start-Up Voltage		●		2.3	2.4	V
Input Operating Range		●	2.4		5.5	V
Output Voltage Adjust Range		●	2.4		5.25	V
Feedback Voltage		●	1.19	1.22	1.25	V
Feedback Input Current	V_{FB} = 1.22V			1	50	nA
Quiescent Current, Burst Mode Operation	BURST = 0V			35	60	µA
Quiescent Current, Shutdown	$\overline{SHDN}$ = 0V, Not Including Switch Leakage, V_{OUT} = 0V			0.1	1	µA
Quiescent Current, Active	V_C = 0V, BURST = V_{IN} (Note 3)			600	1000	µA
NMOS Switch Leakage	Switches B and C			0.1	5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} = 3.6V, R_T = 64.9k, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PMOS Switch Leakage	Switches A and D			0.1	10	µA
NMOS Switch On Resistance	Switches B and C			0.36		Ω
PMOS Switch On Resistance	Switches A and D			0.42		Ω
Input Current Limit			0.8	1.1	1.45	A
Maximum Duty Cycle	Boost (% Switch C On) Buck (% Switch A On)	● ●	70 100	88		% %
Minimum Duty Cycle		●			0	%
Frequency Accuracy		●	575	740	885	kHz
Burst Threshold (Falling)				0.88		V
Burst Threshold (Rising)				1.12		V
Burst Current Ratio	Ratio of I_{OUT} to I_{BURST}			8000		
Error Amp AVOL				90		dB
Error Amp Source Current	V_C = 1.4V			15		µA
Error Amp Sink Current	V_C = 2V			310		µA
$\overline{SHDN}$/SS Threshold	When IC is Enabled When EA is at Maximum Boost Duty Cycle	●	0.4	1 2.2	1.5	V V
$\overline{SHDN}$/SS Input Current	$V_{\overline{SHDN}}$ = 5.5V			0.01	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3532E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlations with statistical process controls.

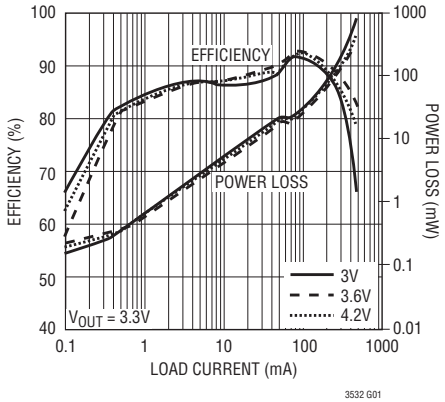
Note 3: Current measurements are performed when the outputs are not switching.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

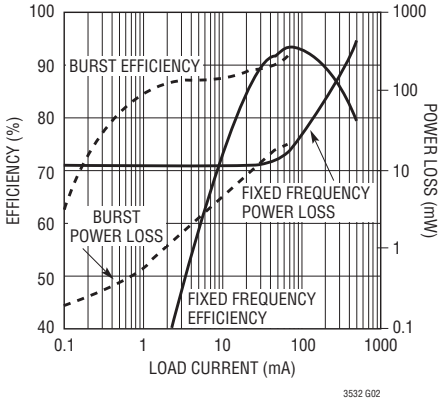
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise specified.

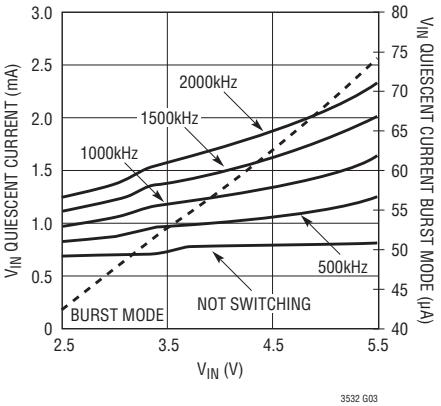
Efficiency and Power Loss vs Load Autoburst Mode



Efficiency and Power Loss vs Load

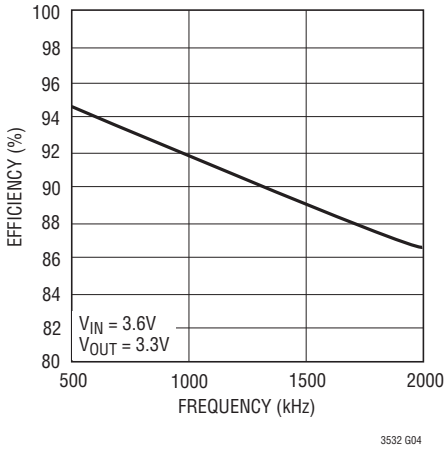


Fixed Frequency and Burst Mode Quiescent Current vs V_{IN}

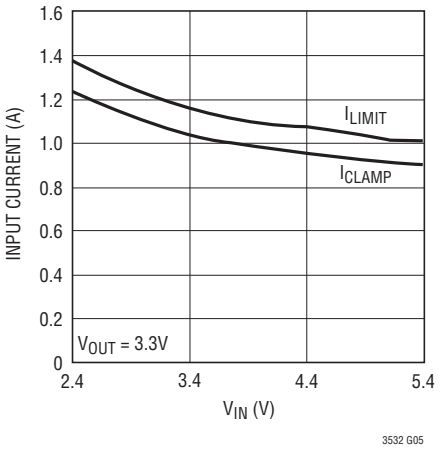


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise specified.

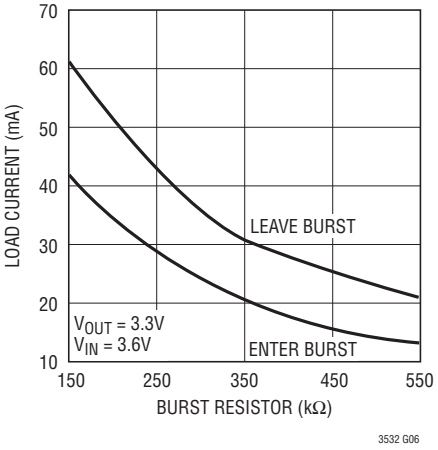
Efficiency vs Frequency



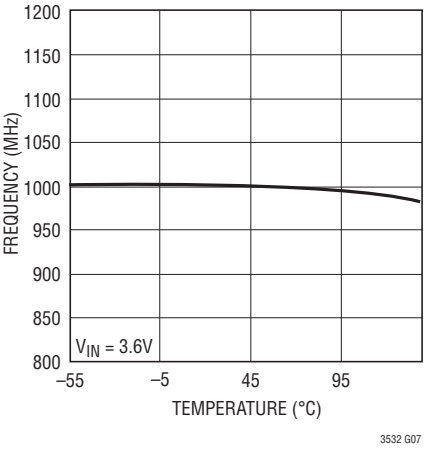
Peak Current Clamp and Limit vs V_{IN}



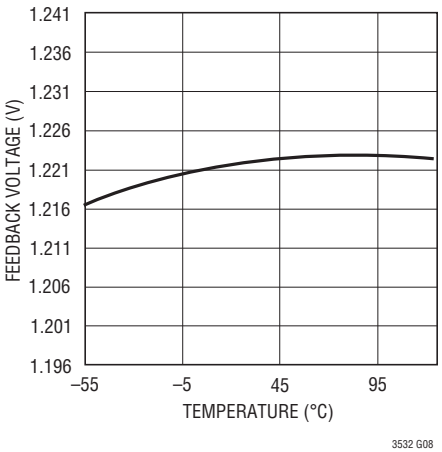
Automatic Burst Threshold vs R_{BURST}



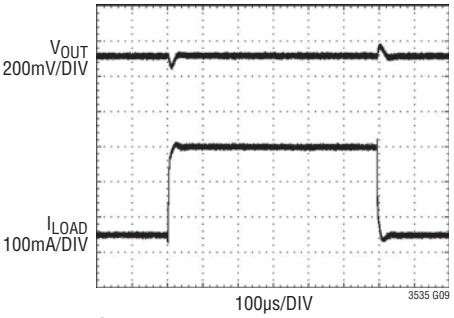
Frequency vs Temperature



Feedback Voltage vs Temperature

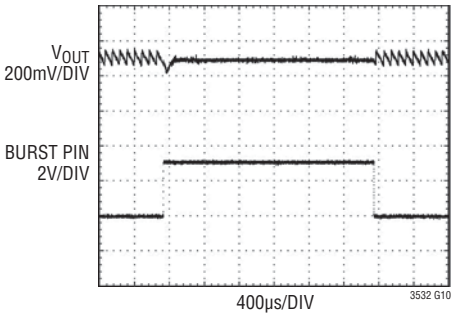


Load Transient Response in Fixed Frequency Mode



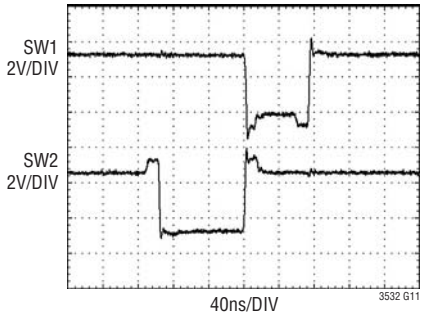
C_{OUT} = 10µF
V_{IN} = 3.6V
V_{OUT} = 3.3V

Burst Mode to Fixed Frequency Transition



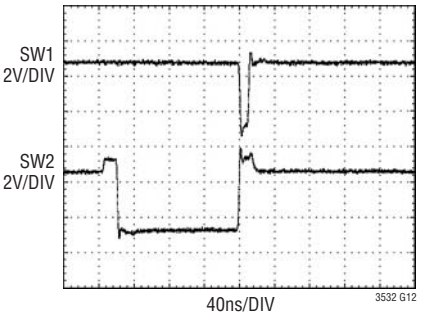
C_{OUT} = 22µF
V_{IN} = 3.6V
V_{OUT} = 3.3V

Switch Pins in Buck-Boost Mode



V_{IN} = 3.3V
V_{OUT} = 3.3V
I_{LOAD} = 100mA

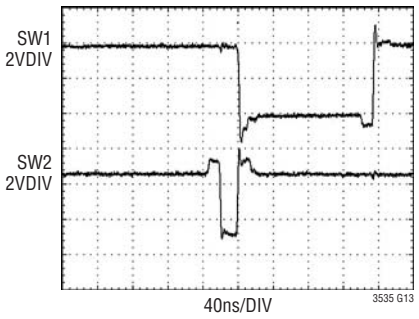
Switch Pins Before Entering Boost Mode



V_{IN} = 2.9V
V_{OUT} = 3.3V
I_{LOAD} = 100mA

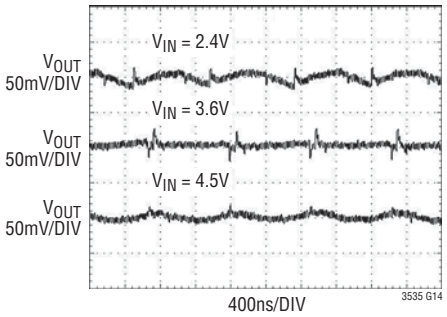
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise specified.

Switch Pins Before Entering Buck Mode



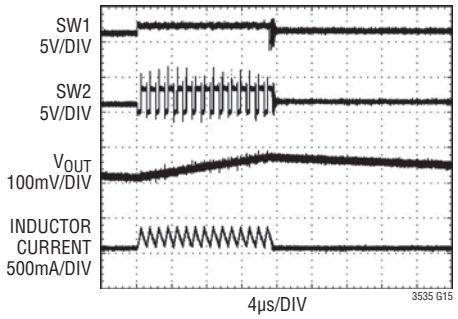
V_{IN} = 4V
VOUT = 3.3V
I_{LOAD} = 100mA

Output Ripple at 100mA Load



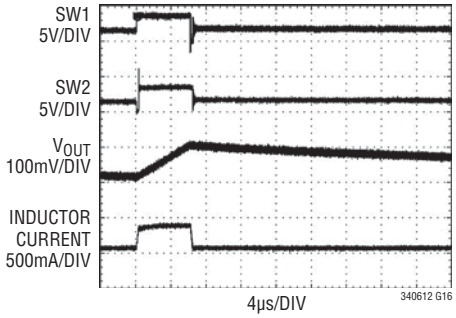
V_{OUT} = 3.6V
I_{OUT} = 100mA
C_{OUT} = 10µF

Burst Mode, Boost



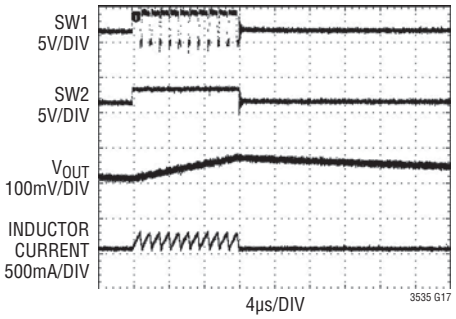
V_{IN} = 2.4V
V_{OUT} = 3.3V
I_{LOAD} = 20mA
C_{OUT} = 22µF

Burst Mode, Buck-Boost



V_{IN} = 3.75V
V_{OUT} = 3.3V
I_{LOAD} = 20mA
C_{OUT} = 22µF

Burst Mode, Buck



V_{IN} = 4.2V
V_{OUT} = 3.3V
I_{LOAD} = 20mA
C_{OUT} = 22µF

PIN FUNCTIONS

RT (Pin 1): Timing Resistor to Program the Oscillator Frequency. The programming range is 300kHz to 2MHz.

$$f(kHz) = \frac{48{,}000}{R_T(k\Omega)}$$

BURST (Pin 2): Used to Set the Automatic Burst Mode Operation Threshold. Place a resistor and capacitor in parallel from this pin to ground. See the Applications Information section for component value selection. For manual control, ground the pin to force Burst Mode operation, connect to V_{OUT} to force fixed frequency mode.

SW1 (Pin 3): Switch Pin Where the Internal Switches A and B are Connected. Connect inductor from SW1 to SW2. An optional Schottky diode can be connected from SW1 to ground. Minimize trace length to minimize EMI.

SW2 (Pin 4): Switch Pin Where the Internal Switches C and D are Connected. For applications with output voltages over 4.3V, a Schottky diode is required from SW2 to V_{OUT} to ensure SW2 does not exhibit excess voltage.

GND (Pin 5): Signal and Power Ground for the IC.

V_{OUT} (Pin 6): Output of the Synchronous Rectifier. A filter capacitor is placed from V_{OUT} to GND.

V_{IN} (Pin 7): Input Supply Pin. Supplies current to the inductor through SW1 and supplies internal V_{CC} for the IC. A ceramic bypass capacitor as close to the V_{IN} pin and GND (Pin 5) is required.

PIN FUNCTIONS

$\overline{SHDN}$/SS (Pin 8): Combined Soft-Start and Shutdown. Grounding this pin shuts down the IC. Tie to >1.5V to enable the IC and >2.4V to ensure the error amp is not clamped from soft-start. For Burst Mode operation, this pin must be pulled up to within 0.5V of V_{IN}. An RC from the shutdown command signal to this pin will provide a soft-start function by limiting the rise time of the V_C pin.

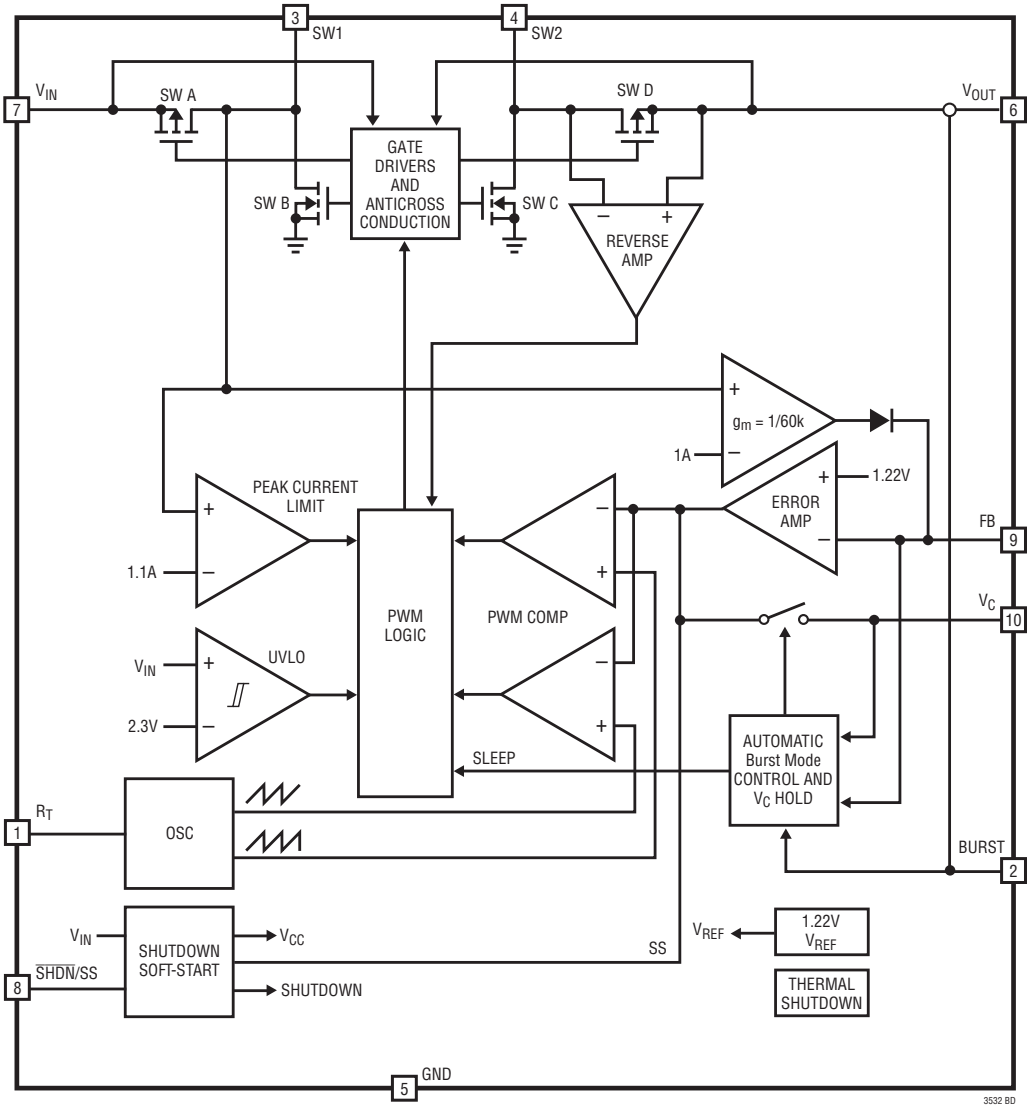
FB (Pin 9): Feedback Pin. Connect resistor divider tap here. The output voltage can be adjusted from 2.4V to 5.25V. The feedback reference is typically 1.22V. Set V_{OUT} according to the formula:

$$V_{OUT} = \frac{1.22V \bullet (R1 + R2)}{R2}$$

V_C (Pin10): Error Amp Output: A frequency compensation network is connected from this pin to the FB pin to compensate the loop. Refer to the Applications Information section for component value selection.

Exposed Pad (Pin11): The exposed pad (DFN Package) must be soldered to PCB ground for electrical contact and rated thermal performance.

BLOCK DIAGRAM



OPERATION

The LTC3532 provides high efficiency, low noise power for applications such as portable instrumentation, digital cameras, and MP3 players. The LTC proprietary topology allows input voltages above, below or equal to the output voltage by properly phasing the output switches. The error amp output voltage on V_C determines the output duty cycle of the switches. Since V_C is a filtered signal, it provides rejection of frequencies well below the switching frequency. The low $R_{DS(ON)}$, low gate charge synchronous switches provide high frequency pulse width modulation control at high efficiency. Schottky diodes across the synchronous switch D and synchronous switch B are not required, but provide a lower voltage drop during the break-before-make time (typically 15ns). Schottky diodes will improve peak efficiency by typically 1% to 2%. High efficiency is achieved at light loads when Burst Mode operation is entered and the IC's quiescent current drops to a low 35µA.

LOW NOISE FIXED FREQUENCY OPERATION

Oscillator

The frequency of operation is programmed by an external resistor from R_T to ground, according to the following equation:

$$f(kHz) = \frac{48{,}000}{R_T(k\Omega)}$$

Error Amp

The error amplifier is a voltage mode amplifier. The loop compensation components are configured around the amplifier (from FB to V_C) to obtain stability of the converter. For improved bandwidth, an additional RC feedforward network can be placed across the upper feedback divider resistor. The voltage on $\overline{SHDN}$/SS clamps the error amp output, V_C, to provide a soft-start function.

Internal Current Limit

There are two different current limit circuits in the LTC3532. They have internally fixed thresholds which vary inversely with V_{IN}. The first circuit is a high speed peak current limit comparator that will shut off switch A if the current exceeds 1.1A typical. The delay to output of this amplifier is typically 50ns. A second amplifier will begin to source current into the FB pin to drop the output voltage once the peak input current exceeds 1A typical. This method provides a closed loop means of clamping the input current. During conditions where V_{OUT} is near ground, such as during a short-circuit or during startup, this threshold is cut in half providing a fold back feature. For this current limit feature to be most effective, the Thevenin resistance from FB to ground should be greater than 100k.

Reverse Current Limit

During fixed frequency operation, the LTC3532 operates in forced continuous conduction mode. The reverse current limit amplifier monitors the inductor current from the output through switch D. Once the negative inductor current exceeds 340mA typical, the IC will shut off switch D.

4-Switch Control

Figure 1 shows a simplified diagram of how the four internal switches are connected to the inductor, V_{IN}, V_{OUT} and GND. Figure 2 shows the regions of operation for the LTC3532 as a function of the internal control voltage, V_{CI}. Depending on the control voltage, the IC will operate in either buck, buck/boost or boost mode. The V_{CI} voltage is a level shifted voltage from the output of the error amp (V_C) (see Figure 5). The four power switches are properly phased so the transfer between operating modes is continuous, smooth and transparent to the user. When V_{IN} approaches V_{OUT} the buck/boost region is reached where the conduction time of the 4-switch region is typically 150ns. Referring to Figures 1 and 2, the various regions of operation will now be described.

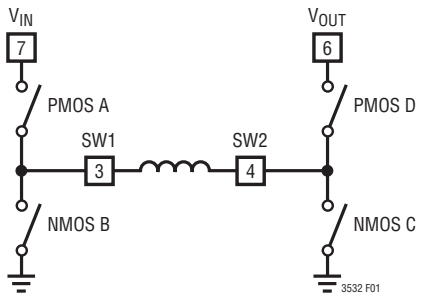


Figure 1. Simplified Diagram of Output Switches

OPERATION

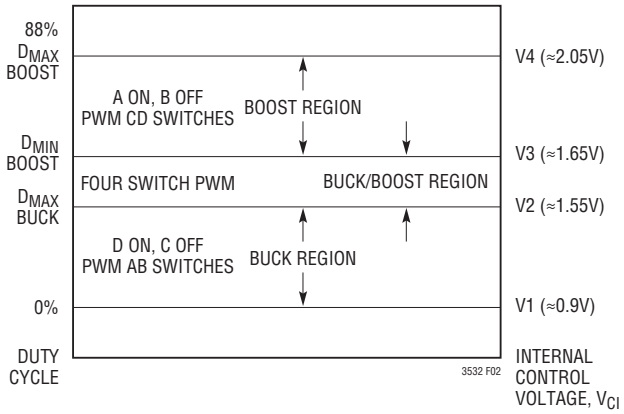


Figure 2. Switch Control vs Internal Control Voltage, V_{CI}

Buck Region ($V_{IN} > V_{OUT}$)

Switch D is always on and switch C is always off during this mode. When the internal control voltage, V_{CI}, is above voltage V1, output A begins to switch. During the off-time of switch A, synchronous switch B turns on for the remainder of the time. Switches A and B will alternate like a typical synchronous buck regulator. As the control voltage increases, the duty cycle of switch A increases until the maximum duty cycle of the converter in buck mode reaches D_{MAX_BUCK}, given by:

$$D_{MAX\_BUCK} = 100 - D4_{SW}\ \%$$

where $D4_{SW}$ = duty cycle % of the 4-switch range.

$$D4_{SW} = (150ns \bullet f) \bullet 100\ \%$$

where f = operating frequency, Hz.

Beyond this point the "4-switch," or buck/boost region is reached.

Buck/Boost or 4-Switch ($V_{IN} \sim V_{OUT}$)

When the internal control voltage, V_{CI}, is above voltage V2, switch pair AD remain on for duty cycle D_{MAX_BUCK}, and the switch pair AC begins to phase in. As switch pair AC phases in, switch pair BD phases out accordingly. When the V_{CI} voltage reaches the edge of the buck/boost range, at voltage V3, the AC switch pair completely phase out the BD pair, and the boost phase begins at duty cycle $D4_{SW}$. The input voltage, V_{IN}, where the 4-switch region begins is given by:

$$V_{IN} = \frac{V_{OUT}}{1 - (150ns \bullet f)}$$

The point at which the 4-switch region ends is given by:

$$V_{IN} = V_{OUT}(1 - D) = V_{OUT}(1 - 150ns \bullet f)\ V$$

Boost Region ($V_{IN} < V_{OUT}$)

Switch A is always on and switch B is always off during this mode. When the internal control voltage, V_{CI}, is above voltage V3, switch pair CD will alternately switch to provide a boosted output voltage. This operation is like a synchronous boost regulator. The maximum duty cycle of the converter is limited to 88% typical and is reached when V_{CI} is above V4.

Burst Mode OPERATION

Burst Mode operation occurs when the IC delivers energy to the output until it is regulated and then goes into a sleep mode where the outputs are off and the IC is consuming only 35µA of quiescent current from V_{IN}. In this mode the output ripple has a variable frequency component that depends upon load current, and will typically be about 2% peak-to-peak. Burst Mode operation ripple can be reduced slightly by using more output capacitance (47µF or greater). Another method of reducing Burst Mode operation ripple is to place a small feedforward capacitor across the upper resistor in the V_{OUT} feedback divider network (as in Type III compensation). During the period where the device is delivering energy to the output, the peak switch current will be equal to 250mA typical and the inductor current will terminate at zero current for each cycle. In this mode the typical maximum average output current is given by:

$$I_{OUT(MAX)BURST} \approx \frac{0.2 \bullet V_{IN}}{V_{OUT} + V_{IN}}\ A$$

OPERATION

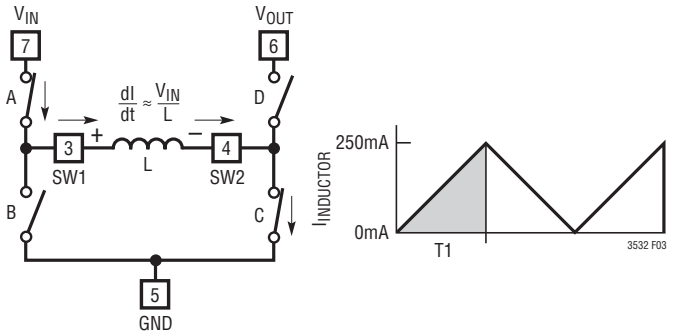


Figure 3. Inductor Charge Cycle During Burst Mode Operation

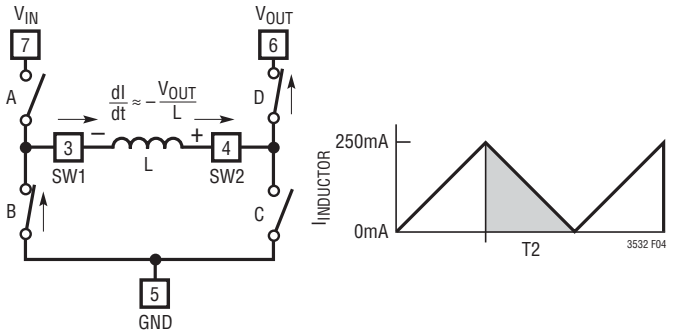


Figure 4. Inductor Disharge Cycle During Burst Mode Operation

Note that the peak efficiency during Burst Mode operation is less than the peak efficiency during fixed frequency because the part enters full-time 4-switch mode (when servicing the output) with discontinuous inductor current as illustrated in Figures 3 and 4. During Burst Mode operation, the control loop is nonlinear and cannot utilize the control voltage from the error amp to determine the control mode, therefore full-time 4-switch mode is required to maintain the buck/boost function. The efficiency below 1mA becomes dominated primarily by the quiescent current. The Burst Mode operation efficiency is given by:

$$\text{EFFICIENCY} \cong \frac{n \bullet I_{LOAD}}{35\mu A + I_{LOAD}}$$

where n is typically 88% during Burst Mode operation.

Automatic Burst Mode Operation Control

Burst Mode operation can be automatic or manually controlled with a single pin. In automatic mode, the IC will enter Burst Mode operation at light load and return to fixed frequency operation at heavier loads. The load current at which the mode transition occurs is programmed using a single external resistor from the BURST pin to ground, according to the following equations:

$$\text{Enter Burst Mode Operation: } I = \frac{10.5V}{R_{BURST}}$$

$$\text{Leave Burst Mode Operation: } I = \frac{7V}{R_{BURST}}$$

where R_{BURST} is in kΩ and I_{BURST} is the load transition current in Amps. For automatic operation, a filter capacitor should also be connected from BURST to ground to prevent ripple on BURST from causing the IC to oscillate in and out of Burst Mode operation. The equation for the minimum capacitor value is:

$$C_{BURST(MIN)} \geq \frac{C_{OUT} \bullet V_{OUT}}{60{,}000V}$$

where $C_{BURST(MIN)}$ and C_{OUT} are in µF. In the event that a load transient causes the feedback pin to drop by more than 4% from the regulation value while in Burst Mode operation, the IC will immediately switch to fixed frequency mode and an internal pull-up will be momentarily applied to BURST, rapidly charging the BURST capacitor. This prevents the IC from immediately reentering Burst Mode operation once the output achieves regulation.

Manual Burst Mode Operation

For manual control of Burst Mode operation, the RC network connected to BURST can be eliminated. To force fixed frequency mode, BURST should be connected to V_{OUT}. To force Burst Mode operation, BURST should be grounded. When commanding Burst Mode operation manually, the circuit connected to BURST should be able to sink up to 2mA. For optimum transient response with large dynamic loads, the operating mode should be controlled manually by the host. By commanding fixed frequency operation prior to a sudden increase in load, output voltage droop can

OPERATION

be minimized. Note that if the load current applied during forced Burst Mode operation (BURST pin is grounded) exceeds the current that can be supplied, the output voltage will start to droop and the IC will automatically come out of Burst Mode operation and enter fixed frequency mode, raising V_{OUT}. Once regulation is achieved, the IC will then enter Burst Mode operation once again, and the cycle will repeat, resulting in about 4% output ripple. Note that Burst Mode operation is inhibited during soft-start.

Burst Mode Operation to Fixed Frequency Transient Response

In Burst Mode operation, the compensation network is not used and V_C is disconnected from the error amplifier. During long periods of Burst Mode operation, leakage currents in the external components or on the PC board could cause the compensation capacitor to charge (or discharge), which could result in a large output transient when returning to fixed frequency mode of operation, even at the same load current. To prevent this, the LTC3532 incorporates an active clamp circuit that holds the voltage on V_C at an optimal voltage during Burst Mode operation. This minimizes any output transient when returning to fixed frequency mode operation. For optimum transient response, Type 3 compensation is also recommended to broad band the control loop and roll off past the two pole response of the output LC filter. (See Closing the Feedback Loop.)

Soft-Start

The soft-start function is combined with shutdown. When the $\overline{SHDN}$/SS pin is brought above 1V typical, the IC is enabled but the EA duty cycle is clamped from V_C. A detailed diagram of this function is shown in Figure 5. The components R_{SS} and C_{SS} provide a slow ramping voltage on $\overline{SHDN}$/SS to provide a soft-start function. To ensure that V_C is not being clamped, $\overline{SHDN}$/SS must be raised above 2.4V. To enable Burst Mode operation, $\overline{SHDN}$/SS must be raised to within 0.5V of V_{IN}.

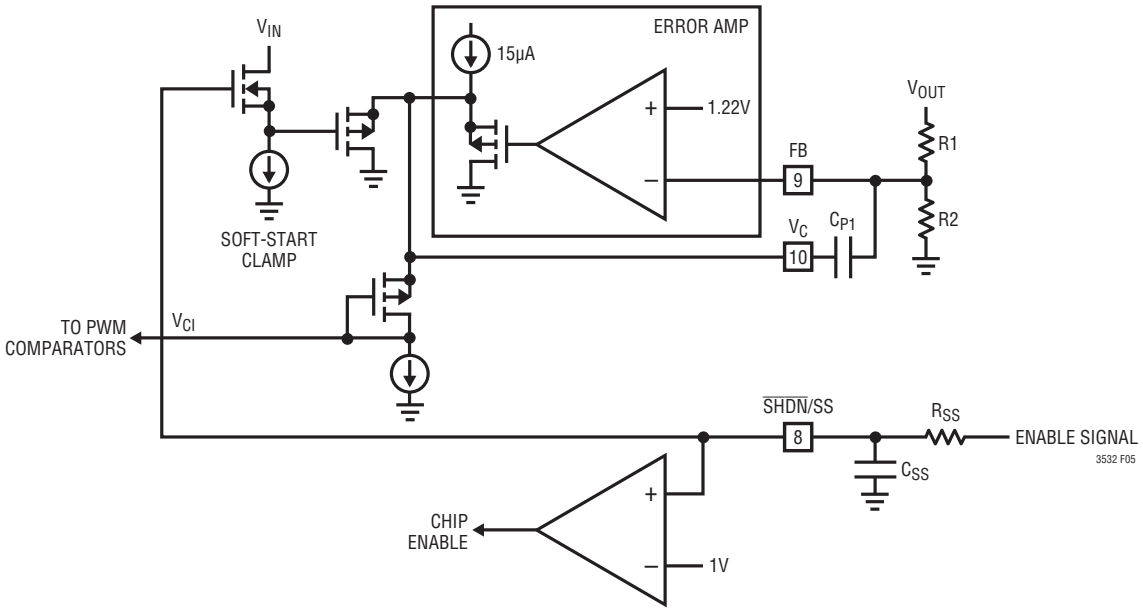


Figure 5. Soft-Start Circuitry

APPLICATIONS INFORMATION

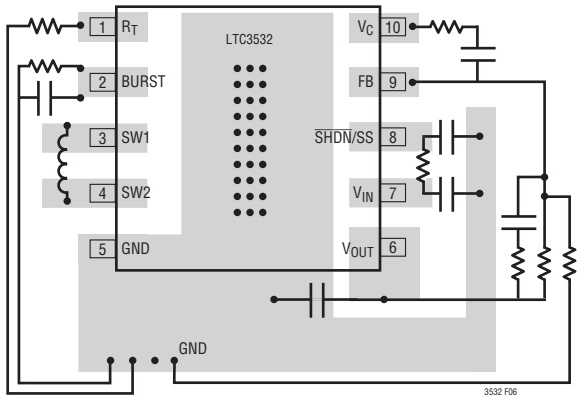


Figure 6. Recommended Component Placement. Traces Carrying High Current are Direct. Trace area at FB and V_C Pins are Kept Low. Lead Length to Battery Should be Kept Short

Inductor Selection

The high frequency operation of the LTC3532 allows the use of small surface mount inductors. The inductor ripple current is typically set to 20% to 40% of the maximum inductor current. For a given ripple the inductance terms are given as follows:

$$L_{BOOST} > \frac{V_{IN(MIN)} \bullet (V_{OUT} - V_{IN(MIN)})}{f \bullet \Delta I_L \bullet V_{OUT}} H$$

$$L_{BUCK} > \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{f \bullet \Delta I_L \bullet V_{IN(MAX)}} H$$

where f = Operating frequency, Hz

ΔIL = Maximum allowable inductor ripple current, A

$V_{IN(MIN)}$ = Minimum input voltage

$V_{IN(MAX)}$ = Maximum input voltage

V_{OUT} = Output voltage

$I_{OUT(MAX)}$ = Maximum output load current

For high efficiency, choose a ferrite inductor with a high frequency core material to reduce core losses. The inductor should have low ESR (equivalent series resistance) to reduce the I2R losses, and must be able to handle the peak inductor current without saturating. Molded chokes or chip inductors usually do not have enough core to support the peak inductor currents in the 1A to 2A region. To minimize radiated noise, use a shielded inductor. See Table 1 for a suggested list of inductor suppliers.

Table 1. Inductor Vendor Information

SUPPLIER	WEB SITE
Coilcraft	www.coilcraft.com
Murata	www.murata.com
Sumida	www.sumida.com
TDK	www.component.tdk.com
TOKO	www.tokoam.com

Output Capacitor Selection

The bulk value of the output filter capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The steady state ripple due to charge is given by:

$$\%\ RIPPLE\_BOOST = \frac{I_{OUT(MAX)} \bullet (V_{OUT} - V_{IN(MIN)}) \bullet 100}{C_{OUT} \bullet V_{OUT}^2 \bullet f}\ \%$$

$$\%\ RIPPLE\_BUCK = \frac{1}{8LCf^2} \bullet \frac{(V_{IN(MAX)} - V_{OUT}) \bullet 100\%}{V_{IN(MAX)}}$$

where C_{OUT} = output filter capacitor in Farads and f = switching frequency in Hz.

The output capacitance is usually many times larger than the minimum value in order to handle the transient response requirements of the converter. As a rule of thumb, the ratio of the operating frequency to the unity-gain bandwidth of the converter is the amount the output capacitance will have to increase from the above calculations in order to maintain the desired transient response.

The other component of ripple is due to the ESR (equivalent series resistance) of the output capacitor. Low ESR capacitors should be used to minimize output voltage ripple. For surface mount applications, Taiyo Yuden or TDK ceramic capacitors, AVX TPS series tantalum capacitors or Sanyo POSCAP are recommended. See Table 2 for contact information.

APPLICATIONS INFORMATION

Table 2. Capacitor Vendor Information

SUPPLIER	WEB SITE
AVX	www.avxcorp.com
Murata	www.murata.com
Sanyo	www.sanyovideo.com
Taiyo Yuden	www.t-yuden.com
TDK	www.component.tdk.com

Input Capacitor Selection

Since V_{IN} is the supply voltage for the IC, as well as the input to the power stage of the converter, it is recommended to place at least a 4.7µF, low ESR ceramic bypass capacitor close to the V_{IN} and GND pins. It is also important to minimize any stray resistance from the converter to the battery or other power source.

Optional Schottky Diodes

The Schottky diodes across the synchronous switches B and D are not required (V_{OUT} < 4.3V), but provide a lower drop during the break-before-make time (typically 15ns) improving efficiency. Use a surface mount Schottky diode such as an MBRM120T3 or equivalent. Do not use ordinary rectifier diodes, since the slow recovery times will compromise efficiency. For applications with an output voltage above 4.3V, a Schottky diode is required from SW2 to V_{OUT}.

Output Voltage > 4.3V

A Schottky diode from SW2 to V_{OUT} is required for output voltages over 4.3V. The diode must be located as close to the pins as possible in order to reduce the peak voltage on SW2 due to the parasitic lead and trace inductance.

Input Voltage > 4.5V

For applications with input voltages above 4.5V which could exhibit an overload or short-circuit condition, a 2Ω/1nF series snubber is required between SW1 and GND. A Schottky diode from SW1 to V_{IN} should also be added as close to the pins as possible. For the higher input voltages, V_{IN} bypassing becomes more critical; therefore, a ceramic bypass capacitor as close to the V_{IN} and SGND pins as possible is also required.

Operating Frequency Selection

Higher operating frequencies allow the use of a smaller inductor and smaller input and output filter capacitors, thus reducing board area and component height. However, higher operating frequencies also increase the IC's total quiescent current due to the gate charge of the four switches, as given by:

Buck: $I_Q = (0.125 \bullet V_{IN} \bullet f)$ mA
Boost: $I_Q = [0.06 \bullet (V_{IN} + V_{OUT}) \bullet f]$ mA
Buck/Boost: $I_Q = [f \bullet (0.19 \bullet V_{IN} + 0.06 \bullet V_{OUT})]$ mA

where f = switching frequency in MHz. Therefore frequency selection is a compromise between the optimal efficiency and the smallest solution size.

Closing the Feedback Loop

The LTC3532 incorporates voltage mode PWM control. The control to output gain varies with operation region (buck, boost, buck/boost), but is usually no greater than 15. The output filter exhibits a double pole response, as given by:

$$f_{FILTER\_POLE} = \frac{1}{2 \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}} \text{ Hz}$$

(in buck mode)

$$f_{FILTER\_POLE} = \frac{V_{IN}}{2 \bullet V_{OUT} \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}} \text{ Hz}$$

(in boost mode)

where L is in henrys and C_{OUT} is in farads.

The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}} \text{ Hz}$$

where R_{ESR} is the equivalent series resistance of the output capacitor.

A troublesome feature in boost mode is the right-half plane zero (RHP), given by:

$$f_{RHPZ} = \frac{V_{IN}^2}{2 \bullet \pi \bullet I_{OUT} \bullet L \bullet V_{OUT}} \text{ Hz}$$

APPLICATIONS INFORMATION

The loop gain is typically rolled off before the RHP zero frequency.

A simple Type I compensation network can be incorporated to stabilize the loop, but at a cost of reduced bandwidth and slower transient response. To ensure proper phase margin using Type I compensation, the loop must be crossed over a decade before the LC double pole. The unity-gain frequency of the error amplifier with the Type I compensation is given by:

$$f_{UG} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{P1}} Hz$$

referring to Figure 7.

Most applications demand an improved transient response to allow a smaller output filter capacitor. To achieve a higher bandwidth, Type III compensation is required, providing two zeros to compensate for the double-pole response of the output filter. Referring to Figure 8, the location of the poles and zeros are given by:

$$f_{POLE1} \cong \frac{1}{2 \bullet \pi \bullet 32e^3 \bullet R1 \bullet CP1} Hz$$

(which is extremely close to DC)

$$f_{ZERO1} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{P1}} Hz$$

$$f_{ZERO2} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{Z1}} Hz$$

$$f_{POLE2} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{P2}} Hz$$

where resistance is in ohms and capacitance is in farads.

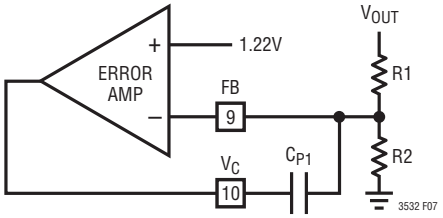


Figure 7. Error Amplifier with Type I Compensation

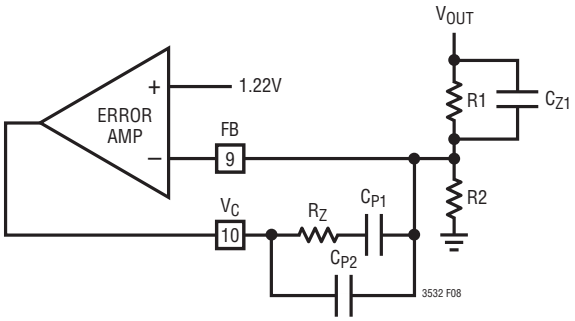
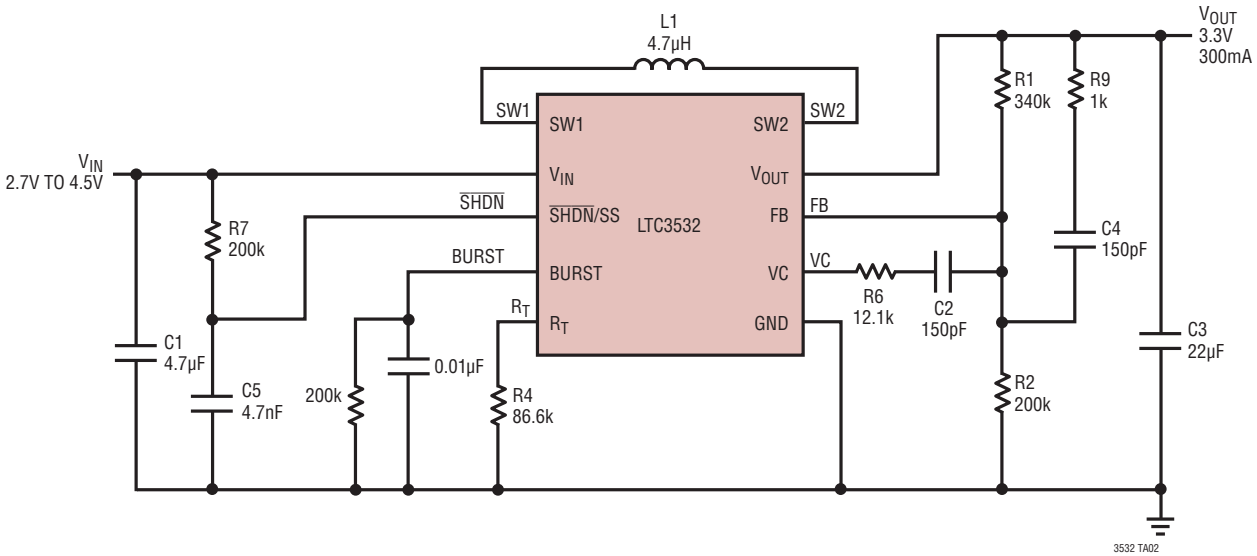


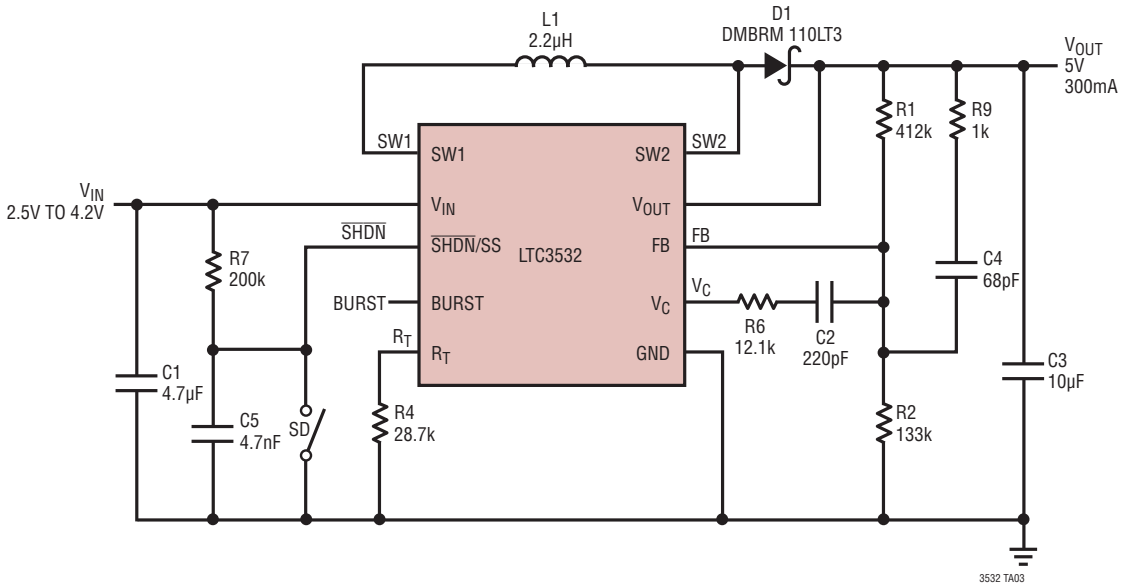
Figure 8. Error Amplifier with Type III Compensation

TYPICAL APPLICATIONS

Three Cell to 3.3V at 300mA Buck-Boost Converter With Automatic Burst Mode Operation and Soft-Start

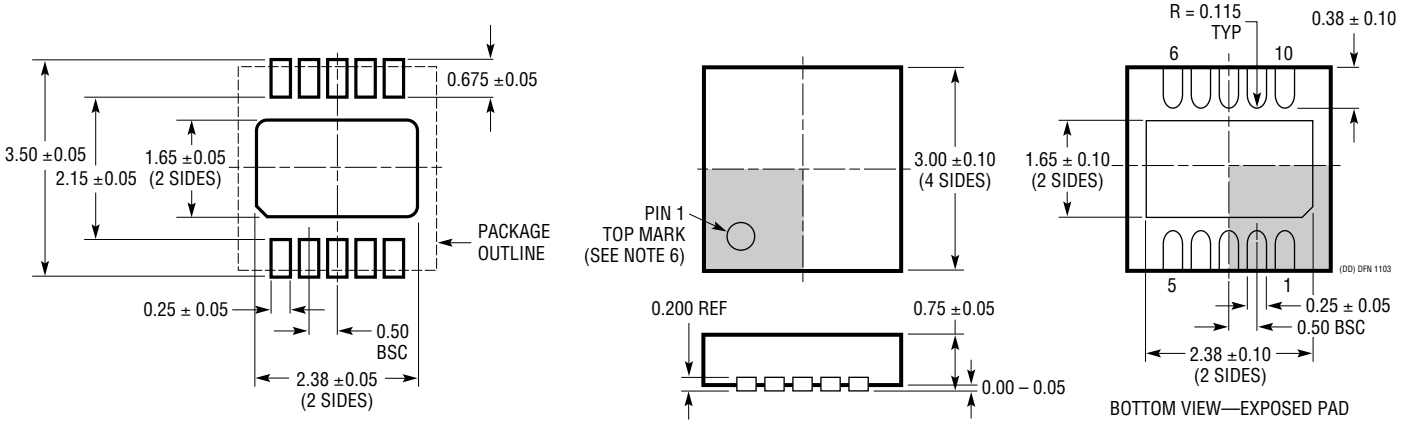


Li-Ion to 5V Boost Converter with Output Disconnect



PACKAGE DESCRIPTION

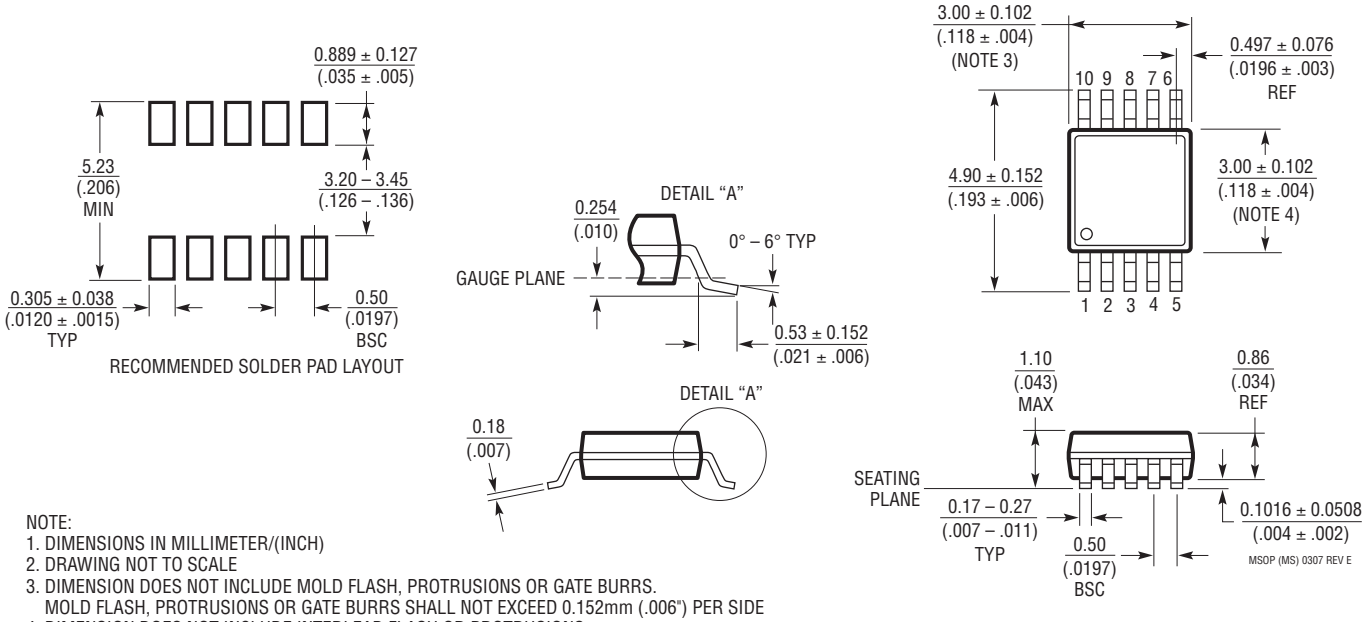
DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

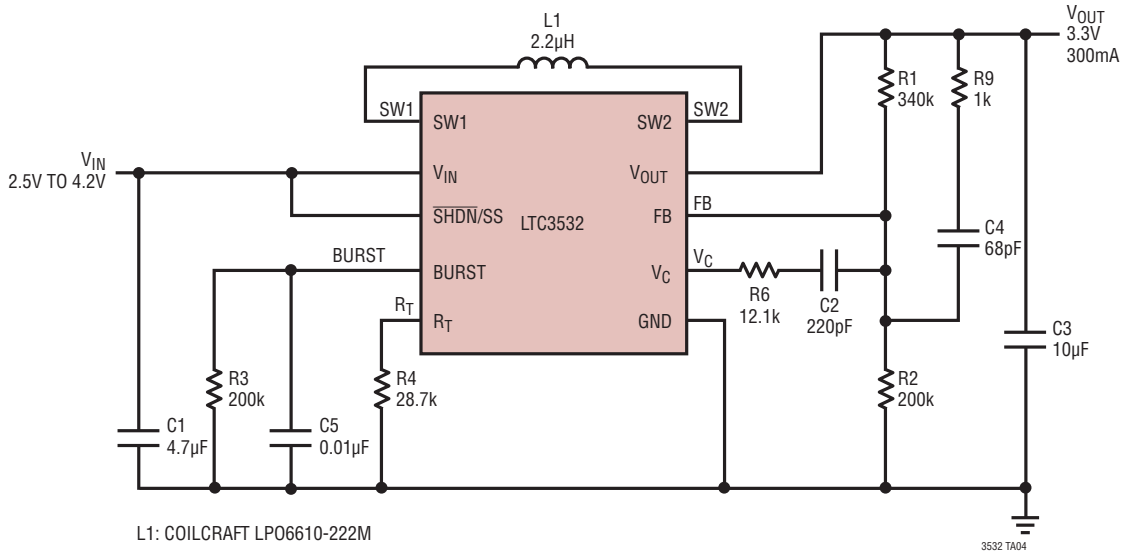
MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev E)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Low Profile Li-Ion to 3.3V at 300mA Converter with Automatic Burst Mode Operation



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3440	600mA I_{OUT}, 2MHz, Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(RANGE)}$: 2.5V to 5.5V, I_Q = 25µA, I_{SD} = <1µA, MS10/DFN Package
LTC3441	1.2A I_{OUT}, 1MHz, Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.4V to 5.5V, $V_{OUT(RANGE)}$: 2.4V to 5.25V, I_Q = 25µA, I_{SD} = <1µA, DFN Package
LTC3442	1.2A I_{OUT}, 2MHz, Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.4V to 5.5V, $V_{OUT(RANGE)}$: 2.4V to 5.25V, I_Q = 35µA, I_{SD} = <1µA, DFN Package
LTC3443	1.2A I_{OUT}, 600kHz, Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.4V to 5.5V, $V_{OUT(RANGE)}$: 2.4V to 5.25V, I_Q = 28µA, I_{SD} = <1µA, MS10 Package
LTC3444	500mA I_{OUT}, 1.5MHz, Synchronous Buck-Boost DC/DC Converter Optimized for WCDMA	V_{IN}: 2.7V to 5.5V, $V_{OUT(RANGE)}$: 0.5V to 5.25V, I_{SD} = <1µA, 3 × 3 DFN Package
LTC3531/ LTC3531-3.3/ LTC3531-3	200mA I_{OUT}, Synchronous Buck-Boost DC/DC Converters in SOT-23	V_{IN}: 1.8V to 5.5V, $V_{OUT(RANGE)}$: 2V to 5.25V, I_Q = 16µA, I_{SD} = <1µA, SOT-23 and 3 × 3 DFN Packages

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