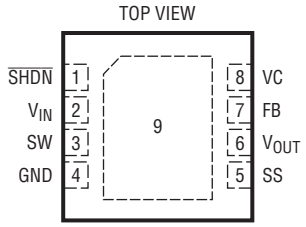
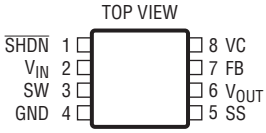
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} to GND ..... – 7V to 7V
V_{OUT} to GND ..... – 0.3V to 7V
SW to V_{OUT} ..... – 7V to 1V
SW to GND
DC ..... –7V to 7V
Pulsed < 100ns ..... –7V to 8V
$\overline{SHDN}$ to GND ..... – 7V to 7V
FB, SS to GND ..... – 0.3V to 7V
Operating Temperature Range
(Notes 3, 4) ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
MSOP ..... 300°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 45°C
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 160°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3499EDD#PBF	LTC3499EDD#TRPBF	LBRB	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3499BEDD#PBF	LTC3499BEDD#TRPBF	LCDZ	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3499EMS8#PBF	LTC3499EMS8#TRPBF	LTBRC	8-Lead Plastic MSOP	–40°C to 85°C
LTC3499BEMS8#PBF	LTC3499BEMS8#TRPBF	LTCFB	8-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 2.4V, V_{OUT} = 5V, $\overline{SHDN}$ = 2.4V, T_A = T_J unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply							
V_{IN}	Minimum Start-Up Voltage		●		1.6	1.8	V
V_{OUT}	Output Voltage Adjust Range		●	2		6	V
V_{FB}	FB Voltage		●	1.195	1.220	1.245	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 2.4V, V_{OUT} = 5V, $\overline{SHDN}$ = 2.4V, $T_A = T_J$ unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{FB}	FB Input Current	V_{FB} = 1.22V			3	50	nA
I_{VIN}	V_{IN} Quiescent Current	No Output Load	●		300	600	µA
I_{SD}	V_{IN} Quiescent Current in Shutdown	$\overline{SHDN}$ = 0V, V_{OUT} = 0V			0.1	1	µA
I_{BURST}	Quiescent Current – Burst Mode Operation	V_{IN} Current at 2.4V (LTC3499 Only) V_{OUT} Current at 5V (LTC3499 Only)			20 1.5		µA µA
I_{NMOS}	NMOS Switch Leakage Current	V_{SW} = 6V			0.1	5	µA
I_{PMOS}	PMOS Switch Leakage Current	V_{OUT} = 6V, V_{SW} = 0V			0.1	5	µA
R_{NMOS}	NMOS Switch On Resistance	V_{OUT} = 3.3V V_{OUT} = 5V			0.45 0.4		Ω Ω
R_{PMOS}	PMOS Switch On Resistance	V_{OUT} = 3.3V V_{OUT} = 5V			0.58 0.45		Ω Ω
I_{LIM}	NMOS Current Limit		●	0.75	1		A
$t_{DLY, ILIM}$	Current Limit Delay to Output	Note 2			60		ns
D_{MAX}	Maximum Duty Cycle		●	80	85		%
D_{MIN}	Minimum Duty Cycle		●			0	%
f_{OSC}	Frequency Accuracy		●	1	1.2	1.4	MHz
G_{mEA}	Error Amplifier Transconductance				40		µmhos
I_{SOURCE}	Error Amplifier Source Current				–5		µA
I_{SINK}	Error Amplifier Sink Current				5		µA
I_{SS}	SS Current Source	V_{SS} = 1V			–3		µA
V_{OV}	V_{OUT} Overvoltage Threshold				6.8		V
$V_{OV(HYST)}$	V_{OUT} Overvoltage Hysteresis				400		mV
Shutdown							
$V_{\overline{SHDN}(LOW)}$	$\overline{SHDN}$ Input Low Voltage		●			0.2	V
$V_{\overline{SHDN}(HIGH)}$	$\overline{SHDN}$ Input High Voltage	Measured at SW	●	1.2			V
I_{SD}	$\overline{SHDN}$ Input Current					1	µA
Reverse Battery							
$I_{VOUT,REVBATT}$	V_{OUT} Reverse-Battery Current	V_{OUT} = 0V, V_{IN} = $V_{\overline{SHDN}}$ = V_{SW} = –6V	●			5	µA
$I_{VIN,REVBATT}$	V_{IN} and V_{SW} Reverse-Battery Current	V_{OUT} = 0V, V_{IN} = $V_{\overline{SHDN}}$ = V_{SW} = –6V	●			–5	µA
$I_{\overline{SHDN},REVBATT}$	$\overline{SHDN}$ Reverse-Battery Current	V_{OUT} = 0V, V_{IN} = $V_{\overline{SHDN}}$ = V_{SW} = –6V	●			–5	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

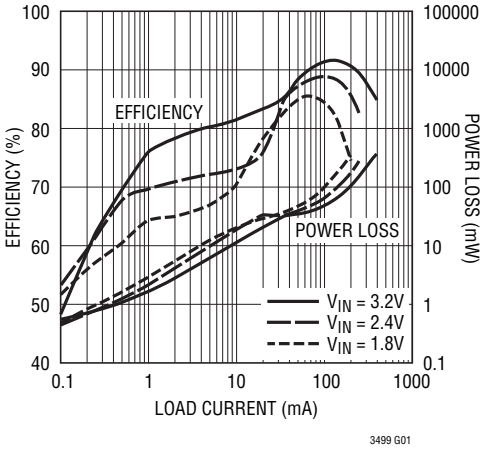
Note 2: Specification is guaranteed by design and not 100% tested in production.

Note 3: The LTC3499E/LTC3499BE are guaranteed to meet device specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature are assured by design, characterization and correlation with statistical process controls.

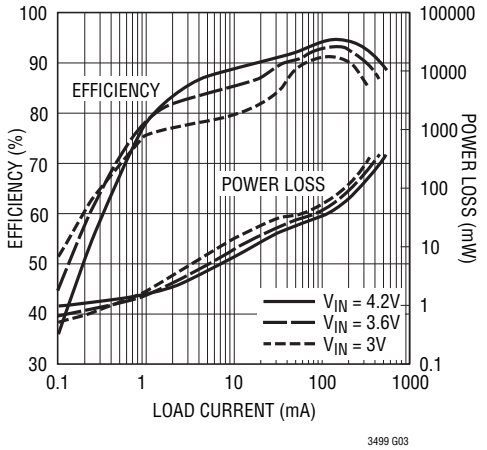
Note 4: These ICs include overtemperature protection that is intended to protect the devices during momentary overload conditions. Junction temperatures will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating temperature range may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

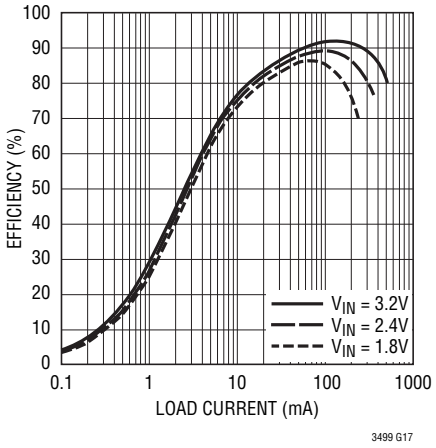
2-Cell to 5V Efficiency vs Load Current (LTC3499 Only)



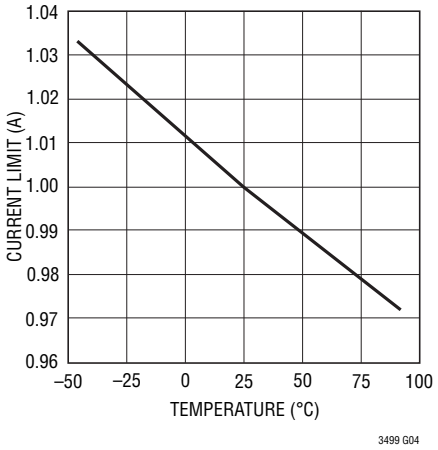
Li-Ion to 5V Efficiency vs Load Current (LTC3499 Only)



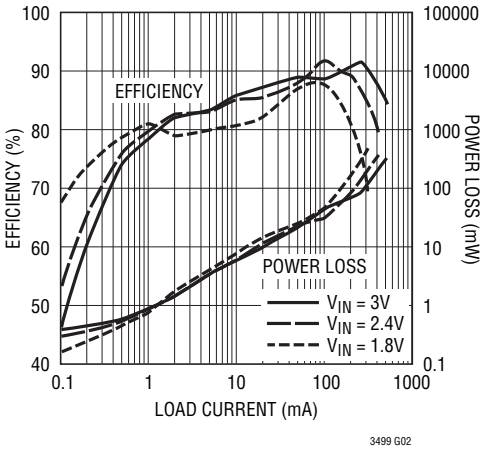
2-Cell to 5V Efficiency vs Load Current (LTC3499B Only)



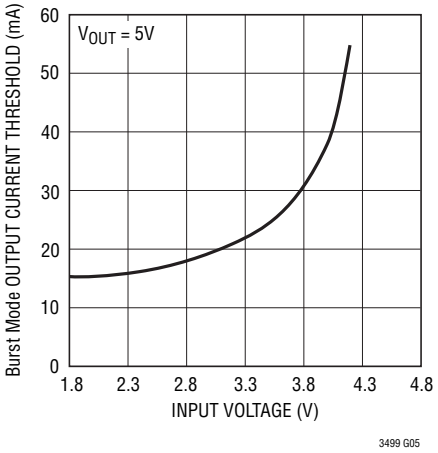
Current Limit Accuracy vs Temperature



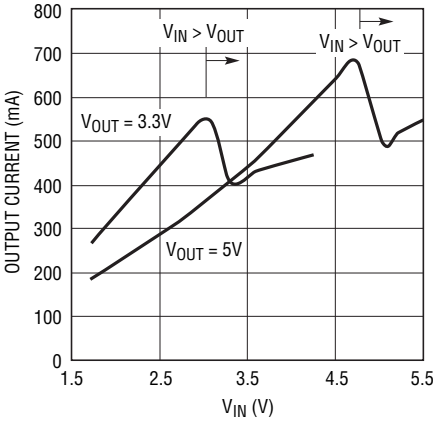
2-Cell to 3.3V Efficiency vs Load Current (LTC3499 Only)



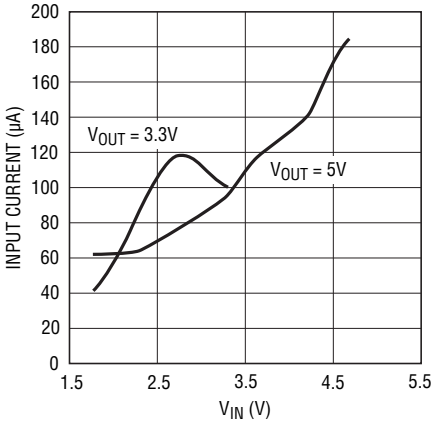
Burst Mode Output Current Threshold vs Input Voltage (LTC3499 Only)



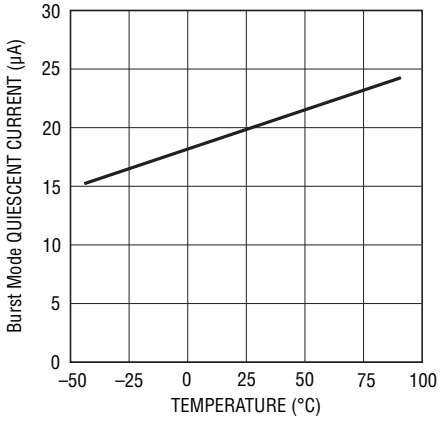
Maximum Output Current Capability vs V_{IN}



No Load Input Current vs V_{IN} (LTC3499 Only)

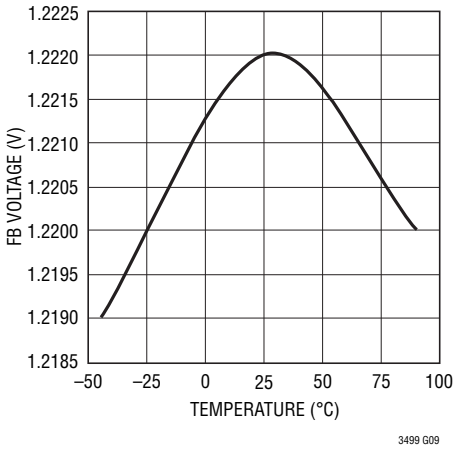


Burst Mode Quiescent Current vs Temperature (LTC3499 Only)

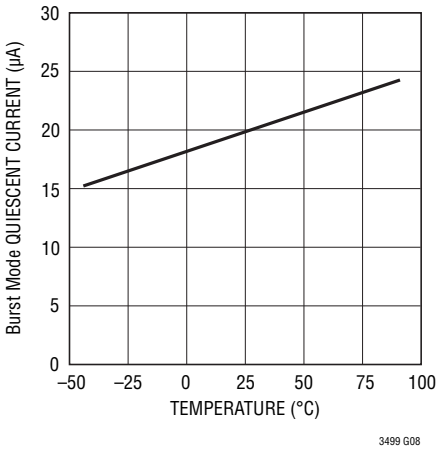


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

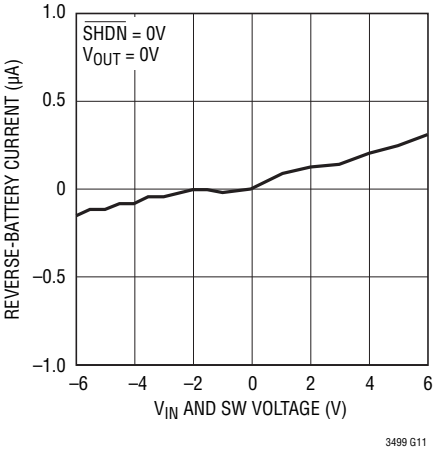
FB Voltage vs Temperature



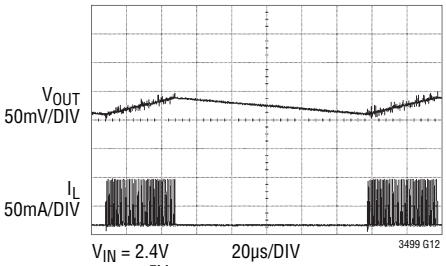
Burst Mode Quiescent Current vs Temperature



V_{IN} and SW Reverse-Battery Current vs V_{IN} and SW Voltage

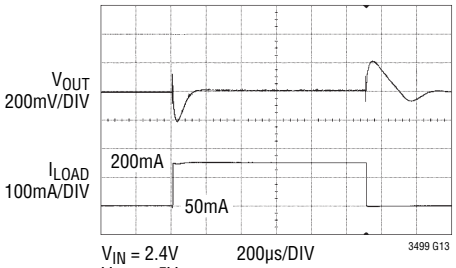


Burst Mode Operation (LTC3499 Only)



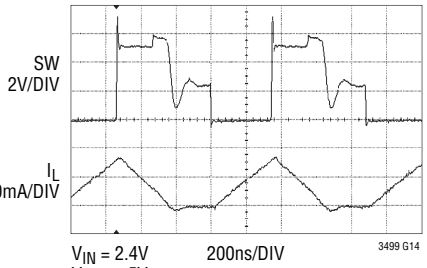
V_{IN} = 2.4V 20µs/DIV
V_{OUT} = 5V
L = 4.7µH
C_{OUT} = 10µF
C_{FF} = 10pF (FEEDFORWARD CAPACITOR FROM V_{OUT} TO FB)

Load Transient 50mA to 200mA



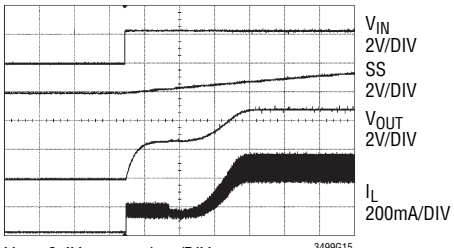
V_{IN} = 2.4V 200µs/DIV
V_{OUT} = 5V
I_{LOAD} = 50mA to 200mA
R_Z = 100k
C_F = 680pF
C_{OUT} = 10µF
L = 4.7µH

Fixed Frequency Discontinous Mode Operation



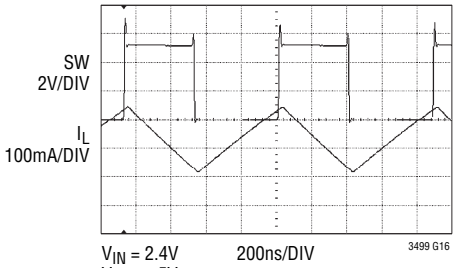
V_{IN} = 2.4V 200ns/DIV
V_{OUT} = 5V
L = 4.7µH

Soft-Start into 25Ω Load



V_{IN} = 2.4V 1ms/DIV
V_{OUT} = 5V
L = 4.7µH
C_{SS} = 0.01µF
C_{OUT} = 10µF

Fixed Frequency Operation



V_{IN} = 2.4V 200ns/DIV
V_{OUT} = 5V
L = 4.7µH

PIN FUNCTIONS

SHDN (Pin 1): Shutdown Input for IC. Connect to a voltage greater than 1.2V to enable and a voltage less than 0.2V to disable the LTC3499/LTC3499B.

V_{IN} (Pin 2): Input Supply Voltage. The valid operating voltage is between 1.8V to 5.5V. V_{IN} has reverse battery protection. Since the LTC3499/LTC3499B use V_{IN} as the main bias source, bypass with a low ESR ceramic capacitor of at least 2.2µF.

SW (Pin 3): Switch Pin. Connect an inductor from V_{IN} to this pin with a value between 2.2µH and 10µH. Keep PCB trace lengths as short and wide as possible to minimize EMI and voltage overshoot. If the inductor current falls to zero or $\overline{SHDN}$ is low an internal 250Ω antiringing switch is connected from V_{IN} to SW to minimize EMI.

GND (Pin 4/Exposed Pad, DD Package Pin 9): Signal and Power Ground. The DD package exposed pad must be soldered to the PCB power ground plane for electrical connection and rated thermal performance.

SS (Pin 5): Soft-Start Input. Connect a capacitor from SS to ground to control the inrush current at start-up. An internal 3µA current source charges this pin. SS will be discharged if $\overline{SHDN}$ is pulled low, thermal shutdown occurs or V_{IN} is below the minimum operating voltage.

V_{OUT} (Pin 6): Power Supply Output. Connect a low ESR output filter capacitor from this pin to the ground plane.

FB (Pin 7): FB Input to Error Amplifier. Connect a resistor divider tap from V_{OUT} to this pin to set the output voltage. The output voltage can be adjusted between 2V and 6V. Referring to the Functional Block Diagram, the output voltage is given by:

$$V_{OUT} = 1.22 \bullet \left[1 + \left(\frac{R1}{R2}\right)\right]$$

VC (Pin 8): Error Amplifier Output. A frequency compensation network is connected from this pin to GND to compensate the boost converter loop. See Closing the Feedthrough Loop section for guidelines.

FUNCTIONAL BLOCK DIAGRAM

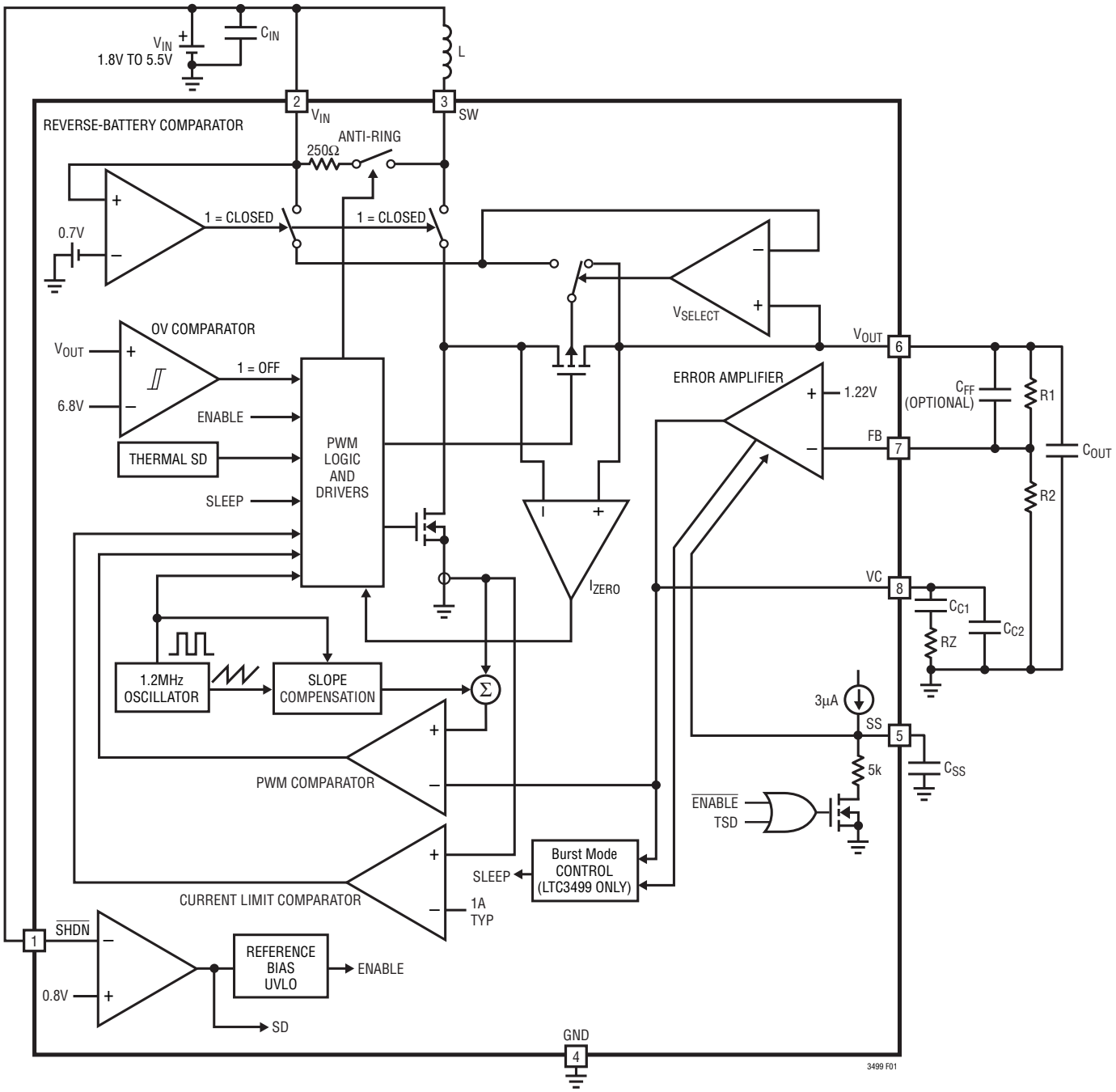


Figure 1: Functional Block Diagram

OPERATION

The LTC3499/LTC3499B provide high efficiency, low noise power for boost applications with output voltages up to 6V. Operation can be best understood by referring to the Functional Block Diagram in Figure 1. The synchronous boost converters are housed in either an 8-lead (3mm × 3mm) DFN or MSOP package and operates at a fixed 1.2MHz. With a 1.6V typical minimum V_{IN} voltage these devices are well suited for applications using two or three alkaline or nickel-metal hydride (NiMH) cells or one Lithium-Ion (Li-Ion) cell. The LTC3499/LTC3499B have integrated circuitry which protects the battery, IC, and circuitry powered by the device in the event that the input batteries are connected backwards (reverse battery protection). The true output disconnect feature eliminates inrush current and allows V_{OUT} to be zero volts during shutdown. The current mode architecture simplifies loop compensation with excellent load transient response. The low $R_{DS(ON)}$, low gate charge synchronous switches eliminate the need for an external Schottky diode rectifier, and provide efficient high frequency pulse width modulation (PWM). Burst Mode quiescent current to the LTC3499 is only 20µA from V_{IN}, maximizing battery life. The LTC3499B does not have Burst Mode operation and the device continues switching at constant frequency. This results in the absence of low frequency output ripple at the expense of light load efficiency.

LOW NOISE FIXED FREQUENCY OPERATION

Shutdown

The LTC3499/LTC3499B are shut down by pulling $\overline{SHDN}$ below 0.2V, and activated by pulling the pin above 1.2V. $\overline{SHDN}$ can be driven above V_{IN} or V_{OUT} as long as it is limited to less than the absolute maximum rating.

Soft-Start

The soft-start time is programmed with an external capacitor to ground on SS. An internal current source charges the capacitor, C_{SS}, with a nominal 3µA. The voltage on SS is used to clamp the voltage on VC. The soft-start time is given by

$$t_{(msec)} = C_{SS}\ (\mu F) \bullet 200$$

In the event of an external shutdown or thermal shutdown (TSD), C_{SS} is discharged through a nominal 5kΩ impedance to GND. Once the condition is removed and SS is discharged near ground, a soft-start will automatically be re-initiated.

Error Amplifier

A transconductance amplifier generates an error voltage from the difference between the positive input internally connected to the 1.22V reference and the negative input connected to FB. A simple compensation network is placed from VC to ground. Internal clamps limit the minimum and maximum error amplifier output voltage for improved large signal transient response. A voltage divider from V_{OUT} to GND programs the output voltage via FB from 2V to 6V and is defined by the following equation:

$$V_{OUT} = 1.22 \bullet \left[1 + \left(\frac{R1}{R2}\right)\right]$$

Current Sensing

Lossless current sensing converts the peak current signal into a voltage which is summed with the internal slope compensation. This summed signal is compared to the error amplifier output to provide a peak current control command for the PWM. Peak switch current is limited to 750mA minimum.

Antiringing Control

The antiringing control connects a resistor across the inductor to damp the ringing on SW in discontinuous conduction mode. The LC resonant ringing (L = inductor, C_{SW} = capacitance on SW) is low energy, but can cause EMI radiation if antiringing control is not present.

Zero Current Comparator

The zero current comparator monitors the inductor current to the output and shuts off the synchronous rectifier once this current reduces to approximately 40mA, preventing negative inductor current.

OPERATION

Reverse-Battery Protection

Connecting the battery backwards poses a severe problem to most power converters. At a minimum the battery will be quickly discharged. Almost all ICs have an inherent diode from V_{IN} (cathode) to ground (anode) which conducts appreciable current when V_{IN} drops more than 0.7V below ground. Under this condition the integrated circuit will most likely be damaged due to the excessive current draw. There exists the possibility for the battery and circuitry powered by the device to also be damaged. The LTC3499/LTC3499B have integrated circuitry which allows negligible current flow under a reverse-battery condition, protecting the battery, device and circuitry attached to the output. A graph of the reverse-battery current drawn is shown in the Typical Performance Characteristics.

Discrete methods of reverse battery protection put additional dissipative elements in the high current path reducing efficiency while increasing component count to implement protection. The LTC3499/LTC3499B do not suffer from either of these drawbacks.

Burst Mode Operation (LTC3499 only)

Portable devices frequently spend extended time in low power or stand-by mode, only drawing high power when specific functions are enabled. In order to improve battery life in these types of products, high power converter efficiency needs to be maintained over a wide output power range. In addition to its high efficiency at moderate and heavy loads, the LTC3499 includes automatic Burst Mode operation that improves efficiency of the power converter at light loads. Burst Mode operation is initiated if the output load current falls below an internally programmed threshold (see Typical Performance graph, Output Load Burst Mode Threshold vs V_{IN}). Once initiated the Burst Mode operation circuitry shuts down most of the circuitry in the LTC3499, keeping alive only the circuitry required to monitor the output voltage.

This state is referred to as sleep. In sleep, the LTC3499 only draws 20µA from the input supply, greatly enhancing efficiency. When the output has drooped approximately 1% from its nominal regulation point, the LTC3499 wakes up and commences normal PWM operation. The output capacitor will recharge causing the LTC3499 to re-enter sleep if the output load current remains less than the sleep threshold. The frequency of this intermittent PWM (or burst) operation is proportional to load current. Therefore, as the load current drops further below the burst threshold, the LTC3499 operates in PWM mode less frequently. When the load current increases above the burst threshold, the LC3499 will resume continuous PWM operation seamlessly.

Referring to the Functional Block Diagram, an optional capacitor, C_{FF}, between V_{OUT} and FB in some circumstances can reduce peak-to-peak V_{OUT} ripple and input quiescent current during Burst Mode operation. Typical values for C_{FF} range from 10pF to 220pF.

Output Disconnect and Inrush Current Limiting

The LTC3499/LTC3499B are designed to allow true output disconnect by eliminating body diode conduction of the internal P-channel MOSFET switch. This allows V_{OUT} to go to zero volts during shutdown without drawing any current from the input source. It also provides for inrush current limiting at turn-on, minimizing surge current seen by the input supply.

$V_{IN} > V_{OUT}$ Operation

The LTC3499/LTC3499B will maintain voltage regulation when the input voltage is above the output voltage. This is achieved by terminating the switching on the synchronous P-channel MOSFET and applying V_{IN} statically on the gate. This will ensure the volts • seconds of the inductor will reverse during the time current is flowing to the output. Since this mode will dissipate more power in the IC, the maximum output current is limited in order to maintain an acceptable junction temperature:

$$I_{OUT(MAX)} \cong \frac{125 - T_A}{\theta_{JA} \bullet \left(\left(V_{IN} + 1.5 \right) - V_{OUT} \right)}$$

where T_A = ambient temperature and θ_{JA} is the package thermal resistance (45°C/W for the DD8 and 160°C/W for the MS8).

For example at V_{IN} = 4.5V, V_{OUT} = 3.3V and T_A = 85°C in the DD8 package, the maximum output current is 330mA.

APPLICATIONS INFORMATION

PCB LAYOUT GUIDELINES

The high speed operation of the LTC3499/LTC3499B demand careful attention to board layout. Advertised performance will not be achieved with careless layout. Figure 2 shows the recommended component placement. A large copper area will help to lower the chip temperature. Traces carrying high current (SW, V_{OUT}, GND) are kept short. The lead length to the battery should be kept as short as possible. The V_{IN} and V_{OUT} ceramic capacitors should be placed as close to the IC pins as possible.

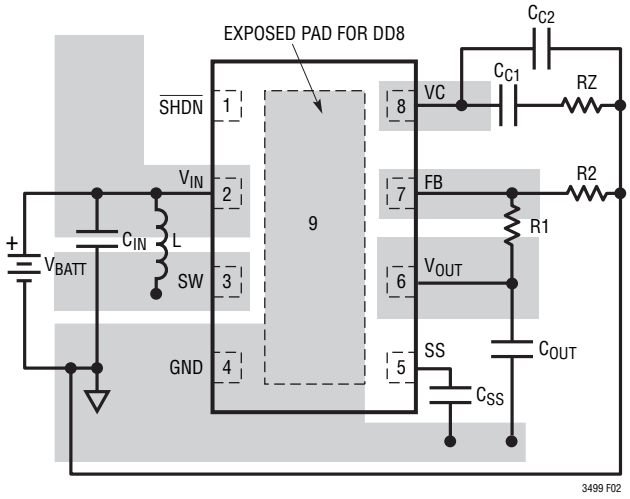


Figure 2: Recommended Component Placement

COMPONENT SELECTION

Inductor Selection

The LTC3499/LTC3499B allow the use of small surface mount inductors and chip inductors due to the fast 1.2MHz switching frequency. A minimum inductance value of 2.2µH is required. Larger values of inductance will allow greater output current capability by reducing the inductor ripple current. Increasing the inductance above 10µH will increase total solution area while providing minimal improvement in output current capability.

The inductor current ripple is typically set to 20% to 40% of the maximum inductor current. For high efficiency, choose an inductor with high frequency core material, such as ferrite, to reduce core losses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R power losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroidal or shielded inductor. See Table 1 for some suggested inductor suppliers.

Table 1. Inductor Vendor Information

PART NUMBER	SUPPLIER	WEB SITE
MSS5131 and MOS6020 Series	Coilcraft	www.coilcraft.com
SLF7028 and SLF7045 Series	TDK	www.component.tdk.com
LQH55D Series	Murata	www.murata.com
CDRH4D28 Series	Sumida	www.sumida.com
D53LC and D62CB Series	Toko	www.tokoam.com
DT0703 Series	CoEV	www.coev.net
MJPF2520 Series	FDK	www.fdk.com

Output Capacitor Selection

The output voltage ripple has three components to it. The bulk value of the capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The maximum ripple voltage due to charge is given by:

$$V_{RBULK} = I_P \bullet \frac{V_{IN}}{(C_{OUT} \bullet V_{OUT} \bullet f)}$$

where I_P = peak inductor current and f = switching frequency.

The ESR (equivalent series resistance) is usually the most dominant factor for ripple in most power converters. The ripple due to capacitor ESR is simply given by:

$$V_{RCESR} = I_P \bullet C_{ESR}$$

where C_{ESR} = capacitor equivalent series resistance.

APPLICATIONS INFORMATION

The ESL (equivalent series inductance) is also an important factor for high frequency converters. Using small surface mount ceramic capacitors, placed as close as possible to V_{OUT}, will minimize ESL.

Low ESR capacitors should be used to minimize output voltage ripple. A 4.7µF to 10µF output capacitor is sufficient for most applications and should be placed as close to V_{OUT} as possible. Larger values may be used to obtain even lower output ripple and improve transient response. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges.

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the input source and reduces input switching noise. Ceramic capacitors are a good choice for input decoupling due to their low ESR and ability to withstand reverse voltage (i.e. non-polar nature). The capacitor should be located as close as possible to the device. In most applications a 2.2µF input capacitor is sufficient. Larger values may be used without limitations. Table 2 shows a list of several ceramic capacitor manufacturers.

Table 2. Capacitor Vendor Information

SUPPLIER	WEB SITE
AVX	www.avxcorp.com
Murata	www.murata.com
TDK	www.component.tdk.com
Taiyo Yuden	www.t-yuden.com

Thermal Considerations

For the LTC3499/LTC3499B to deliver full output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. For the DFN package, this can be accomplished by taking advantage of the large thermal pad on the underside of the device. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the part and into a copper plane with as much area as possible. If the junction temperature continues to rise, the part will go into thermal shutdown where switching will stop until the temperature drops.

Closing the Feedback Loop

The LTC3499/LTC3499B utilize current mode control, with internal slope compensation. Current mode control eliminates the 2nd order filter due to the inductor and output capacitor exhibited in voltage mode controllers, thus simplifying it to a single pole filter response. The product of the modulator control to output DC gain and the error amp open loop gain gives the DC gain of the system:

$$G_{DC} = G_{CONTROL} \bullet G_{EA} \bullet \frac{V_{REF}}{V_{OUT} \bullet G_{CURRENT\_SENSE}}$$

$$G_{CONTROL} = 2 \bullet \frac{V_{IN}}{I_{OUT}},$$

$$G_{EA} \approx 1000,\ G_{CURRENT\_SENSE} = \frac{1}{R_{DS(ON)}}$$

The output filter pole is given by:

$$f_{FILTER\_POLE} = \frac{I_{OUT}}{(\pi \bullet V_{OUT} \bullet C_{OUT})}$$

where C_{OUT} is the output filter capacitor.

The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{(2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT})}$$

where R_{ESR} is the capacitor equivalent series resistance.

A troublesome feature of the boost regulator topology is the right half plane (RHP) zero, given by:

$$f_{RHPZ} = \frac{V_{IN}^{\ 2}}{(2 \bullet \pi \bullet I_{OUT} \bullet V_{OUT} \bullet L)}$$

APPLICATIONS INFORMATION

There is a resultant gain increase with a phase lag which makes it difficult to compensate the loop. At heavy loads the right half plane zero can occur at a relatively low frequency. The loop gain is typically rolled off before the RHP zero frequency.

The typical error amp compensation is shown in Figure 3, following the equations for the loop dynamics:

$$f_{POLE1} \sim \frac{1}{(2 \bullet \pi \bullet 10e6 \bullet C_{C1})}$$

which is extremely close to DC.

$$f_{ZERO1} = \frac{1}{(2 \bullet \pi \bullet R_Z \bullet C_{C1})}$$

$$f_{POLE2} = \frac{1}{(2 \bullet \pi \bullet R_Z \bullet C_{C2})}$$

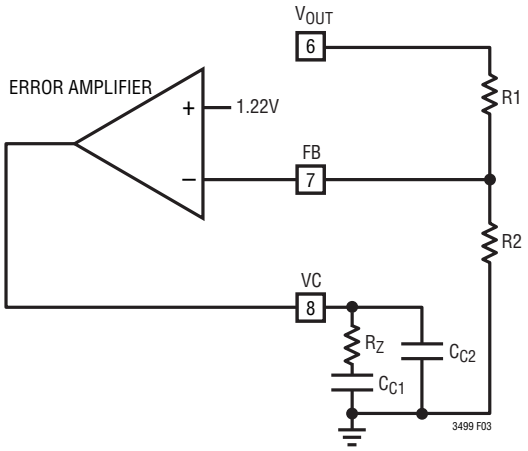
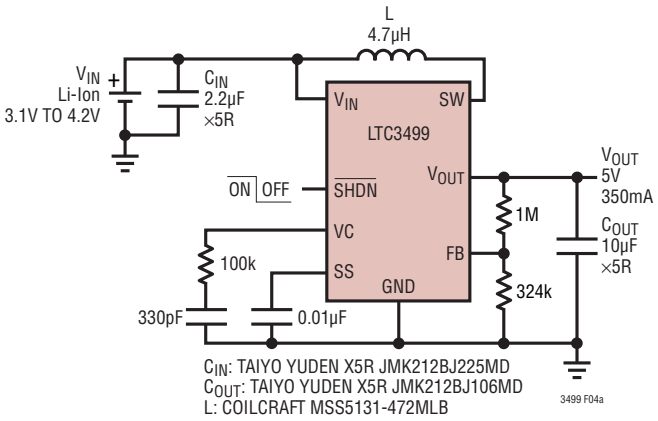


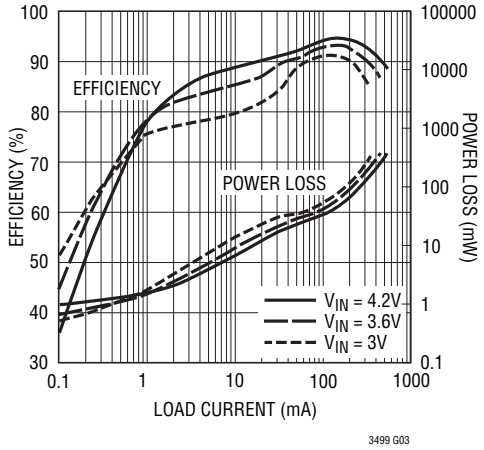
Figure 3: Typical Error Amplifier Compensation

TYPICAL APPLICATIONS

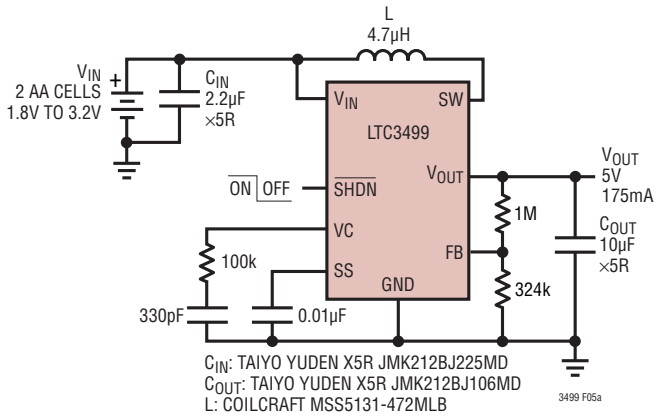
Lithium-Ion to 5V, 350mA



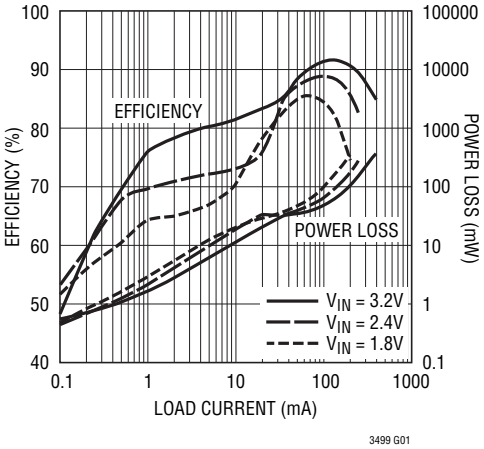
Lithium-Ion to 5V Efficiency



Two Cells to 5V, 175mA

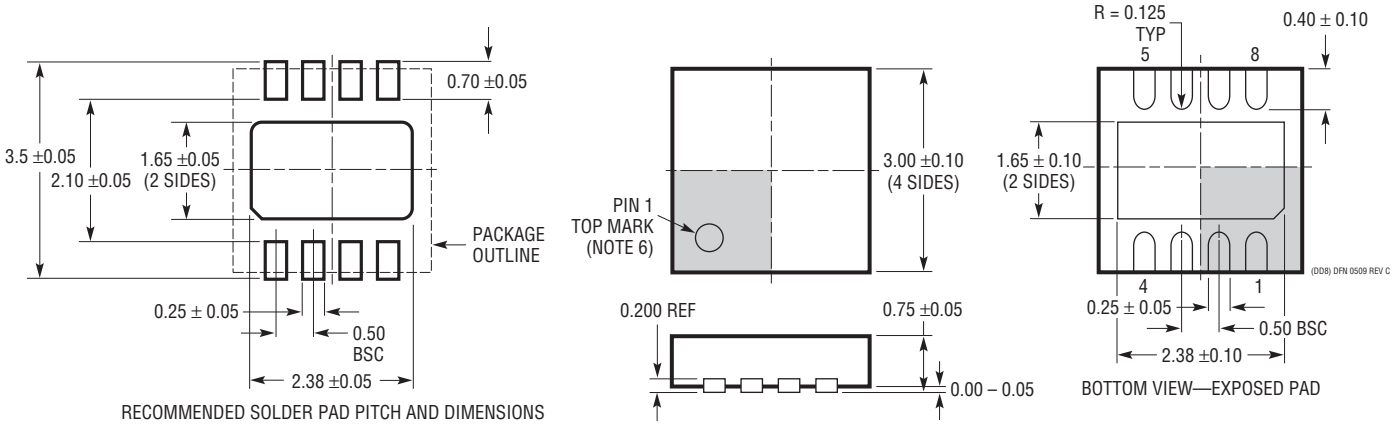


Two Cells to 5V Efficiency



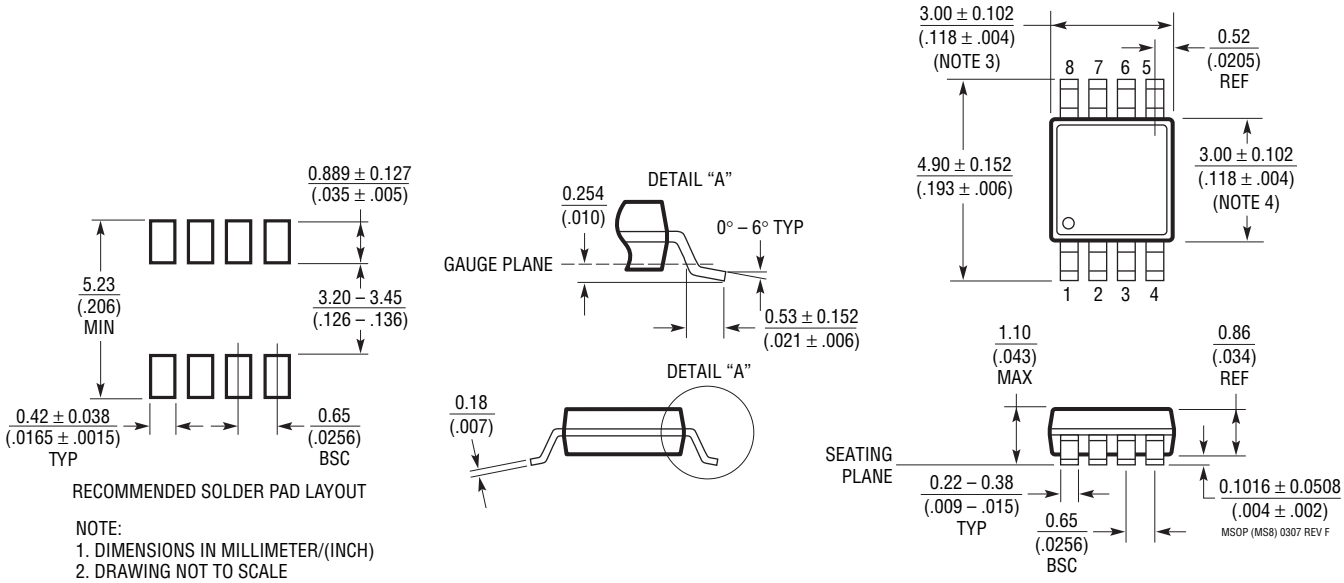
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)



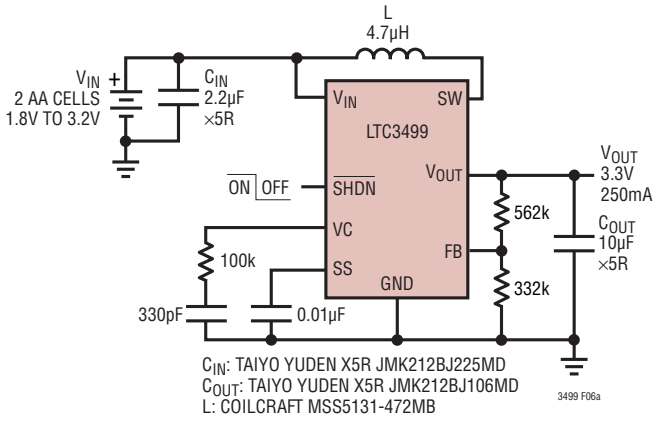
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	3/11	Updated Pin Functions for Pins 4 and 9.	6
		Corrected typo in Equation from f_{RPHZ} to f_{RHPZ}.	11

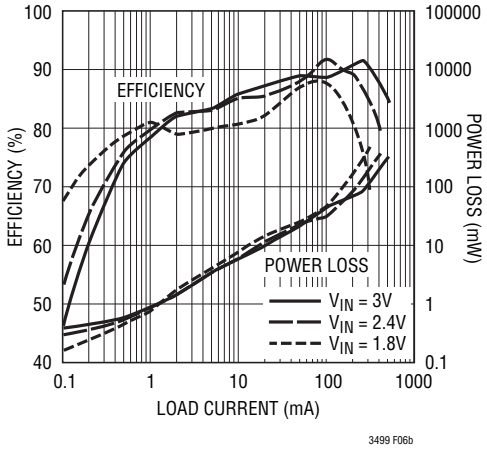
TYPICAL APPLICATION

Two Cells to 3.3V, 250mA



CIN: TAIYO YUDEN X5R JMK212BJ225MD
COUT: TAIYO YUDEN X5R JMK212BJ106MD
L: COILCRAFT MSS5131-472MB

Two Cells to 5V Efficiency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1930/LT1930A	1A (I_{SW}), 1.2MHz/2.2MHz, High Efficiency Step-Up DC/DC Converter	High Efficiency, V_{IN}: 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 4.2mA/5.5mA, I_{SD} < 1µA, ThinSOT Package
LT1961	1.5A (I_{SW}), 1.25MHz, High Efficiency Step-Up DC/DC Converter	90% Efficiency, V_{IN}: 3V to 25V, $V_{OUT(MAX)}$ = 35V, I_Q = 0.9mA, I_{SD} < 6µA, MS8E Package
LTC3400/LTC3400B	600mA (I_{SW}), 1.2MHz, Synchronous Step-Up DC/DC Converter	92% Efficiency, V_{IN}: 0.5V to 5V, $V_{OUT(MAX)}$ = 5V, I_Q = 19µA/300µA, I_{SD} < 1µA, ThinSOT Package
LTC3401	1A (I_{SW}), 3MHz, Synchronous Step-Up DC/DC Converter	97% Efficiency, VIN: 0.5V to 5V, $V_{OUT(MAX)}$ = 5.5V, I_Q = 38µA, I_{SD} < 1µA, 10-Lead MS Package
LTC3402	2A (I_{SW}), 3MHz, Synchronous Step-Up DC/DC Converter	97% Efficiency, VIN: 0.5V to 5V, $V_{OUT(MAX)}$ = 5.5V, I_Q = 38µA, I_{SD} < 1µA, 10-Lead MS Package
LTC3421	3A (I_{SW}), 3MHz, Synchronous Step-Up DC/DC Converter with Output Disconnect	95% Efficiency, V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 12µA, I_{SD} < 1µA, 24-Lead QFN Package
LTC3422	1.5A (I_{SW}), 3MHz, Synchronous Step-Up DC/DC Converter with Output Disconnect	95% Efficiency, V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 25µA, I_{SD} < 1µA
LTC3425	5A (I_{SW}), 8MHz, 4-Phase Synchronous Step-Up DC/DC Converter with Output Disconnect	95% Efficiency, V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 12µA, I_{SD} < 1µA, 32-Lead QFN Package
LTC3427	500mA (I_{SW}), 1.25MHz, Synchronous Step-Up DC/DC Converter with Soft-Start/Output Disconnect	94% Efficiency, V_{IN}: 1.8V to 5V, $V_{OUT(MAX)}$ = 5.25V, I_{SD} < 1µA, DFN Package
LTC3429/LTC3429B	600mA (I_{SW}), 550kHz, Synchronous Step-Up DC/DC Converters with Soft-Start/Output Disconnect	92% Efficiency, V_{IN}: 0.5V to 4.3V, $V_{OUT(MAX)}$ = 5V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3458/LTC3458L	1.4A/1.7A (I_{SW}), 1.5MHz, Synchronous Step-Up DC/DC Converter with Soft-Start/Output Disconnect	93% Efficiency, V_{IN}: 1.5V to 6V, $V_{OUT(MAX)}$ = 7.5V/6V, I_Q = 15µA, I_{SD} < 1µA, DFN Package
LTC3525	400mA (I_{SW}), Synchronous Step-Up DC/DC Converter in SC70	94% Efficiency, V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 7µA, I_{SD} < 1µA, Output Disconnect

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