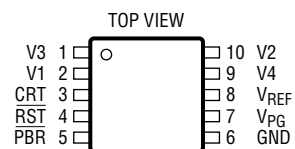
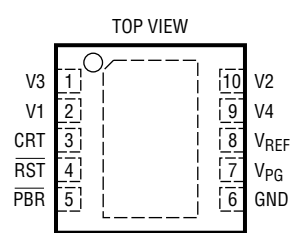


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

V1, V2, V3, V4, V _{PG} , PBR	–0.3V to 7V	V4 Input Current (–ADJ Mode)	–1mA
RST (LTC2900-1)	–0.3V to 7V	Operating Temperature Range	
RST (LTC2900-2)	–0.3V to (V _{CC} + 0.3V)	LTC2900-1C/LTC2900-2C	0°C to 70°C
CRT	–0.3V to (V _{CC} + 0.3V)	LTC2900-1I/LTC2900-2I	–40°C to 85°C
V _{REF}	–0.3V to (V _{CC} + 0.3V)	Storage Temperature Range	–65°C to 150°C
Reference Load Current (I _{VREF})	±1mA	Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

 MS PACKAGE 10-LEAD PLASTIC MSOP T_{JMAX} = 125°C, θ_{JA} = 250°C/W	ORDER PART NUMBER	 DD PACKAGE 10-LEAD (3mm x 3mm) PLASTIC DFN T_{JMAX} = 125°C, θ_{JA} = 43°C/W	ORDER PART NUMBER
	LTC2900-1CMS LTC2900-2CMS LTC2900-1IMS LTC2900-2IMS		LTC2900-1CDD LTC2900-2CDD LTC2900-1IDD LTC2900-2IDD
	MS PART MARKING		DD PART MARKING
	LTYJ LTYL LTYK LTYM		LABU LABW LABV LABX

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{RT50}	5V, 5% Reset Threshold	V1 Input Threshold ●	4.600	4.675	4.750	V
V _{RT33}	3.3V, 5% Reset Threshold	V1, V2 Input Threshold ●	3.036	3.086	3.135	V
V _{RT30}	3V, 5% Reset Threshold	V2 Input Threshold ●	2.760	2.805	2.850	V
V _{RT25}	2.5V, 5% Reset Threshold	V2, V3 Input Threshold ●	2.300	2.338	2.375	V
V _{RT18}	1.8V, 5% Reset Threshold	V3, V4 Input Threshold ●	1.656	1.683	1.710	V
V _{RT15}	1.5V, 5% Reset Threshold	V3, V4 Input Threshold ●	1.380	1.403	1.425	V
V _{RTA}	ADJ Reset Threshold	V3, V4 Input Threshold ●	0.492	0.500	0.508	V
V _{RTAN}	–ADJ Reset Threshold	V4 Input Threshold ●	–18	0	18	mV
V _{CC}	Minimum Internal Operating Voltage	RST in Correct Logic State, V _{CC} Rising Prior to Program ●			1	V
V _{CCMINP}	Minimum Required for Programming	V _{CC} Rising ●			2.42	V
V _{REF}	Reference Voltage	V _{CC} ≥ 2.3V, I _{VREF} = ±1mA, C _{REF} ≤ 1000pF ●	1.192	1.210	1.228	V
V _{PG}	Programming Voltage Range	V _{CC} ≥ V _{CCMINP} ●	0		V _{REF}	V
I _{VPG}	V _{PG} Input Current	V _{PG} = V _{REF} ●			±20	nA
I _{V1}	V1 Input Current	V1 = 5V, I _{VREF} = 12μA, (Note 4) ●		43	75	μA

2900f

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC} = 5\text{V}$, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{V2}	V2 Input Current	$V2 = 3.3\text{V}$	●	0.8	2	μA
I_{V3}	V3 Input Current	$V3 = 2.5\text{V}$ $V3 = 0.55\text{V}$ (ADJ Mode)	● ●	0.52	1.2 15	μA nA
I_{V4}	V4 Input Current	$V4 = 1.8\text{V}$ $V4 = 0.55\text{V}$ (ADJ Mode) $V4 = -0.05\text{V}$ (-ADJ Mode)	● ● ●	0.34	0.8 15 15	μA nA nA
$I_{\text{CRT(UP)}}$	CRT Pull-Up Current	$V_{\text{CRT}} = 0\text{V}$	●	-1.4	-2	μA
$I_{\text{CRT(DN)}}$	CRT Pull-Down Current	$V_{\text{CRT}} = 1.3\text{V}$	●	10	20	μA
t_{RST}	Reset Time-Out Period	$C_{\text{RT}} = 1500\text{pF}$	●	5	7	ms
t_{UV}	V_X Undervoltage Detect to $\overline{\text{RST}}$	V_X Less Than Reset Threshold V_{RTX} by More Than 1%		150		μs
V_{OL}	Output Voltage Low $\overline{\text{RST}}$	$I_{\text{SINK}} = 2.5\text{mA}$; $V1 = 3\text{V}$, $V2 = 3\text{V}$; $V3, V4 = 0\text{V}$; $V_{\text{PG}} = 0\text{V}$	●	0.15	0.4	V
		$I_{\text{SINK}} = 100\mu\text{A}$; $V2 = 1\text{V}$; $V1, V3, V4 = 0\text{V}$	●	0.05	0.3	V
		$I_{\text{SINK}} = 100\mu\text{A}$; $V1 = 1\text{V}$; $V2, V3, V4 = 0\text{V}$	●	0.05	0.3	V
V_{OH}	Output Voltage High $\overline{\text{RST}}$ (LTC2900-1) (Note 5)	$I_{\text{SOURCE}} = 1\mu\text{A}$	●	$V2 - 1$		V
	Output Voltage High $\overline{\text{RST}}$ (LTC2900-2) (Note 6)	$I_{\text{SOURCE}} = 200\mu\text{A}$	●	$0.8 \cdot V2$		V

Manual Reset Pin

V_{IH}	$\overline{\text{PBR}}$ Input Threshold High	$V_{\text{CC}} = 3.3\text{V}$ to 5.5V	●		1.6	V
V_{IL}	$\overline{\text{PBR}}$ Input Threshold Low	$V_{\text{CC}} = 3.3\text{V}$ to 5.5V	●	0.4		V
t_{PBW}	$\overline{\text{PBR}}$ Input Pulse Width	$V_{\text{CC}} = 3.3\text{V}$	●	150		ns
t_{PBD}	Manual Reset Propagation Delay	$V_{\text{CC}} = 3.3\text{V}$, $V_{\overline{\text{PBR}}}$ Falling	●	0.1	1	μs
I_{PBR}	$\overline{\text{PBR}}$ Pull-Up Current	$V_{\overline{\text{PBR}}} = 0\text{V}$		-10		μA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise noted.

Note 3: The greater of $V1$, $V2$ is the internal supply voltage (V_{CC}).

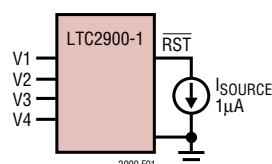
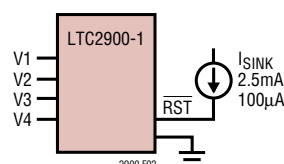
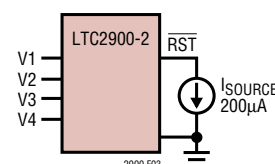
Note 4: Under static no-fault conditions, $V1$ will necessarily supply quiescent current. If at any time $V2$ is larger than $V1$, $V2$ must be capable of supplying

the quiescent current, programming (transient) current and reference load current.

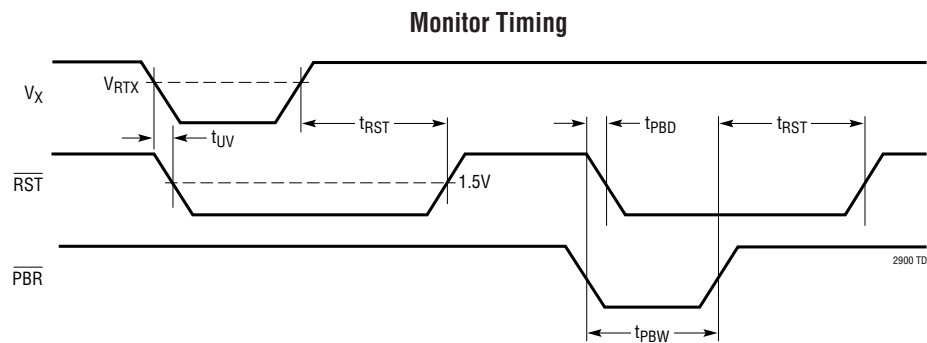
Note 5: The $\overline{\text{RST}}$ output pin on the LTC2900-1 has an internal pull-up to $V2$ of typically $6\mu\text{A}$. However, an external pull-up resistor may be used when faster rise times are required or for V_{OH} voltages greater than $V2$.

Note 6: The push-pull $\overline{\text{RST}}$ output pin on the LTC2900-2 is *actively* pulled up to $V2$.

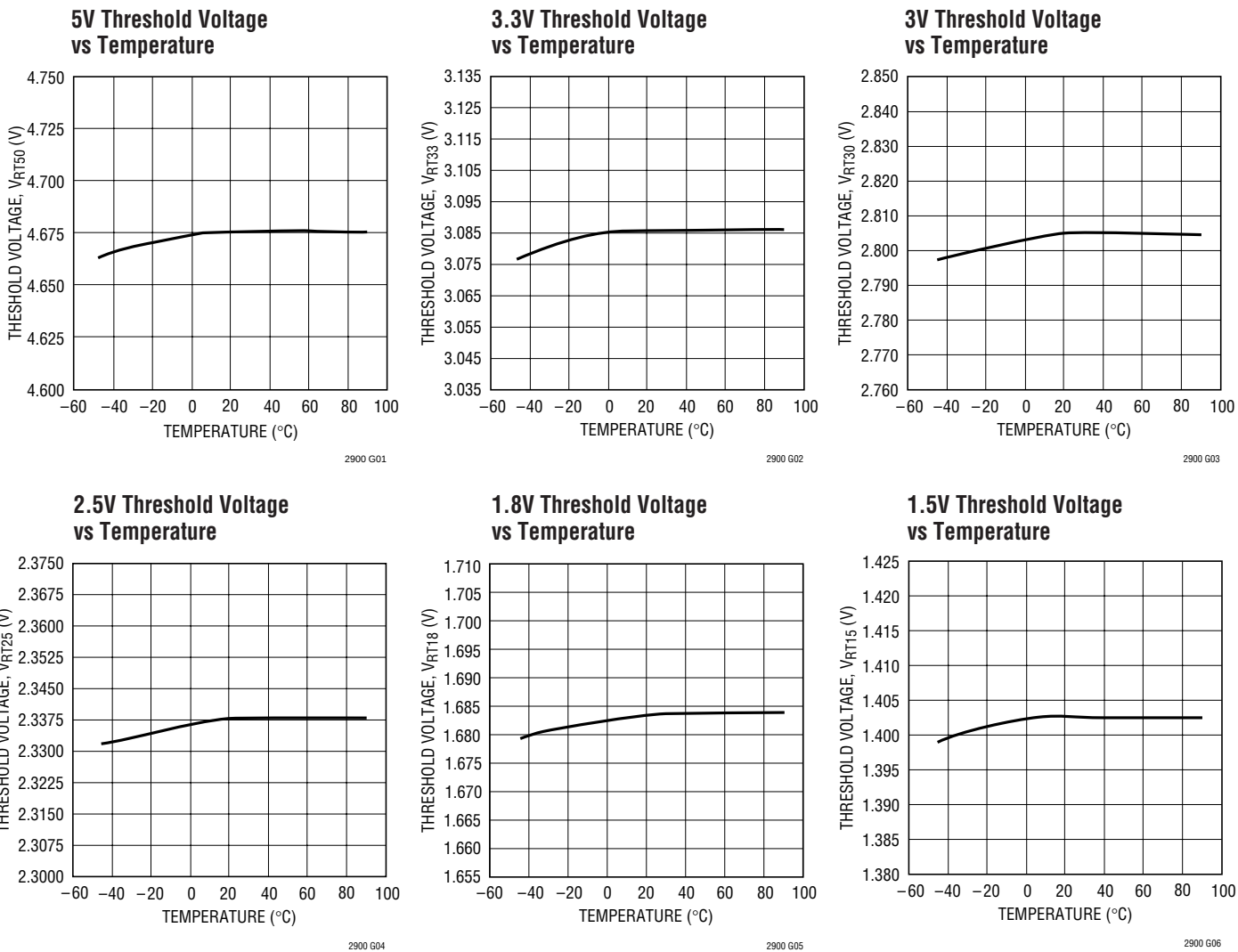
TEST CIRCUITS

Figure 1. $\overline{\text{RST}}$ V_{OH} TestFigure 2. $\overline{\text{RST}}$ V_{OL} TestFigure 3. Active Pull-Up
 $\overline{\text{RST}}$ V_{OH} Test

TIMING DIAGRAM

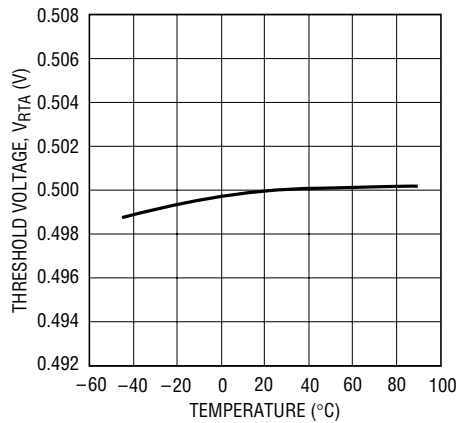


TYPICAL PERFORMANCE CHARACTERISTICS



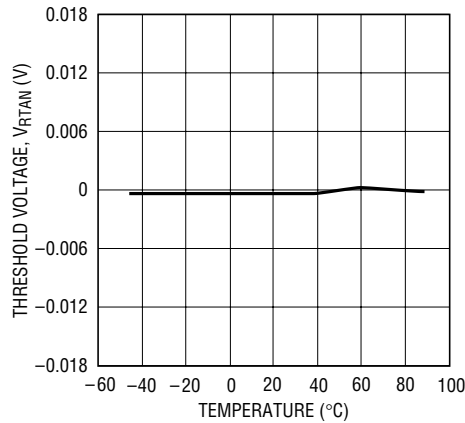
TYPICAL PERFORMANCE CHARACTERISTICS

**ADJ Threshold Voltage
vs Temperature**



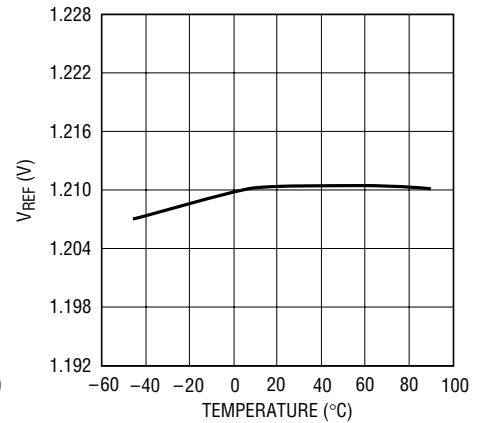
2900 G07

**-ADJ Threshold Voltage
vs Temperature**



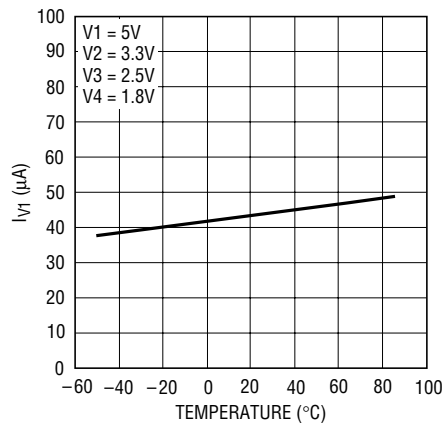
2900 G08

V_{REF} vs Temperature



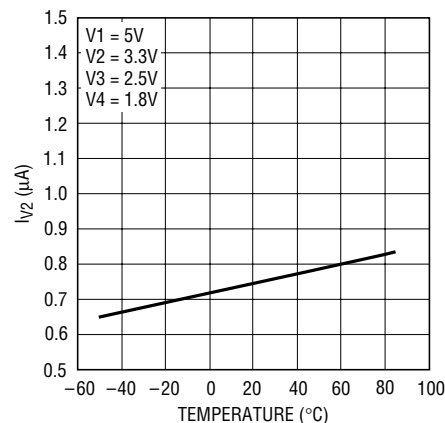
2900 G21

I_{V1} vs Temperature



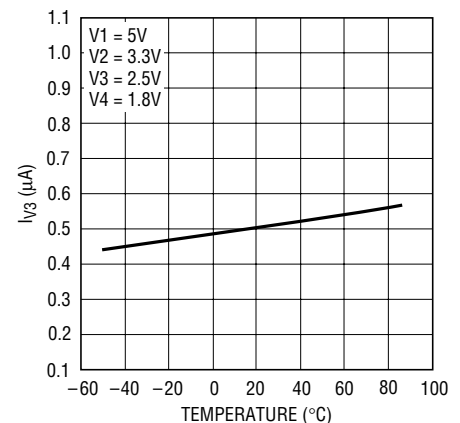
2900 G09

I_{V2} vs Temperature



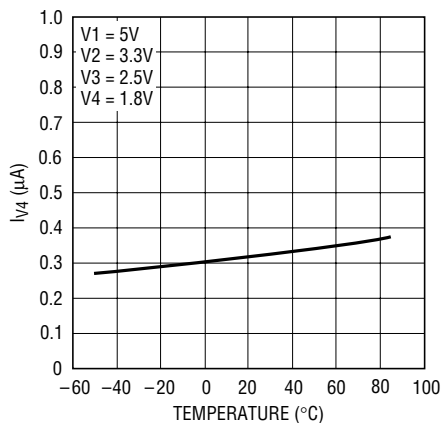
2900 G10

I_{V3} vs Temperature



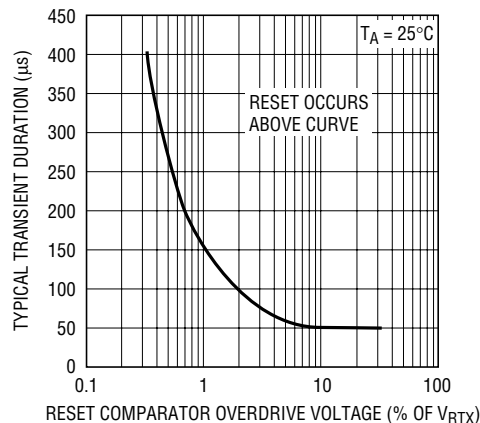
2900 G11

I_{V4} vs Temperature



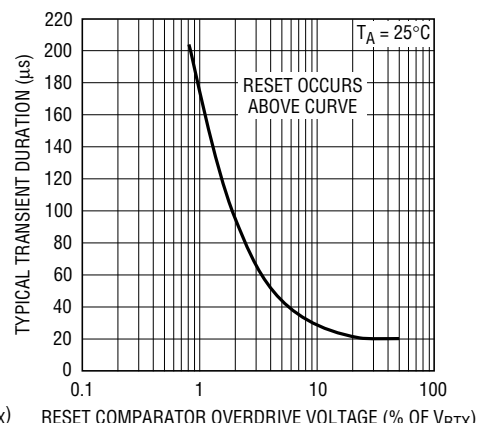
2900 G12

**Typical Transient Duration
vs Comparator Overdrive (V1, V2)**



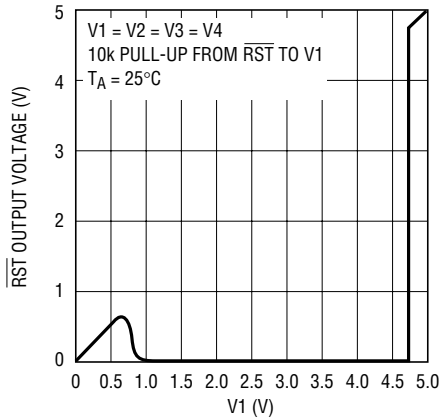
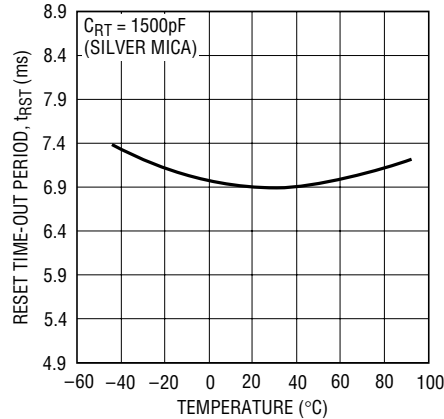
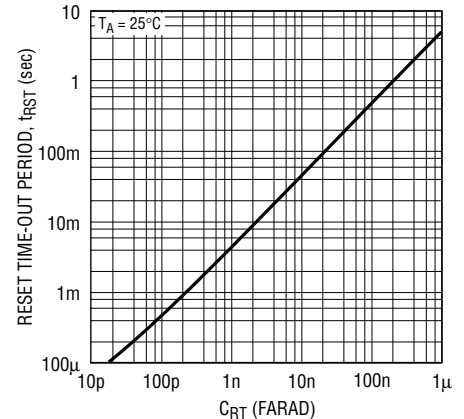
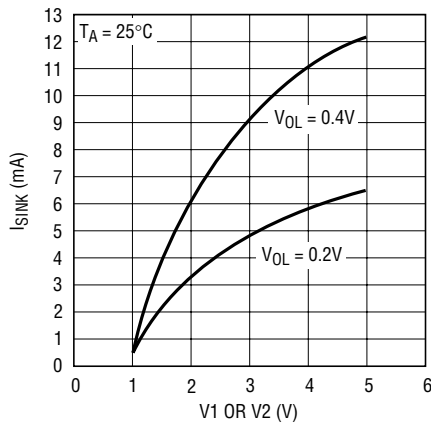
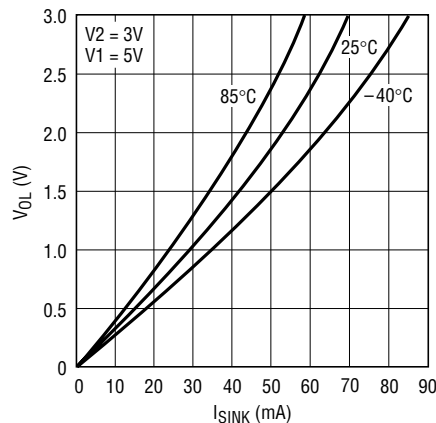
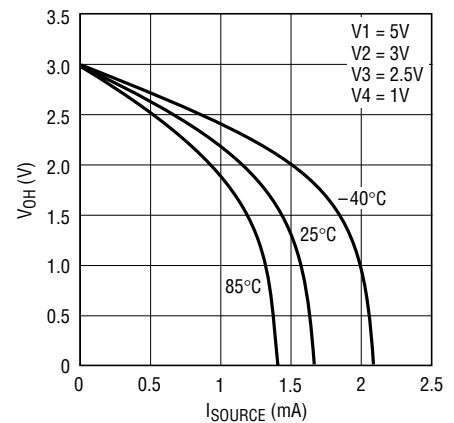
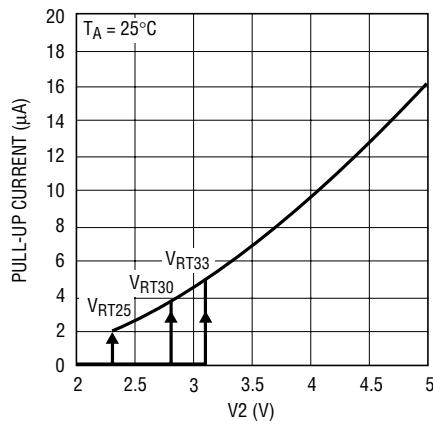
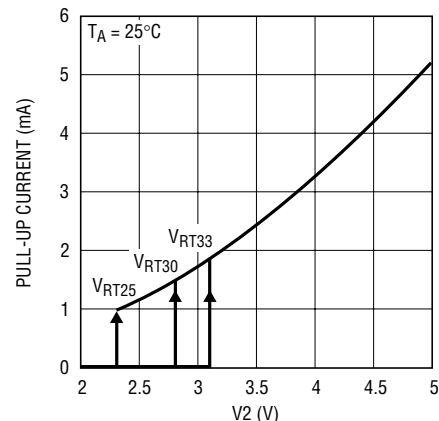
2900 G13

**Typical Transient Duration
vs Comparator Overdrive (V3, V4)**



2900 G20

TYPICAL PERFORMANCE CHARACTERISTICS

**RST Output Voltage
vs V1, $V_{PG} = 0V$**

**Reset Time-Out Period
vs Temperature**

**Reset Time-Out Period
vs Capacitance**

RST, I_{SINK} vs Supply Voltage

**RST Voltage Output Low
vs Output Sink Current**

**RST High Level Output Voltage
vs Output Source Current
(LTC2900-2)**

**RST Pull-Up Current vs V2
(LTC2900-1)**

**RST Pull-Up Current vs V2
(LTC2900-2)**


PIN FUNCTIONS

V3 (Pin 1): Voltage Input 3. Select from 2.5V, 1.8V, 1.5V or ADJ. See Table 1 for details.

V1 (Pin 2): Voltage Input 1. Select from 5V or 3.3V. See Table 1 for details. The greater of (V1, V2) is also V_{CC} for the device. Bypass this pin to ground with a 0.1 μ F (or greater) capacitor.

CRT (Pin 3): Reset Delay Time Programming Pin. Attach an external capacitor (C_{RT}) to GND to set a reset delay time of 4.6ms/nF. Leaving the pin open generates a minimum delay of approximately 50 μ s. A 47nF capacitor will generate a 216ms reset delay time.

RST (Pin 4): Reset Logic Output. Active low with weak pull-up to V2 (LTC2900-1) or active pull-up to V2 (LTC2900-2). Pulls low when any voltage input is below the reset threshold and held low for the programmed delay time after all voltage inputs are above threshold. May be pulled above V2 using an external pull-up (LTC2900-1 only).

PBR (Pin 5): Manual Reset Pin. Attach a push-button switch between this pin and ground. A logic low on this pin will pull $\overline{RST}$ low. When the $\overline{PBR}$ pin returns high, $\overline{RST}$ will return high after the programmed reset delay assuming all four voltage inputs are above threshold. A weak internal pull-up allows the pin to be left floating for normal monitor

operation. When using a switch, the switch is debounced through the reset circuitry using the delay provided by the C_{RT} timing capacitor.

GND (Pin 6): Ground.

V_{PG} (Pin 7): Voltage Threshold Combination Select Input. Connect to an external 1% resistive divider between V_{REF} and GND to select 1 of 16 combinations of preset and/or $\pm$ adjustable voltage thresholds (see Table 1). Do not add capacitance on the V_{PG} pin.

V_{REF} (Pin 8): Buffered Reference Voltage. A 1.210V nominal reference used for the programming voltage (V_{PG}) and for the offset of negative adjustable applications. The buffered reference can source and sink up to 1mA. The reference can drive a bypass capacitor of up to 1000pF without oscillation.

V4 (Pin 9): Voltage Input 4. Select from 1.8V, 1.5V, ADJ or –ADJ. See Table 1 for details.

V2 (Pin 10): Voltage Input 2. Select from 3.3V, 3V or 2.5V. See Table 1 for details. The greater of (V1, V2) is also V_{CC} for the device. Bypass this pin to ground with a 0.1 μ F (or greater) capacitor. $\overline{RST}$ is weakly pulled up to V2 (LTC2900-1). $\overline{RST}$ is actively pulled up to V2 in the LTC2900-2.



APPLICATIONS INFORMATION

Power-Up

The greater of V1, V2 is the internal supply voltage (V_{CC}). On power-up, V_{CC} will power the drive circuits for the $\overline{RST}$ pin. This ensures that the $\overline{RST}$ output will be low as soon as V1 or V2 reaches 1V. The $\overline{RST}$ output will remain low until the part is programmed. After programming, if any one of the V_X inputs is below its programmed threshold, $\overline{RST}$ will be a logic low. Once all the V_X inputs rise above their thresholds, an internal timer is started and $\overline{RST}$ is released after the programmed delay time. If $V_{CC} < (V3 - 1)$ and $V_{CC} < 2.4V$, the V3 input impedance will be low ($1k\Omega$ typ).

Monitor Programming

The LTC2900 input voltage combination is selected by placing the recommended resistive divider from V_{REF} to GND and connecting the tap point to V_{PG} , as shown in Figure 4. Table 1 offers recommended 1% resistor values

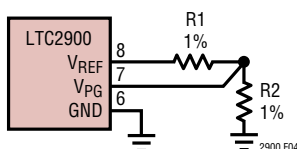


Figure 4. Monitor Programming

for the various modes. The last column in Table 1 specifies optimum V_{PG}/V_{REF} ratios (± 0.01) to be used when programming with a ratiometric DAC.

During power-up, once V1 or V2 reaches 2.4V max, the monitor enters a programming period of approximately $150\mu s$ during which the voltage on the V_{PG} pin is sampled and the monitor is configured to the desired input combination. Do not add capacitance to the V_{PG} pin. Immediately after programming, the comparators are enabled and supply monitoring will begin.

Table 1. Voltage Threshold Programming

MODE	V1 (V)	V2 (V)	V3 (V)	V4 (V)	R1 (k Ω)	R2 (k Ω)	V_{PG}/V_{REF}
0	5.0	3.3	ADJ	ADJ	Open	Short	0.000
1	5.0	3.3	ADJ	–ADJ	93.1	9.53	0.094
2	3.3	2.5	ADJ	ADJ	86.6	16.2	0.156
3	3.3	2.5	ADJ	–ADJ	78.7	22.1	0.219
4	3.3	2.5	1.5	ADJ	71.5	28.0	0.281
5	5.0	3.3	2.5	ADJ	66.5	34.8	0.344
6	5.0	3.3	2.5	1.8	59.0	40.2	0.406
7	5.0	3.3	2.5	1.5	53.6	47.5	0.469
8	5.0	3.0	2.5	ADJ	47.5	53.6	0.531
9	5.0	3.0	ADJ	ADJ	40.2	59.0	0.594
10	3.3	2.5	1.8	1.5	34.8	66.5	0.656
11	3.3	2.5	1.8	ADJ	28.0	71.5	0.719
12	3.3	2.5	1.8	–ADJ	22.1	78.7	0.781
13	5.0	3.3	1.8	–ADJ	16.2	86.6	0.844
14	5.0	3.3	1.8	ADJ	9.53	93.1	0.906
15	5.0	3.0	1.8	ADJ	Short	Open	1.000

Supply Monitoring

The LTC2900 is a low power, high accuracy programmable quad supply monitoring circuit with a common reset output and a manual reset input. Reset timing is adjustable using an external capacitor. Single pin programming selects 1 of 16 input voltage monitor combinations. All four voltage inputs must be above predetermined thresholds for the reset not to be invoked. The LTC2900 will assert the reset output during power-up, power-down and brownout conditions on any one of the voltage inputs.

The inverting inputs on the V3 and/or V4 comparators are set to 0.5V when the positive adjustable modes are selected (Figure 5). The tap point on an external resistive divider, connected between the positive voltage being

APPLICATIONS INFORMATION

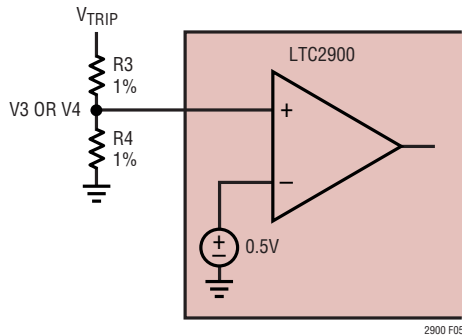


Figure 5. Setting the Positive Adjustable Trip Point

sensed and ground, is connected to the high impedance noninverting inputs (V3, V4). The trip voltage is calculated from:

VTRIP = 0.5V(1 + R3/R4)

In the negative adjustable mode, the noninverting input on the V4 comparator is connected to ground (Figure 6). The tap point on an external resistive divider, connected between the negative voltage being sensed and the VREF pin, is connected to the high impedance inverting input (V4). VREF provides the necessary level shift required to operate at ground. The trip voltage is calculated from:

VTRIP = -VREF(R3/R4); VREF = 1.210V Nominal

In a negative adjustable application, the minimum value for R4 is limited by the sourcing capability of VREF (±1mA). With no other load on VREF, R4 (minimum) is:

1.21V ÷ 1mA = 1.21kΩ.

Tables 2 and 3 offer suggested 1% resistor values for various adjustable applications.

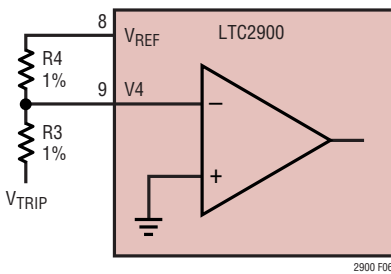


Figure 6. Setting the Negative Adjustable Trip Point

Table 2. Suggested 1% Resistor Values for the ADJ Inputs

VSUPPLY (V)	VTRIP (V)	R3 (kΩ)	R4 (kΩ)
12	11.25	2150	100
10	9.4	1780	100
8	7.5	1400	100
7.5	7	1300	100
6	5.6	1020	100
5	4.725	845	100
3.3	3.055	511	100
3	2.82	464	100
2.5	2.325	365	100
1.8	1.685	237	100
1.5	1.410	182	100
1.2	1.120	124	100
1	0.933	86.6	100
0.9	0.840	68.1	100

Table 3. Suggested 1% Resistor Values for the -ADJ Input

VSUPPLY (V)	VTRIP (V)	R3 (kΩ)	R4 (kΩ)
-2	-1.87	187	121
-5	-4.64	464	121
-5.2	-4.87	487	121
-10	-9.31	931	121
-12	-11.30	1130	121

APPLICATIONS INFORMATION

Although all four supply monitor comparators have built-in glitch immunity, bypass capacitors on V1 and V2 are recommended because the greater of V1 or V2 is also the V_{CC} for the device. Filter capacitors on the V3 and V4 inputs are allowed.

Power-Down

On power-down, once any of the V_X inputs drop below their threshold, $\overline{RST}$ is held at a logic low. A logic low of 0.4V is guaranteed until both V1 and V2 drop below 1V. If the bandgap reference becomes invalid ($V_{CC} < 2V$ typ), the part will reprogram once V_{CC} rises above 2.4V max.

Monitor Output Rise and Fall Time Estimation

The $\overline{RST}$ output has strong pull-down capability. If the external load capacitance (C_{LOAD}) is known, output fall time (10% to 90%) is estimated using:

$$t_{FALL} \approx 2.2 \cdot R_{PD} \cdot C_{LOAD}$$

where R_{PD} is the on-resistance of the internal pull-down transistor. The typical performance curve (V_{OL} vs I_{SINK}) demonstrates that the pull-down current is somewhat linear versus output voltage. Using the 25°C curve, R_{PD} is estimated to be approximately 40Ω. Assuming a 150pF load capacitance, the fall time is about 13.2ns.

Although the $\overline{RST}$ output of the LTC2900-1 is considered to be “open-drain,” it does have weak pull-up capability (see $\overline{RST}$ Pull-Up Current vs V2 curve). Output rise time (10% to 90%) is estimated using:

$$t_{RISE} \approx 2.2 \cdot R_{PU} \cdot C_{LOAD}$$

where R_{PU} is the on-resistance of the pull-up transistor. The on-resistance as a function of the V2 voltage at room temperature is estimated using:

$$R_{PU} = \frac{6 \cdot 10^5}{V2 - 1} \Omega$$

with $V2 = 3.3V$, R_{PU} is about 260k. Using 150pF for load capacitance, the rise time is 86μs. If the output needs to pull up faster and/or to a higher voltage, a smaller external pull-up resistor may be used. Using a 10k pull-up resistor, the rise time is reduced to 3.3μs for a 150pF load capacitance.

The LTC2900-2 has an active pull-up to V2 on the $\overline{RST}$ output. The typical performance curve ($\overline{RST}$ Pull-Up Current vs V2 curve) demonstrates that the pull-up current is somewhat linear versus the V2 voltage and R_{PU} is estimated to be approximately 625Ω. A 150pF load capacitance makes the rise time about 206ns.

Selecting the Reset Timing Capacitor

The reset time-out period is adjustable in order to accommodate a variety of microprocessor applications. The reset time-out period, t_{RST} , is adjusted by connecting a capacitor, C_{RT} , between the CRT pin and ground. The value of this capacitor is determined by:

$$C_{RT} = t_{RST} \cdot 217 \cdot 10^{-9}$$

with C_{RT} in Farads and t_{RST} in seconds. The C_{RT} value per millisecond of delay can also be expressed as $C_{RT}/ms = 217$ (pF/ms).

Leaving the CRT pin unconnected will generate a minimum reset time-out of approximately 50μs. Maximum reset time-out is limited by the largest available low leakage capacitor. The accuracy of the time-out period will be affected by capacitor leakage (the nominal charging current is 2μA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

APPLICATIONS INFORMATION

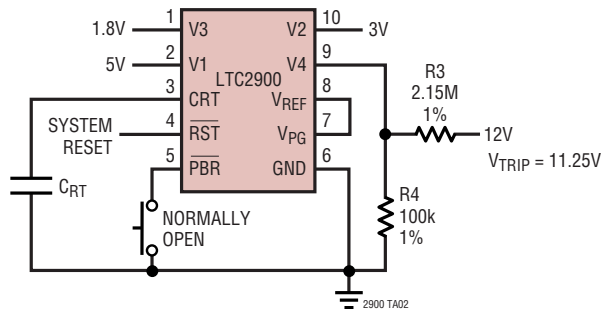
Ensuring Reset Valid for V_{CC} Down to 0V (LTC2900-2)

Some applications require the reset output ($\overline{RST}$) to be valid with V_{CC} down to 0V. The LTC2900-2 is designed to handle this requirement with the addition of an external resistor from $\overline{RST}$ to ground. The resistor will provide a path for stray charge and/or leakage currents, preventing the $\overline{RST}$ output from floating to undetermined voltages

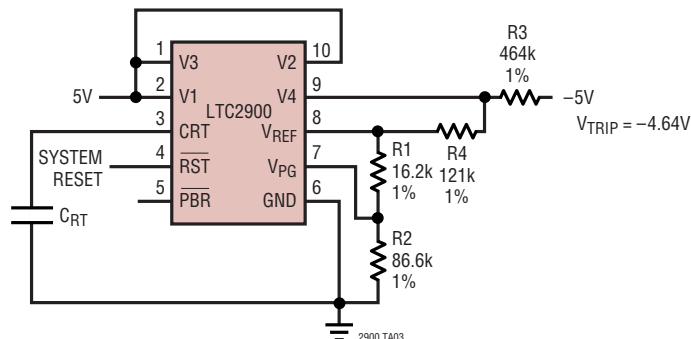
when connected to high impedance (such as CMOS logic inputs). The resistor value should be small enough to provide effective pull-down without excessively loading the active pull-up circuitry. Too large a value may not pull down well enough. A 100k resistor from $\overline{RST}$ to ground is satisfactory for most applications.

TYPICAL APPLICATIONS

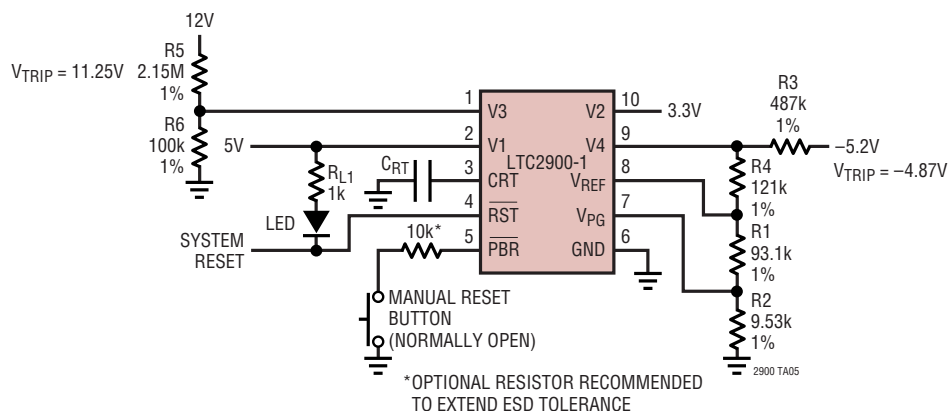
Quad Supply Monitor with Push-Button Reset
5V, 3V, 1.8V, 12V (ADJ)



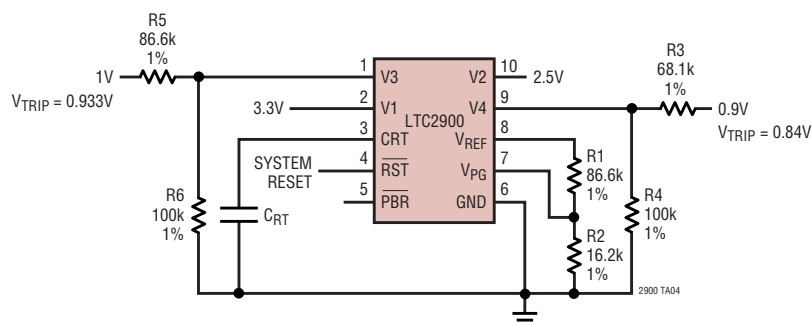
5V, -5V Monitor and Unused V2, V3 Inputs
Pulled Above Trip Thresholds



TYPICAL APPLICATIONS

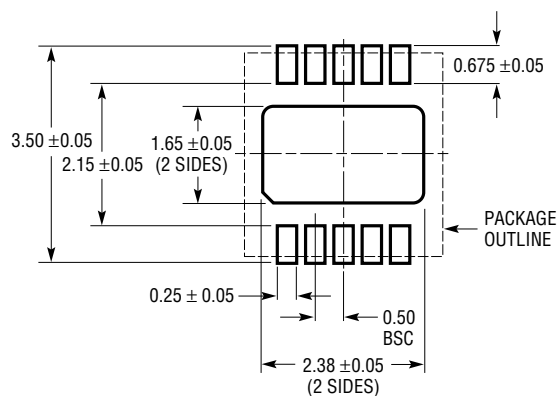
5V, 3.3V, 12V, -5.2V Monitor with Manual Reset and LED Indication on $\overline{\text{RST}}$ 

Low Voltage Quad Supply Monitor 3.3V, 2.5V, 1V (ADJ), 0.9V (ADJ)

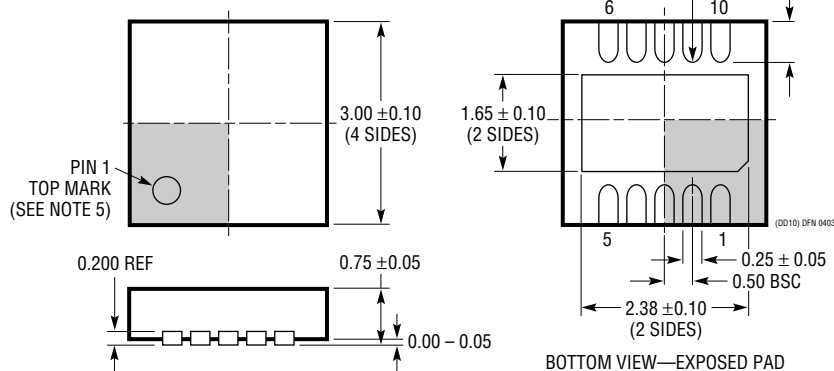


PACKAGE DESCRIPTION

DD Package 10-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1699)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

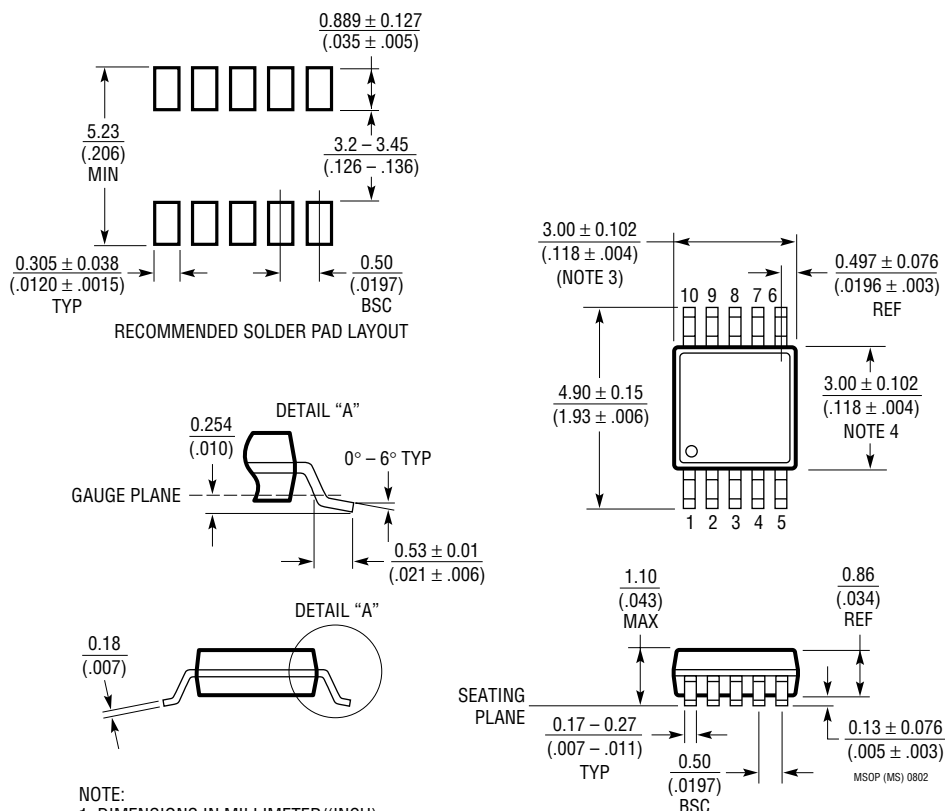


NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS Package 10-Lead Plastic MSOP (Reference LTC DWG # 05-08-1661)



NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

