

# LTC1860/LTC1861

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

|                                 |                                     |                                      |                |
|---------------------------------|-------------------------------------|--------------------------------------|----------------|
| Supply Voltage ( $V_{CC}$ )     | 7V                                  | Power Dissipation                    | 400mW          |
| Ground Voltage Difference       |                                     | Operating Temperature Range          |                |
| AGND, DGND LTC1861 MSOP Package | $\pm 0.3V$                          | LTC1860C/LTC1861C                    | 0°C to 70°C    |
| Analog Input                    | (GND – 0.3V) to ( $V_{CC} + 0.3V$ ) | LTC1860I/LTC1861I                    | –40°C to 85°C  |
| Digital Input                   | (GND – 0.3V) to 7V                  | LTC1860H/LTC1861H                    | –40°C to 125°C |
| Digital Output                  | (GND – 0.3V) to ( $V_{CC} + 0.3V$ ) | Storage Temperature Range            | –65°C to 150°C |
|                                 |                                     | Lead Temperature (Soldering, 10 sec) | 300°C          |

## PIN CONFIGURATION

|                                                                                                                                         |                                                                                                                                         |
|-----------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| <b>LTC1860</b><br><br><p>MS8 PACKAGE<br/>8-LEAD PLASTIC MSOP<br/><math>T_{JMAX} = 150^{\circ}C, \theta_{JA} = 210^{\circ}C/W</math></p> | <b>LTC1861</b><br><br><p>MS PACKAGE<br/>10-LEAD PLASTIC MSOP<br/><math>T_{JMAX} = 150^{\circ}C, \theta_{JA} = 210^{\circ}C/W</math></p> |
| <b>LTC1860</b><br><br><p>S8 PACKAGE<br/>8-LEAD PLASTIC SO<br/><math>T_{JMAX} = 150^{\circ}C, \theta_{JA} = 175^{\circ}C/W</math></p>    | <b>LTC1861</b><br><br><p>S8 PACKAGE<br/>8-LEAD PLASTIC SO<br/><math>T_{JMAX} = 150^{\circ}C, \theta_{JA} = 175^{\circ}C/W</math></p>    |

**ORDER INFORMATION** <http://www.linear.com/product/LTC1860#orderinfo>

| LEAD FREE FINISH | TAPE AND REEL     | PART MARKING | PACKAGE DESCRIPTION  | TEMPERATURE RANGE |
|------------------|-------------------|--------------|----------------------|-------------------|
| LTC1860CMS8#PBF  | LTC1860CMS8#TRPBF | LTWR         | 8-Lead Plastic MSOP  | 0°C to 70°C       |
| LTC1860IMS8#PBF  | LTC1860IMS8#TRPBF | LTWS         | 8-Lead Plastic MSOP  | -40°C to 85°C     |
| LTC1860HMS8#PBF  | LTC1860HMS8#TRPBF | LTWS         | 8-Lead Plastic MSOP  | -40°C to 125°C    |
| LTC1860CS8#PBF   | LTC1860CS8#TRPBF  | 1860         | 8-Lead Plastic SO    | 0°C to 70°C       |
| LTC1860IS8#PBF   | LTC1860IS8#TRPBF  | 1860I        | 8-Lead Plastic SO    | -40°C to 85°C     |
| LTC1861CMS#PBF   | LTC1861CMS#TRPBF  | LTWT         | 10-Lead Plastic MSOP | 0°C to 70°C       |
| LTC1861IMS#PBF   | LTC1861IMS#TRPBF  | LTWU         | 10-Lead Plastic MSOP | -40°C to 85°C     |
| LTC1861HMS#PBF   | LTC1861HMS#TRPBF  | LTWU         | 10-Lead Plastic MSOP | -40°C to 125°C    |
| LTC1861CS8#PBF   | LTC1861CS8#TRPBF  | 1861         | 8-Lead Plastic SO    | 0°C to 70°C       |
| LTC1861IS8#PBF   | LTC1861IS8#TRPBF  | 1861I        | 8-Lead Plastic SO    | -40°C to 85°C     |

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 5\text{V}$ ,  $V_{REF} = 5\text{V}$ ,  $f_{SCK} = f_{SCK}(\text{MAX})$  as defined in Recommended Operating Conditions, unless otherwise noted.

| SYMBOL                           | CONDITIONS                                            | MIN            | TYP      | MAX                           | UNITS              |
|----------------------------------|-------------------------------------------------------|----------------|----------|-------------------------------|--------------------|
| Resolution                       | ●                                                     | 12             |          |                               | Bits               |
| No Missing Codes Resolution      | ●                                                     | 12             |          |                               | Bits               |
| INL                              | (Note 3) ●                                            |                |          | ±1                            | LSB                |
| Transition Noise                 |                                                       |                | 0.07     |                               | LSB <sub>RMS</sub> |
| Gain Error                       | ●                                                     |                |          | ±20                           | mV                 |
| Offset Error                     | LTC1860 SO-8 and MSOP, LTC1861 MSOP<br>LTC1861 SO-8 ● |                | ±2<br>±3 | ±5<br>±7                      | mV<br>mV           |
| Input Differential Voltage Range | $V_{IN} = IN^+ - IN^-$ ●                              | 0              |          | $V_{REF}$                     | V                  |
| Absolute Input Range             | IN <sup>+</sup> Input<br>IN <sup>-</sup> Input        | -0.05<br>-0.05 |          | $V_{CC} + 0.05$<br>$V_{CC}/2$ | V<br>V             |
| $V_{REF}$ Input Range            | LTC1860 SO-8 and MSOP, LTC1861 MSOP                   | 1              |          | $V_{CC}$                      | V                  |
| Analog Input Leakage Current     | (Note 4) ●                                            |                |          | ±1                            | μA                 |
| $C_{IN}$ Input Capacitance       | In Sample Mode<br>During Conversion                   |                | 12<br>5  |                               | pF<br>pF           |

## DYNAMIC ACCURACY

$T_A = 25^\circ\text{C}$ .  $V_{CC} = 5\text{V}$ ,  $f_{SAMPLE} = 250\text{kHz}$ , unless otherwise specified.

| SYMBOL    | PARAMETER                                    | CONDITIONS                   | MIN | TYP | MAX | UNITS |
|-----------|----------------------------------------------|------------------------------|-----|-----|-----|-------|
| SNR       | Signal-to-Noise Ratio                        |                              |     | 72  |     | dB    |
| S/(N + D) | Signal-to-Noise Plus Distortion Ratio        | 100kHz Input Signal          |     | 71  |     | dB    |
| THD       | Total Harmonic Distortion Up to 5th Harmonic | 100kHz Input Signal          |     | 77  |     | dB    |
|           | Full Power Bandwidth                         |                              |     | 20  |     | MHz   |
|           | Full Linear Bandwidth                        | $S/(N + D) \geq 68\text{dB}$ |     | 125 |     | kHz   |

**DIGITAL AND DC ELECTRICAL CHARACTERISTICS** The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 5\text{V}$ ,  $V_{REF} = 5\text{V}$ , unless otherwise noted.

| SYMBOL   | PARAMETER                 | CONDITIONS                                                                                              | MIN        | TYP          | MAX  | UNITS  |
|----------|---------------------------|---------------------------------------------------------------------------------------------------------|------------|--------------|------|--------|
| $V_{IH}$ | High Level Input Voltage  | $V_{CC} = 5.25\text{V}$ ●                                                                               | 2.4        |              |      | V      |
| $V_{IL}$ | Low Level Input Voltage   | $V_{CC} = 4.75\text{V}$ ●                                                                               |            |              | 0.8  | V      |
| $I_{IH}$ | High Level Input Current  | $V_{IN} = V_{CC}$ ●                                                                                     |            |              | 2.5  | μA     |
| $I_{IL}$ | Low Level Input Current   | $V_{IN} = 0\text{V}$ ●                                                                                  |            |              | -2.5 | μA     |
| $V_{OH}$ | High Level Output Voltage | $V_{CC} = 4.75\text{V}$ , $I_O = 10\mu\text{A}$ ●<br>$V_{CC} = 4.75\text{V}$ , $I_O = 360\mu\text{A}$ ● | 4.5<br>2.4 | 4.74<br>4.72 |      | V<br>V |
| $V_{OL}$ | Low Level Output Voltage  | $V_{CC} = 4.75\text{V}$ , $I_O = 1.6\text{mA}$ ●                                                        |            |              | 0.4  | V      |

## DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 5\text{V}$ ,  $V_{REF} = 5\text{V}$ , unless otherwise noted.

| SYMBOL       | PARAMETER                                               | CONDITIONS                                                                                                        | MIN | TYP                    | MAX           | UNITS                                |
|--------------|---------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-----|------------------------|---------------|--------------------------------------|
| $I_{OZ}$     | Hi-Z Output Leakage                                     | CONV = $V_{CC}$ ●                                                                                                 |     |                        | ±3            | $\mu\text{A}$                        |
| $I_{SOURCE}$ | Output Source Current                                   | $V_{OUT} = 0\text{V}$                                                                                             |     | -25                    |               | mA                                   |
| $I_{SINK}$   | Output Sink Current                                     | $V_{OUT} = V_{CC}$                                                                                                |     | 20                     |               | mA                                   |
| $I_{REF}$    | Reference Current (LTC1860 SO-8, MSOP and LTC1861 MSOP) | CONV = $V_{CC}$ ●<br>$f_{SMPL} = f_{SMPL(MAX)}$ ●                                                                 |     | 0.001<br>0.05          | 3<br>0.1      | $\mu\text{A}$<br>mA                  |
| $I_{CC}$     | Supply Current                                          | CONV = $V_{CC}$ After Conversion ●<br>CONV = $V_{CC}$ After Conversion, H-Grade ●<br>$f_{SMPL} = f_{SMPL(MAX)}$ ● |     | 0.001<br>0.001<br>0.85 | 3<br>5<br>1.3 | $\mu\text{A}$<br>$\mu\text{A}$<br>mA |
| $P_D$        | Power Dissipation                                       | $f_{SMPL} = f_{SMPL(MAX)}$                                                                                        |     | 1.25                   |               | mW                                   |

## RECOMMENDED OPERATING CONDITIONS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^\circ\text{C}$ .

| SYMBOL       | PARAMETER                                          | CONDITIONS                           | MIN                       | TYP      | MAX        | UNITS         |
|--------------|----------------------------------------------------|--------------------------------------|---------------------------|----------|------------|---------------|
| $V_{CC}$     | Supply Voltage                                     |                                      | 4.75                      |          | 5.25       | V             |
| $f_{SCK}$    | Clock Frequency                                    | H-Grade ●                            |                           |          | 20<br>16.7 | MHz<br>MHz    |
| $t_{CYC}$    | Total Cycle Time                                   |                                      | $12 \cdot SCK + t_{CONV}$ |          |            | $\mu\text{s}$ |
| $t_{SMPL}$   | Analog Input Sampling Time                         | LTC1860 (Note 5)<br>LTC1861 (Note 5) | 12<br>10                  |          |            | SCK<br>SCK    |
| $t_{suCONV}$ | Setup Time CONV↓ Before First SCK↑, (See Figure 1) | H-Grade                              | 60<br>65                  | 30<br>30 |            | ns<br>ns      |
| $t_{hDI}$    | Holdtime SDI After SCK↑                            | LTC1861                              | 15                        |          |            | ns            |
| $t_{suDI}$   | Setup Time SDI Stable Before SCK↑                  | LTC1861                              | 15                        |          |            | ns            |
| $t_{WHCLK}$  | SCK High Time                                      | $f_{SCK} = f_{SCK(MAX)}$             | 40%                       |          |            | $1/f_{SCK}$   |
| $t_{WLCLK}$  | SCK Low Time                                       | $f_{SCK} = f_{SCK(MAX)}$             | 40%                       |          |            | $1/f_{SCK}$   |
| $t_{WHCONV}$ | CONV High Time Between Data Transfer Cycles        | (Note 5)                             | $t_{CONV}$                |          |            | $\mu\text{s}$ |
| $t_{WLCONV}$ | CONV Low Time During Data Transfer                 | (Note 5)                             | 12                        |          |            | SCK           |
| $t_{hCONV}$  | Hold Time CONV Low After Last SCK↑                 |                                      |                           | 13       |            | ns            |

**TIMING CHARACTERISTICS** The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 5\text{V}$ ,  $V_{REF} = 5\text{V}$ ,  $f_{SCK} = f_{SCK(MAX)}$  as defined in Recommended Operating Conditions, unless otherwise noted.

| SYMBOL           | PARAMETER                                            | CONDITIONS                                                                                 |             | MIN        | TYP          | MAX            | UNITS                                     |
|------------------|------------------------------------------------------|--------------------------------------------------------------------------------------------|-------------|------------|--------------|----------------|-------------------------------------------|
| $t_{CONV}$       | Conversion Time (See Figure 1)                       | H-Grade                                                                                    | ●<br>●      |            | 2.75<br>2.75 | 3.2<br>3.3     | $\mu\text{s}$<br>$\mu\text{s}$            |
| $f_{SAMPL(MAX)}$ | Maximum Sampling Frequency                           | H-Grade                                                                                    | ●<br>●      | 250<br>248 |              |                | $\text{kHz}$<br>$\text{kHz}$              |
| $t_{dDO}$        | Delay Time, $SCK\downarrow$ to SDO Data Valid        | $C_{LOAD} = 20\text{pF}$<br>$C_{LOAD} = 20\text{pF}$<br>$C_{LOAD} = 20\text{pF}$ , H-Grade | ●<br>●<br>● |            | 15           | 20<br>25<br>30 | $\text{ns}$<br>$\text{ns}$<br>$\text{ns}$ |
| $t_{dis}$        | Delay Time, $CONV\uparrow$ to SDO Hi-Z               | H-Grade                                                                                    | ●<br>●      |            | 30<br>30     | 60<br>65       | $\text{ns}$<br>$\text{ns}$                |
| $t_{en}$         | Delay Time, $CONV\downarrow$ to SDO Enabled          | $C_{LOAD} = 20\text{pF}$<br>$C_{LOAD} = 20\text{pF}$ , H-Grade                             | ●<br>●      |            | 30<br>30     | 60<br>65       | $\text{ns}$<br>$\text{ns}$                |
| $t_{hDO}$        | Time Output Data Remains Valid After $SCK\downarrow$ | $C_{LOAD} = 20\text{pF}$                                                                   | ●           | 5          | 10           |                | $\text{ns}$                               |
| $t_r$            | SDO Rise Time                                        | $C_{LOAD} = 20\text{pF}$                                                                   |             |            | 8            |                | $\text{ns}$                               |
| $t_f$            | SDO Fall Time                                        | $C_{LOAD} = 20\text{pF}$                                                                   |             |            | 4            |                | $\text{ns}$                               |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to GND.

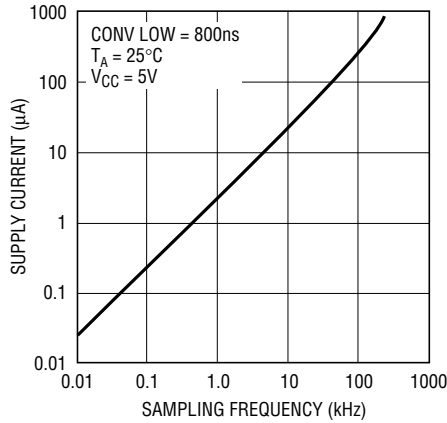
**Note 3:** Integral nonlinearity is defined as deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 4:** Channel leakage current is measured while the part is in sample mode.

**Note 5:** Guaranteed by design, not subject to test.

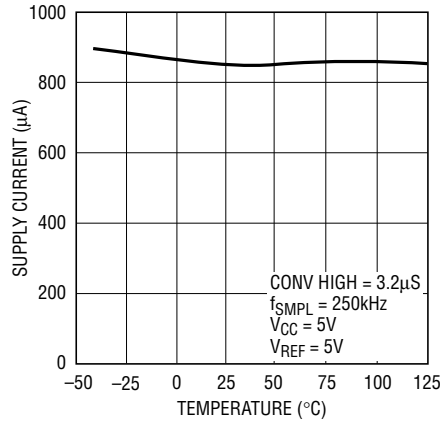
# TYPICAL PERFORMANCE CHARACTERISTICS

### Supply Current vs Sampling Frequency



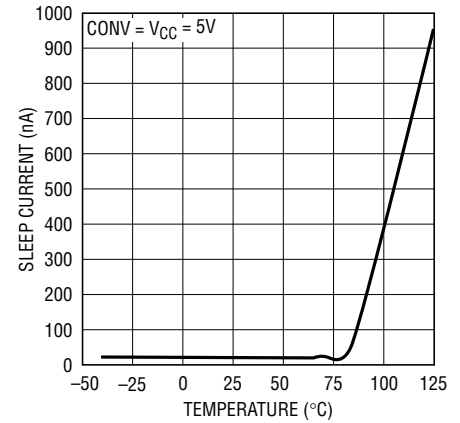
1860/61 G01

### Supply Current vs Temperature



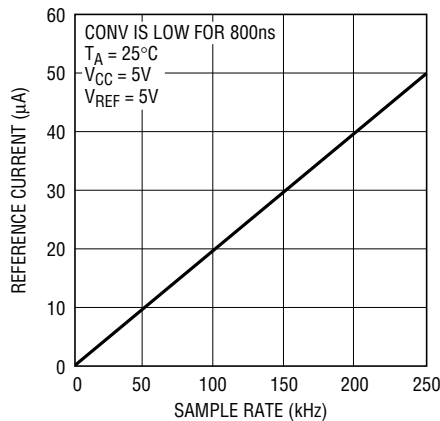
1860/61 G02

### Sleep Current vs Temperature



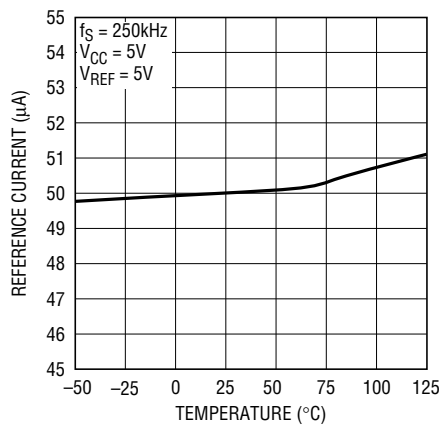
1860/61 G03

### Reference Current vs Sample Rate



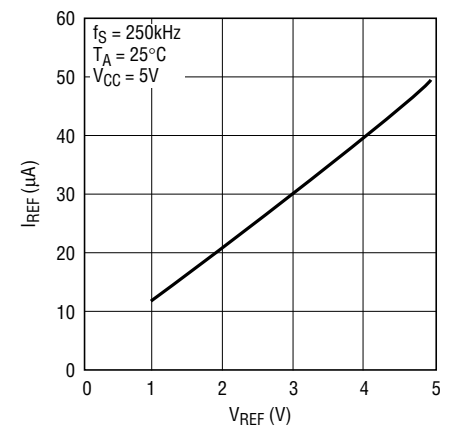
1860/61 G04

### Reference Current vs Temperature



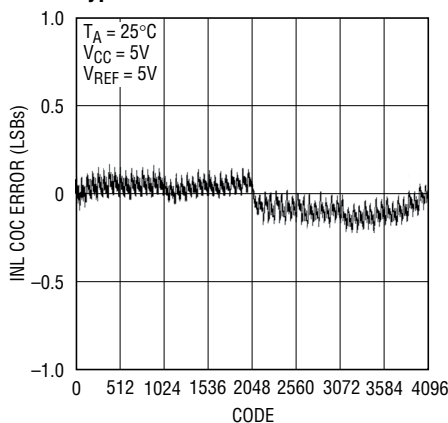
1860/61 G05

### Reference Current vs Reference Voltage



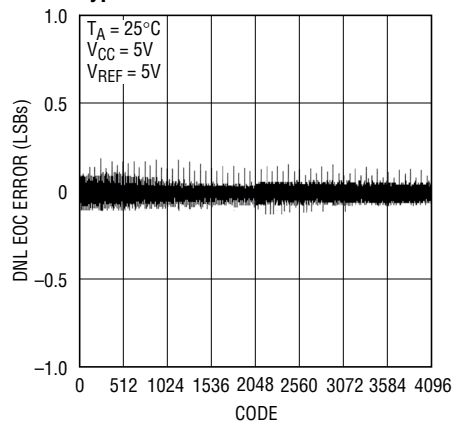
1860/61 G06

### Typical INL Curve



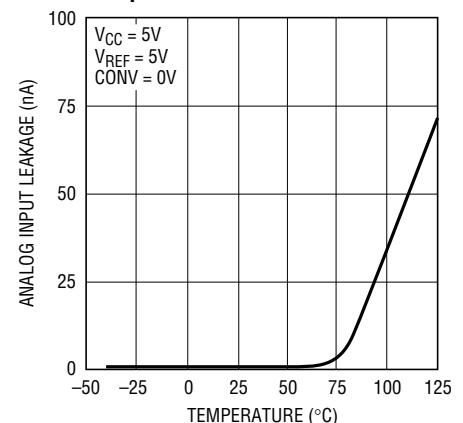
1860/61 G07

### Typical DNL Curve



1860/61 G07

### Analog Input Leakage vs Temperature

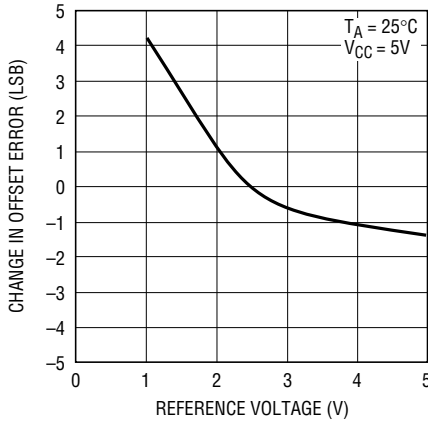


1860/61 G09

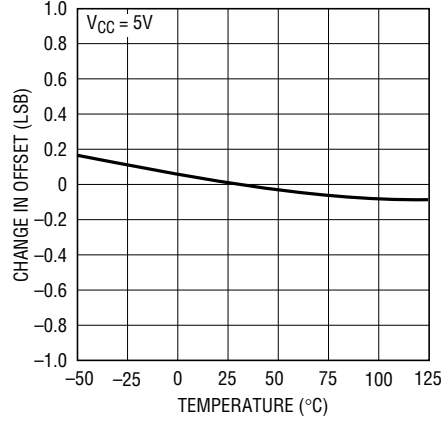
18601fb

## TYPICAL PERFORMANCE CHARACTERISTICS

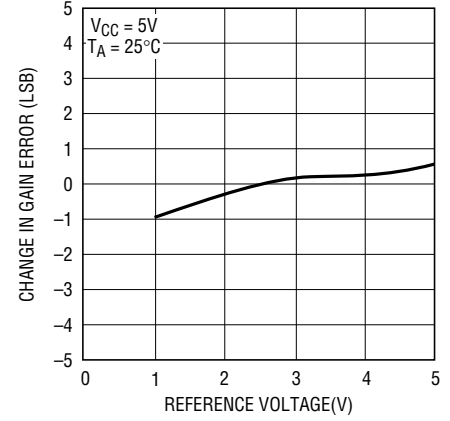
**Change in Offset Error vs Reference Voltage**



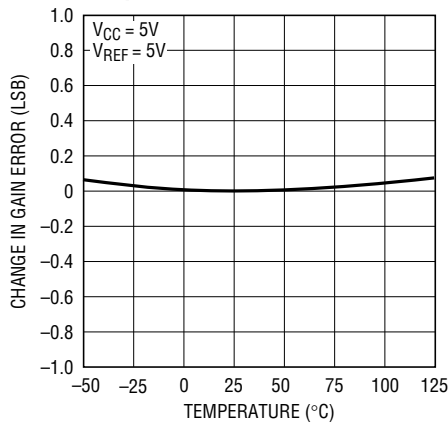
**Change in Offset vs Temperature**



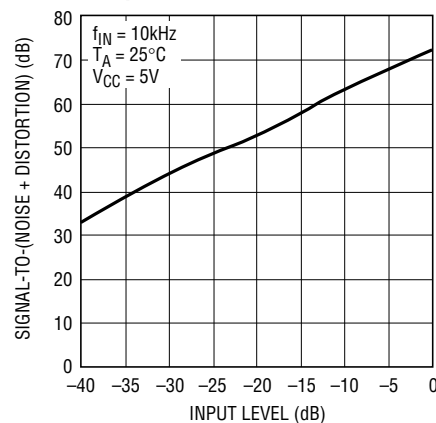
**Change in Gain Error vs Reference Voltage**



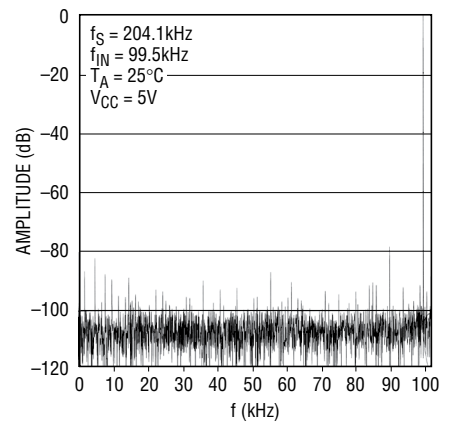
**Change in Gain Error vs Temperature**



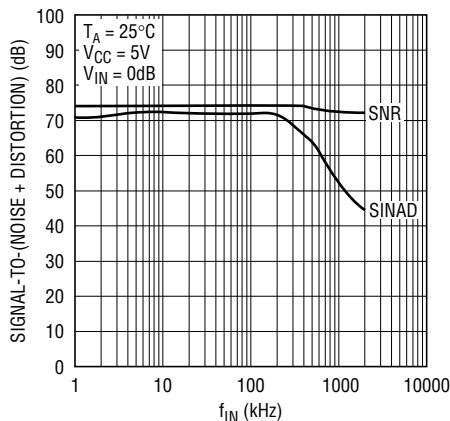
**Signal-to-(Noise + Distortion) vs Input Level**



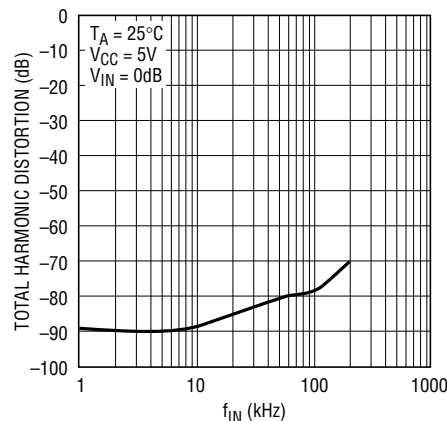
**4096 Point FFT**



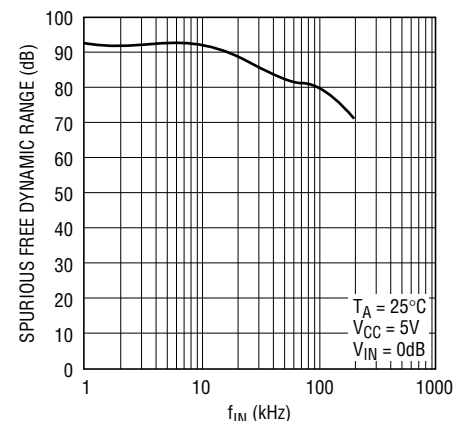
**Signal-to-(Noise + Distortion) vs f<sub>IN</sub>**



**Total Harmonic Distortion vs f<sub>IN</sub>**



**Spurious Free Dynamic Range vs f<sub>IN</sub>**



## PIN FUNCTIONS

### LTC1860

**V<sub>REF</sub> (Pin 1):** Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

**IN<sup>+</sup>, IN<sup>-</sup> (Pins 2, 3):** Analog Inputs. These inputs must be free of noise with respect to GND.

**GND (Pin 4):** Analog Ground. GND should be tied directly to an analog ground plane.

**CONV (Pin 5):** Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

**SDO (Pin 6):** Digital Data Output. The A/D conversion result is shifted out of this pin.

**SCK (Pin 7):** Shift Clock Input. This clock synchronizes the serial data transfer.

**V<sub>CC</sub> (Pin 8):** Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

### LTC1861 (MSOP Package)

**CONV (Pin 1):** Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

**CH0, CH1 (Pins 2, 3):** Analog Inputs. These inputs must be free of noise with respect to AGND.

**AGND (Pin 4):** Analog Ground. AGND should be tied directly to an analog ground plane.

**DGND (Pin 5):** Digital Ground. DGND should be tied directly to an analog ground plane.

**SDI (Pin 6):** Digital Data Input. The A/D configuration word is shifted into this input.

**SDO (Pin 7):** Digital Data Output. The A/D conversion result is shifted out of this output.

**SCK (Pin 8):** Shift Clock Input. This clock synchronizes the serial data transfer.

**V<sub>CC</sub> (Pin 9):** Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

**V<sub>REF</sub> (Pin 10):** Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to AGND.

### LTC1861 (SO-8 Package)

**CONV (Pin 1):** Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

**CH0, CH1 (Pins 2, 3):** Analog Inputs. These inputs must be free of noise with respect to GND.

**GND (Pin 4):** Analog Ground. GND should be tied directly to an analog ground plane.

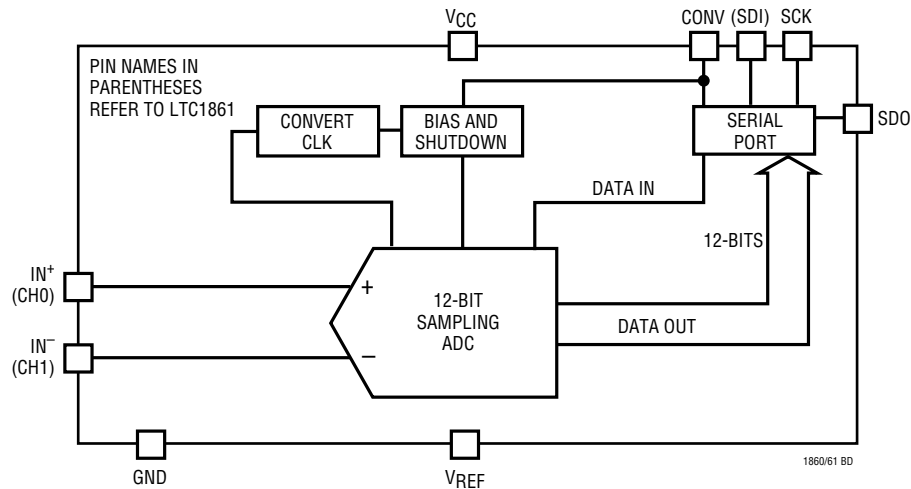
**SDI (Pin 5):** Digital Data Input. The A/D configuration word is shifted into this input.

**SDO (Pin 6):** Digital Data Output. The A/D conversion result is shifted out of this output.

**SCK (Pin 7):** Shift Clock Input. This clock synchronizes the serial data transfer.

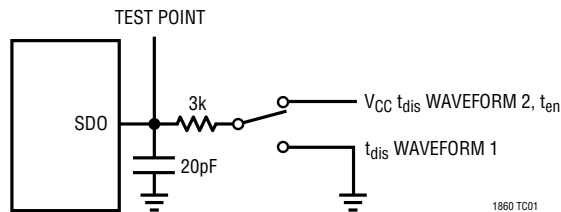
**V<sub>CC</sub> (Pin 8):** Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane. V<sub>REF</sub> is tied internally to this pin.

## FUNCTIONAL BLOCK DIAGRAM

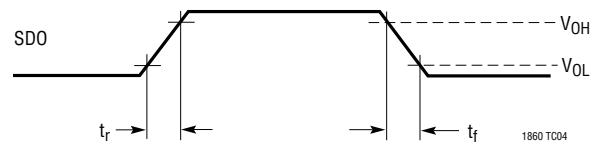


## TEST CIRCUITS

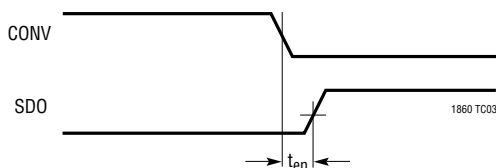
Load Circuit for  $t_{dDO}$ ,  $t_r$ ,  $t_f$ ,  $t_{dis}$  and  $t_{en}$



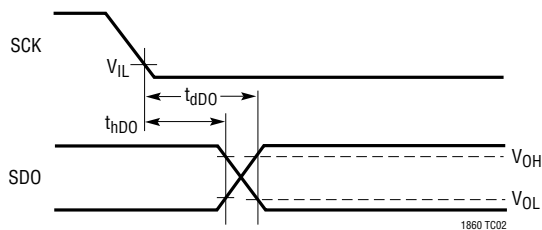
Voltage Waveforms for SDO Rise and Fall Times,  $t_r$ ,  $t_f$



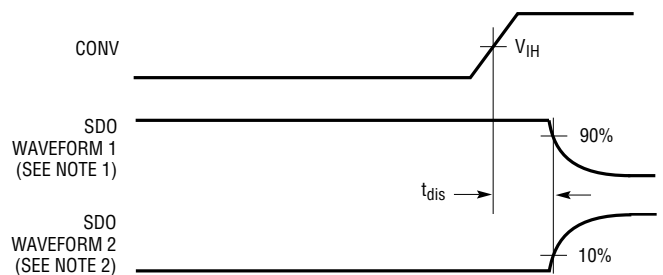
Voltage Waveforms for  $t_{en}$



Voltage Waveforms for SDO Delay Times,  $t_{dDO}$  and  $t_{hDO}$



Voltage Waveforms for  $t_{dis}$



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL  
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL

1860 TC05

## APPLICATIONS INFORMATION

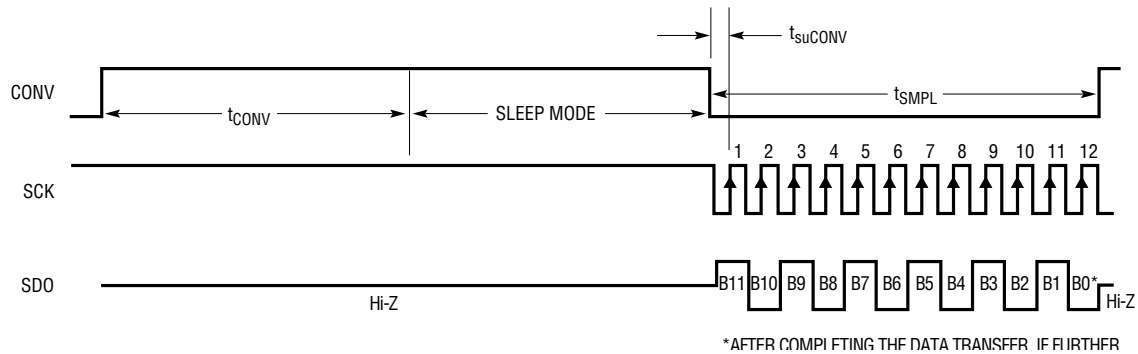


Figure 1. LTC1860 Operating Sequence

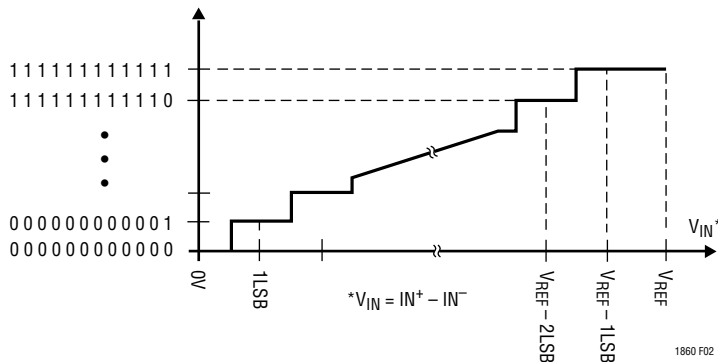


Figure 2. LTC1860 Transfer Curve

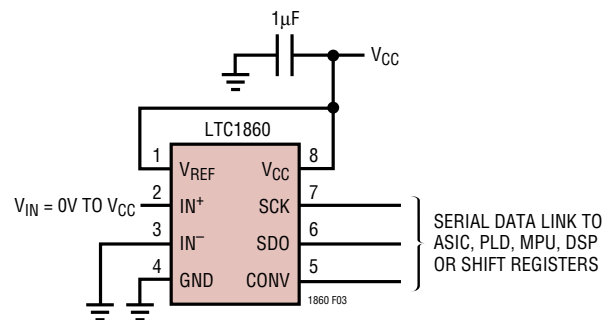


Figure 3. LTC1860 with Rail-to-Rail Input Span

## LTC1860 OPERATION

## Operating Sequence

The LTC1860 conversion cycle begins with the rising edge of CONV. After a period equal to  $t_{CONV}$ , the conversion is finished. If CONV is left high after this time, the LTC1860 goes into sleep mode drawing only leakage current. On the falling edge of CONV, the LTC1860 goes into sample mode and SDO is enabled. SCK synchronizes the data transfer with each bit being transmitted from SDO on the falling SCK edge. The receiving system should capture the data from SDO on the rising edge of SCK. After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 1.

## Analog Inputs

The LTC1860 has a unipolar differential analog input. The converter will measure the voltage between the “IN+” and “IN-” inputs. A zero code will occur when IN+ minus IN- equals zero. Full scale occurs when IN+ minus IN- equals  $V_{REF}$  minus 1LSB. See Figure 2. Both the “IN+” and “IN-” inputs are sampled at the same time, so common mode noise on the inputs is rejected by the ADC. If “IN-” is grounded and  $V_{REF}$  is tied to  $V_{CC}$ , a rail-to-rail input span will result on “IN+” as shown in Figure 3.

## Reference Input

The voltage on the reference input of the LTC1860 (and the LTC1861 MSOP package) defines the full-scale range of the A/D converter. These ADCs can operate with reference voltages from  $V_{CC}$  to 1V.

APPLICATIONS INFORMATION

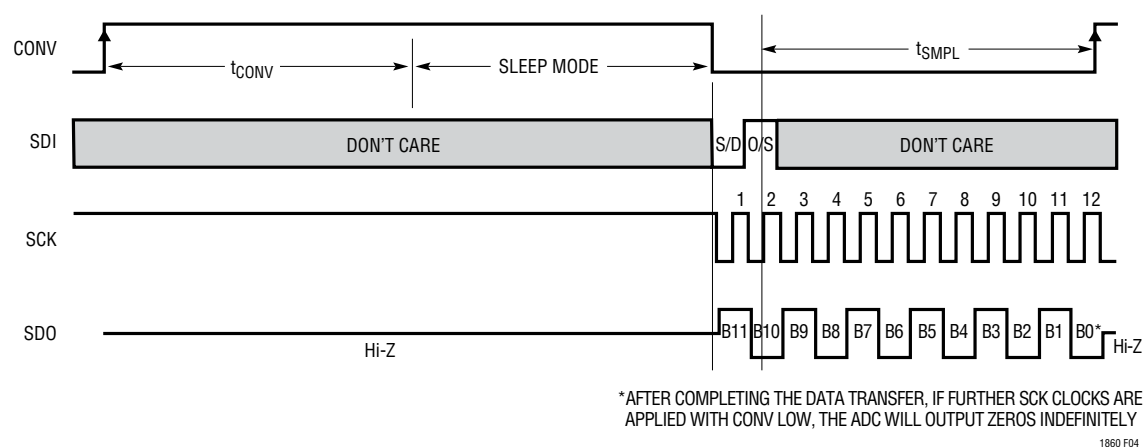


Figure 4. LTC1861 Operating Sequence

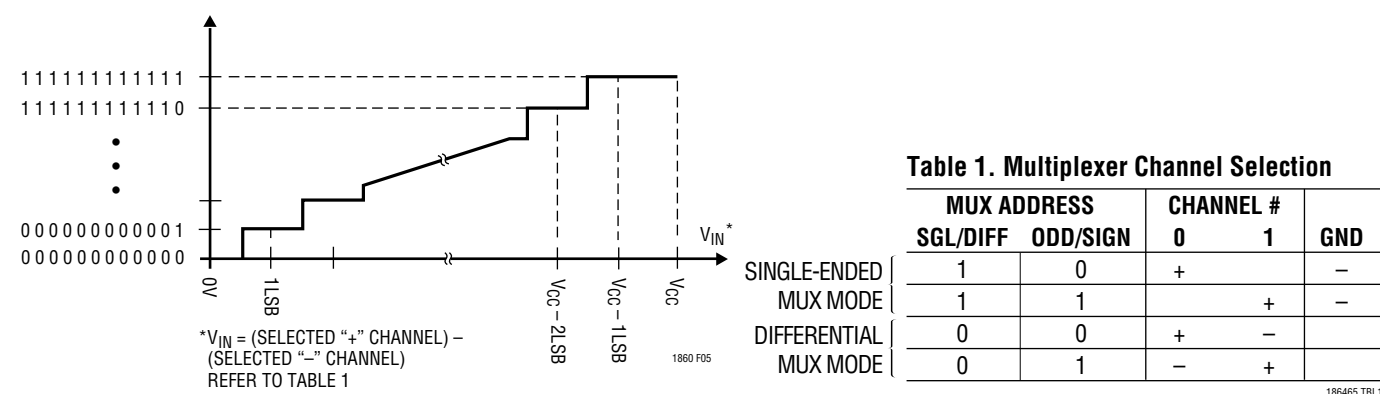


Figure 5. LTC1861 Transfer Curve

LTC1861 OPERATION

Operating Sequence

The LTC1861 conversion cycle begins with the rising edge of CONV. After a period equal to  $t_{CONV}$ , the conversion is finished. If CONV is left high after this time, the LTC1861 goes into sleep mode. The LTC1861's 2-bit data word is clocked into the SDI input on the rising edge of SCK after CONV goes low. Additional inputs on the SDI pin are then ignored until the next CONV cycle. The shift clock (SCK) synchronizes the data transfer with each bit being transmitted on the falling SCK edge and captured on the rising SCK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex). After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 4.

Analog Inputs

The two bits of the input word (SDI) assign the MUX configuration for the next requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "–" signs in the selected row of the following table. In single-ended mode, all input channels are measured with respect to GND (or AGND). A zero code will occur when the "+" input minus the "–" input equals zero. Full scale occurs when the "+" input minus the "–" input equals  $V_{REF}$  minus 1LSB. See Figure 5. Both the "+" and "–" inputs are sampled at the same time so common mode noise is rejected. The input span in the SO-8 package is fixed at  $V_{REF} = V_{CC}$ . If the "–" input in differential mode is grounded, a rail-to-rail input span will result on the "+" input.

## APPLICATIONS INFORMATION

### Reference Input

The reference input of the LTC1861 SO-8 package is internally tied to  $V_{CC}$ . The span of the A/D converter is therefore equal to  $V_{CC}$ . The voltage on the reference input of the LTC1861 MSOP package defines the span of the A/D converter. The LTC1861 MSOP package can operate with reference voltages from 1V to  $V_{CC}$ .

### GENERAL ANALOG CONSIDERATIONS

#### Grounding

The LTC1860/LTC1861 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance, use a printed circuit board. The ground pins (AGND and DGND for the LTC1861 MSOP package and GND for the LTC1860 and LTC1861 SO-8 package) should be tied directly to the analog ground plane with minimum lead length.

### Bypassing

For good performance, the  $V_{CC}$  and  $V_{REF}$  pins must be free of noise and ripple. Any changes in the  $V_{CC}/V_{REF}$  voltage with respect to ground during the conversion cycle can induce errors or noise in the output code. Bypass the  $V_{CC}$  and  $V_{REF}$  pins directly to the analog ground plane with a minimum of 1 $\mu$ F tantalum. Keep the bypass capacitor leads as short as possible.

### Analog Inputs

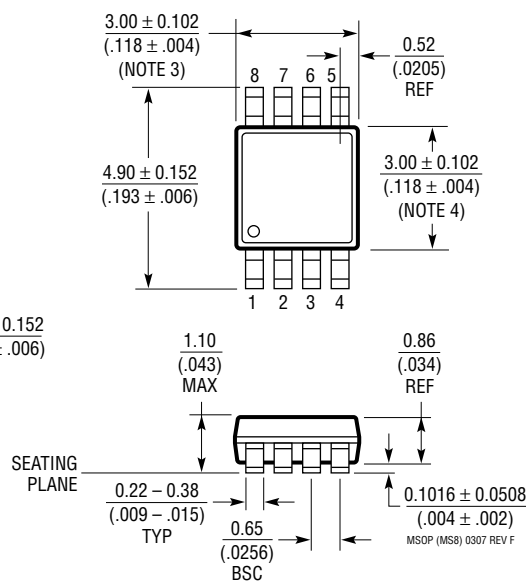
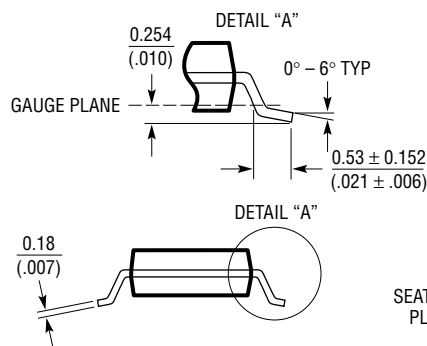
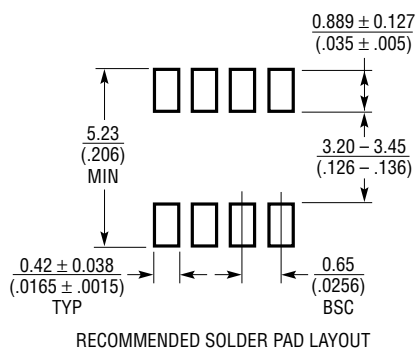
Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1860/LTC1861 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem if source resistances are less than 200 $\Omega$  or high speed op amps are used (e.g., the LT<sup>®</sup>1211, LT1469, LT1807, LT1810, LT1630, LT1226 or LT1215). But if large source resistances are used, or if slow settling op amps drive the inputs, take care to ensure the transients caused by the current spikes settle completely before the conversion begins.

## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC1860#packaging> for the most recent package drawings.

### MS8 Package 8-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1660 Rev F)



#### NOTE:

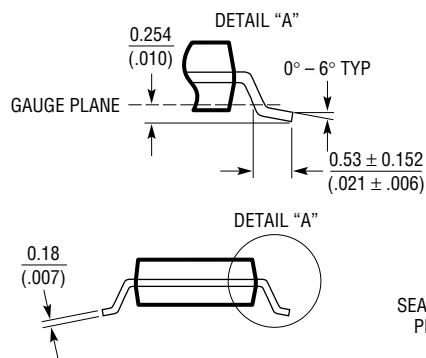
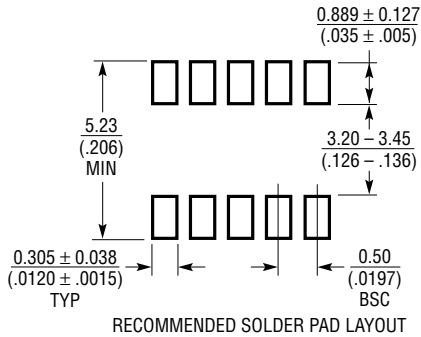
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.  
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.  
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC1861#packaging> for the most recent package drawings.

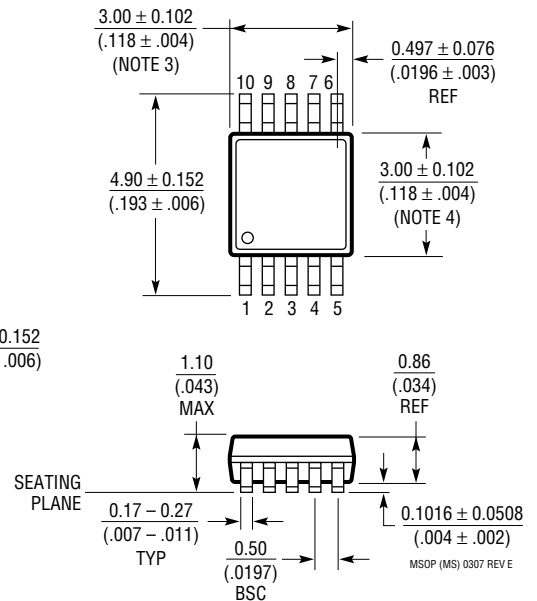
### MS Package 10-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1661 Rev E)



#### NOTE:

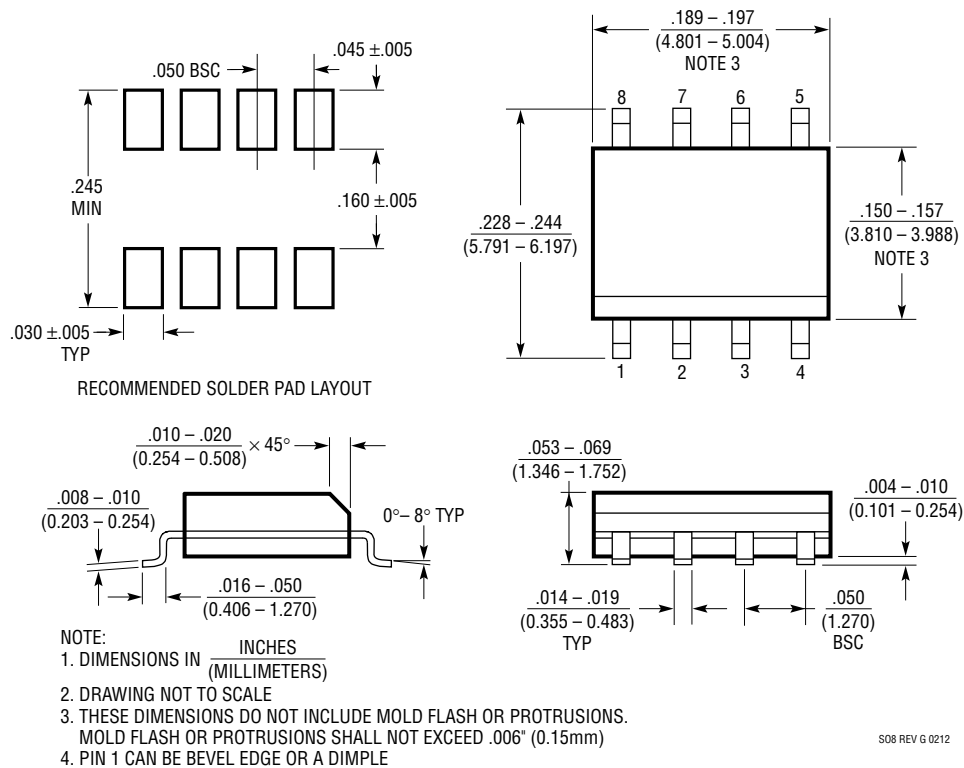
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.  
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED  $0.152\text{mm}$  ( $.006$ ) PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.  
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED  $0.152\text{mm}$  ( $.006$ ) PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE  $0.102\text{mm}$  ( $.004$ ) MAX



## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC1860#packaging> for the most recent package drawings.

### S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610 Rev G)

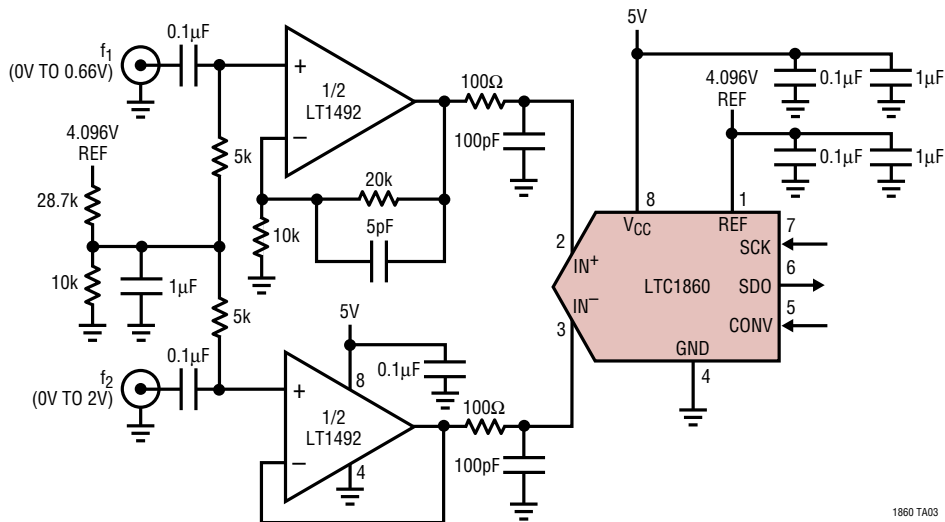


**REVISION HISTORY** (Revision history begins at Rev B)

| REV | DATE  | DESCRIPTION                 | PAGE NUMBER |
|-----|-------|-----------------------------|-------------|
| B   | 05/16 | Corrected Order Information | 3           |

TYPICAL APPLICATION

Sample Two Channels Simultaneously with a Single Input ADC



1860 TA03

RELATED PARTS

| PART NUMBER                     | SAMPLE RATE                           | POWER DISSIPATION | DESCRIPTION                                                      |
|---------------------------------|---------------------------------------|-------------------|------------------------------------------------------------------|
| <b>12-Bit Serial I/O ADCs</b>   |                                       |                   |                                                                  |
| <a href="#">LTC1286/LTC1298</a> | 12.5ksps/11.1ksps                     | 1.3mW/1.7mW       | 1-Channel with Ref. Input (LTC1286), 2-Channel (LTC1298), 5V     |
| <a href="#">LTC1400</a>         | 400ksps                               | 75mW              | 1-Channel, Bipolar or Unipolar Operation, Internal Reference, 5V |
| <a href="#">LTC1401</a>         | 200ksps                               | 15mW              | SO-8 with Internal Reference, 3V                                 |
| <a href="#">LTC1402</a>         | 2.2Msps                               | 90mW              | Serial I/O, Bipolar or Unipolar, Internal Reference              |
| <a href="#">LTC1404</a>         | 600ksps                               | 25mW              | SO-8 with Internal Reference, Bipolar or Unipolar, 5V            |
| <b>14-Bit Serial I/O ADCs</b>   |                                       |                   |                                                                  |
| <a href="#">LTC1417</a>         | 400ksps                               | 20mW              | 16-Pin SSOP, Unipolar or Bipolar, Reference, 5V                  |
| <a href="#">LTC1418</a>         | 200ksps                               | 15mW              | Serial/Parallel I/O, Internal Reference, 5V                      |
| <b>16-Bit Serial I/O ADCs</b>   |                                       |                   |                                                                  |
| <a href="#">LTC1609</a>         | 200ksps                               | 65mW              | Configurable Bipolar or Unipolar Input Ranges, 5V                |
| <a href="#">LTC1864/LTC1865</a> | 250ksps                               | 4.25mW            | SO-8, MS8, 1-Channel, 5V/SO-8, MS10, 2-Channel, 5V               |
| <b>References</b>               |                                       |                   |                                                                  |
| <a href="#">LT1460</a>          | Micropower Precision Series Reference |                   | Bandgap, 130µA Supply Current, 10ppm/°C, Available in SOT-23     |
| <a href="#">LT1790</a>          | Micropower Low Dropout Reference      |                   | 60µA Supply Current, 10ppm/°C, SOT-23                            |