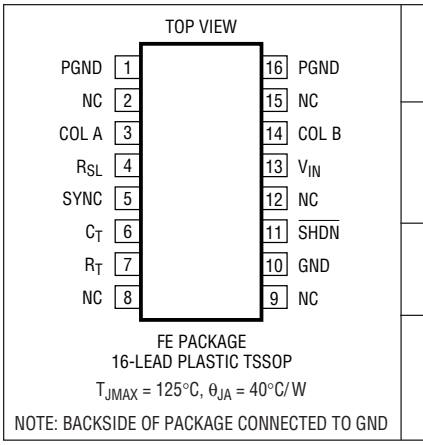
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage 20V
COL A, COL B Voltage 35V
SHDN, SYNC Voltage 20V
Maximum Junction Temperature ..... 150°C
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
16-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W

NOTE: BACKSIDE OF PACKAGE CONNECTED TO GND

ORDER PART NUMBER
LT3439EFE
FE PART MARKING
3439EFE

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V; R_T = 16.9k; C_T = 680pF; R_{SL} = 16.9k; COL A, COL B, SHDN pins open, unless otherwise noted.

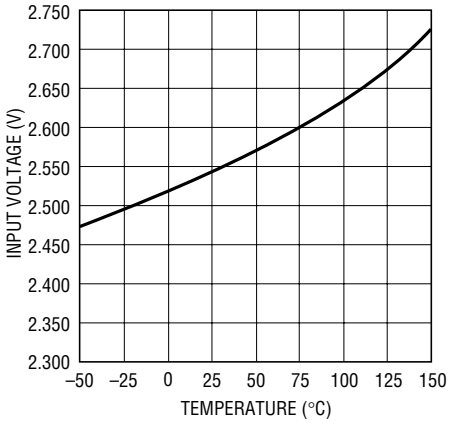
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply and Shutdown							
V_{IN}	Operating Range		●	2.8		17.5	V
$V_{IN(MIN)}$	Minimum Input Voltage				2.55	2.7	V
I_{VIN}	Supply Current	2.8V ≤ V_{IN} ≤ 17.5V	●		12		mA
$I_{VIN(\overline{SHDN})}$	Supply Current in Shutdown Mode	2.8V ≤ V_{IN} ≤ 17.5V, $V_{\overline{SHDN}}$ = 0V			5	20	µA
$V_{\overline{SHDN}(ON)}$	Shutdown Turn-On Threshold	2.8V ≤ V_{IN} ≤ 17.5V	●		1.3	1.4	V
$V_{\overline{SHDN}(OFF)}$	Shutdown Turn-Off Threshold	2.8V ≤ V_{IN} ≤ 17.5V	●	1.20	1.26		V
$I_{\overline{SHDN}}$	Shutdown Pin Current Hysteresis	2.8V ≤ V_{IN} ≤ 17.5V, $V_{\overline{SHDN}}$ = 1.4V	●	10	20	40	µA
Oscillator and Sync							
f_{MAX}	Oscillator Frequency		●			250	kHz
f_{SYNC}	Synchronization Frequency Range		●			300	kHz
V_{SYNC}	SYNC Pin Threshold		●		1.4	2.25	V
R_{SYNC}	SYNC Pin Input Resistance				40		kΩ
Output Switches (COL A, COL B)							
DC	Switch Duty Cycle		●		50		%
BV	Output Switch Breakdown Voltage	2.8V ≤ V_{IN} ≤ 17.5V	●	35	50		V
R_{ON}	Output Switch On Resistance	I_{COLA} or I_{COLB} = 0.75A	●		0.5	0.95	Ω
$I_{LIM(MAX)}$	Switch Current Limit			1.2	1.4	1.65	A
Slew Control							
V_{SLEWR}	Output Voltage Slew Rising Edge	Collector A or B			17		V/µs
V_{SLEWF}	Output Voltage Slew Falling Edge	Collector A or B			17		V/µs
I_{SLEWR}	Output Current Slew Rising Edge	Collector A or B			5		A/µs
I_{SLEWF}	Output Current Slew Falling Edge	Collector A or B			5		A/µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

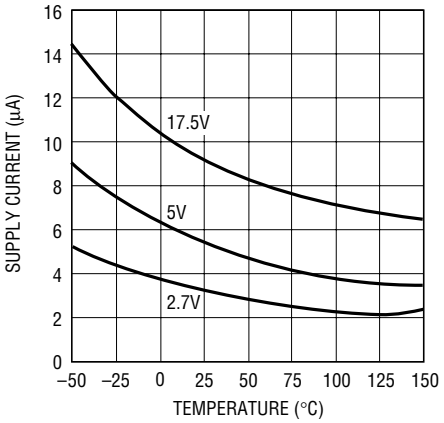
Note 2: The LT3439E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls.

TYPICAL PERFORMANCE CHARACTERISTICS

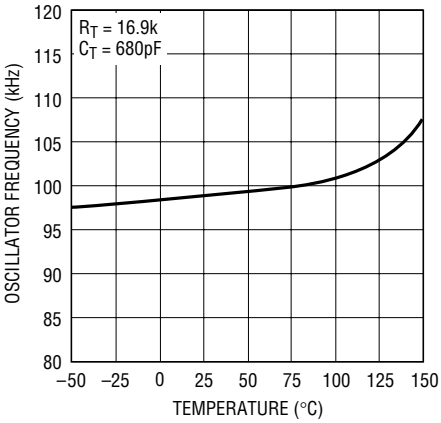
Minimum Input Voltage vs Temperature



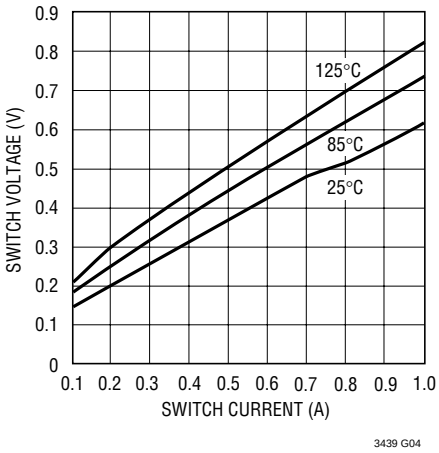
Supply Current in Shutdown Mode vs Temperature



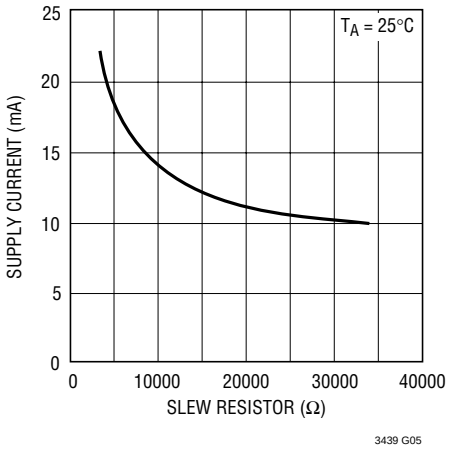
Oscillator Frequency vs Temperature



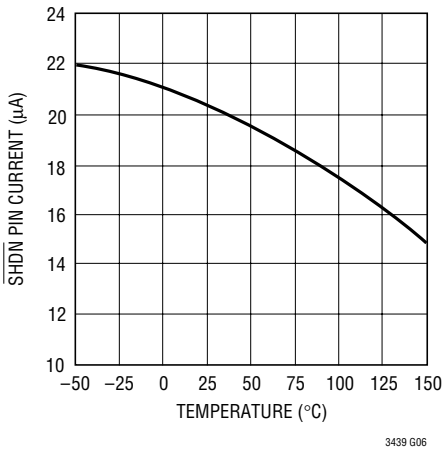
Switch Voltage Drop vs Switch Current



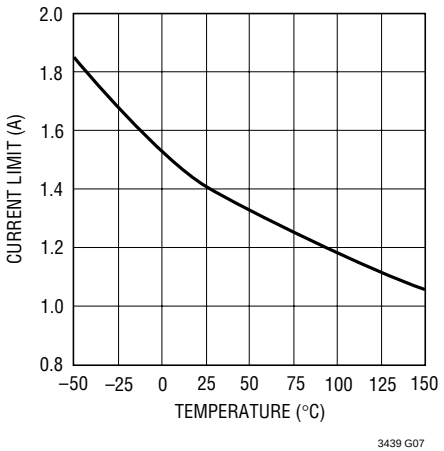
Supply Current vs Slew Resistor



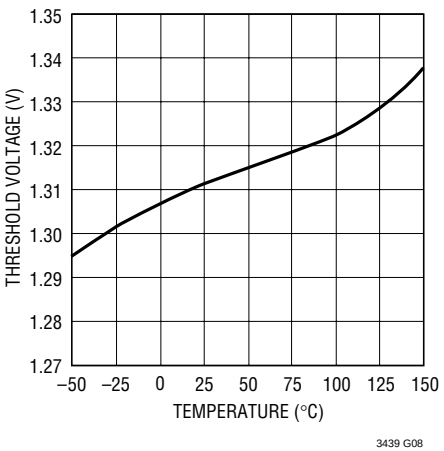
$\overline{SHDN}$ Pin Hysteresis Current vs Temperature



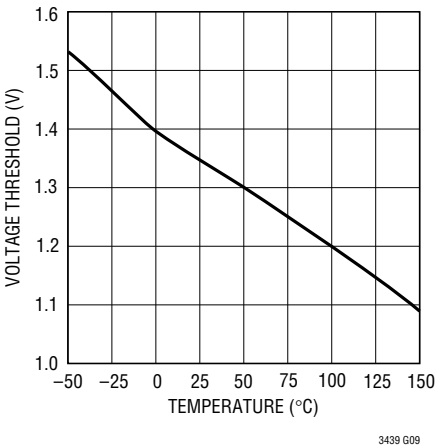
Current Limit vs Temperature



$\overline{SHDN}$ Pin Voltage Threshold vs Temperature



SYNC Pin Voltage Threshold vs Temperature



PIN FUNCTIONS

PGND (Pins 1, 16): Power ground is connected to the emitter of the power switches via an internal sense resistor. It has large currents flowing through it and should be connected to a good quality ground plane.

COL A, COL B (Pins 3, 14): These are the open collectors of the output power switches. They are connected to the outer terminals of the center tap transformer. Large currents flow into these pins so external traces should be kept as short as possible.

R_{SL} (Pin 4): The slew control resistor sets the maximum current and voltage slew rate for the collectors A and B. The minimum resistor value is 3.4k for fast slewing and the maximum resistor is 34k for slow slewing. For more details, see "Slew Rate Setting" in the Applications Information section of this data sheet.

SYNC (Pin 5): The SYNC pin can be used to synchronize the oscillator to an external clock. R_T and C_T should be set such that the oscillator clock frequency is approximately 10% below the external clock frequency. If unused, this pin should be tied to GND. For more details, see "Oscillator Sync" in the Applications Information section of this data sheet.

C_T (Pin 6): The oscillator capacitor pin is used in conjunction with the R_T pin to set the oscillator frequency. For R_T = 16.9k, C_T can be calculated as follows:

$$C_T(nF) = 70/f_{OSC}(kHz)$$

The transformer operating frequency and the frequency of each output is one half of the frequency of the oscillator.

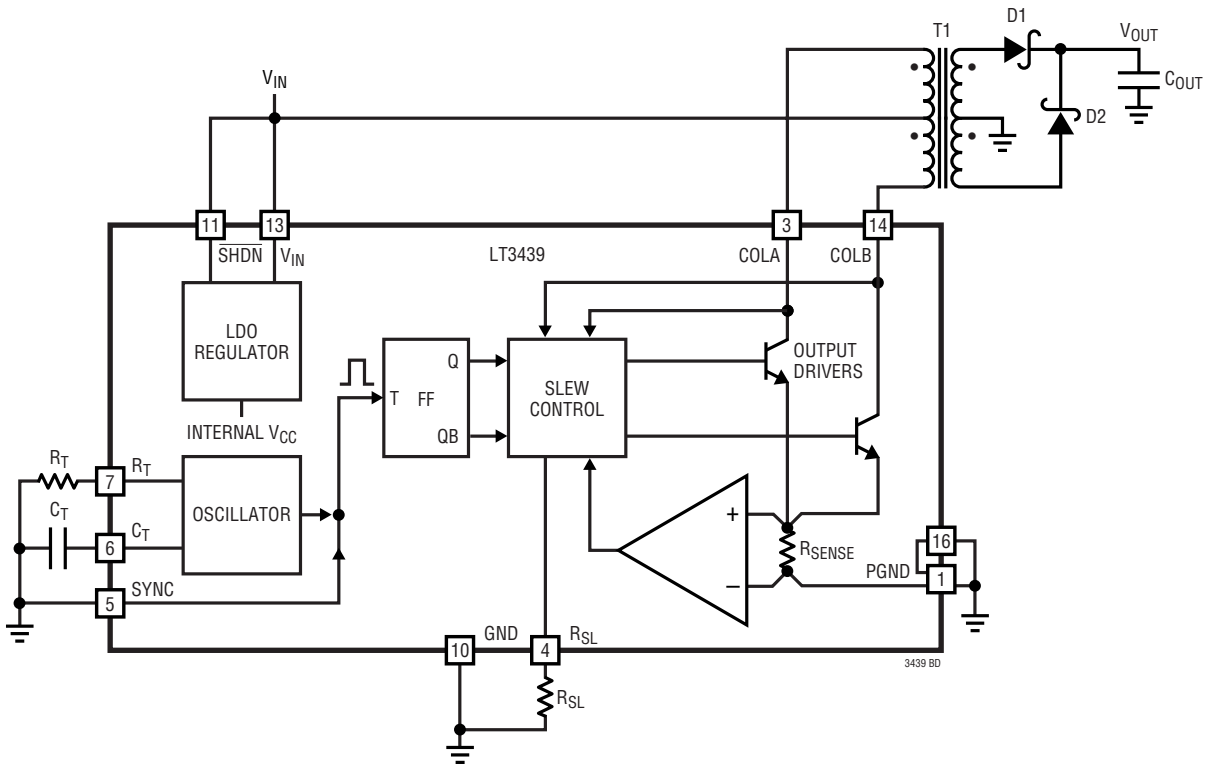
R_T (Pin 7): The oscillator resistor pin is used to set the charge and discharge currents of the oscillator capacitor. The nominal value is 16.9k. The resistance can be adjusted between ±25% of nominal for better frequency accuracy.

$\overline{SHDN}$ (Pin 11): The $\overline{SHDN}$ pin is used to shut down the part. Grounding this pin will disable all internal circuitry. Increasing the $\overline{SHDN}$ voltage above the turn-on threshold will enable the part. At the turn-on threshold, approximately 20µA of current is sourced out of the pin. This current, in conjunction with the Thevenin resistance on the pin, sets up the hysteresis. This allows the user to set the undervoltage lockout (UVLO) of the supply and the amount of start-up hysteresis with a resistor divider off of the input voltage. Above 2.1V on the $\overline{SHDN}$ pin, the hysteresis current is reduced to zero. If unused the pin can be left floating or tied directly to the input voltage.

GND (Pin 10): Signal Ground. The oscillator, slew control circuitry and the internal regulator are referred to signal ground. Internally, signal ground is tied to substrate and the exposed backside of the device. Connect the GND pin to the ground plane and keep the connection free of large currents.

V_{IN} (Pin 13): This is the supply pin for the part and should be bypassed with a 4.7µF or greater, low ESR capacitor. When $V_{IN} \leq 2.5V$, an internal undervoltage lockout circuit will trip and turn both outputs off.

BLOCK DIAGRAM



OPERATION

Push-Pull Topology

The push-pull DC transformer topology is a very straightforward switching power supply. The two switches are turned on out of phase at 50% duty cycles. During the switch on time, V_{IN} is applied across the primary side of the transformer. The voltage on the secondary side of the transformer is simply V_{IN} times the turns ratio. The diodes rectify the secondary voltage and generate the output voltage. The output capacitor is for hold-up and filtering.

Some of the topology's advantages are: 1) Stepping up or down the input voltage can easily be done by setting the turns ratio. 2) The transformer provides isolation between the input and output. 3) Each switch cycle applies V_{IN} across the transformer in opposite polarities. Therefore, the transformer core never saturates and a separate reset circuit is not necessary.

The push-pull topology is not without its concerns. An imbalance in the two sides of the transformer can eventually cause the transformer to saturate. Also, during the turn-off of the switches, the leakage inductance causes a large undesirable voltage spike. The LT3439 slew control feature addresses both of these concerns and is discussed in the Applications Information section.

Slew Control

Control of voltage and current slew rate is maintained via two feedback loops. One loop controls the output switch collector voltage dV/dt and the other loop controls the emitter current dI/dt. Output slew control is achieved by comparing the two currents generated by these slewing events to a current set by the external resistor R_{SL}. The two control loops work together to provide a smooth transition from voltage slew control to current slew control.

Internal Regulator

Most of the control circuitry operates from an internal 2.4V low dropout regulator that is powered from V_{IN}. V_{IN} can

OPERATION

vary from 2.8V to 17.5V with very little change in device performance. When the part is in shutdown mode, the internal regulator is turned off, drawing less than 20μA of current from V_{IN}.

Overcurrent Protection

A linearly controlled current limit circuit is provided to protect the circuit from excessive currents and to facilitate start-up into a highly capacitive load. Upon reaching current limit, the switching cycle is not terminated, instead the base drive to the output transistor is regulated to maintain the maximum current over the entire switch cycle. Very high power dissipation in the switches occurs during this mode of operation. If the current limit is enabled for a long enough period of time, over temperature protection shutdown will be enabled to protect the device.

Overtemperature Protection

When the IC has exceeded the maximum temperature the part will trigger the overtemperature protection circuit where both output drivers are turned off.

Undervoltage Lockout Protection

When V_{IN} is below 2.55V the part will go into undervoltage lockout mode where both output drivers are turned off.

No Load Operation

The operation of the supply is stable all the way down to zero load and a preload is not required.

APPLICATIONS INFORMATION

Reducing EMI from switching power supplies has traditionally invoked fear in designers. Many switchers are designed solely on efficiency and, as such, produce waveforms filled with high frequency harmonics that propagate through the rest of the supply.

The LT3439 provides control of two of the primary variables for controlling EMI while switching inductive loads: switch voltage slew rate and switch current slew rate. The use of this part will reduce noise and EMI over conventional switch mode controllers. Because these variables are under control, a supply built with this part will exhibit far less tendency to create EMI and less chance of running into problems during production.

It is beyond the scope of this data sheet to get into EMI fundamentals. AN70, "A Monolithic Switching Regulator with 100μV Output Noise" contains much information concerning noise in switching regulators and should be consulted.

Oscillator Frequency

The internal oscillator generates the switching frequency that determines the fundamental positioning of the harmonics. Using quality external components is important to ensure oscillator frequency stability. A current defined by external resistor R_T charges and discharges the capacitor C_T creating a saw tooth waveform where the outputs' states change at the peak. The frequency of each output is one half of the frequency of the oscillator.

By having both components external, the user has greater flexibility in setting the frequency and the frequency is less susceptible to any temperature variations in the device.

The external capacitance C_T is chosen by:

$$C_T(nF) = 1183/[f_{OSC}(kHz) \bullet R_T(k\Omega)]$$

where f_{OSC} is the desired oscillator frequency.

For R_T equal to 16.9k, this simplifies to:

$$C_T(nF) = 70/f_{OSC}(kHz)$$

e.g., C_T = 1nF for f_{OSC} = 70kHz

Nominally, R_T should be set to 16.9k.

Low tolerance and low temperature coefficient components are recommended.

APPLICATIONS INFORMATION

Oscillator SYNC

The oscillator can be synchronized to an external clock. Set the RC timing components for an oscillator frequency 10% below the desired sync frequency.

It is recommended that the SYNC pin be driven with a square wave that has an amplitude greater than 2V, a pulse width greater than 1µs and a rise time less than 500ns. The rising edge of the sync waveform triggers the change in the state of the outputs.

Slew Rate Setting

Setting the LT3439 maximum slew rate is easy. The external resistor to ground on the R_{SL} pin sets the maximum slew rate. To determine the maximum slew rate connect a 50k resistor pot with a 3.4k series resistance to the R_{SL} pin. Start at the lowest resistance setting and increase the pot until the noise level meets your requirements. Note that slower slewing waveforms will lower the power supply efficiency. Consult Linear Technology Application Note 70, "A Monolithic Switching Regulator with 100µV Output Noise" for recommended noise measurement techniques.

Shutdown

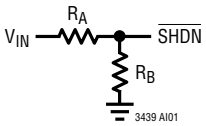
The $\overline{SHDN}$ pin is used to shut down the part. Grounding this pin will disable all internal circuitry.

Increasing the $\overline{SHDN}$ voltage above the turn-on threshold, approximately 1.3V, will enable the part. At the turn-on threshold approximately 20µA of current is sourced out of the pin. This current, in conjunction with the Thevenin resistance on the pin, sets up the amount of hysteresis. This allows the user to set the turn-on voltage of the supply and the start-up hysteresis with a resistor divider. The hysteresis can be used to prevent the part from shutting down due to input voltage sag from an initial high current draw. When the $\overline{SHDN}$ pin is greater than 2.1V, the hysteresis current is reduced to zero.

In addition to the current hysteresis, there is also approximately 35mV of voltage hysteresis on the $\overline{SHDN}$ pin.

If a resistor divider is used to set the turn on threshold the resistors are determined by the following equations:

$$V_{ON} = \left(\frac{R_A + R_B}{R_B}\right) \bullet V_{\overline{SHDN}}$$



V_{ON} is the input voltage at which the supply will turn on and $V_{\overline{SHDN}}$ is the $\overline{SHDN}$ pin turn-on threshold, typically 1.3V.

$$V_{HYST} = R_A \bullet \left(\frac{\Delta V_{\overline{SHDN}}}{R_A || R_B} + I_{\overline{SHDN}}\right)$$

V_{HYST} is the actual hysteresis voltage seen at the input voltage. I_{SHDN} is the current hysteresis sourced by the IC at the turn-on threshold, typically 20µA. $\Delta V_{\overline{SHDN}}$ is the voltage hysteresis seen at the $\overline{SHDN}$ pin at the turn-on threshold, typically 35mV.

The resistors can be calculated as follows:

$$R_A = \frac{\left(V_{HYST} \bullet V_{\overline{SHDN}} - V_{ON} \bullet \Delta V_{\overline{SHDN}}\right)}{I_{\overline{SHDN}} \bullet V_{\overline{SHDN}}}$$

$$R_B = \frac{\left(V_{HYST} \bullet V_{\overline{SHDN}} - V_{ON} \bullet \Delta V_{\overline{SHDN}}\right)}{I_{\overline{SHDN}} \bullet \left(V_{ON} - V_{\overline{SHDN}}\right)}$$

For example if the turn-on voltage was to be set at 5V with 0.5V of hysteresis:

$$R_A = \frac{\left(0.5V \bullet 1.3V - 5V \bullet 35mV\right)}{20\mu A \bullet 1.3V} = 18.27k$$

$$R_B = \frac{\left(0.5V \bullet 1.3V - 5V \bullet 35mV\right)}{20\mu A \bullet \left(5V - 1.3V\right)} = 6.42k$$

The nearest 1% values would be 18.2k and 6.49k.

A resistor in series with the $\overline{SHDN}$ pin could further change hysteresis without changing the turn-on voltage.

Thermal Considerations

Decreasing the noise by lowering the slew rate of the output switches does not come for free. Lower slew rates

APPLICATIONS INFORMATION

mean greater switching losses in the internal output switches. However, efficiency is only modestly reduced for a large improvement in EMI.

Care should be taken to ensure that the worst-case input voltage and load current conditions do not cause an excessive die temperature. The total power dissipation of the IC is dominated by three loss terms, regulator losses, saturation losses and switching losses. The following formulas may be used to approximate these losses:

1. Regulator Dissipation:

$$P_{VIN} = V_{IN}\left(12mA + \frac{I}{60}\right)$$

where I is the average switch current.

2. Switch Saturation Dissipation:

$$P_{VSAT} = (V_{SAT})(I)$$

3. Switch Switching Dissipation:

$$P_{SW} = 10^{-6} \bullet V_{IN} \bullet I \bullet f_{OSC}\left(\frac{I}{\left(-2.3 \bullet 10^{-4} \bullet R_{SL} + 10.8\right)} + \frac{V}{\left(-1.7 \bullet 10^{-3} \bullet R_{SL} + 65.8\right)}\right)$$

Total IC power dissipation (P_D) is the sum of these three terms. Die junction temperature can be computed as follows:

$$T_J = T_{AMB} + (P_D)(\theta_{JA})$$

where T_{AMB} is the ambient temperature, T_J is the junction temperature and θ_{JA} is the thermal resistance from junction to ambient.

The LT3439 comes in the 16-pin TSSOP with exposed backside package that has a very low junction-to-ambient thermal resistance (θ_{JA}) of approximately 40°C/W.

Transformer Design

Table 1 lists recommended center tapped transformers for a variety of input voltage, output voltage and power combinations.

Table 1

NOMINAL INPUT VOLTAGE	NOMINAL OUTPUT VOLTAGE	OUTPUT POWER	COILTRONICS PART NUMBER
5V	12V	1.5W	CTX02-13716-X1
5V	12V	3.0W	CTX02-13665-X1
5V	±15V	1.5W	CTX02-13713-X1
5V	±15V	3.0W	CTX02-13664-X1
5V	12V	1.5W	CTX02-13834-X3
5V	12V	10W	CTX02-13949-X1
12V	–12V	6W	CTX02-16076

These transformers will yield slightly high output voltages so that they can accommodate an LDO regulator on the output.

If your application is not listed, the LTC Applications group is available to assist in the choice and/or the design of the transformer.

In the design/selection of the transformer the following characteristics are critical and should be considered.

Turns Ratio

The turns ratio of the transformer determines the output voltage. The following equation can be used as a first pass to calculate the turns ratio:

$$\frac{N_S}{N_P} = \frac{V_{OUT} + V_F}{V_{IN} - V_{SW}}$$

where V_F is the forward voltage of the output diode and V_{SW} is the voltage drop across the internal switches (see Typical Performance curves).

Sufficient margin should be added to the turns ratio to account for voltage drops due to transformer winding resistances. Also, if using an LDO for regulating the output voltage, don't forget to take into account the voltage drop that should be added to V_{OUT}.

Magnetizing Current

The primary inductance of the transformer causes a ripple current that is independent of load current. The ripple current manifests itself in the output voltage through the parasitic resistances of the supply. Increasing the transformer magnetizing inductance can reduce the ripple

APPLICATIONS INFORMATION

current. This can be accomplished by adding more turns onto a given core or selecting a new core with a higher inductance per turn squared characteristic (A_L).

The following equation can be used to set the transformer primary inductance:

$$L_{PRI} = V_{IN} \frac{t_{ON}}{\Delta I}$$

t_{ON} can be calculated by $1/f_{OSC}$.

ΔI is somewhat arbitrary but a general rule of thumb is to set it between 10% to 30% of I_{PRI} where I_{PRI} is calculated as follows:

$$I_{PRI} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN}\ Eff}$$

Eff can be estimated at 70%.

Winding Resistance

Resistance in either the primary or secondary winding will reduce overall efficiency and degrade load regulation. If efficiency or load regulation is unsatisfactory, verify that the voltage drops in the transformer windings are not excessive.

Leakage Inductance

When the output switches turn off, the transformer leakage inductance causes a voltage spike on the output switch collector. The size of the voltage spike is proportional to the magnitude of the leakage inductance and to the square of the load current (energy stored in the leakage inductance). The voltage spike should be limited so that it does not exceed the voltage breakdown of the output switches. This can be accomplished by reducing the transformer's leakage inductance or by reducing the maximum slew rate. The voltage slew control will limit the voltage spike by dissipating the leakage energy in the power switches.

Transformer Imbalance

A common concern for the push-pull topology is transformer imbalance. If the volt/second products of each half of the switching cycle do not match, the transformer's flux level walks up the BH curve and the transformer goes into saturation. This is undesirable because the effective magnetizing inductance drops off and the magnetizing current increases rapidly. Fortunately, there are parasitics in the circuit that counteract the transformer saturation. When the transformer begins to saturate the magnetizing current increases in one half of the switching cycle and therefore, the IR drops increase thereby reducing the volt/second product of that half cycle. The transformer balance is maintained. Also, the losses in the transformer and the main switches have positive temperature coefficients eliminating the potential for thermal runaway. The LT3439 can compensate for small circuit imbalances, however care should be taken to balance both sides of the circuit including transformer design and PCB layout.

Transformer Design Example

The following is an example of the design of a DC transformer for a 5V to 5V at 500mA supply.

Supply specs: V_{IN} = 5V, V_{OUT} = 5V, I_{OUT} = 500mA, f_{OSC} = 100kHz

Assume: V_F = 0.5V (forward voltage of output diode)
Efficiency ≈ 70%

Calculate the primary switch current (I_{PRI}):

$$I_{PRI} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN}\ Eff} = \frac{5V \bullet 500mA}{5V \bullet 70\%} = 0.714A$$

The "Switch Voltage Drop vs Switch Current" Typical Performance curve gives a typical value of the switch voltage drop (V_{SW}) for a given switch current (I_{PRI}). In this example, $I_{PRI} \approx 0.7A$, therefore $V_{SW} \approx 0.5V$.

Next, calculate the turns ratio:

$$\frac{N_S}{N_P} = \frac{V_{OUT} + V_F}{V_{IN} - V_{SW}} = \frac{5V + 0.5V}{5V - 0.5V} = 1.22$$

Add 15% margin to account for winding resistance of the transformer:

$$\frac{N_S}{N_P} = 1.22 + 15\% = 1.41$$

APPLICATIONS INFORMATION

The primary inductance is then calculated:

$$L_{PRI} = V_{IN}\frac{\frac{1}{f_{OSC}}}{\Delta I_{PRI}} = 5\frac{\frac{1}{100kHz}}{0.107A} = 467\mu H$$

$$\Delta I = 15\% \text{ of } I_{PRI} = 0.15 \bullet 0.714A = 0.107A$$

Next, build a transformer with the calculated values of turns ratio and primary inductance. Minimize resistance in the windings. The turns ratio can be tweaked to get the specified output voltage.

Capacitors

The DC transformer topology runs effectively at 100% duty cycle (50% each side). This means that the input supply current is approximately constant. Therefore, large "hold-up type" capacitors are not necessary. A low value (>4.7µF), low ESR ceramic will be adequate to filter high frequency noise at the input.

The output capacitors supply energy to the output load only during switch transitions. Therefore, large capacitance values are not necessary. Low ESR, surface mount capacitors such as ceramic, OS-CON of POSCAPs are recommended. An additional LC filter can be added in addition to the output capacitor to further reduce output noise.

Transformer winding capacitance between the isolated primary and secondary have parasitic currents that can cause noise on the grounds. Providing a high frequency, low impedance path between the primary and secondary gives the parasitic currents a local return path. A 2.2nF, 1kV ceramic capacitor is recommended.

Switching Diode Selection

A fast recovery, surface mount diode such as a Schottky is recommended. The proximity of the diodes to the transformer outputs is important and should be as close as possible with short, wide traces connecting them.

Optional LC Filter

An optional LC filter, as shown on the Typical Application on the first page of this data sheet, should be included if ultralow noise and ripple are required. It is recommended that the corner frequency of the filter should be set a decade below the switching frequency so that the switch noise is attenuated by a factor of 100. For example, if the f_{OSC} = 100kHz, then f_{CORNER} = 10kHz where:

$$f_{CORNER}\frac{1}{2 \bullet \pi\sqrt{LC}}$$

Output Voltage Regulation

The output voltage of the DC transformer topology is unregulated. Variations in the input voltage will cause the output voltage to vary because the output voltage is a function of the input voltage and the transformer turn ratio. Also, variations in the output load will cause the output voltage to change because of circuit parasitics, such as the transformer DC resistance and power switch on resistance. If regulation is necessary, a post regulator such as a linear regulator can be added to the output of the supply. See the Typical Applications for examples of adding a linear regulator.

More Help

AN70: "A Monolithic Switching Regulator with 100µV Output Noise" contains much information concerning applications and noise measurement techniques.

AN19: "LT1070 Design Manual"

AN29: "Some Thoughts on DC-DC Converters" also have general knowledge on switching regulators.

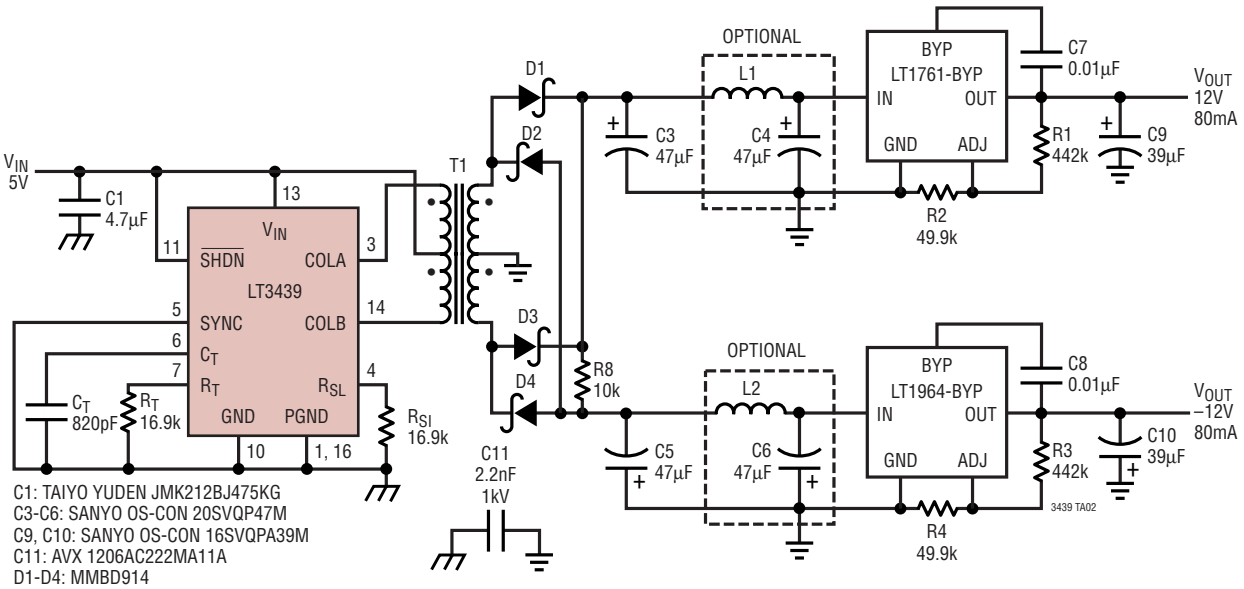
An LTC SwitcherCAD™ model is available to verify design performance.

The LTC Applications department is always ready to lend a helping hand.

SwitcherCAD is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

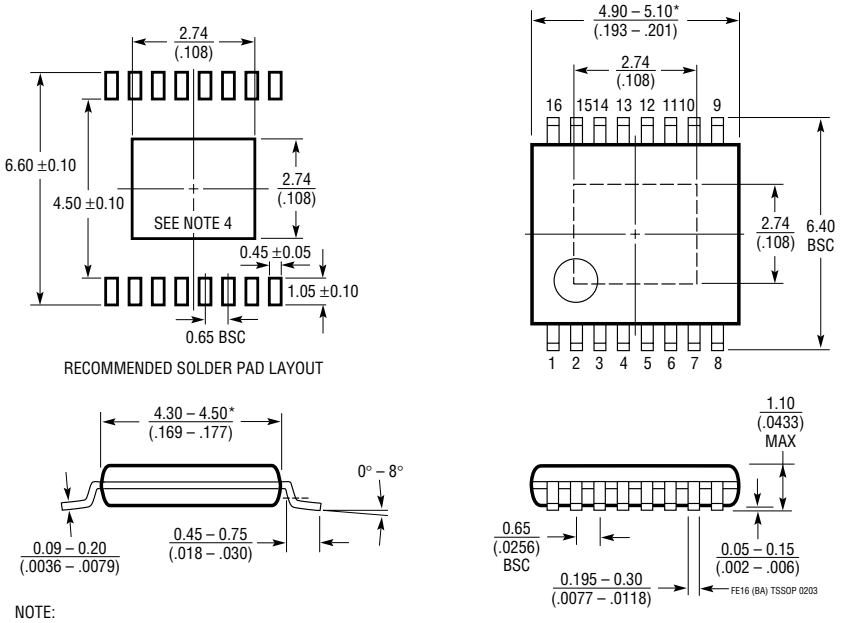
Low Noise 5V to ±12V Push-Pull DC Transformer



C1: TAIYO YUDEN JMK212BJ475KG
C3-C6: SANYO OS-CON 20SVQP47M
C9, C10: SANYO OS-CON 16SVQPA39M
C11: AVX 1206AC222MA11A
D1-D4: MMBD914
L1, L2: COILCRAFT DT1608C-333
T1: COILTRONICS CTX02-16030

PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation BA

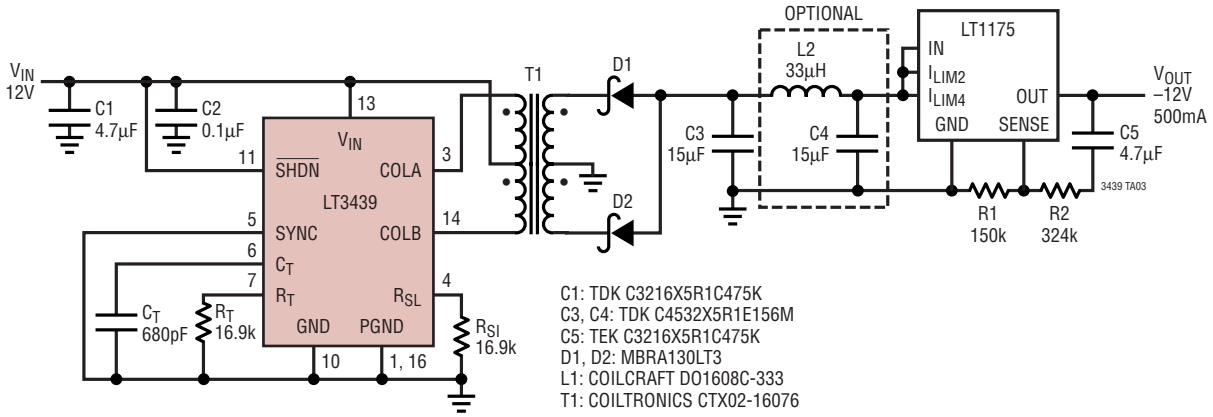


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

Low Noise 12V to –12V, 6W Push-Pull DC Transformer



C1: TDK C3216X5R1C475K
C3, C4: TDK C4532X5R1E156M
C5: TEK C3216X5R1C475K
D1, D2: MBRA130LT3
L1: COILCRAFT DO1608C-333
T1: COILTRONICS CTX02-16076

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1533	Slew Rate Controlled Ultralow Noise 1A Switching Regulator	V_{IN}: 2.7V to 23V, I_Q (Supply): 12mA, I_{SD}: <12µA, SO-16, Low Noise: <100µV_{P-P}, Independent Control of Switch Voltage and Current Slew Rates
LT1534/LT1534-1	Slew Rate Controlled Ultralow Noise 2A Switching Regulators	V_{IN}: 2.7V to 23V, I_Q (Supply): 12mA, I_{SD}: <12µA, SO-16, Low Noise: <2mV_{P-P}, Independent Control of Switch Voltage and Current Slew Rates
LT1683	Slew Rate Controlled Ultralow Noise Push-Pull Controller	V_{IN}: 2.7V to 20V, I_Q (Supply): 25mA, I_{SD}: <24µA, SSOP-20, Low Noise: <200µV_{P-P}, Independent Control of Switch Voltage and Current Slew Rates
LT1738	Slew Rate Controlled Ultralow Noise DC/DC Controller	V_{IN}: 2.7V to 20V, I_Q (Supply): 12mA, I_{SD}: <24µA, SSOP-20, Greatly Reduced Conducted and Radiated EMI, Independent Control of Switch Voltage and Current Slew Rates
LT1763	500mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$: 1.22V, Dropout Voltage (V at I_{OUT}): 0.30V, I_Q (Supply): 30µA, V_{OUT}: 1.5V, 1.8V, 2.5V, 3V, 3.3V, 5V, I_{SD}: <1µA, SO-8, Low Noise: <20µV_{RMSP-P}
LT1764/LT1764A	3A, Low Noise, Fast Transient Response, LDOs	V_{IN}: 2.7V to 20V, $V_{OUT(MIN)}$: 1.21V, Dropout Voltage (V at I_{OUT}): 0.34V, I_Q (Supply): 1mA, V_{OUT}: 1.8V, 2.5V, 3.3V, I_{SD}: <1µA, DD, TO220-5, Low Noise: <40µV_{RMSP-P}, "A" Version Stable with Ceramic Capacitors
LT1962	300mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$: 1.22V, Dropout Voltage (V at I_{OUT}): 0.27V, I_Q (Supply): 30µA, V_{OUT}: 1.5V, 1.8V, 2.5V, 3V, 3.3V, 5V, I_{SD}: <1µA, MS8, Low Noise: <20µV_{RMSP-P}
LT1963/LT1963A	1.5A, Low Noise, Fast Transient Response, LDOs	V_{IN}: 2.1V to 20V, $V_{OUT(MIN)}$: 1.21V, Dropout Voltage (V at I_{OUT}): 0.34V, I_Q (Supply): 1mA, V_{OUT}: 1.5V, 1.8V, 2.5V, 3.3V, I_{SD}: <1µA, DD, TO220-5, SOT-223, SO-8, Low Noise: <40µV_{RMSP-P}, "A" Version Stable with Ceramic Capacitors
LT1964	200mA, Low Noise Micropower, Negative LDO	V_{IN}: –0.9V to –20V, $V_{OUT(MIN)}$: –1.21V, Dropout Voltage (V at I_{OUT}): 0.34V, I_Q (Supply): 30µA, V_{OUT}: Adj, –5V, I_{SD}: <3µA, ThinSOT™, Low Noise: <30µV_{RMSP-P}, Stable with Ceramic Capacitors

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