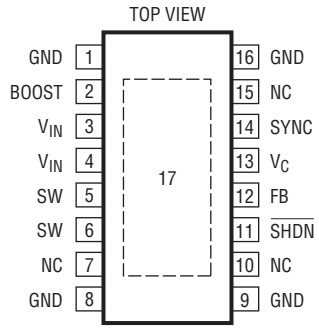
ABSOLUTE MAXIMUM RATINGS (Note 1)

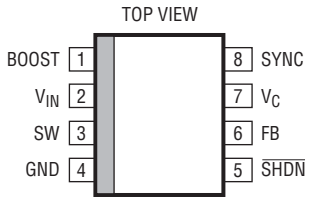
Input Voltage 25V
BOOST Pin Above SW 20V
Max BOOST Pin Voltage.....35V
$\overline{SHDN}$ Pin..... 25V
FB Pin Current..... 1mA
SYNC Pin Current 1mA
Operating Junction Temperature Range
(Note 2)..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



FE PACKAGE
16-LEAD PLASTIC TSSOP

θ_{JA} = 45°C/W, $\theta_{JC(PAD)}$ = 10°C/W
EXPOSED PAD (PIN 17) SOLDERED TO LARGE COPPER PLANE



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 90°C/W, $\theta_{JC(PIN\ 4)}$ = 30°C/W
GROUND PIN CONNECTED TO LARGE COPPER AREA

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1765EFE#PBF	LT1765EFE#TRPBF	1765EFE	16-Lead Plastic TSSOP	–40°C to 125°C
LT1765EFE-1.8#PBF	LT1765EFE-1.8#TRPBF	1765EFE-1.8	16-Lead Plastic TSSOP	–40°C to 125°C
LT1765EFE-2.5#PBF	LT1765EFE-2.5#TRPBF	1765EFE-2.5	16-Lead Plastic TSSOP	–40°C to 125°C
LT1765EFE-3.3#PBF	LT1765EFE-3.3#TRPBF	1765EFE-3.3	16-Lead Plastic TSSOP	–40°C to 125°C
LT1765EFE-5#PBF	LT1765EFE-5#TRPBF	1765EFE-5	16-Lead Plastic TSSOP	–40°C to 125°C
LT1765ES8#PBF	LT1765ES8#TRPBF	1765	8-Lead Plastic SO	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT1765EFE	LT1765EFE#TR	1765EFE	16-Lead Plastic TSSOP	–40°C to 125°C
LT1765EFE-1.8	LT1765EFE-1.8#TR	1765EFE-1.8	16-Lead Plastic TSSOP	–40°C to 125°C
LT1765EFE-2.5	LT1765EFE-2.5#TR	1765EFE-2.5	16-Lead Plastic TSSOP	–40°C to 125°C
LT1765EFE-3.3	LT1765EFE-3.3#TR	1765EFE-3.3	16-Lead Plastic TSSOP	–40°C to 125°C
LT1765EFE-5	LT1765EFE-5#TR	1765EFE-5	16-Lead Plastic TSSOP	–40°C to 125°C
LT1765ES8	LT1765ES8#TR	1765	8-Lead Plastic SO	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, V_C = 0.8V, Boost = V_{IN} + 5V, $\overline{SHDN}$, SYNC and switch open unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Maximum Switch Current Limit				3	4	6	A
Oscillator Frequency	3.3V < V_{IN} < 25V		●	1.1	1.25	1.6	MHz
Switch On Voltage Drop	I = 3A		●		270	430	mV
V_{IN} Undervoltage Lockout	(Note 3)		●	2.47	2.6	2.73	V
V_{IN} Supply Current			●		1	1.3	mA
Shutdown Supply Current	$V_{\overline{SHDN}}$ = 0V, V_{IN} = 25V, V_{SW} = 0V		 ●		15	35 55	µA µA
Feedback Voltage	3V < V_{IN} < 25V, 0.4V < V_C < 0.9V (Note 3)	LT1765 (Adj)	 ●	1.182 1.176	1.2	1.218 1.224	V V
		LT1765-1.8	●	1.764	1.8	1.836	V
		LT1765-2.5	●	2.45	2.5	2.55	V
		LT1765-3.3	●	3.234	3.3	3.366	V
		LT1765-5	●	4.9	5	5.1	V
FB Input Current	LT1765 (Adj)		●		–0.25	–0.5	µA
FB Input Resistance	LT1765-1.8 LT1765-2.5 LT1765-3.3 LT1765-5		● ● ● ●	10.5 14.7 19 29	15 21 27.5 42	21 30 39 60	kΩ kΩ kΩ kΩ
FB Error Amp Voltage Gain	0.4V < V_C < 0.9V			150	350		
FB Error Amp Transconductance	ΔI_{VC} = ±10µA		●	500	850	1300	µMho
V_C Pin Source Current	V_{FB} = V_{NOM} – 17%		●	80	120	160	µA
V_C Pin Sink Current	V_{FB} = V_{NOM} + 17%		●	70	110	180	µA
V_C Pin to Switch Current Transconductance					5		A/V
V_C Pin Minimum Switching Threshold	Duty Cycle = 0%				0.4		V
V_C Pin 3A ISW Threshold					0.9		V
Maximum Switch Duty Cycle	V_C = 1.2V, I_{SW} = 800mA, V_{IN} = 6V		 ●	85 80	90		% %
Minimum Boost Voltage Above Switch	I_{SW} = 3A		●		1.8	2.7	V
Boost Current	I_{SW} = 1A (Note 4) I_{SW} = 3A (Note 4)		● ●		20 70	30 140	mA mA
$\overline{SHDN}$ Threshold Voltage			●	1.27	1.33	1.40	V
$\overline{SHDN}$ Threshold Current Hysteresis			●	4	7	10	µA
$\overline{SHDN}$ Input Current (Shutting Down)	$\overline{SHDN}$ = 60mV Above Threshold		●	–7	–10	–13	µA
SYNC Threshold Voltage					1.5	2.2	V
SYNC Input Frequency				1.6		2	MHz
SYNC Pin Resistance	I_{SYNC} = 1mA				20		kΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

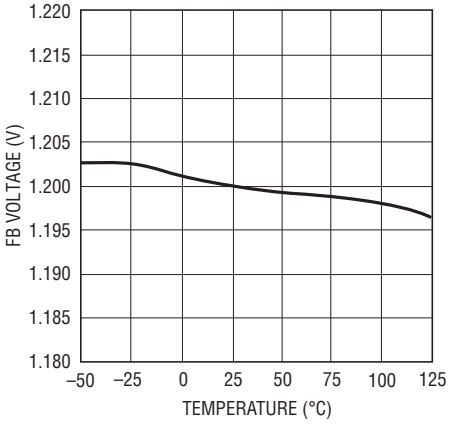
Note 2: The LT1765E is guaranteed to meet performance specifications from 0°C to 125°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Minimum input voltage is defined as the voltage where the internal regulator enters lockout. Actual minimum input voltage to maintain a regulated output will depend on output voltage and load current. See Applications Information.

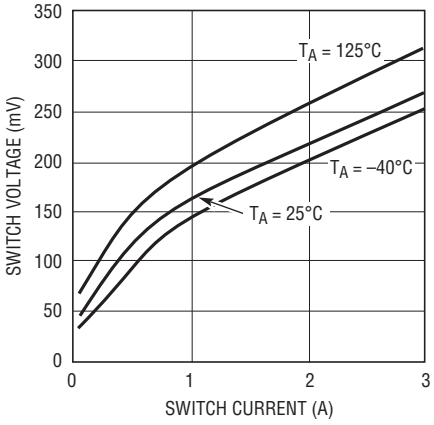
Note 4: Current flows into the BOOST pin only during the on period of the switch cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

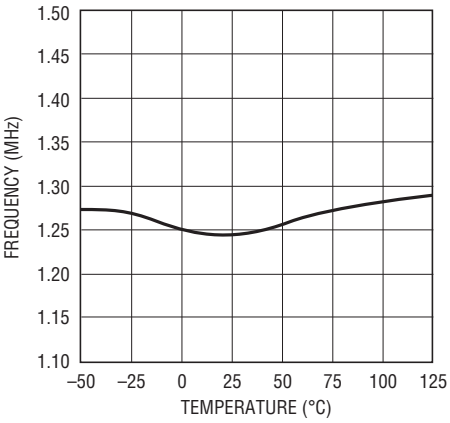
FB vs Temperature (Adj)



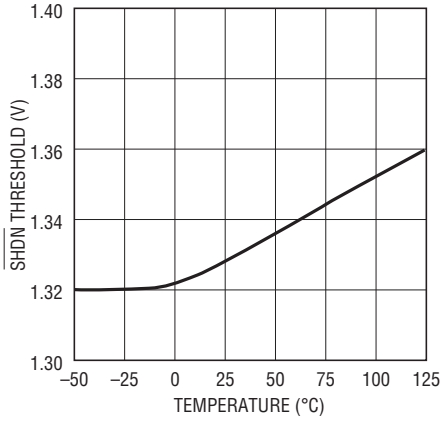
Switch On Voltage Drop



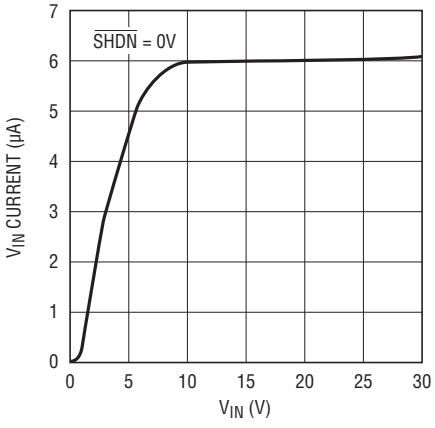
Oscillator Frequency



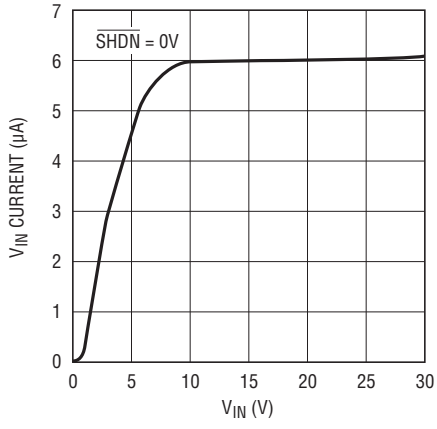
$\overline{SHDN}$ Threshold vs Temperature



$\overline{SHDN}$ Supply Current vs V_{IN}

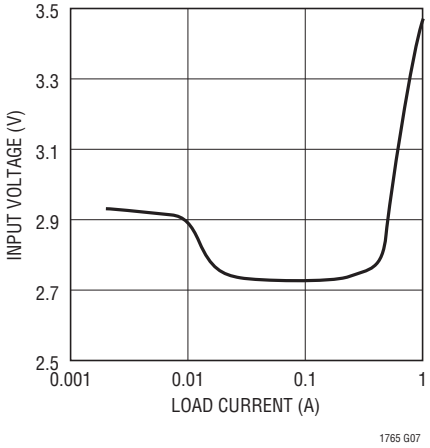


$\overline{SHDN}$ I_P Current vs Temperature

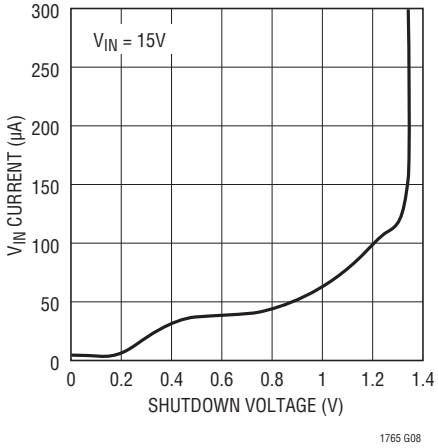


TYPICAL PERFORMANCE CHARACTERISTICS

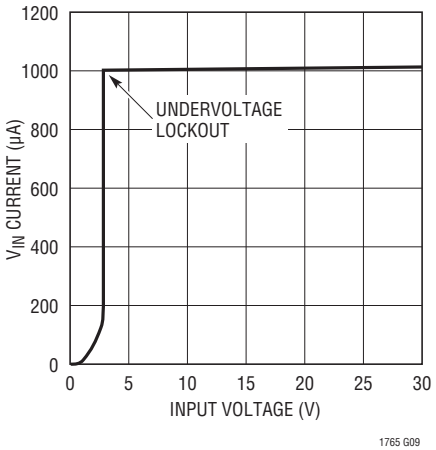
Minimum Input Voltage for 2.5V Out



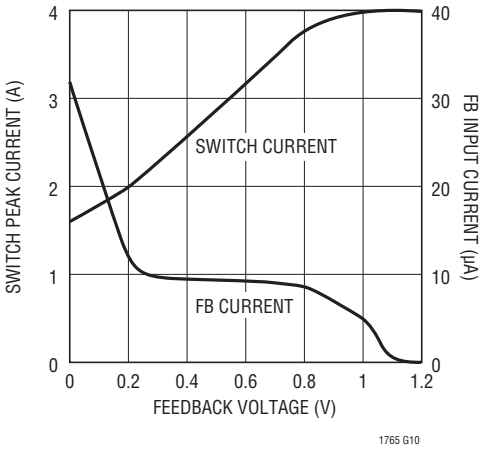
$\overline{SHDN}$ Supply Current



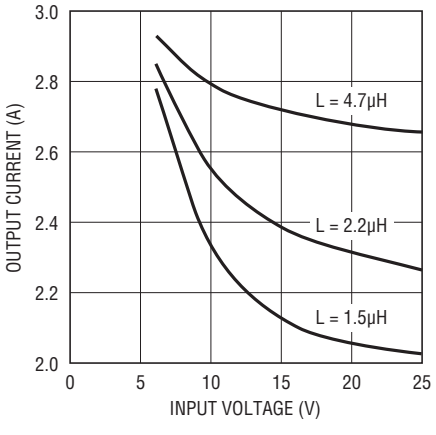
Input Supply Current



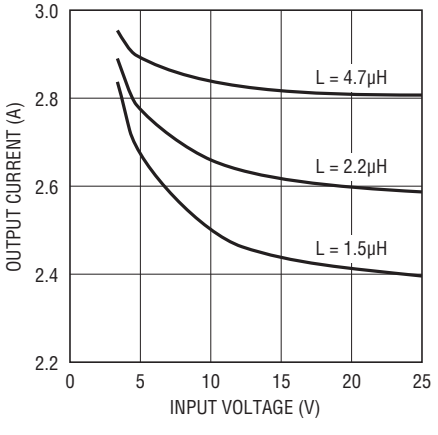
Current Limit Foldback



Maximum Load Current, V_{OUT} = 5V



Maximum Load Current, V_{OUT} = 2.5V



PIN FUNCTIONS

FB: The feedback pin is used to set output voltage using an external voltage divider (adjustable version) that generates 1.2V at the pin when connected to the desired output voltage. The fixed voltage 1.8V, 2.5V, 3.3V and 5V versions have the divider network included internally and the FB pin is connected directly to the output. If required, the current limit can be reduced during start up or short-circuit when the FB pin is below 0.5V (see the Current Limit Foldback graph in the Typical Performance Characteristics section). An impedance of less than 5kΩ on the adjustable version at the FB pin is needed for this feature to operate.

BOOST: The BOOST pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch.

V_{IN}: This is the collector of the on-chip power NPN switch. This pin powers the internal circuitry and internal regulator. At NPN switch on and off, high di/dt edges occur on this pin. Keep the external bypass capacitor and catch diode close to this pin. All trace inductance on this path will create a voltage spike at switch off, adding to the V_{CE} voltage across the internal NPN. Both V_{IN} pins of the TSSOP package must be shorted together on the PC board.

GND: The GND pin acts as the reference for the regulated output, so load regulation will suffer if the "ground" end of the load is not at the same voltage as the GND pin of the IC. This condition will occur when load current or other currents flow through metal paths between the GND pin and the load ground point. Keep the ground path short between the GND pin and the load and use a ground plane when possible. Keep the path between the input bypass and the GND pin short. The exposed GND pad and/or GND pins of the package are directly attached to the internal tab. These pins/pad should be attached to a large copper area to reduce thermal resistance.

V_{SW}: The switch pin is the emitter of the on-chip power NPN switch. This pin is driven up to the input pin voltage during switch on time. Inductor current drives the switch pin negative during switch off time. Negative voltage must be clamped with an external catch diode with a V_{BR} <0.8V. Both V_{SW} pins of the TSSOP package must be shorted together on the PC board.

SYNC: The sync pin is used to synchronize the internal oscillator to an external signal. It is directly logic compatible and can be driven with any signal between 20% and 80% duty cycle. The synchronizing range is from 1.6MHz to 2MHz. See Synchronization section in Applications Information for details. When not in use, this pin should be grounded.

$\overline{SHDN}$: The shutdown pin is used to turn off the regulator and to reduce input drain current to a few microamperes. The 1.33V threshold can function as an accurate undervoltage lockout (UVLO), preventing the regulator from operating until the input voltage has reached a predetermined level. Float or pull high to put the regulator in the operating mode.

V_C: The V_C pin is the output of the error amplifier and the input of the peak switch current comparator. It is normally used for frequency compensation, but can do double duty as a current clamp or control loop override. This pin sits at about 0.4V for very light loads and 0.9V at maximum load. It can be driven to ground to shut off the output.

BLOCK DIAGRAM

The LT1765 is a constant frequency, current mode buck converter. This means that there is an internal clock and two feedback loops that control the duty cycle of the power switch. In addition to the normal error amplifier, there is a current sense amplifier that monitors switch current on a cycle-by-cycle basis. A switch cycle starts with an oscillator pulse which sets the R_S flip-flop to turn the switch on. When switch current reaches a level set by the inverting input of the comparator, the flip-flop is reset and the switch turns off. Output voltage control is obtained by using the output of the error amplifier to set the switch current trip point. This technique means that the error amplifier commands current to be delivered to the output rather than voltage. A voltage fed system will have low phase shift up to the resonant frequency of the inductor and output capacitor, then an abrupt 180° shift will occur. The current fed system will have 90° phase shift at a much lower frequency, but will not have the additional 90° shift until well beyond the LC resonant frequency. This makes it much easier to frequency compensate the feedback loop and also gives much quicker transient response.

High switch efficiency is attained by using the BOOST pin to provide a voltage to the switch driver which is higher than the input voltage, allowing the switch to be saturated. This boosted voltage is generated with an external capacitor and diode. A comparator connected to the shutdown pin disables the internal regulator, reducing supply current.

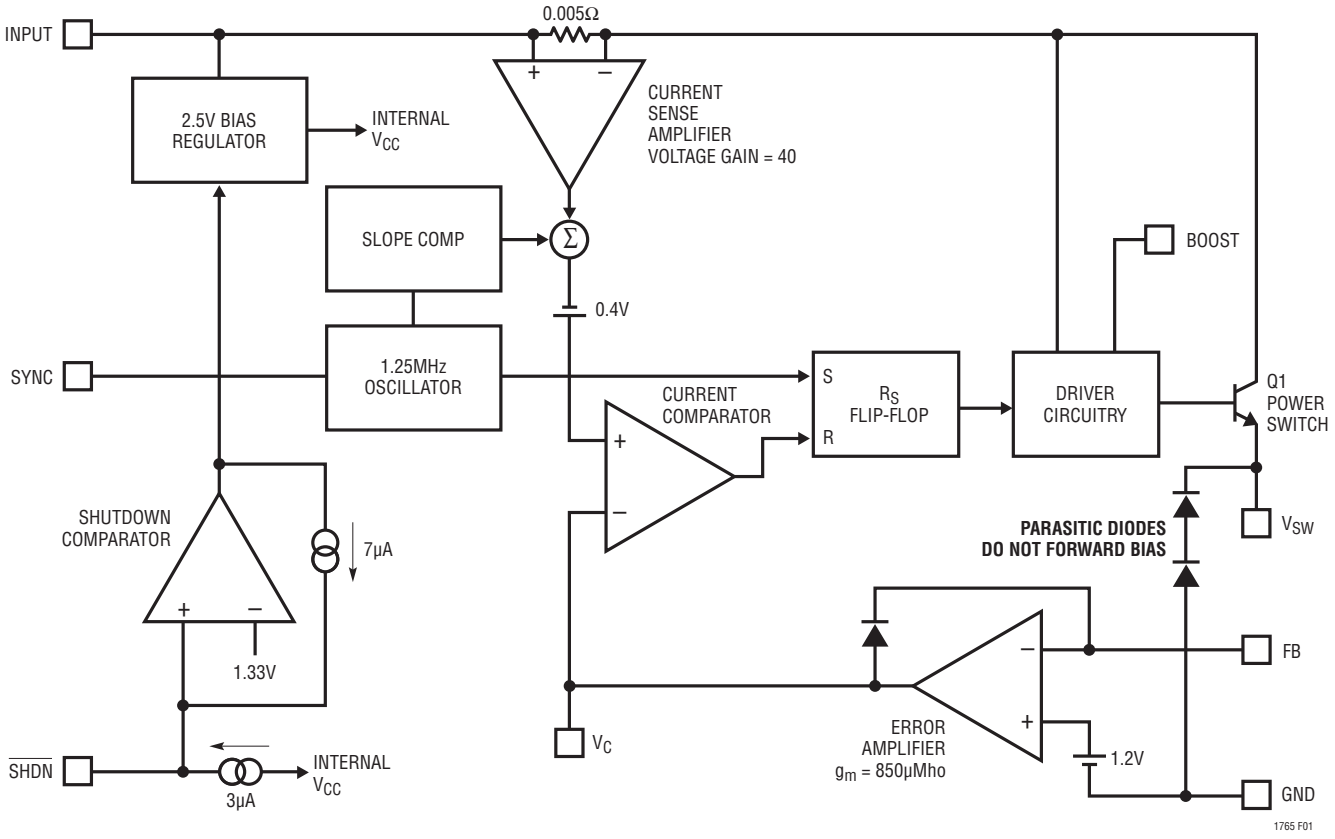


Figure 1. Block Diagram

APPLICATIONS INFORMATION

FB RESISTOR NETWORK

If an output voltage of 1.8V, 2.5V, 3.3V or 5V is required, the respective fixed option part, -1.8, -2.5, -3.3 or -5, should be used. The FB pin is tied directly to the output; the necessary resistive divider is already included on the part. For other voltage outputs, the adjustable part should be used and an external resistor divider added. The suggested resistor (R2) from FB to ground is 10k. This reduces the contribution of FB input bias current to output voltage to less than 0.25%. The formula for the resistor (R1) from V_{OUT} to FB is:

$$R1 = \frac{R2(V_{OUT} - 1.2)}{1.2 - R2(0.25\mu A)}$$

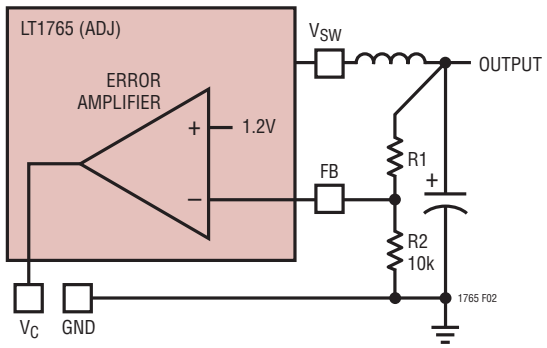


Figure 2. Feedback Network

INPUT CAPACITOR

Step-down regulators draw current from the input supply in pulses. The rise and fall times of these pulses are very fast. The input capacitor is required to reduce the voltage ripple at the input of LT1765 and to force the switching current into a tight local loop, thereby minimizing EMI. The RMS ripple current can be calculated from:

$$I_{RIPPLE(RMS)} = I_{OUT}\sqrt{V_{OUT}(V_{IN} - V_{OUT})/V_{IN}^2}$$

Ceramic capacitors are ideal for input bypassing. At higher switching frequency, the energy storage requirement of the input capacitor is reduced so values in the range of 1µF to 4.7µF are suitable for most applications. Their high frequency capacitive nature removes most ripple current rating and turn-on surge problems. Y5V or similar type ceramics can be used since the absolute value of capacitance is less important and has no significant effect on loop stability. If operation is required close to the minimum input required by the output or the LT1765, a larger value may be required. This is to prevent excessive ripple causing dips below the minimum operating voltage resulting in erratic operation.

If tantalum capacitors are used, values in the 22µF to 470µF range are generally needed to minimize ESR and meet ripple current and surge ratings. Care should be taken to ensure the ripple and surge ratings are not exceeded. The AVX TPS and Kemet T495 series tantalum capacitors are surge rated. AVX recommends derating capacitor operating voltage by 2:1 for high surge applications.

OUTPUT CAPACITOR

Unlike the input capacitor, RMS ripple current in the output capacitor is normally low enough that ripple current rating is not an issue. The current waveform is triangular, with an RMS value given by:

$$I_{RIPPLE(RMS)} = \frac{0.29(V_{OUT})(V_{IN} - V_{OUT})}{(L)(f)(V_{IN})}$$

The LT1765 will operate with both ceramic and tantalum output capacitors. Ceramic capacitors are generally chosen for their small size, very low ESR (effective series resistance), and good high frequency operation. Ceramic output capacitors in the 1µF to 10µF range, X7R or X5R type are recommended.

Tantalum capacitors are usually chosen for their bulk capacitance properties, useful in high transient load applications. ESR rather than absolute value defines output ripple at 1.25MHz. Typical LT1765 applications require a tantalum capacitor with less than 0.3Ω ESR at 22µF to 500µF, see Table 2. This ESR provides a useful zero in the frequency response. Ceramic output capacitors with low ESR usually require a larger V_C capacitor or an additional series R to compensate for this.

APPLICATIONS INFORMATION

Table 2. Surface Mount Solid Tantalum Capacitor ESR and Ripple Current

E Case Size	ESR (Max, Ω)	Ripple Current (A)
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
AVX TAJ	0.7 to 0.9	0.4
D Case Size		
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
C Case Size		
AVX TPS	0.2 (typ)	0.5 (typ)

Figure 3 shows a comparison of output ripple for a ceramic and tantalum capacitor at 200mA ripple current.

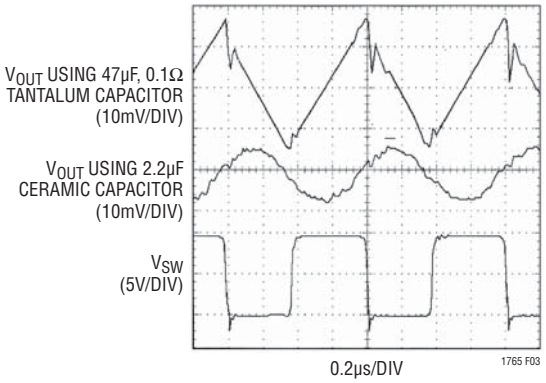


Figure 3. Output Ripple Voltage Waveform

INDUCTOR CHOICE AND MAXIMUM OUTPUT CURRENT

Maximum output current for an LT1765 buck converter is equal to the maximum switch rating (I_P) minus one half peak to peak inductor ripple current. The LT1765 maintains a constant switch current rating at all duty cycles. (Patent Pending)

For most applications, the output inductor will be in the 1µH to 10µH range. Lower values are chosen to reduce the physical size of the inductor, higher values allow higher output currents due to reduced peak to peak ripple current. The following formula gives maximum output current for continuous mode operation, implying that the peak to peak ripple (2x the term on the right) is less than the maximum switch current.

$$I_{OUT(MAX)} = \text{Continuous Mode}\quad I_P - \frac{(V_{OUT})(V_{IN}-V_{OUT})}{2(L)(f)(V_{IN})}$$

For V_{IN} = 8V, V_{OUT} = 5V and L = 3.3µH,

$$I_{OUT(MAX)} = 3 - \frac{(5)(8-5)}{2\left(3.3\bullet10^{-6}\right)\left(1.25\bullet10^{6}\right)(8)}$$
$$= 3 - 0.23 = 2.77A$$

Note that the worst case (minimum output current available) condition is at the maximum input voltage. For the same circuit at 15V, maximum output current would be only 2.6A.

Inductor Selection

The output inductor should have a saturation current rating greater than the peak inductor current set by the current comparator of the LT1765. The peak inductor current will depend on the output current, input and output voltages and the inductor value:

$$I_{PEAK} = I_{OUT} + \frac{V_{OUT}\left(V_{IN}-V_{OUT}\right)}{2(L)(f)(V_{IN})}$$

V_{IN} = Maximum input voltage
f = Switching frequency, 1.25MHz

If an inductor with a peak current lower than the maximum switch current of the LT1765 is chosen a soft-start circuit in Figure 10 should be used. Also, short-circuit conditions should not be allowed because the inductor may saturate resulting in excessive power dissipation.

Also, consideration should be given to the resistance of the inductor. Inductor conduction loses are directly proportional to the DC resistance of inductor. Sometime, the manufacturers will also provide maximum current rating based on the allowable losses in the inductor. Care should be taken, however. At high input voltages and low DCR, excessive switch current could flow during shorted output condition.

Suitable inductors are available from Coilcraft, Coiltronics, Dale, Sumida, Toko, Murata, Panasonic and other manufacturers.

APPLICATIONS INFORMATION

Table 3

PART NUMBER	VALUE (µH)	IRMS (Amps)	DCR (Ω)	HEIGHT (mm)
Coiltcraft				
DO1608C-222	2.2	2.4	0.07	2.9
Sumida				
CDRH3D16-1R5	1.5	1.6	0.043	1.8
CDRH4D18-1R0	1.0	1.7	0.035	2.0
CDC5D23-2R2	2.2	2.2	0.03	2.5
CR43-1R4	1.4	2.5	0.056	3.5
CDRH5D28-2R6	2.6	2.6	0.013	3.0
Toko				
(D62F)847FY-2R4M	2.4	2.5	0.037	2.7
(D73LF)817FY-2R2M	2.2	2.7	0.03	3.0

CATCH DIODE

The diode D1 conducts current only during switch off time. Peak reverse voltage is equal to regulator input voltage. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = \frac{I_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN}}$$

The only reason to consider a larger than 3A diode is the worst-case condition of a high input voltage and shorted output. With a shorted condition, diode current will increase to a typical value of 4A, determined by peak switch current limit of the LT1765. A higher forward voltage will also limit switch current. This is safe for short periods of time, but it would be prudent to check with the diode manufacturer if continuous operation under these conditions must be tolerated.

BOOST PIN

For most applications, the boost components are a 0.18µF capacitor and a CMDSH-3 diode. The anode is typically connected to the regulated output voltage to generate a voltage approximately V_{OUT} above V_{IN} to drive the output stage. The output driver requires at least 2.7V of headroom throughout the on period to keep the switch fully saturated. However, the output stage discharges the boost capacitor during this on time. If the output voltage is less than 3.3V, it is recommended that an alternate boost supply is used.

The boost diode can be connected to the input, although, care must be taken to prevent the 2x V_{IN} boost voltage from exceeding the BOOST pin absolute maximum rating. The additional voltage across the switch driver also increases power loss, reducing efficiency. If available, an independent supply can be used with a local bypass capacitor.

A 0.18µF boost capacitor is recommended for most applications. Almost any type of film or ceramic capacitor is suitable, but the ESR should be <1Ω to ensure it can be fully recharged during the off time of the switch. The capacitor value is derived from worst-case conditions of 700ns on-time, 90mA boost current, and 0.7V discharge ripple. This value is then guard banded by 2x for secondary factors such as capacitor tolerance, ESR and temperature effects. The boost capacitor value could be reduced under less demanding conditions, but this will not improve circuit operation or efficiency. Under low input voltage and low load conditions, a higher value capacitor will reduce discharge ripple and improve start up operation.

SHUTDOWN AND UNDERVOLTAGE LOCKOUT

Figure 4 shows how to add undervoltage lockout (UVLO) to the LT1765. Typically, UVLO is used in situations where the input supply is *current limited*, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. UVLO prevents the regulator from operating at source voltages where these problems might occur.

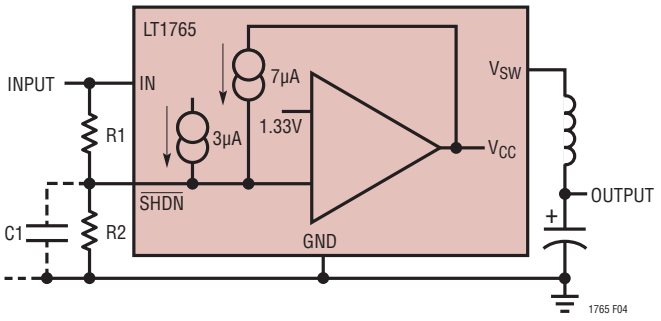


Figure 4. Undervoltage Lockout

APPLICATIONS INFORMATION

An internal comparator will force the part into shutdown below the minimum V_{IN} of 2.6V. This feature can be used to prevent excessive discharge of battery-operated systems. If an adjustable UVLO threshold is required, the shutdown pin can be used. The threshold voltage of the shutdown pin comparator is 1.33V. A 3µA internal current source defaults the open pin condition to be operating (see Typical Performance Graphs). Current hysteresis is added above the $\overline{SHDN}$ threshold. This can be used to set voltage hysteresis of the UVLO using the following:

$$R1 = \frac{V_H - V_L}{7\mu A}$$

$$R2 = \frac{1.33V}{\frac{(V_H - 1.33V)}{R1} + 3\mu A}$$

V_H – Turn-on threshold

V_L – Turn-off threshold

Example: switching should not start until the input is above 4.75V and is to stop if the input falls below 3.75V.

$V_H = 4.75V$

$V_L = 3.75V$

$$R1 = \frac{4.75V - 3.75V}{7\mu A} = 143k$$

$$R2 = \frac{1.33V}{\frac{(4.75V - 1.33V)}{143k} + 3\mu A} = 49.4k$$

Keep the connections from the resistors to the $\overline{SHDN}$ pin short and make sure that the interplane or surface capacitance to the switching nodes are minimized. If high resistor values are used, the $\overline{SHDN}$ pin should be bypassed with a 1nF capacitor to prevent coupling problems from the switch node.

SYNCHRONIZATION

The SYNC pin is used to synchronize the internal oscillator to an external signal. The SYNC input must pass from a logic level low, through the maximum synchronization threshold with a duty cycle between 20% and 80%. The input can be driven directly from a logic level output. The synchronizing range is equal to *initial* operating frequency up to 2MHz. This means that *minimum* practical sync frequency is equal to the worst-case *high* self-oscillating frequency (1.6MHz), not the typical operating frequency of 1.25MHz. Caution should be used when synchronizing above 1.8MHz because at higher sync frequencies the amplitude of the internal slope compensation used to prevent subharmonic switching is reduced. This type of subharmonic switching only occurs at input voltages less than twice output voltage. Higher inductor values will tend to eliminate this problem. See Frequency Compensation section for a discussion of an entirely different cause of subharmonic switching before assuming that the cause is insufficient slope compensation. Application Note 19 has more details on the theory of slope compensation.

LAYOUT CONSIDERATIONS

As with all high frequency switchers, when considering layout, care must be taken in order to achieve optimal electrical, thermal and noise performance. For maximum efficiency, switch rise and fall times are typically in the nanosecond range. To prevent noise both radiated and conducted, the high speed switching current path, shown in Figure 5, must be kept as short as possible. Shortening this path will also reduce the parasitic trace inductance of approximately 25nH/inch. At switch off, this parasitic inductance produces a flyback spike across the LT1765 switch. When operating at higher currents and input voltages, with poor layout, this spike can generate voltages across the LT1765 that may exceed its absolute maximum

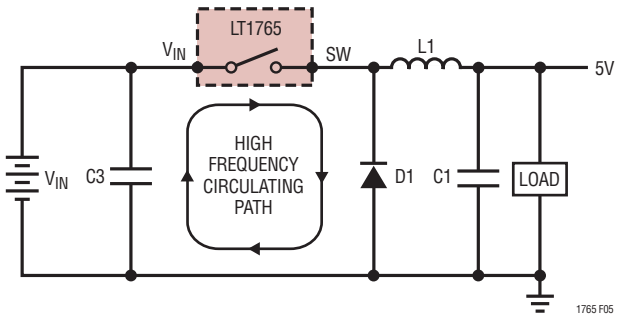


Figure 5. High Speed Switching Path

APPLICATIONS INFORMATION

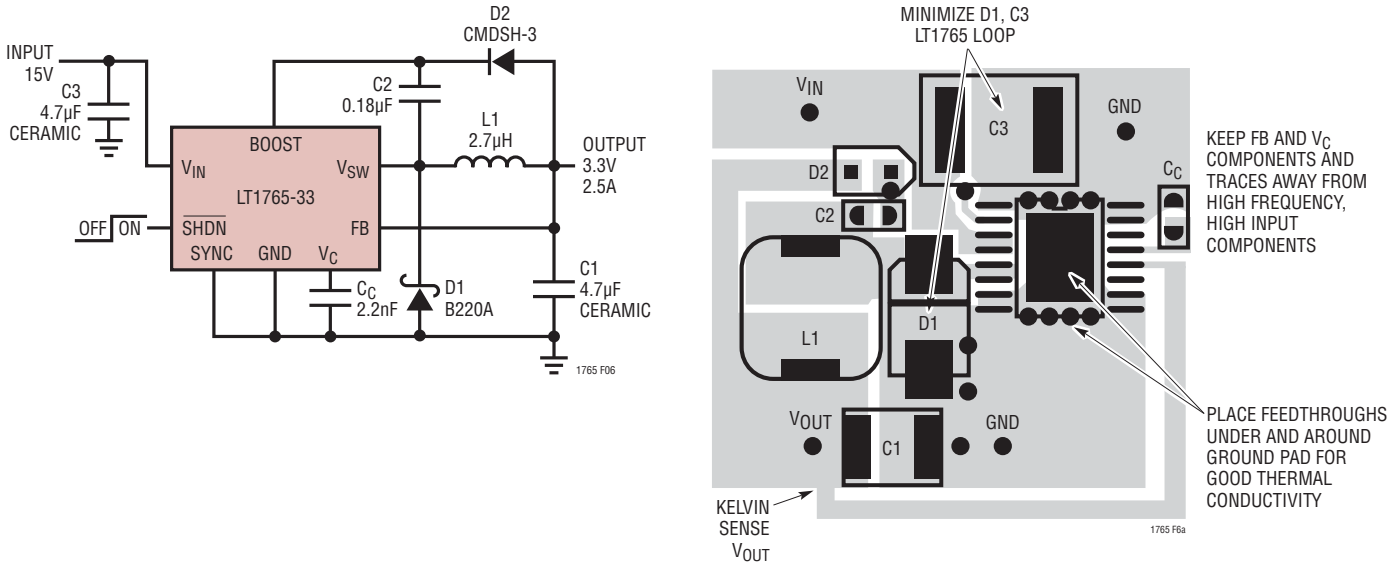


Figure 6. Typical Application and Layout (Topside Only Shown)

rating. A ground plane should always be used under the switcher circuitry to prevent interplane coupling and overall noise.

The V_C and FB components should be kept as far away as possible from the switch and boost nodes. The LT1765 pinout has been designed to aid in this. The ground for these components should be separated from the switch current path. Failure to do so will result in poor stability or subharmonic like oscillation.

Board layout also has a significant effect on thermal resistance. The exposed pad or GND pin is a continuous copper plate that runs under the LT1765 die. This is the best thermal path for heat out of the package as can be seen by the low θ_{JC} of the exposed pad package. Reducing the thermal resistance from Pin 4 or exposed pad onto the board will reduce die temperature and increase the power capability of the LT1765. This is achieved by providing as much copper area as possible around this pin/pad. Also, having multiple solder filled feedthroughs to a continuous copper plane under LT1765 will help in reducing thermal resistance. Ground plane is usually suitable for this purpose. In multilayer PCB designs, placing a ground plane next to the layer with the LT1765 will reduce thermal resistance to a minimum.

THERMAL CALCULATIONS

Power dissipation in the LT1765 chip comes from four sources: switch DC loss, switch AC loss, boost circuit current, and input quiescent current. The following formulas show how to calculate each of these losses. These formulas assume continuous mode operation, so they should not be used for calculating efficiency at light load currents.

Switch loss:

$$P_{SW} = \frac{R_{SW}(I_{OUT})^2(V_{OUT})}{V_{IN}} + 17ns(I_{OUT})(V_{IN})(f)$$

Boost current loss for VBOOST = VOUT:

$$P_{BOOST} = \frac{V_{OUT}{}^2(I_{OUT}/50)}{V_{IN}}$$

Quiescent current loss:

$$P_Q = V_{IN}(0.001)$$

R_{SW} = Switch resistance (≈0.13Ω at hot)
17ns = Equivalent switch current/voltage overlap time
f = Switch frequency

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Example: with V_{IN} = 10V, V_{OUT} = 5V and I_{OUT} = 2A:

$$P_{SW} = \frac{(0.13)(2)^2(5)}{10} + \left(17 \bullet 10^{-9}\right)(2)(10)\left(1.25 \bullet 10^{6}\right)$$
$$= 0.26 + 0.43 = 0.69W$$

$$P_{BOOST} = \frac{(5)^2(2/50)}{10} = 0.1W$$

$$P_Q = 10(0.001) = 0.01W$$

Total power dissipation, P_{TOT}, is 0.69 + 0.1 + 0.01 = 0.8W.

Thermal resistance for the LT1765 16-lead TSSOP exposed pad package is influenced by the presence of internal or backside planes. With a full plane under the package, thermal resistance will be about 45°C/W. With no plane under the package, thermal resistance will increase to about 110°C/W. For the exposed pad package $\theta_{JC(PAD)}$ = 10°C/W. Thermal resistance is dominated by board performance. To calculate die temperature, use the appropriate thermal resistance number and add in worst-case ambient temperature:

$$T_J = T_A + \theta_{JA\ (PTOT)}$$

When estimating ambient, remember the nearby catch diode will also be dissipating power.

$$P_{DIODE} = \frac{(V_F)(V_{IN} - V_{OUT})(I_{LOAD})}{V_{IN}}$$

V_F = Forward voltage of diode (assume 0.5V at 2A)

$$P_{DIODE} = \frac{(0.5)(10-5)(2)}{10} = 0.5W$$

Notice that the catch diode's forward voltage contributes a significant loss in the overall system efficiency. A larger, lower V_F diode can improve efficiency by several percent.

Typical thermal resistance of the board θ_B is 35°C/W. At an ambient temperature of 25°C,

$$T_J = T_A + \theta_{JA}(P_{TOT}) + \theta_B(P_{DIODE})$$

$$T_J = 25 + 45\ (0.8) + 35\ (0.5) = 79°C$$

DIE TEMPERATURE MEASUREMENT

If a true die temperature is required, a measurement of the SYNC to GND pin resistance can be used. The SYNC pin resistance across temperature must first be calibrated, with no significant output load, in an oven. An initial value of 40k with a temperature coefficient of 0.16%/°C is typical. The same measurement can then be used in operation to indicate the die temperature.

FREQUENCY COMPENSATION

Before starting on the theoretical analysis of frequency response, the following should be remembered—the worse the board layout, the more difficult the circuit will be to stabilize. This is true of almost all high frequency analog circuits, read the 'LAYOUT CONSIDERATIONS' section first. Common layout errors that appear as stability problems are distant placement of input decoupling capacitor and/or catch diode, and connecting the V_C compensation to a ground track carrying significant switch current. In addition, the theoretical analysis considers only first order ideal component behavior. For these reasons, it is important that a final stability check is made with production layout and components.

The LT1765 uses current mode control. This alleviates many of the phase shift problems associated with the inductor. The basic regulator loop is shown in Figure 7, with both tantalum and ceramic capacitor equivalent circuits. The LT1765 can be considered as two g_m blocks, the error amplifier and the power stage.

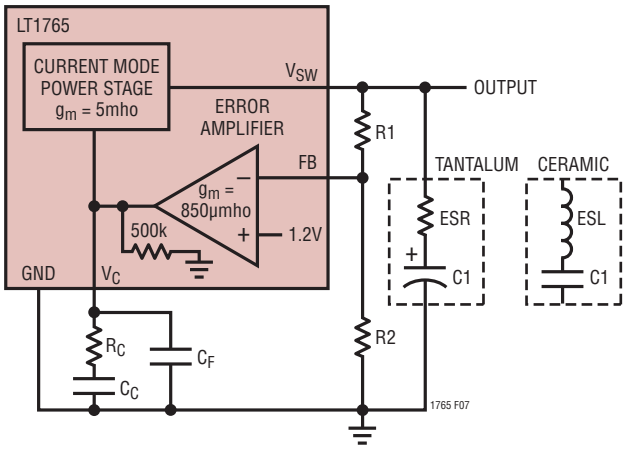

Figure 7. Model for Loop Response

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Figure 8 shows the overall loop response with a 330pF VC capacitor and a typical 100µF tantalum output capacitor. The response is set by the following terms:

Error amplifier:

DC gain set by g_m and R_L = 850µ • 500k = 425. Pole set by C_F and R_L = $(2\pi \bullet 500k \bullet 330p)^{-1}$ = 965Hz. Unity-gain set by C_F and g_m = $(2\pi \bullet 330p \bullet 850\mu^{-1})^{-1}$ = 410kHz.

Power stage:

DC gain set by g_m and R_L (assume 5Ω) = 5 • 5 = 25. Pole set by C_{OUT} and R_L = $(2\pi \bullet 100\mu \bullet 10)^{-1}$ = 159Hz. Unity-gain set by C_{OUT} and g_m = $(2\pi \bullet 100\mu \bullet 5^{-1})^{-1}$ = 8kHz.

Tantalum output capacitor:

Zero set by C_{OUT} and C_{ESR} = $(2\pi \bullet 100\mu \bullet 0.1)^{-1}$ = 15.9kHz.

The zero produced by the ESR of the tantalum output capacitor is very useful in maintaining stability. Ceramic output capacitors do not have a zero due to very low ESR, but are dominated by their ESL. They form a notch in the 1MHz to 10MHz range. Without this zero, the V_C pole must be made dominant. A typical value of 2.2nF will achieve this.

If better transient response is required, a zero can be added to the loop using a resistor (R_C) in series with the compensation capacitor. As the value of R_C is increased, transient response will generally improve, but two effects limit its value. First, the combination of output capacitor ESR and a large R_C may stop loop gain rolling off altogether.

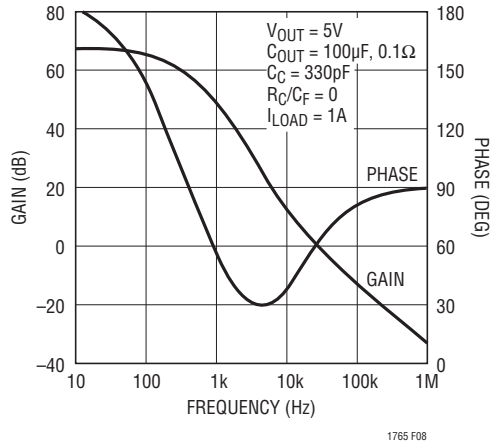


Figure 8. Overall Loop Response

Second, if the loop gain is not rolled sufficiently at the switching frequency, output ripple will perturb the V_C pin enough to cause unstable duty cycle switching similar to subharmonic oscillation. This may not be apparent at the output. Small signal analysis will not show this since a continuous time system is assumed. If needed, an additional capacitor (C_F) can be added to the V_C pin to form a pole at typically one fifth the switching frequency (If R_C = ~ 5k, C_F = ~ 100pF)

When checking loop stability, the circuit should be operated over the application's full voltage, current and temperature range. Any transient loads should be applied and the output voltage monitored for a well-damped behavior.

CONVERTER WITH BACKUP OUTPUT REGULATOR

In systems with a primary and backup supply, for example, a battery powered device with a wall adapter input, the output of the LT1765 can be held up by the backup supply with its input disconnected. In this condition, the SW pin will source current into the V_{IN} pin. If the $\overline{SHDN}$ pin is held at ground, only the shutdown current of 6µA will be pulled via the SW pin from the second supply. With the $\overline{SHDN}$ pin floating, the LT1765 will consume its quiescent operating current of 1mA. The V_{IN} pin will also source current to any other components connected to the input line. If this load is greater than 10mA or the input could be shorted to ground, a series Schottky diode must be added, as shown in Figure 9. With these safeguards, the output can be held at voltages up to the V_{IN} absolute maximum rating.

BUCK CONVERTER WITH ADJUSTABLE SOFT-START

Large capacitive loads or high input voltages can cause high input currents at start-up. Figure 10 shows a circuit that limits the dv/dt of the output at start-up, controlling the capacitor charge rate. The buck converter is a typical configuration with the addition of R3, R4, C_{SS} and Q1. As the output starts to rise, Q1 turns on, regulating switch current via the V_C pin to maintain a constant dv/dt at the output. Output rise time is controlled by the current through C_{SS} defined by R4 and Q1's V_{BE}. Once the output is in regulation, Q1 turns off and the circuit operates normally. R3 is transient protection for the base of Q1.

APPLICATIONS INFORMATION

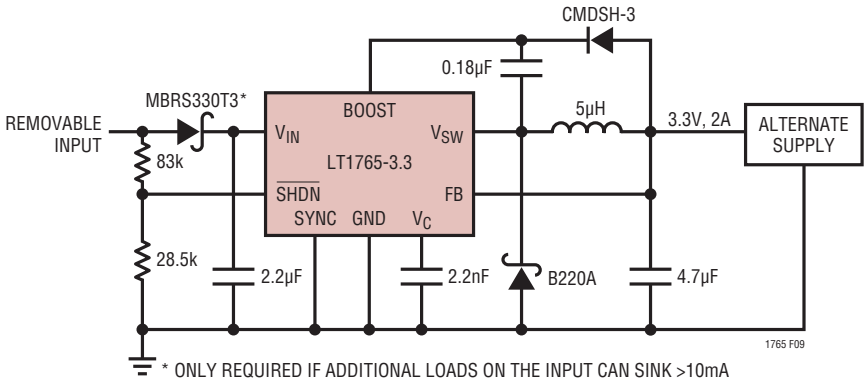


Figure 9. Dual Source Supply with 6µA Reverse Leakage

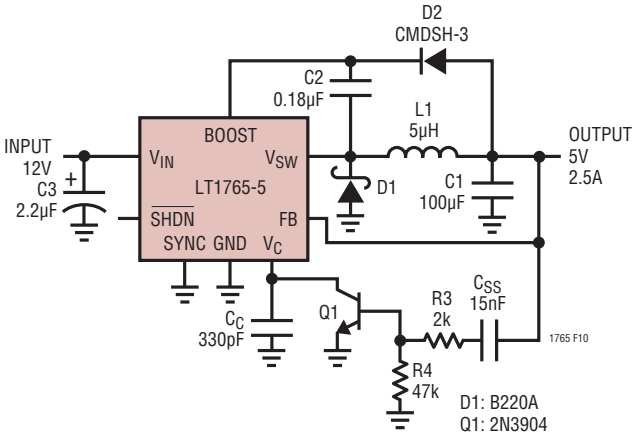


Figure 10. Buck Converter with Adjustable Soft Start

$$\text{RiseTime} = \frac{(R4)(C_{SS})(V_{OUT})}{(V_{BE})}$$

Using the values shown in Figure 10,

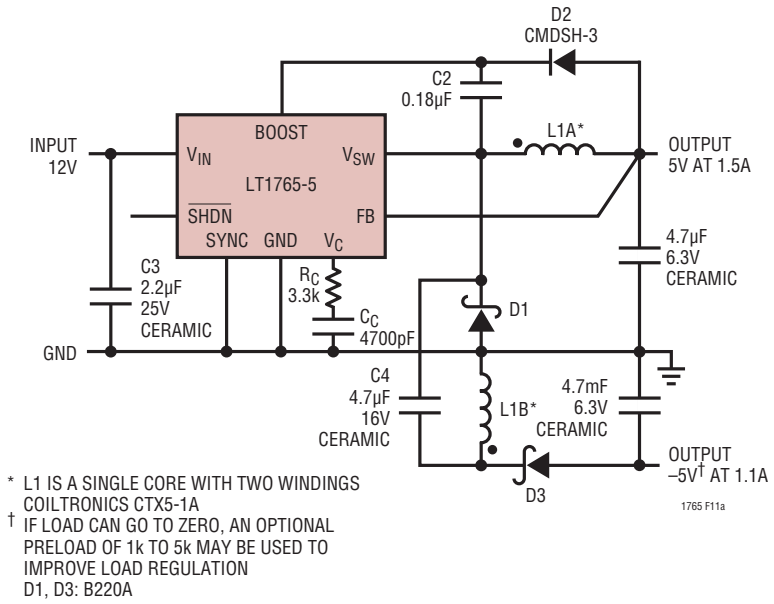
$$\text{RiseTime} = \frac{(47 \bullet 10^{3})(15 \bullet 10^{-9})(5)}{0.7} = 5\text{ms}$$

The ramp is linear and rise times in the order of 100ms are possible. Since the circuit is voltage controlled, the ramp rate is unaffected by load characteristics and maximum output current is unchanged. Variants of this circuit can be used for sequencing multiple regulator outputs.

Dual Output Converter

The circuit in Figure 11 generates both positive and negative 5V outputs with a single piece of magnetics. The two inductors shown are actually just two windings on a standard B H Electronics inductor. The topology for the 5V output is a standard buck converter. The –5V topology would be a simple flyback winding coupled to the buck converter if C4 were not present. C4 creates a SEPIC (single-ended primary inductance converter) topology which improves regulation and reduces ripple current in L1. Without C4, the voltage swing on L1B compared to L1A would vary due to relative loading and coupling losses. C4 provides a low impedance path to maintain an equal voltage swing in L1B, improving regulation. In a flyback converter, during switch on time, all the converter's energy is stored in L1A only, since no current flows in L1B. At switch off, energy is transferred by magnetic coupling into L1B, powering the –5V rail. C4 pulls L1B positive during switch on time, causing current to flow, and energy to build in L1B and C4. At switch off, the energy stored in both L1B and C4 supply the –5V rail. This reduces the current in L1A and changes L1B current waveform from square to triangular. For details on this circuit, including maximum output currents, see Design Note 100

APPLICATIONS INFORMATION



* L1 IS A SINGLE CORE WITH TWO WINDINGS
COILTRONICS CTX5-1A
† IF LOAD CAN GO TO ZERO, AN OPTIONAL
PRELOAD OF 1k TO 5k MAY BE USED TO
IMPROVE LOAD REGULATION
D1, D3: B220A

Figure 11a. Dual Output Converter

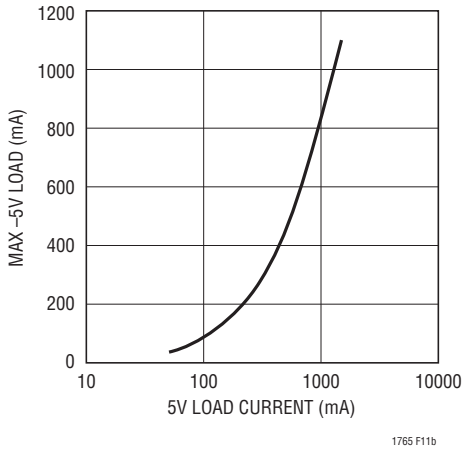


Figure 11b. Dual Output Converter (Output Currents)

APPLICATIONS INFORMATION

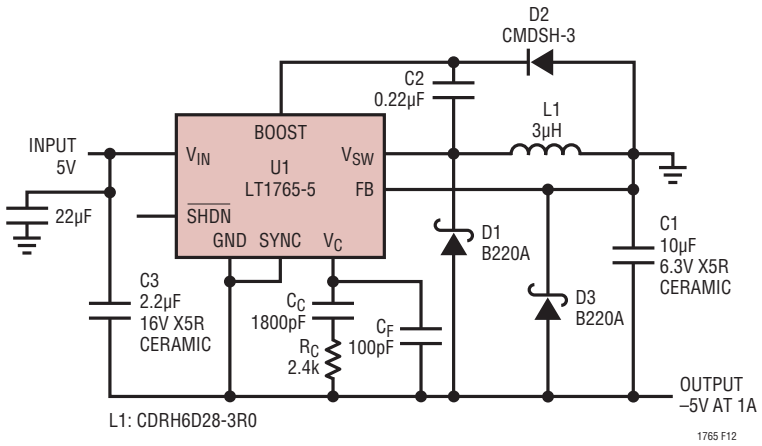


Figure 12. Positive-to-Negative Low Output Ripple Converter

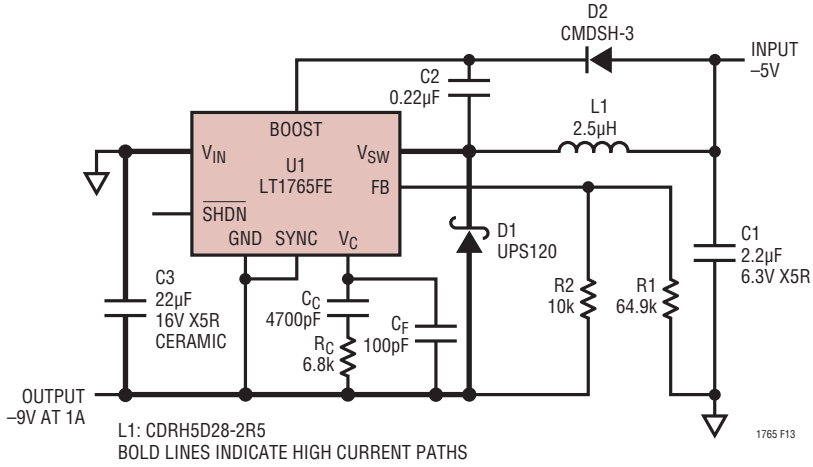
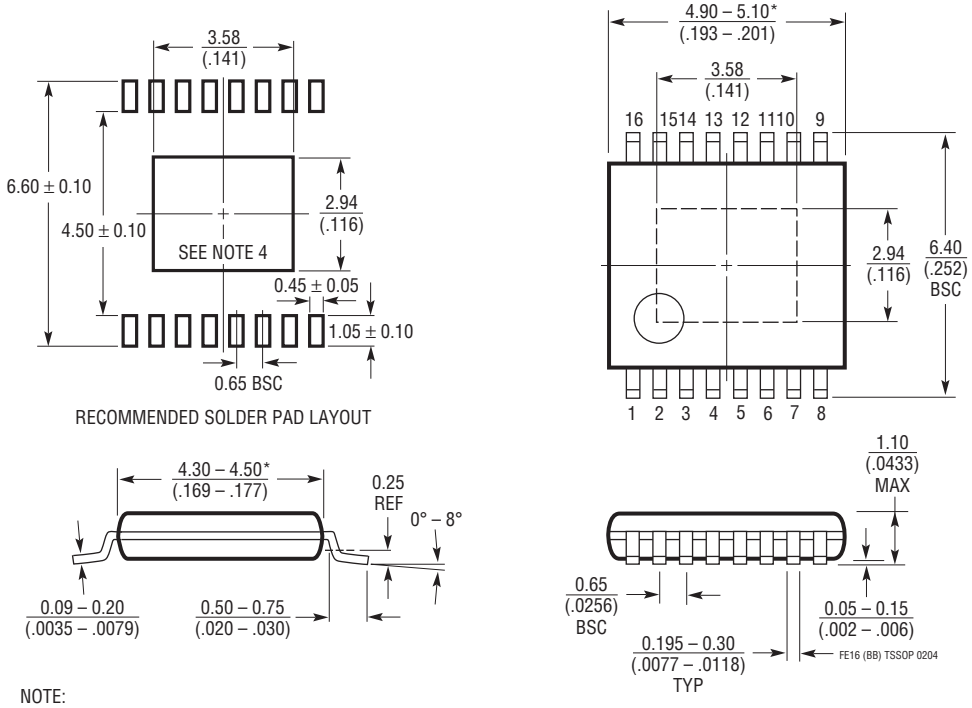


Figure 13. Negative Boost Converter

PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)

Exposed Pad Variation BB

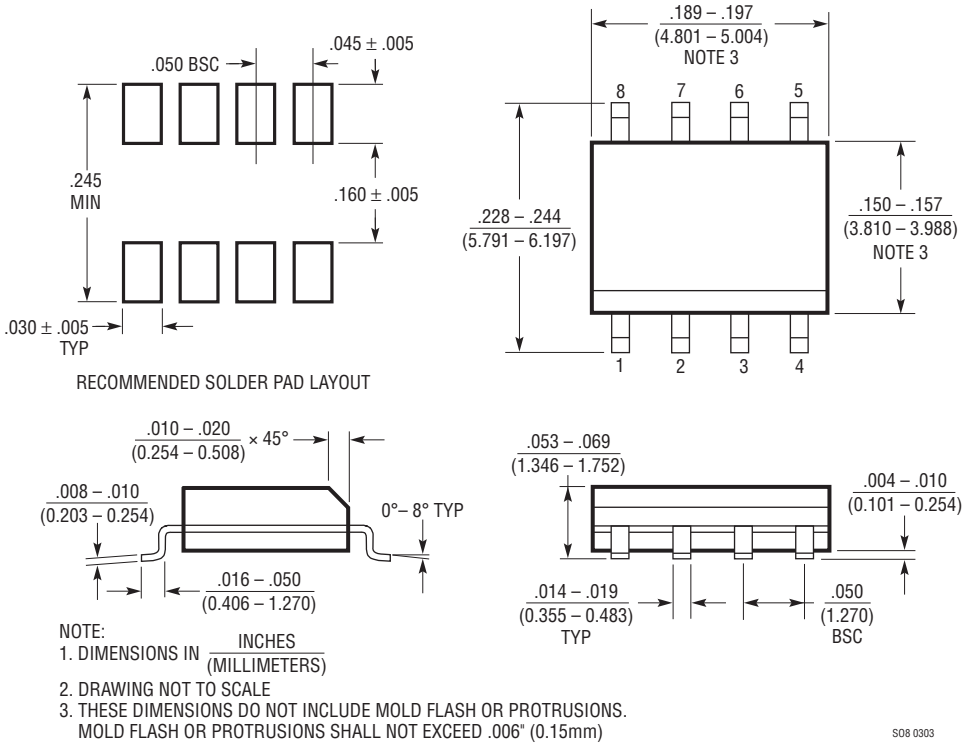


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1074/LT1074HV	4.4A (I_{OUT}), 100kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.3V to 45V/64V, $V_{OUT(MIN)}$ = 2.21V, I_Q = 8.5mA, I_{SD} = 10µA, DD5/7, TO220-5/7
LT1076/LT1076HV	1.6A (I_{OUT}), 100kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.3V to 45V/64V, $V_{OUT(MIN)}$ = 2.21V, I_Q = 8.5mA, I_{SD} = 10µA, DD5/7, TO220-5/7
LT1676	60V, 440mA (I_{OUT}), 100kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.4V to 60V, $V_{OUT(MIN)}$ = 1.24V, I_Q = 3.2mA, I_{SD} < 2.5µA, SO-8
LT1765	25V, 2.75A (I_{OUT}), 1.25MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 1mA, I_{SD} < 15µA, SO-8, TSSOP16E
LT1766	60V, 1.2A (IOUT), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} < 25µA, TSSOP16/E
LT1767	25V, 1.2A (I_{OUT}), 1.25MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 1mA, I_{SD} < 6µA, MS8/E
LT1776	40V, 550mA (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.4V to 40V, $V_{OUT(MIN)}$ = 1.24V, I_Q = 3.2mA, I_{SD} < 30µA, N8, SO-8
LT1940	25V, Dual 1.2A (I_{OUT}), 1.1MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 3.8mA, I_{SD} = < 1µA, TSSOP16E
LT1956	60V, 1.2A (I_{OUT}), 500kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} < 25µA, TSSOP16/E
LT1976	60V, 1.2A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter with Burst Mode® Operation	V_{IN}: 3.3V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 100µA, I_{SD} < 1µA, TSSOP16E
LT3010	80V, 50mA, Low Noise Linear Regulator	V_{IN}: 1.5V to 80V, $V_{OUT(MIN)}$ = 1.28V, I_Q = 30µA, I_{SD} < 1µA, MS8E
LTC3407	Dual 600mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MS10E
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, TSSOP16E
LTC3414	4A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	V_{IN}: 2.3V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, I_{SD} < 1µA, TSSOP20E
LT3430/LT3431	60V, 2.75A (I_{OUT}), 200kHz/500kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} = 30µA, TSSOP16E
LT3433	60V, 400mA (I_{OUT}), 200kHz, High Efficiency Step-Up/Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 4V to 60V, $V_{OUT(MIN)}$ = 3.3V to 20V, I_Q = 100µA, I_{SD} < 1µA, TSSOP16E
LTC3727/LTC3727-1	36V, 500kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 4V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 670µA, I_{SD} < 20µA, QFN32, SSOP28

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