

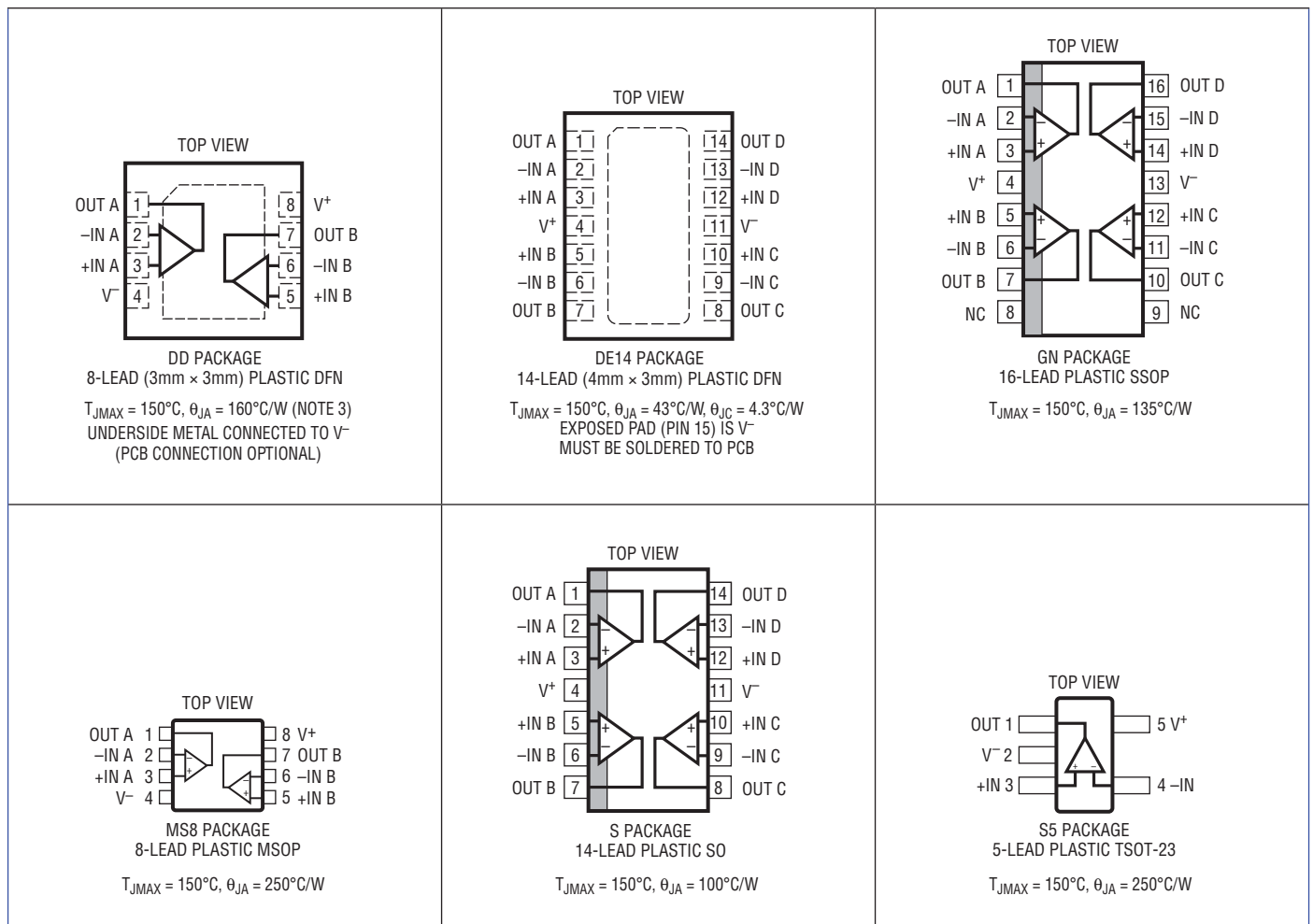
LT1395/LT1396/LT1397

ABSOLUTE MAXIMUM RATINGS (Note 1)

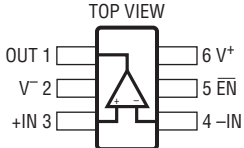
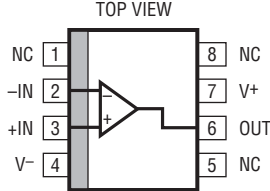
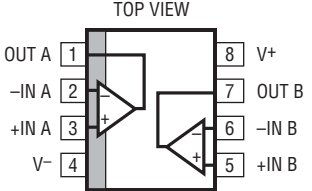
Total Supply Voltage (V^+ to V^-) 12.6V
 Input Current (Note 2)..... $\pm 10\text{mA}$
 Output Current $\pm 100\text{mA}$
 Differential Input Voltage (Note 2)..... $\pm 5\text{V}$
 Output Short-Circuit Duration (Note 3) Continuous
 Operating Temperature Range (Note 4)
 LT1395C/LT1396C/LT1397C -40°C to 85°C
 LT1397H -40°C to 125°C

Specified Temperature Range (Note 5)
 LT1395C/LT1396C/LT1397C 0°C to 70°C
 LT1397H -40°C to 125°C
 Storage Temperature Range..... -65°C to 150°C
 Storage Temperature Range
 (DD Package)..... -65°C to 125°C
 Junction Temperature (Note 6) 150°C
 Junction Temperature (DD Package) (Note 6)..... 125°C
 Lead Temperature (Soldering, 10 sec) 300°C

PIN CONFIGURATION



PIN CONFIGURATION

 TOP VIEW OUT 1 6 V⁺ V⁻ 2 5 EN +IN 3 4 -IN S6 PACKAGE 6-LEAD PLASTIC TSOT-23 T_{JMAX} = 150°C, θ_{JA} = 230°C/W	 TOP VIEW NC 1 8 NC -IN 2 7 V⁺ +IN 3 6 OUT V- 4 5 NC S8 PACKAGE (1395) 8-LEAD PLASTIC SO T_{JMAX} = 150°C, θ_{JA} = 150°C/W	 TOP VIEW OUT A 1 8 V⁺ -IN A 2 7 OUT B +IN A 3 6 -IN B V- 4 5 +IN B S8 PACKAGE (1396) 8-LEAD PLASTIC SO T_{JMAX} = 150°C, θ_{JA} = 150°C/W
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ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1396CDD#PBF	LT1396CDD#TRPBF	LABD	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT1397CDE#PBF	LT1397CDE#TRPBF	1397	14-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LT1397HDE#PBF	LT1397HDE#TRPBF	1397	14-Lead (4mm × 3mm) Plastic DFN	-40°C to 125°C
LT1397CGN#PBF	LT1397CGN#TRPBF	1397	16-Lead Plastic SSOP	0°C to 70°C
LT1396CMS8#PBF	LT1396CMS8#TRPBF	LTDY	8-Lead Plastic MSOP	0°C to 70°C
LT1397CS#PBF	LT1397CS#TRPBF	1397CS	14-Lead Plastic SO	0°C to 70°C
LT1395CS5#PBF	LT1395CS5#TRPBF	LTMA	5-Lead Plastic TSOT-23	0°C to 70°C
LT1395CS6#PBF	LT1395CS6#TRPBF	LTMF	6-Lead Plastic TSOT-23	0°C to 70°C
LT1395CS8#PBF	LT1395CS8#TRPBF	1395	8-Lead Plastic SO	0°C to 70°C
LT1396CS8#PBF	LT1396CS8#TRPBF	1396	8-Lead Plastic SO	0°C to 70°C
LEAD BASED FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1396CDD	LT1396CDD#TR	LABD	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT1397CDE	LT1397CDE#TR	1397	14-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LT1397HDE	LT1397HDE#TR	1397	14-Lead (4mm × 3mm) Plastic DFN	-40°C to 125°C
LT1397CGN	LT1397CGN#TR	1397	16-Lead Plastic SSOP	0°C to 70°C
LT1396CMS8	LT1396CMS8#TR	LTDY	8-Lead Plastic MSOP	0°C to 70°C
LT1397CS	LT1397CS#TR	1397CS	14-Lead Plastic SO	0°C to 70°C
LT1395CS5	LT1395CS5#TR	LTMA	5-Lead Plastic TSOT-23	0°C to 70°C
LT1395CS6	LT1395CS6#TR	LTMF	6-Lead Plastic TSOT-23	0°C to 70°C
LT1395CS8	LT1395CS8#TR	1395	8-Lead Plastic SO	0°C to 70°C
LT1396CS8	LT1396CS8#TR	1396	8-Lead Plastic SO	0°C to 70°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. Consult LTC Marketing for information on nonstandard lead based finish parts.

*Temperature grades are identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the specified operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$.
For each amplifier: $V_{CM} = 0\text{V}$, $V_S = \pm 5\text{V}$, $\overline{EN} = 0.5\text{V}$, pulse tested, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●	1	± 10 ± 12	mV mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift		●	15		$\mu\text{V}/^\circ\text{C}$
I_{IN}^+	Noninverting Input Current		●	10	± 25 ± 30	μA μA
I_{IN}^-	Inverting Input Current		●	10	± 50 ± 60	μA μA
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$, $R_F = 1\text{k}$, $R_G = 10\Omega$, $R_S = 0\Omega$		4.5		$\text{nV}/\sqrt{\text{Hz}}$
$+i_n$	Noninverting Input Noise Current Density	$f = 1\text{kHz}$		6		$\text{pA}/\sqrt{\text{Hz}}$
$-i_n$	Inverting Input Noise Current Density	$f = 1\text{kHz}$		25		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	$V_{IN} = \pm 3.5\text{V}$	●	0.3	1	$\text{M}\Omega$
C_{IN}	Input Capacitance			2.0		pF
V_{INH}	Input Voltage Range, High	$V_S = \pm 5\text{V}$ $V_S = 5\text{V}$, 0V	●	3.5	4.0 4.0	V V
V_{INL}	Input Voltage Range, Low	$V_S = \pm 5\text{V}$ $V_S = 5\text{V}$, 0V	●		-4.0 1.0	V V
V_{OUTH}	Output Voltage Swing, High	$V_S = \pm 5\text{V}$ $V_S = \pm 5\text{V}$ $V_S = 5\text{V}$, 0V	●	3.9 3.7	4.2 4.2	V V V
V_{OUTL}	Output Voltage Swing, Low	$V_S = \pm 5\text{V}$ $V_S = \pm 5\text{V}$ $V_S = 5\text{V}$, 0V	●		-4.2 -3.9 -3.7 0.8	V V V V
V_{OUTH}	Output Voltage Swing, High	$V_S = \pm 5\text{V}$, $R_L = 150\Omega$ $V_S = \pm 5\text{V}$, $R_L = 150\Omega$ $V_S = 5\text{V}$, 0V ; $R_L = 150\Omega$	●	3.4 3.2	3.6 3.6	V V V
V_{OUTL}	Output Voltage Swing, Low	$V_S = \pm 5\text{V}$, $R_L = 150\Omega$ $V_S = \pm 5\text{V}$, $R_L = 150\Omega$ $V_S = 5\text{V}$, 0V ; $R_L = 150\Omega$	●		-3.6 -3.4 -3.2 0.6	V V V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 3.5\text{V}$	●	42	52	dB
$-I_{CMRR}$	Inverting Input Current Common Mode Rejection	$V_{CM} = \pm 3.5\text{V}$ $V_{CM} = \pm 3.5\text{V}$	●	10	16 22	$\mu\text{A}/\text{V}$ $\mu\text{A}/\text{V}$
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2\text{V}$ to $\pm 5\text{V}$	●	56	70	dB
$+I_{PSRR}$	Noninverting Input Current Power Supply Rejection	$V_S = \pm 2\text{V}$ to $\pm 5\text{V}$	●	1	2 3	$\mu\text{A}/\text{V}$ $\mu\text{A}/\text{V}$
$-I_{PSRR}$	Inverting Input Current Power Supply Rejection	$V_S = \pm 2\text{V}$ to $\pm 5\text{V}$	●	2	7	$\mu\text{A}/\text{V}$
A_V	Large-Signal Voltage Gain	$V_{OUT} = \pm 2\text{V}$, $R_L = 150\Omega$		50	65	dB
R_{OL}	Transimpedance, $\Delta V_{OUT}/\Delta I_{IN}^-$	$V_{OUT} = \pm 2\text{V}$, $R_L = 150\Omega$		40	100	$\text{k}\Omega$
I_{OUT}	Maximum Output Current	$R_L = 0\Omega$	●	80		mA
I_S	Supply Current per Amplifier	$V_{OUT} = 0\text{V}$	●	4.6	6.5	mA
	Disable Supply Current	$\overline{EN}$ Pin Voltage = 4.5V , $R_L = 150\Omega$ (LT1395CS6 only)	●	0.1	100	μA
I_{EN}	Enable Pin Current	(LT1395CS6 only)	●	30	110 200	μA μA
SR	Slew Rate (Note 7)	$A_V = -1$, $R_L = 150\Omega$		500	800	$\text{V}/\mu\text{s}$

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the specified operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. For each amplifier: $V_{CM} = 0\text{V}$, $V_S = \pm 5\text{V}$, pulse tested, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{ON}	Turn-On Delay Time (Note 9)	$R_F = R_G = 255\Omega$, $R_L = 100\Omega$, (LT1395CS6 only)		30	75	ns
t_{OFF}	Turn-Off Delay Time (Note 9)	$R_F = R_G = 255\Omega$, $R_L = 100\Omega$, (LT1395CS6 only)		40	100	ns
–3dB BW	–3dB Bandwidth	$A_V = 1$, $R_F = 374\Omega$, $R_L = 100\Omega$ $A_V = 2$, $R_F = R_G = 255\Omega$, $R_L = 100\Omega$		400 350		MHz MHz
0.1dB BW	0.1dB Bandwidth	$A_V = 1$, $R_F = 374\Omega$, $R_L = 100\Omega$ $A_V = 2$, $R_F = R_G = 255\Omega$, $R_L = 100\Omega$		100 100		MHz MHz
t_r , t_f	Small-Signal Rise and Fall Time	$R_F = R_G = 255\Omega$, $R_L = 100\Omega$, $V_{OUT} = 1V_{P-P}$		1.3		ns
t_{PD}	Propagation Delay	$R_F = R_G = 255\Omega$, $R_L = 100\Omega$, $V_{OUT} = 1V_{P-P}$		2.5		ns
os	Small-Signal Overshoot	$R_F = R_G = 255\Omega$, $R_L = 100\Omega$, $V_{OUT} = 1V_{P-P}$		10		%
t_S	Settling Time	0.1%, $A_V = -1$, $R_F = R_G = 280\Omega$, $R_L = 150\Omega$		25		ns
dG	Differential Gain (Note 8)	$R_F = R_G = 255\Omega$, $R_L = 150\Omega$		0.02		%
dP	Differential Phase (Note 8)	$R_F = R_G = 255\Omega$, $R_L = 150\Omega$		0.04		DEG

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This parameter is guaranteed to meet specified performance through design and characterization. It has not been tested.

Note 3: A heat sink may be required depending on the power supply voltage and how many amplifiers have their outputs short circuited. The θ_{JA} specified for the DD package is with minimal PCB heat spreading metal. Using expanded metal area on all layers of a board reduces this value.

Note 4: The LT1395C/LT1396C/LT1397C are guaranteed functional over the operating temperature range of -40°C to 85°C . The LT1397H is guaranteed functional over the operating temperature range of -40°C to 125°C .

Note 5: The LT1395C/LT1396C/LT1397C are guaranteed to meet specified performance from 0°C to 70°C . The LT1395C/LT1396C/LT1397C are designed, characterized and expected to meet specified performance from -40°C and 85°C but are not tested or QA sampled at these temperatures. The LT1397H is guaranteed to meet specified performance from -40°C to 125°C . For guaranteed I-grade parts, consult the factory.

Note 6: T_J is calculated from the ambient temperature T_A and the power dissipation P_D according to the following formula:

$$\text{LT1395CS5: } T_J = T_A + (P_D \cdot 250^\circ\text{C/W})$$

$$\text{LT1396CS6: } T_J = T_A + (P_D \cdot 230^\circ\text{C/W})$$

$$\text{LT1395CS8: } T_J = T_A + (P_D \cdot 150^\circ\text{C/W})$$

$$\text{LT1396CS8: } T_J = T_A + (P_D \cdot 150^\circ\text{C/W})$$

$$\text{LT1396CMS8: } T_J = T_A + (P_D \cdot 250^\circ\text{C/W})$$

$$\text{LT1396CDD: } T_J = T_A + (P_D \cdot 160^\circ\text{C/W})$$

$$\text{LT1397CS14: } T_J = T_A + (P_D \cdot 100^\circ\text{C/W})$$

$$\text{LT1397CGN16: } T_J = T_A + (P_D \cdot 135^\circ\text{C/W})$$

$$\text{LT1397CDE: } T_J = T_A + (P_D \cdot 43^\circ\text{C/W})$$

$$\text{LT1397HDE: } T_J = T_A + (P_D \cdot 43^\circ\text{C/W})$$

Note 7: Slew rate is measured at $\pm 2\text{V}$ on a $\pm 3\text{V}$ output signal.

Note 8: Differential gain and phase are measured using a Tektronix TSG120YC/NTSC signal generator and a Tektronix 1780R Video Measurement Set. The resolution of this equipment is 0.1% and 0.1°. Ten identical amplifier stages were cascaded giving an effective resolution of 0.01% and 0.01°.

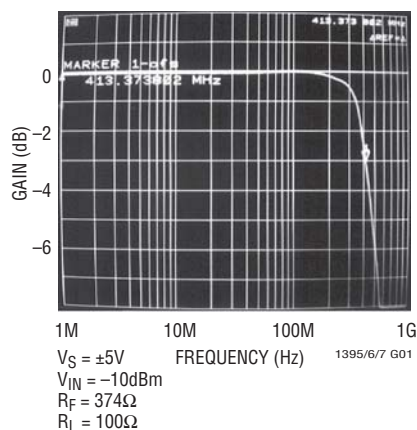
Note 9: For LT1395CS6, turn-on delay time (t_{ON}) is measured from control input to appearance of 1V(50%) at the output, for $V_{IN} = 1\text{V}$ and $A_V = 2$. Likewise, turn-off delay time (t_{OFF}) is measured from control input to appearance of 1V(50%) on the output for $V_{IN} = 1\text{V}$ and $A_V = 2$. This specification is guaranteed by design and characterization.

TYPICAL AC PERFORMANCE

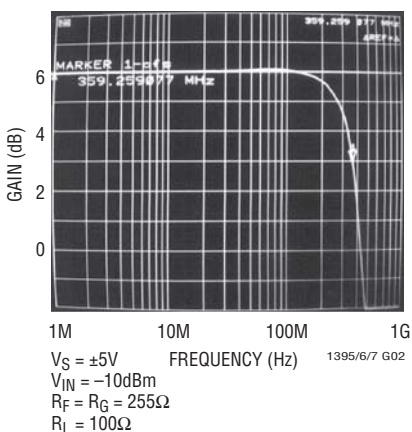
V_S (V)	A_V	R_L (Ω)	R_F (Ω)	R_G (Ω)	SMALL SIGNAL -3dB BW (MHz)	SMALL SIGNAL 0.1dB BW (MHz)	SMALL SIGNAL PEAKING (dB)
± 5	1	100	374	—	400	100	0.1
± 5	2	100	255	255	350	100	0.1
± 5	-1	100	280	280	350	100	0.1
± 5	3	500	221	110	300	100	0.1
± 5	5	500	100	24.9	210	50	0.0
± 5	10	500	90.9	10	65	10	0.0
± 5	10	500	90.9	10 Ω 100pF	100	50	0.1

TYPICAL PERFORMANCE CHARACTERISTICS

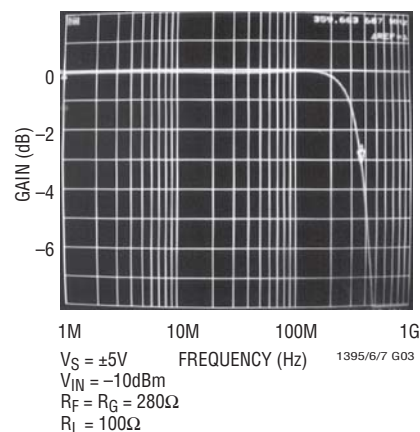
Closed-Loop Gain vs Frequency
($A_V = 1$)



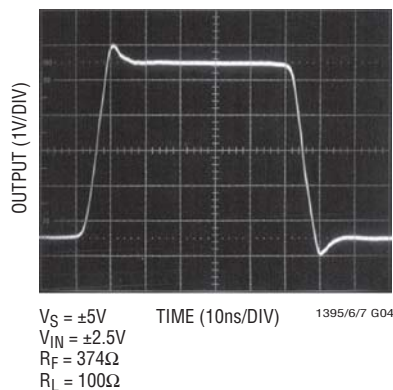
Closed-Loop Gain vs Frequency
($A_V = 2$)



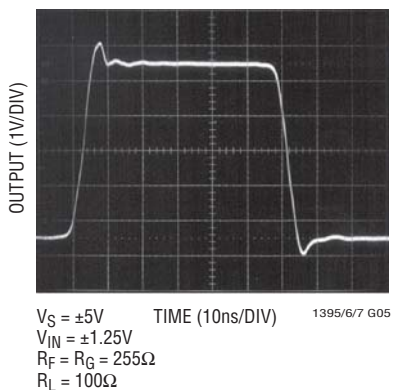
Closed-Loop Gain vs Frequency
($A_V = -1$)



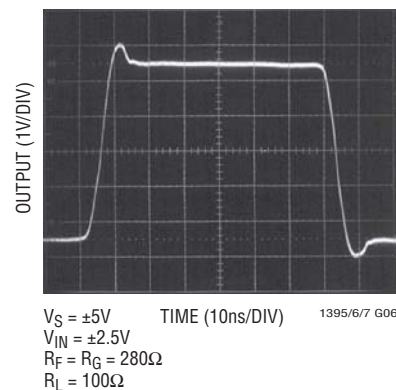
Large-Signal Transient Response
($A_V = 1$)



Large-Signal Transient Response
($A_V = 2$)

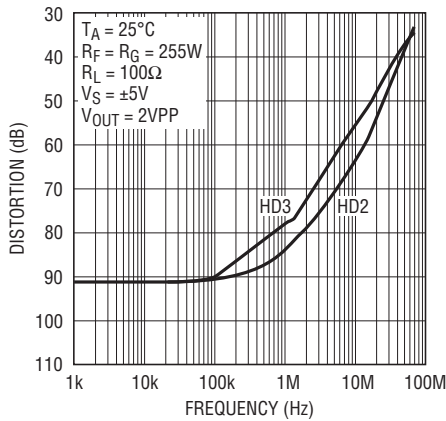


Large-Signal Transient Response
($A_V = -1$)

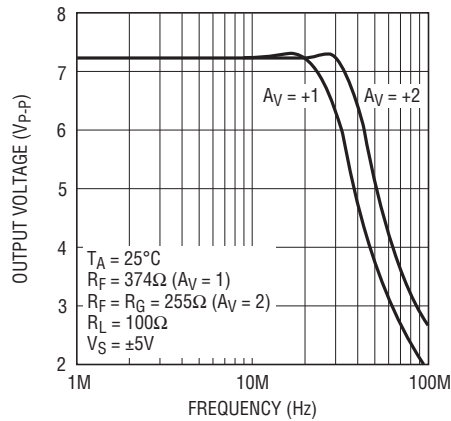


TYPICAL PERFORMANCE CHARACTERISTICS

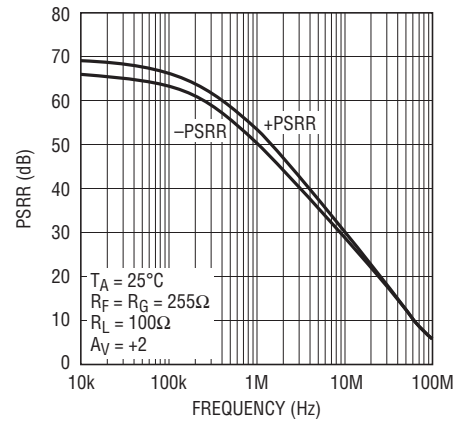
2nd and 3rd Harmonic Distortion vs Frequency



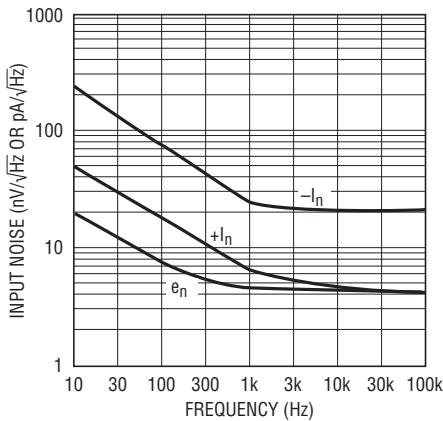
Maximum Undistorted Output Voltage vs Frequency



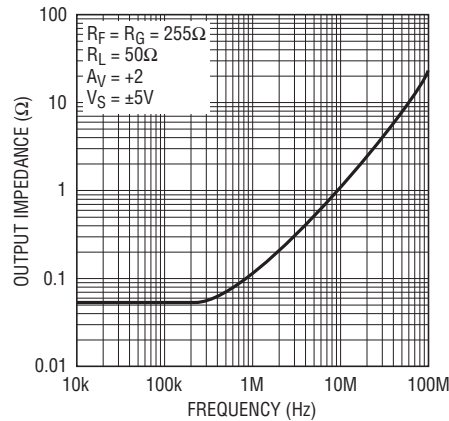
PSRR vs Frequency



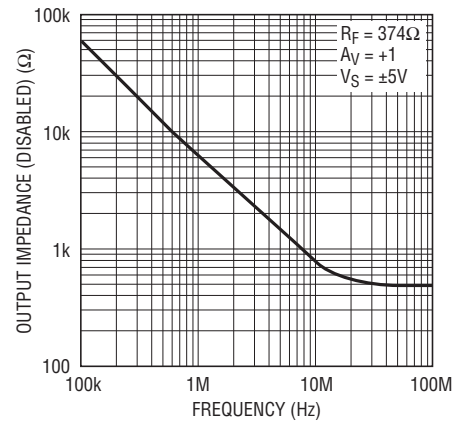
Input Voltage Noise and Current Noise vs Frequency



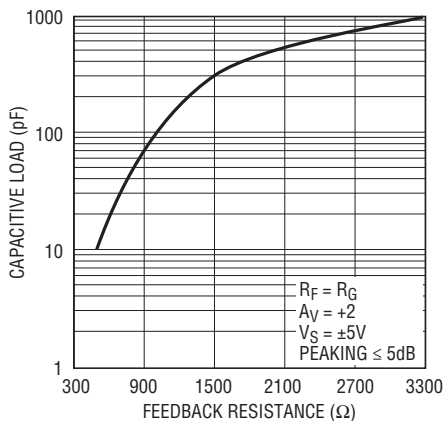
Output Impedance vs Frequency



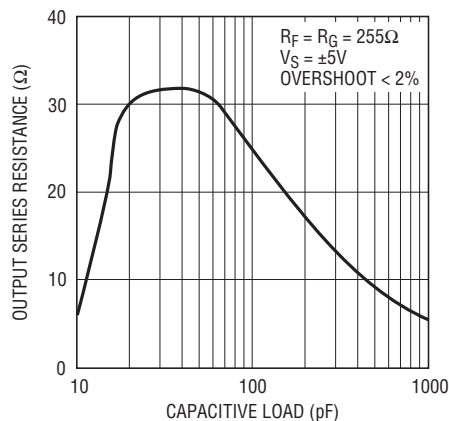
LT1395CS6 Output Impedance (Disabled) vs Frequency



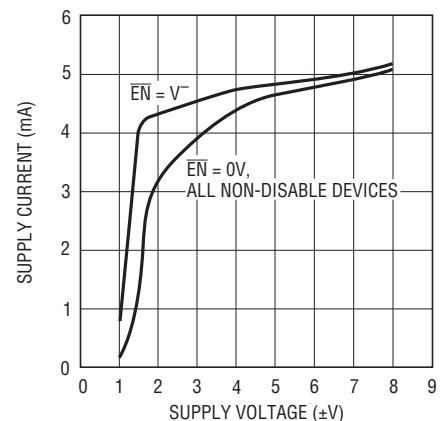
Maximum Capacitive Load vs Feedback Resistor



Capacitive Load vs Output Series Resistor

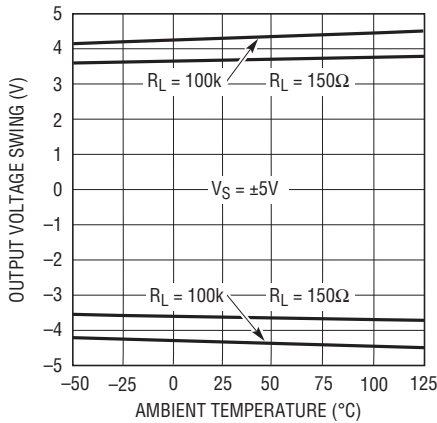


Supply Current vs Supply Voltage

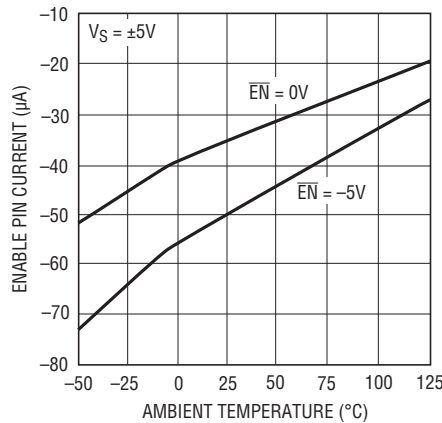


TYPICAL PERFORMANCE CHARACTERISTICS

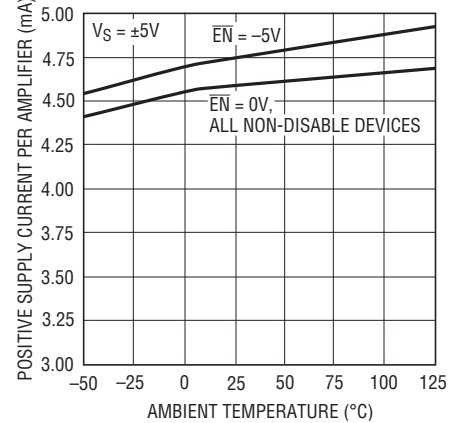
Output Voltage Swing vs Temperature



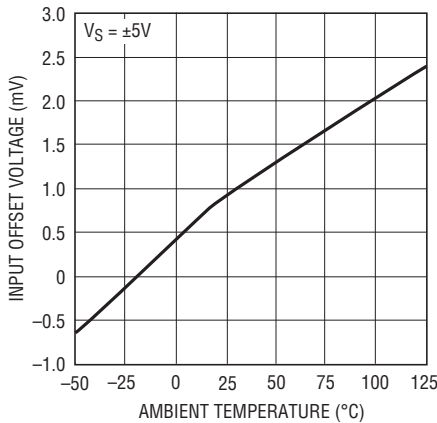
LT1395CS6 Enable Pin Current vs Temperature



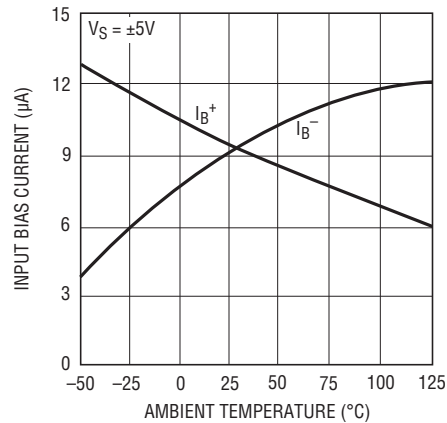
Positive Supply Current per Amplifier vs Temperature



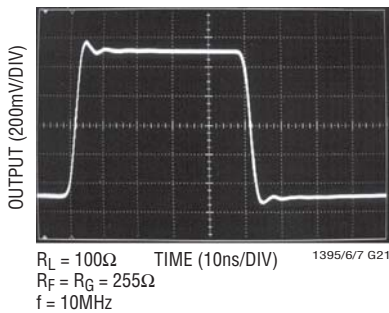
Input Offset Voltage vs Temperature



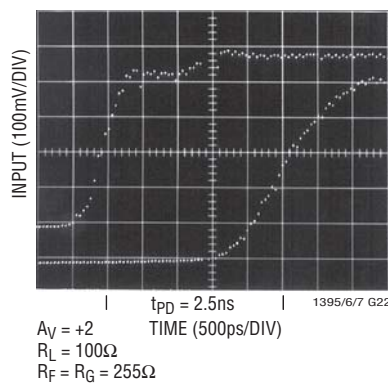
Input Bias Currents vs Temperature



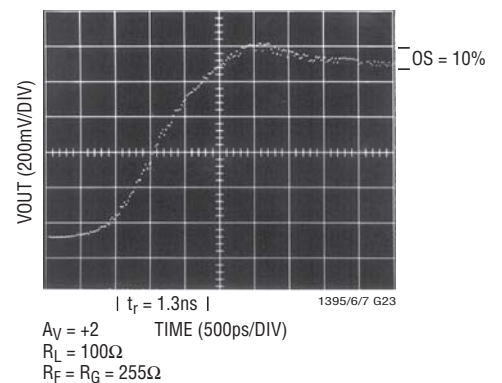
Square Wave Response



Propagation Delay



Rise Time and Overshoot



PIN FUNCTIONS

LT1395CS5

OUT (Pin 1): Output.

V⁻ (Pin 2): Negative Supply Voltage, Usually -5V.

+IN (Pin 3): Noninverting Input.

-IN (Pin 4): Inverting Input.

V⁺ (Pin 5): Positive Supply Voltage, Usually 5V.

LT1395CS6

OUT (Pin 1): Output.

V⁻ (Pin 2): Negative Supply Voltage, Usually -5V.

+IN (Pin 3): Noninverting Input.

-IN (Pin 4): Inverting Input.

$\overline{\text{EN}}$ (Pin 5): Enable Pin. Logic low to enable.

V⁺ (Pin 6): Positive Supply Voltage, Usually 5V.

LT1395CS8

NC (Pin 1): No Connection.

-IN (Pin 2): Inverting Input.

+IN (Pin 3): Noninverting Input.

V⁻ (Pin 4): Negative Supply Voltage, Usually -5V.

NC (Pin 5): No Connection.

OUT (Pin 6): Output.

V⁺ (Pin 7): Positive Supply Voltage, Usually 5V.

NC (Pin 8): No Connection.

LT1396CMS8, LT1396CS8, LT1396CDD

OUT A (Pin 1): A Channel Output.

-IN A (Pin 2): Inverting Input of A Channel Amplifier.

+IN A (Pin 3): Noninverting Input of A Channel Amplifier.

V⁻ (Pin 4): Negative Supply Voltage, Usually -5V.

+IN B (Pin 5): Noninverting Input of B Channel Amplifier.

-IN B (Pin 6): Inverting Input of B Channel Amplifier.

OUT B (Pin 7): B Channel Output.

V⁺ (Pin 8): Positive Supply Voltage, Usually 5V.

LT1397CS, LT1397CDE, LT1397HDE

OUT A (Pin 1): A Channel Output.

-IN A (Pin 2): Inverting Input of A Channel Amplifier.

+IN A (Pin 3): Noninverting Input of A Channel Amplifier.

V⁺ (Pin 4): Positive Supply Voltage, Usually 5V.

+IN B (Pin 5): Noninverting Input of B Channel Amplifier.

-IN B (Pin 6): Inverting Input of B Channel Amplifier.

OUT B (Pin 7): B Channel Output.

OUT C (Pin 8): C Channel Output.

-IN C (Pin 9): Inverting Input of C Channel Amplifier.

+IN C (Pin 10): Noninverting Input of C Channel Amplifier.

V⁻ (Pin 11): Negative Supply Voltage, Usually -5V.

+IN D (Pin 12): Noninverting Input of D Channel Amplifier.

-IN D (Pin 13): Inverting Input of D Channel Amplifier.

OUT D (Pin 14): D Channel Output.

LT1397CGN

OUT A (Pin 1): A Channel Output.

-IN A (Pin 2): Inverting Input of A Channel Amplifier.

+IN A (Pin 3): Noninverting Input of A Channel Amplifier.

V⁺ (Pin 4): Positive Supply Voltage, Usually 5V.

+IN B (Pin 5): Noninverting Input of B Channel Amplifier.

-IN B (Pin 6): Inverting Input of B Channel Amplifier.

OUT B (Pin 7): B Channel Output.

NC (Pin 8): No Connection.

NC (Pin 9): No Connection.

OUT C (Pin 10): C Channel Output.

-IN C (Pin 11): Inverting Input of C Channel Amplifier.

+IN C (Pin 12): Noninverting Input of C Channel Amplifier.

V⁻ (Pin 13): Negative Supply Voltage, Usually -5V.

+IN D (Pin 14): Noninverting Input of D Channel Amplifier.

-IN D (Pin 15): Inverting Input of D Channel Amplifier.

OUT D (Pin 16): D Channel Output.

APPLICATIONS INFORMATION

Feedback Resistor Selection

The small-signal bandwidth of the LT1395/LT1396/LT1397 is set by the external feedback resistors and the internal junction capacitors. As a result, the bandwidth is a function of the supply voltage, the value of the feedback resistor, the closed-loop gain and the load resistor. The LT1395/LT1396/LT1397 have been optimized for $\pm 5V$ supply operation and have a $-3dB$ bandwidth of 400MHz at a gain of 1 and 350MHz at a gain of 2. Please refer to the resistor selection guide in the Typical AC Performance table.

Capacitance on the Inverting Input

Current feedback amplifiers require resistive feedback from the output to the inverting input for stable operation. Take care to minimize the stray capacitance between the output and the inverting input. Capacitance on the inverting input to ground will cause peaking in the frequency response (and overshoot in the transient response).

Capacitive Loads

The LT1395/LT1396/LT1397 can drive many capacitive loads directly when the proper value of feedback resistor is used. The required value for the feedback resistor will increase as load capacitance increases and as closed-loop gain decreases. Alternatively, a small resistor (5Ω to 35Ω) can be put in series with the output to isolate the capacitive load from the amplifier output. This has the advantage that the amplifier bandwidth is only reduced when the capacitive load is present. The disadvantage is that the gain is a function of the load resistance. See the Typical Performance Characteristics curves.

Power Supplies

The LT1395/LT1396/LT1397 will operate from single or split supplies from $\pm 2V$ (4V total) to $\pm 6V$ (12V total). It is not necessary to use equal value split supplies, however the offset voltage and inverting input bias current will change. The offset voltage changes about 2.5mV per volt of supply mismatch. The inverting bias current will typically change about 10 μA per volt of supply mismatch.

Slew Rate

Unlike a traditional voltage feedback op amp, the slew rate of a current feedback amplifier is not independent of the amplifier gain configuration. In a current feedback amplifier, both the input stage and the output stage have slew rate limitations. In the inverting mode, and for gains of 2 or more in the noninverting mode, the signal amplitude between the input pins is small and the overall slew rate is that of the output stage. For gains less than 2 in the noninverting mode, the overall slew rate is limited by the input stage.

The input slew rate of the LT1395/LT1396/LT1397 is approximately 600V/ μs and is set by internal currents and capacitances. The output slew rate is set by the value of the feedback resistor and internal capacitance. At a gain of 2 with 255 Ω feedback and gain resistors and $\pm 5V$ supplies, the output slew rate is typically 800V/ μs . Larger feedback resistors will reduce the slew rate as will lower supply voltages.

Enable/Disable

The LT1395CS6 has a unique high impedance, zero supply current mode which is controlled by the $\overline{EN}$ pin. The LT1395CS6 is designed to operate with CMOS logic; it draws virtually zero current when the $\overline{EN}$ pin is high. To activate the amplifier, its $\overline{EN}$ pin is normally pulled to a logic low. However, supply current will vary as the voltage between the V^+ supply and $\overline{EN}$ is varied. As seen in Figure 1, $+I_S$ does vary with $(V^+ - V_{\overline{EN}})$, particularly when the voltage difference is less than 3V. For normal

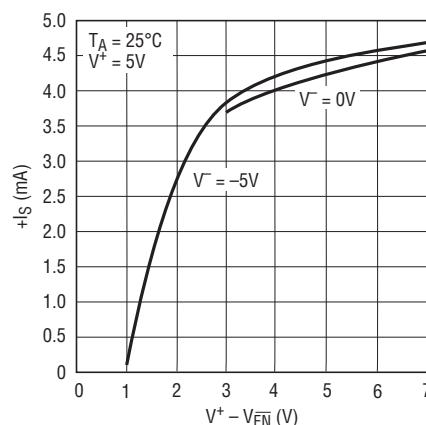


Figure 1. $+I_S$ vs $(V^+ - V_{\overline{EN}})$

1395/6/7 F01

139567fd

APPLICATIONS INFORMATION

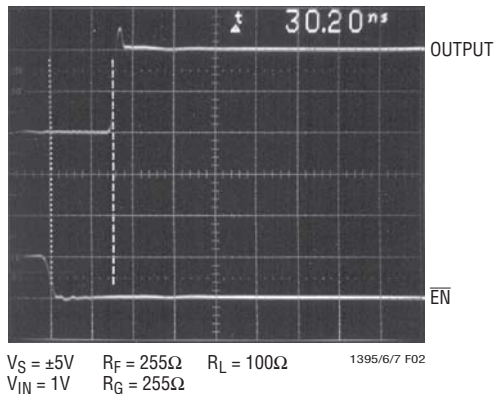


Figure 2. Amplifier Enable Time, $A_V = 2$

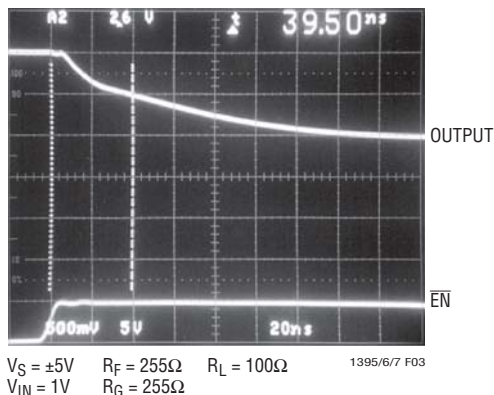


Figure 3. Amplifier Disable Time, $A_V = 2$

operation, it is important to keep the $\overline{\text{EN}}$ pin at least 3V below the V^+ supply. If a V^+ of less than 3V is desired, and the amplifier will remain enabled at all times, then the $\overline{\text{EN}}$ pin should be tied to the V^- supply. The enable pin current is approximately 30 μ A when activated. If using CMOS open-drain logic, an external 1k pull-up resistor is recommended to ensure that the LT1395CS6 remains disabled in spite of any CMOS drain leakage currents.

The enable/disable times are very fast when driven from standard 5V CMOS logic. The LT1395CS6 enables in about 30ns (50% point to 50% point) while operating on ± 5 V supplies (Figure 2). Likewise, the disable time is approximately 40ns (50% point to 50% point) (Figure 3).

Differential Input Signal Swing

To avoid any breakdown condition on the input transistors, the differential input swing must be limited to ± 5 V. In normal operation, the differential voltage between the input pins is small, so the ± 5 V limit is not an issue.

Buffered RGB to Color-Difference Matrix

An LT1397 can be used to create buffered color-difference signals from RGB inputs (Figure 4). In this application, the R input arrives via 75 Ω coax. It is routed to the non-inverting input of LT1397 amplifier A1 and to a 845 Ω resistor R8. There is also an 82.5 Ω termination resistor R11, which yields a 75 Ω input impedance at the R input when considered in parallel with R8. R8 connects to the inverting input of a second LT1397 amplifier (A2), which also sums the weighted G and B inputs to create a $-0.5 \cdot Y$ output. LT1397 amplifier A3 then takes the $-0.5 \cdot Y$ output and amplifies it by a gain of -2 , resulting in the Y output. Amplifier A1 is configured in a noninverting gain of 2 with the bottom of the gain resistor R2 tied to the Y output. The output of amplifier A1 thus results in the color-difference output R-Y.

The B input is similar to the R input. It arrives via 75 Ω coax, and is routed to the noninverting input of LT1397 amplifier A4, and to a 2320 Ω resistor R10. There is also a 76.8 Ω termination resistor R13, which yields a 75 Ω

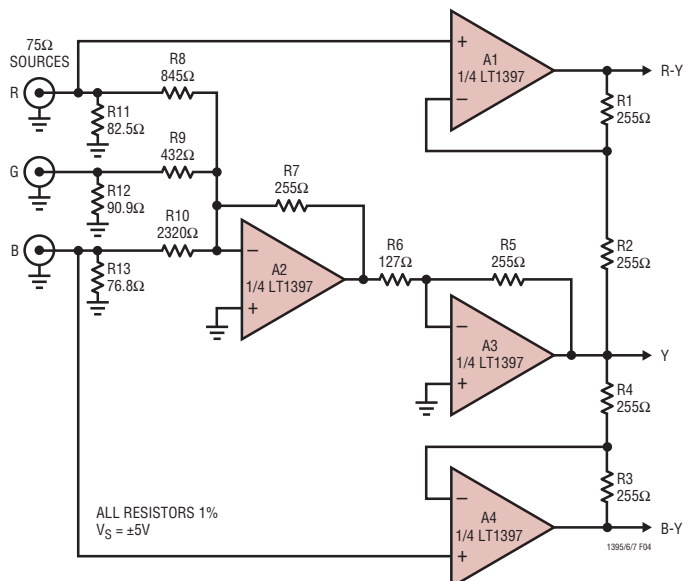


Figure 4. Buffered RGB to Color-Difference Matrix

1395671d

APPLICATIONS INFORMATION

input impedance when considered in parallel with R10. R10 also connects to the inverting input of amplifier A2, adding the B contribution to the Y signal as discussed above. Amplifier A4 is configured in a noninverting gain of 2 configuration with the bottom of the gain resistor R4 tied to the Y output. The output of amplifier A4 thus results in the color-difference output B-Y.

The G input also arrives via 75Ω coax and adds its contribution to the Y signal via a 432Ω resistor R9, which is tied to the inverting input of amplifier A2. There is also a 90.9Ω termination resistor R12, which yields a 75Ω termination when considered in parallel with R9. Using superposition, it is straightforward to determine the output of amplifier A2. Although inverted, it sums the R, G and B signals in the standard proportions of 0.3R, 0.59G and 0.11B that are used to create the Y signal. Amplifier A3 then inverts and amplifies the signal by 2, resulting in the Y output.

Buffered Color-Difference to RGB Matrix

An LT1395 combined with an LT1396 can be used to create buffered RGB outputs from color-difference signals (Figure 5). The R output is a back-terminated 75Ω signal created using resistor R5 and amplifier A1 configured for a gain of +4 via resistors R3 and R4. The noninverting input of amplifier A1 is connected via 1k resistors R1 and R2 to the Y and R-Y inputs respectively, resulting in cancellation of the Y signal at the amplifier input. The remaining R signal is then amplified by A1.

The B output is also a back-terminated 75Ω signal created using resistor R16 and amplifier A3 configured for a gain of +4 via resistors R14 and R15. The noninverting input of amplifier A3 is connected via 1k resistors R12 and R13 to the Y and B-Y inputs respectively, resulting in cancellation of the Y signal at the amplifier input. The remaining B signal is then amplified by A3.

The G output is the most complicated of the three. It is a weighted sum of the Y, R-Y and B-Y inputs. The Y input is attenuated via resistors R6 and R7 such that amplifier A2's noninverting input sees 0.83Y. Using superposition, we can calculate the positive gain of A2 by assuming that

R8 and R9 are grounded. This results in a gain of 2.41 and a contribution at the output of A2 of 2Y. The R-Y input is amplified by A2 with the gain set by resistors R8 and R10, giving an amplification of -1.02. This results in a contribution at the output of A2 of 1.02Y - 1.02R. The B-Y input is amplified by A2 with the gain set by resistors R9 and R10, giving an amplification of -0.37. This results in a contribution at the output of A2 of 0.37Y - 0.37B.

If we now sum the three contributions at the output of A2, we get:

$$A2_{OUT} = 3.40Y - 1.02R - 0.37B$$

It is important to remember though that Y is a weighted sum of R, G and B such that:

$$Y = 0.3R + 0.59G + 0.11B$$

If we substitute for Y at the output of A2 we then get:

$$A2_{OUT} = (1.02R - 1.02R) + 2G + (0.37B - 0.37B) = 2G$$

The back-termination resistor R11 then halves the output of A2 resulting in the G output.

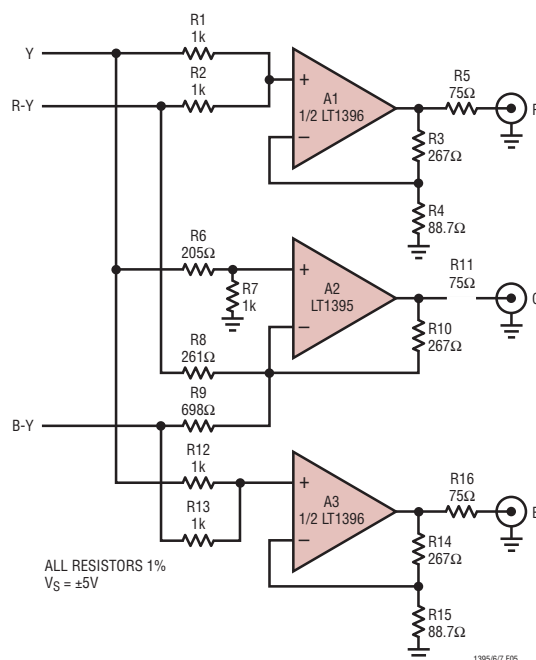
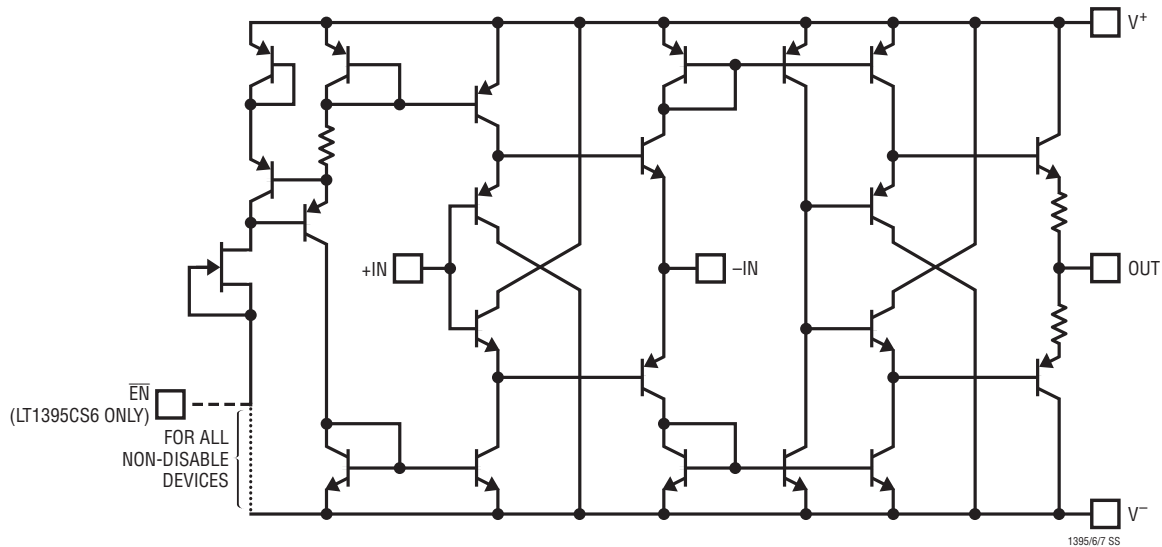


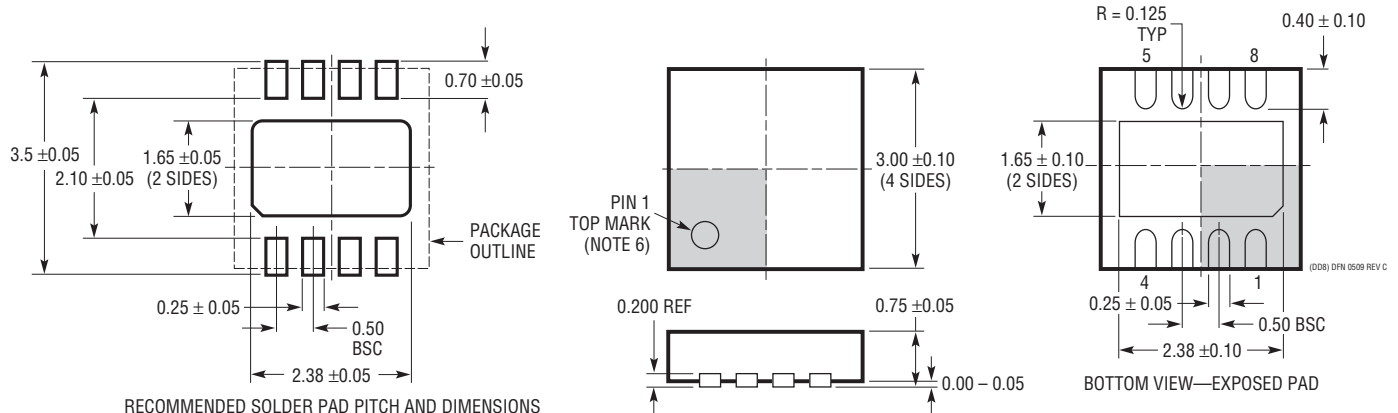
Figure 5. Buffered Color-Difference to RGB Matrix

SIMPLIFIED SCHEMATIC (each amplifier)



PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



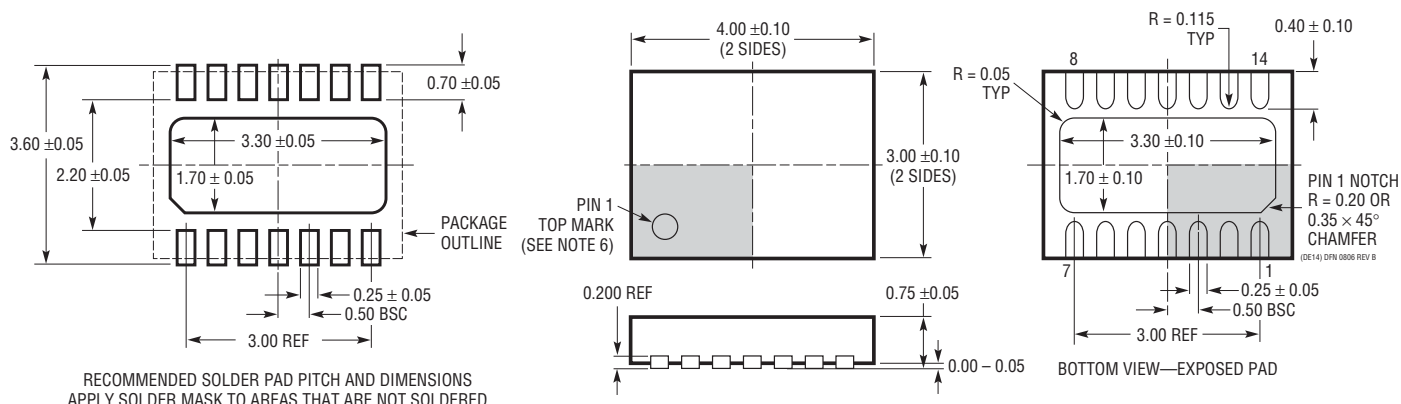
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

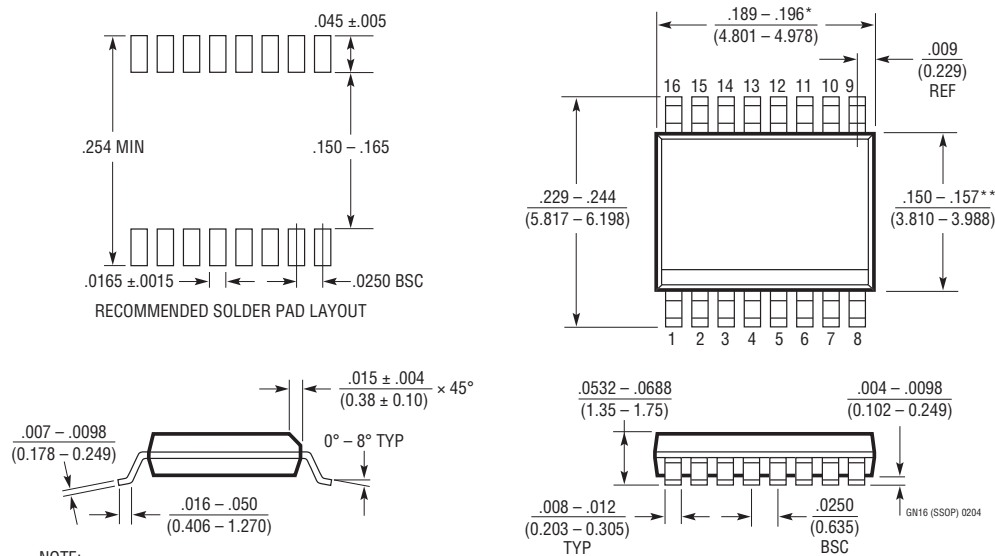
DE Package 14-Lead Plastic DFN (4mm × 3mm) (Reference LTC DWG # 05-08-1708 Rev B)



NOTE:

1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



NOTE:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN INCHES (MILLIMETERS)
3. DRAWING NOT TO SCALE

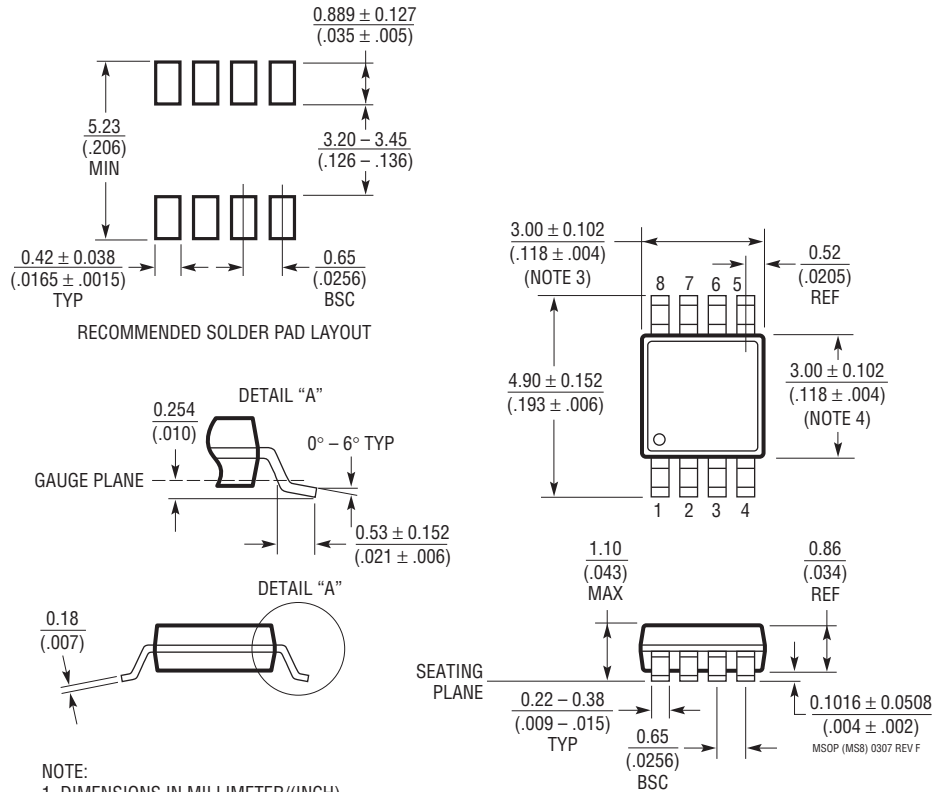
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

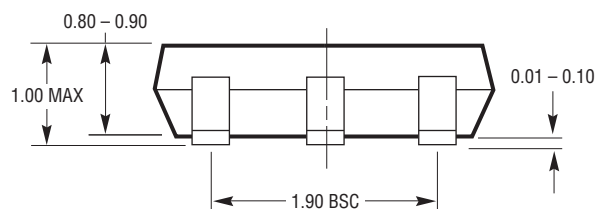
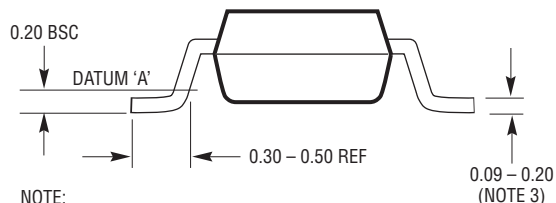
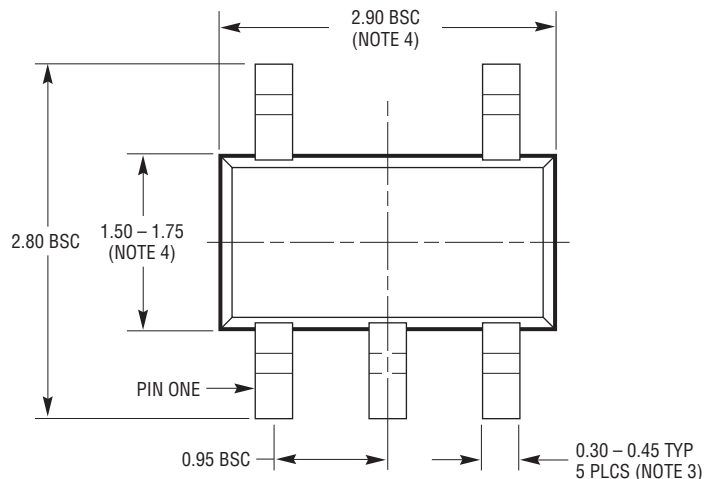
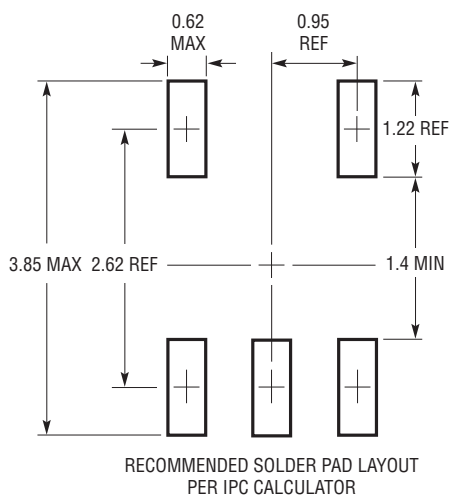
MS8 Package 8-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1660 Rev F)



PACKAGE DESCRIPTION

S5 Package
5-Lead Plastic TSOT-23
 (Reference LTC DWG # 05-08-1633)

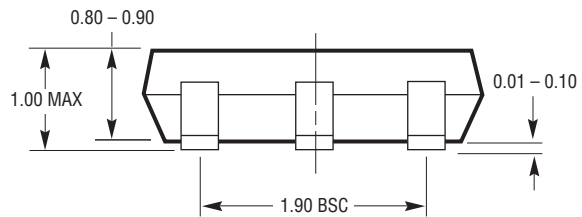
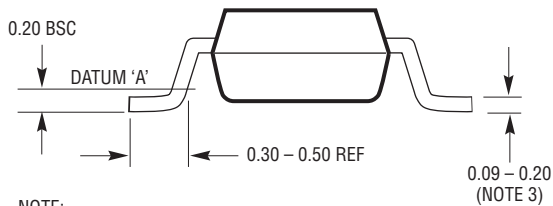
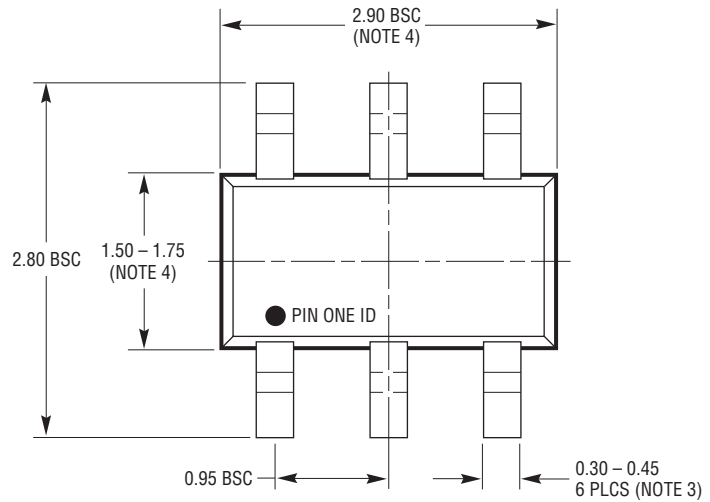
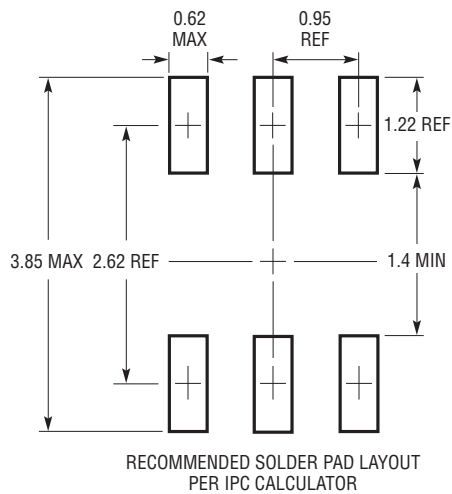


- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
 2. DRAWING NOT TO SCALE
 3. DIMENSIONS ARE INCLUSIVE OF PLATING
 4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
 5. MOLD FLASH SHALL NOT EXCEED 0.254mm
 6. JEDEC PACKAGE REFERENCE IS MO-193

S5 TSOT-23 0302 REV B

PACKAGE DESCRIPTION

S6 Package
6-Lead Plastic TSOT-23
 (Reference LTC DWG # 05-08-1634)

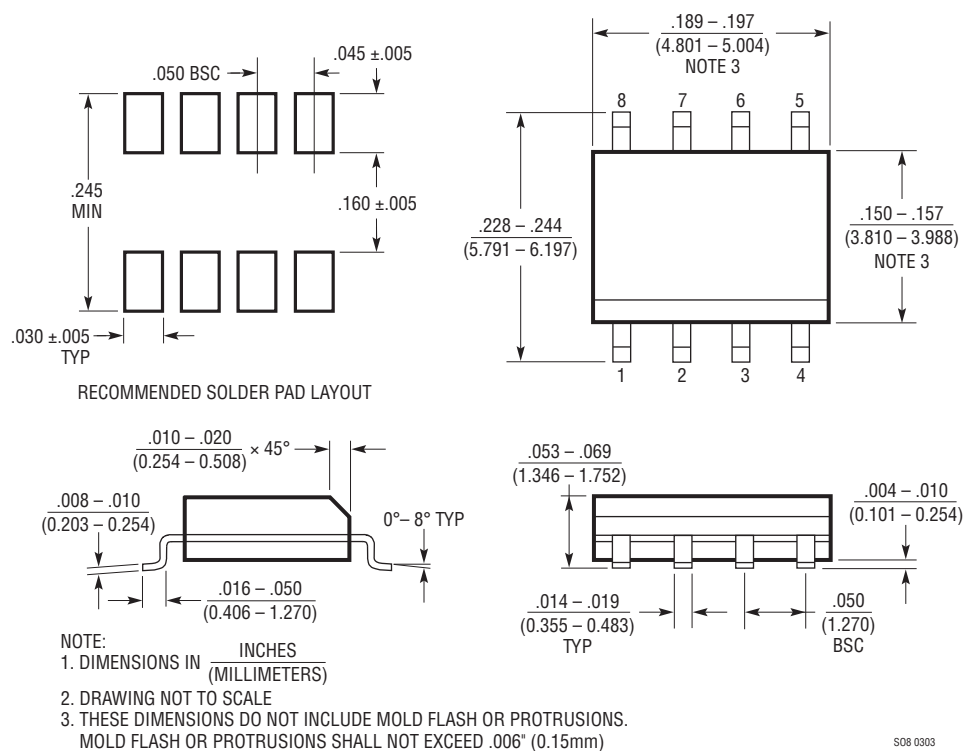


- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
 2. DRAWING NOT TO SCALE
 3. DIMENSIONS ARE INCLUSIVE OF PLATING
 4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
 5. MOLD FLASH SHALL NOT EXCEED 0.254mm
 6. JEDEC PACKAGE REFERENCE IS MO-193

S6 TSOT-23 0302 REV B

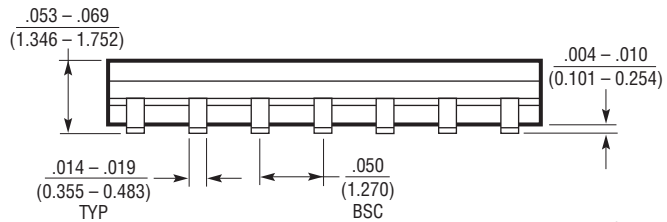
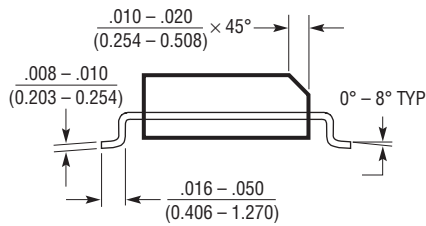
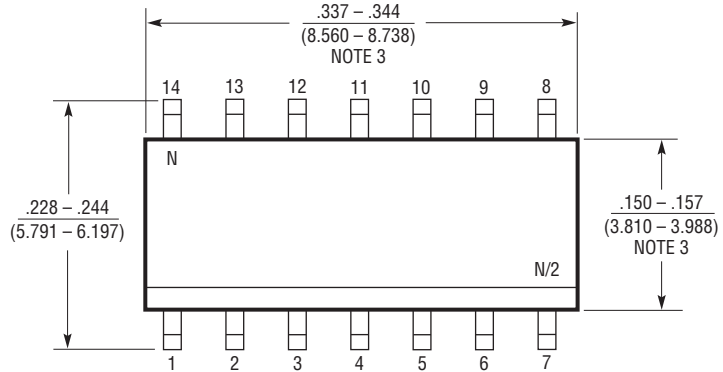
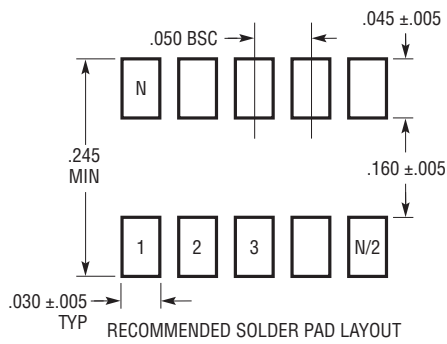
PACKAGE DESCRIPTION

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



PACKAGE DESCRIPTION

S Package 14-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



- NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S14 0502

TYPICAL APPLICATION

Single Supply RGB Video Amplifier

The LT1395 can be used with a single supply voltage of 6V or more to drive ground-referenced RGB video. In Figure 6, two 1N4148 diodes D1 and D2 have been placed in series with the output of the LT1395 amplifier A1 but within the feedback loop formed by resistor R8. These diodes effectively level-shift A1's output downward by 2 diodes, allowing the circuit output to swing to ground.

Amplifier A1 is used in a positive gain configuration. The feedback resistor R8 is 255Ω. The gain resistor is created from the parallel combination of R6 and R7, giving a Thevenin equivalent 63.5Ω connected to 3.75V. This gives an AC gain of +5 from the noninverting input of amplifier A1 to the cathode of D2. However, the video input is also attenuated before arriving at A1's positive

input. Assuming a 75Ω source impedance for the signal driving V_{IN} , the Thevenin equivalent signal arriving at A1's positive input is $3V + 0.4V_{IN}$, with a source impedance of 714Ω. The combination of these two inputs gives an output at the cathode of D2 of $2 \cdot V_{IN}$ with no additional DC offset. The 75Ω back termination resistor R9 halves the signal again such that V_{OUT} equals a buffered version of V_{IN} .

It is important to note that the 4.7μF capacitor C1 has been added to provide enough current to maintain the voltage drop across diodes D1 and D2 when the circuit output drops low enough that the diodes might otherwise turn off. This means that this circuit works fine for continuous video input, but will require that C1 charge up after a period of inactivity at the input.

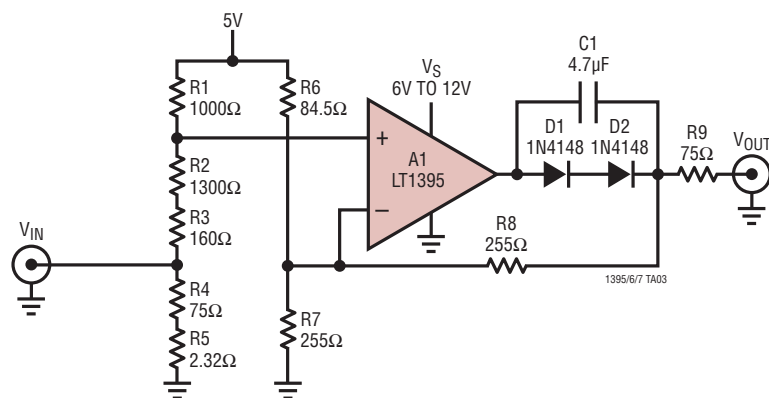


Figure 6. Single Supply RGB Video Amplifier (1 of 4 Channels)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1227/LT1229/LT1230	140MHz Single/Dual/Quad Current Feedback Amplifier	1100V/μs Slew Rate, Single Adds Shutdown Pin
LT1252/LT1253/LT1254	Low Cost Video Amplifiers	Single, Dual and Quad 100MHz Current Feedback Amplifiers
LT1363/LT1364/LT1365	70MHz Single/Dual/Quad Op Amps	1000V/μs Slew Rate, Voltage Feedback
LT1398/LT1399	Dual/Triple Current Feedback Amplifiers	300MHz Bandwidth, 0.1dB Flatness > 150MHz with Shutdown
LT1675	Triple 2:1 Buffered Video Multiplexer	2.5ns Switching Time, 250MHz Bandwidth
LT6559	Low Cost Triple Current Feedback Amplifiers	300MHz Bandwidth, Specified at +5V and ±5V, 3mm × 3mm QFN Package