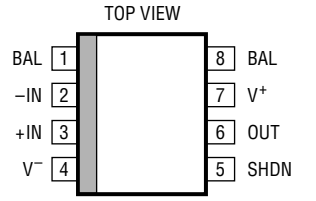
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 18V
Differential Input Voltage ..... ±6V
Input Voltage ..... $\pm V_S$
Output Short-Circuit Duration (Note 2) ..... Continuous
Operating Temperature Range
LT1191M **(OBSOLETE)** ..... –55°C to 125°C
LT1191C ..... 0°C to 70°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S8)

J8 PACKAGE 8-LEAD CERDIP
T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1191CN8 LT1191CS8
S8 PART MARKING
1191
LT1191MJ8 LT1191CJ8

OBSOLETE PACKAGE
Consider the N8 or S8 Packages for Alternate Source

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_S = ±5V, T_A = 25°C, $C_L \leq$ 10pF, Pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER		CONDITIONS	LT1191M/C MIN	LT1191M/C TYP	LT1191M/C MAX	UNITS
V_{OS}	Input Offset Voltage		N8 Package SO-8 Package		1	5 9	mV mV
I_{OS}	Input Offset Current				0.2	1.7	µA
I_B	Input Bias Current				±0.5	±2.5	µA
e_n	Input Noise Voltage		f_O = 10kHz		25		nV/√Hz
i_n	Input Noise Current		f_O = 10kHz		4		pA/√Hz
R_{IN}	Input Resistance	Differential Mode			70		kΩ
		Common Mode			5		MΩ
C_{IN}	Input Capacitance		A_V = +1		2		pF
	Input Voltage Range		(Note 3)	–2.5		3.5	V
CMRR	Common Mode Rejection Ratio		V_{CM} = – 2.5V to 3.5V	60	75		dB
PSRR	Power Supply Rejection Ratio		V_S = ±2.375V to ±8V	60	75		dB
A_{VOL}	Large-Signal Voltage Gain		R_L = 1k, V_O = ±3V R_L = 100Ω, V_O = ±3V V_S = ±8V, R_L = 100Ω, V_O = ±5V	20 4 6	45 9 12		V/mV V/mV V/mV
V_{OUT}	Output Voltage Swing		V_S = ±5V, R_L = 1k V_S = ±8V, R_L = 1k	±3.7 ±6.7	±4 ±7		V V
SR	Slew Rate		A_V = –2, R_L = 1k (Notes 4, 9)	325	450		V/µs
FPBW	Full-Power Bandwidth		V_O = $6V_{P-P}$ (Note 5)	17.2	23.9		MHz
GBW	Gain Bandwidth Product				90		MHz
t_{r1}, t_{f1}	Rise Time, Fall Time		A_V = 50, V_O = ±1.5V, 20% to 80% (Note 9)	100	130	160	ns
t_{r2}, t_{f2}	Rise Time, Fall Time		A_V = 1, V_O = ±125mV, 10% to 90%		1.25		ns
t_{PD}	Propagation Delay		A_V = 1, V_O = ±125mV, 50% to 50%		2.2		ns
	Overshoot		A_V = 1, V_O = ±125mV		25		%
t_s	Settling Time		3V Step, 0.1% (Note 6)		110		ns

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $T_A = 25°C$, $C_L \leq 10pF$, Pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1191M/C MIN	TYP	MAX	UNITS
Diff A_V	Differential Gain	$R_L = 150\Omega$, $A_V = 2$ (Note 7)		0.15		%
Diff Ph	Differential Phase	$R_L = 150\Omega$, $A_V = 2$ (Note 7)		0.09		Deg_{P-P}
I_S	Supply Current			32	38	mA
	Shutdown Supply Current	Pin 5 at V^-		1.3	2	mA
I_{SHDN}	Shutdown Pin Current	Pin 5 at V^-		20	50	µA
t_{ON}	Turn On Time	Pin 5 from V^- to Ground, $R_L = 1k$		100		ns
t_{OFF}	Turn Off Time	Pin 5 from Ground to V^-, $R_L = 1k$		400		ns

$V_S^+ = 5V$, $V_S^- = 0V$, $V_{CM} = 2.5V$, $T_A = 25°C$, $C_L \leq 10pF$, Pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1191M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	N8 Package SO-8 Package			2	7 9	mV mV
I_{OS}	Input Offset Current				0.2	1.2	µA
I_B	Input Bias Current				±0.5	±1.5	µA
	Input Voltage Range	(Note 3)		2		3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = 2V$ to 3.5V		55	70		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L = 100\Omega$ to Ground, $V_O = 1V$ to 3V		5	9		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 100\Omega$ to Ground	V_{OUT} High	3.6	3.8		V
			V_{OUT} Low		0.25	0.4	V
SR	Slew Rate	$A_V = -1$, $V_O = 1V$ to 3V			250		V/µs
GBW	Gain Bandwidth Product				80		MHz
I_S	Supply Current				29	36	mA
	Shutdown Supply Current	Pin 5 at V^-			1.2	2	mA
I_{SHDN}	Shutdown Pin Current	Pin 5 at V^-			20	50	µA

The ● denotes the specifications which apply over the full operating temperature range of $-55°C \leq T_A \leq 125°C$.
$V_S = \pm 5V$, Pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1191M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	N8 Package	●		2	8	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		8		µV/°C
I_{OS}	Input Offset Current		●		0.2	2	µA
I_B	Input Bias Current		●		±0.5	±2.5	µA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to 3.5V	●	55	70		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 5V$	●	55	70		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L = 1k$, $V_O = \pm 3V$ $R_L = 100$, $V_O = \pm 3V$	● ●	16 2	32 5		V/mV V/mV
V_{OUT}	Output Voltage Swing	$R_L = 1k$	●	±3.7	±3.9		V
I_S	Supply Current		●		32	38	mA
	Shutdown Supply Current	Pin 5 at V^- (Note 8)	●		1.5	2.5	mA
I_{SHDN}	Shutdown Pin Current	Pin 5 at V^-	●		20		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of 0°C ≤ T_A ≤ 70°C. V_S = ±5V, Pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1191C MIN	LT1191C TYP	LT1191C MAX	UNITS
V_{OS}	Input Offset Voltage	N8 Package SO-8 Package	● ●		2	6 10	mV mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		8		µV/°C
I_{OS}	Input Offset Current		●		0.2	1.7	µA
I_B	Input Bias Current		●		±0.5	±2.5	µA
CMRR	Common Mode Rejection Ratio	V_{CM} = –2.5V to 3.5V	●	58	70		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±5V	●	58	70		dB
A_{VOL}	Large-Signal Voltage Gain	R_L = 1k, V_O = ±3V R_L = 100, V_O = ±3V	● ●	20 3	40 9		V/mV V/mV
V_{OUT}	Output Voltage Swing	R_L = 1k	●	±3.7	±3.9		V
I_S	Supply Current		●		32	38	mA
	Shutdown Supply Current	Pin 5 at V^- (Note 8)	●		1.4	2.1	mA
I_{SHDN}	Shutdown Pin Current	Pin 5 at V^-	●		20		µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.

Note 3: Exceeding the input common mode range may cause the output to invert.

Note 4: Slew rate is measured between ±1V on the output, with a ±1.5V input step.

Note 5: Full-power bandwidth is calculated from the slew rate measurement:

FPBW = SR/2πV_P.

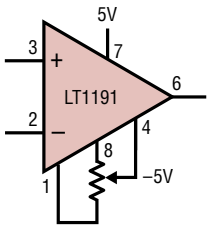
Note 6: Settling time measurement techniques are shown in "Take the Guesswork Out of Settling Time Measurements," EDN, September 19, 1985. A_V = –1, R_L = 1k.

Note 7: NTSC (3.58MHz). For R_L = 1k, Diff A_V = 0.07%, Diff Ph = 0.02°.

Note 8: See Applications section for shutdown at elevated temperatures. Do not operate the shutdown above T_J > 125°C.

Note 9: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J and N suffix) and are sample tested on every lot of the SO packaged parts (S suffix).

Optional Offset Nulling Circuit

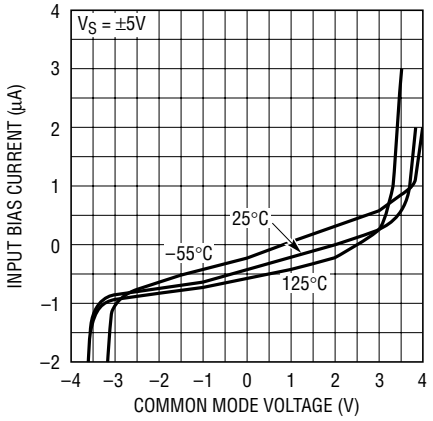


INPUT OFFSET VOLTAGE CAN BE ADJUSTED OVER A ±100mV RANGE WITH A 1kΩ TO 10kΩ POTENTIOMETER

LT1191 • TA03

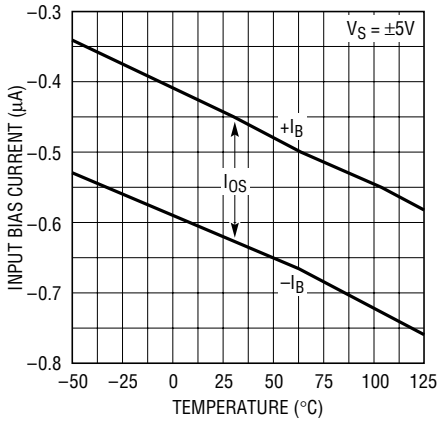
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Common Mode Voltage



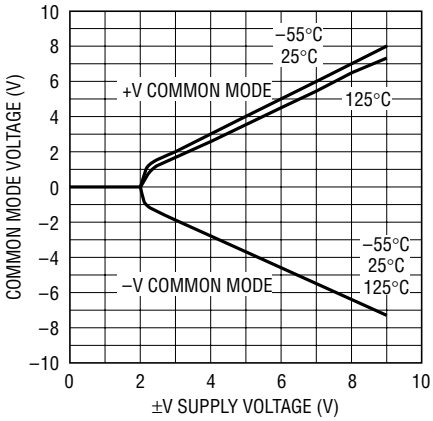
LT1191 • TPC01

Input Bias Current vs Temperature



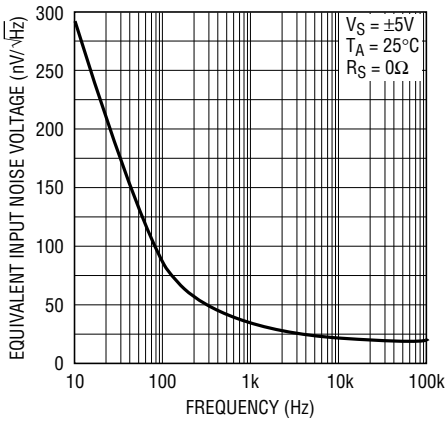
LT1191 • TPC02

Common Mode Voltage vs Supply Voltage



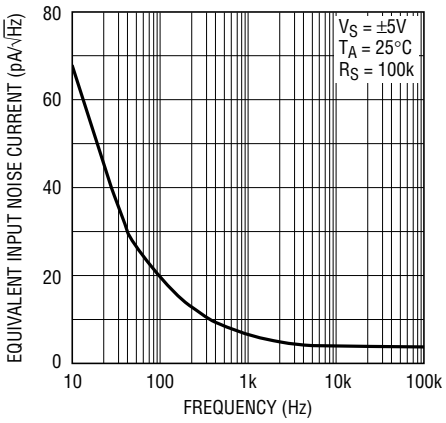
LT1191 • TPC03

Equivalent Input Noise Voltage vs Frequency



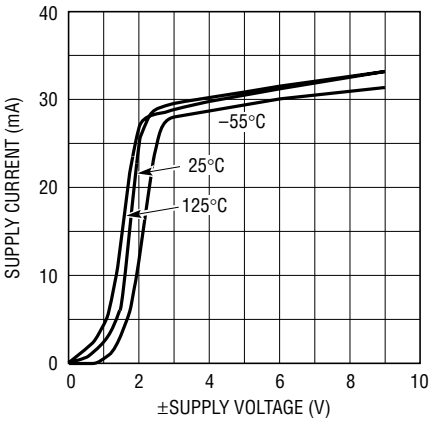
LT1191 • TPC04

Equivalent Input Noise Current vs Frequency



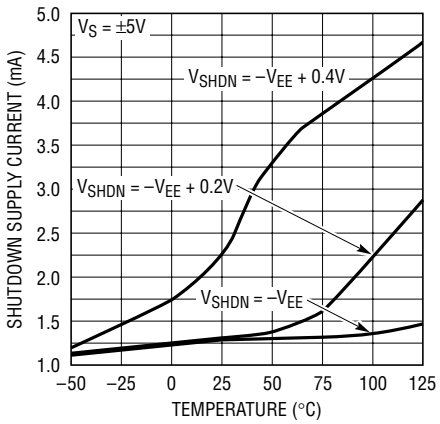
LT1191 • TPC05

Supply Current vs Supply Voltage



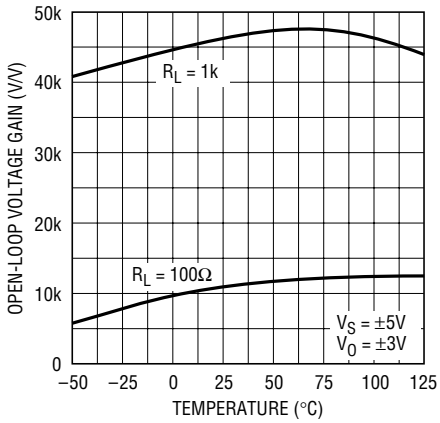
LT1191 • TPC06

Shutdown Supply Current vs Temperature



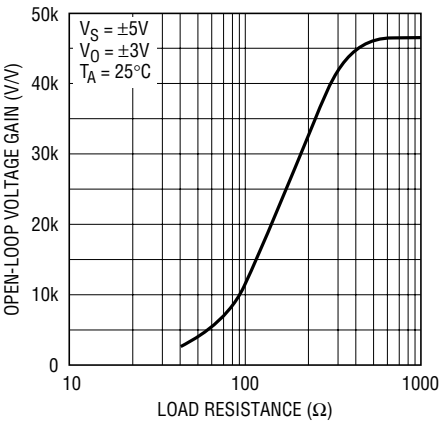
LT1191 • TPC07

Open-Loop Voltage Gain vs Temperature



LT1191 • TPC08

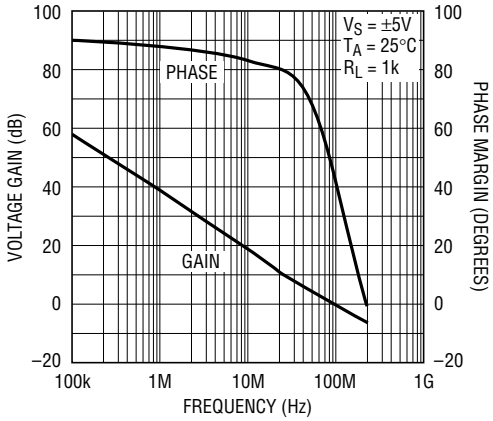
Open-Loop Voltage Gain vs Load Resistance



LT1191 • TPC09

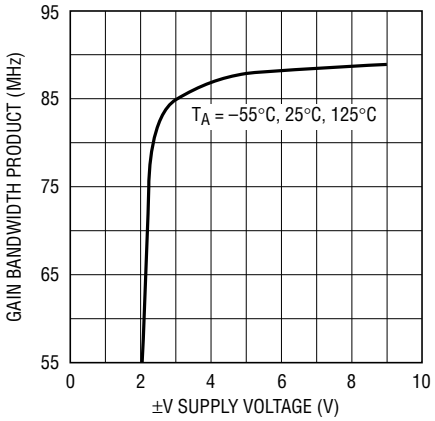
TYPICAL PERFORMANCE CHARACTERISTICS

Gain, Phase vs Frequency



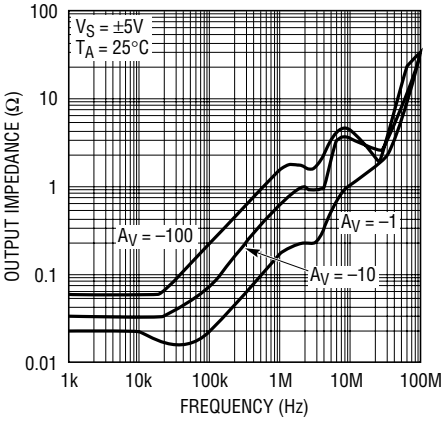
LT1191 • TPC10

Gain Bandwidth Product vs Supply Voltage



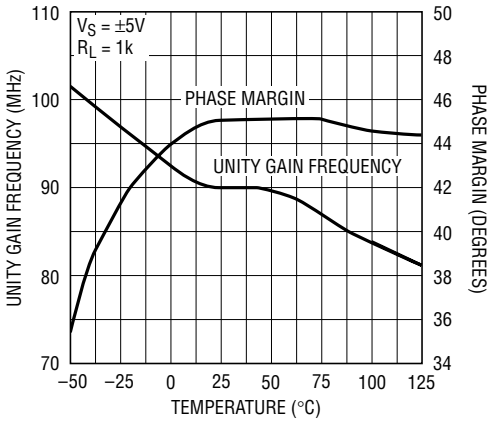
LT1191 • TPC11

Output Impedance vs Frequency



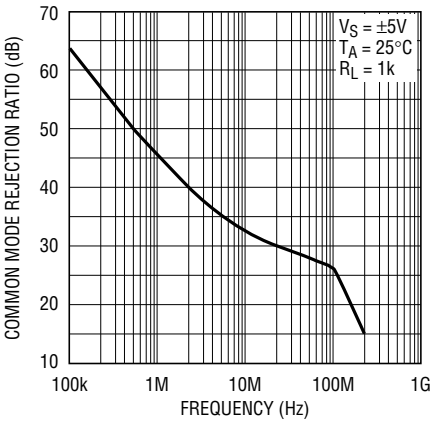
LT1191 • TPC13

Unity Gain Frequency and Phase Margin vs Temperature



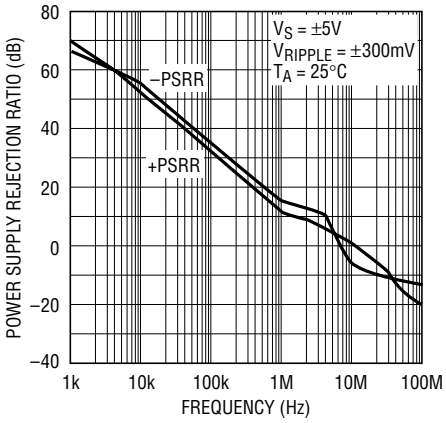
LT1191 • TPC12

Common Mode Rejection Ratio vs Frequency



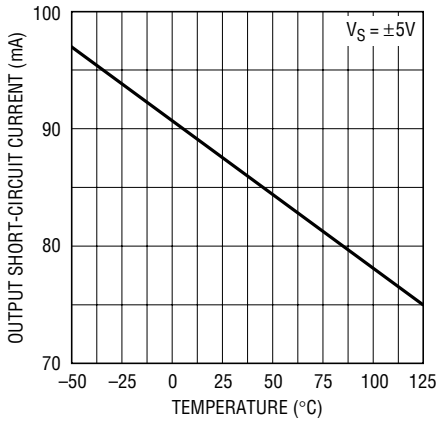
LT1191 • TPC14

Power Supply Rejection Ratio vs Frequency



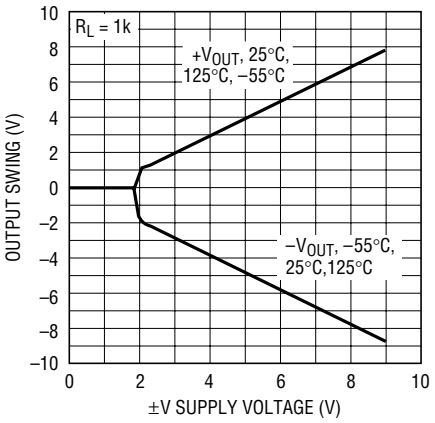
LT1191 • TPC15

Output Short-Circuit Current vs Temperature



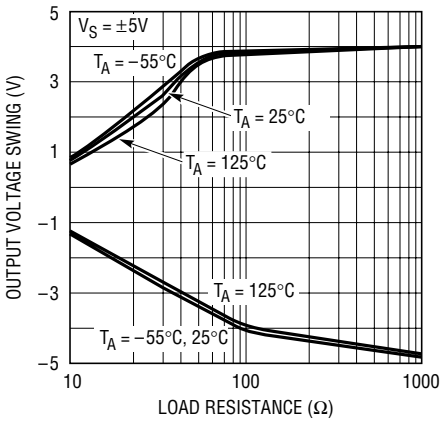
LT1191 • TPC16

Output Swing vs Supply Voltage



LT1191 • TPC17

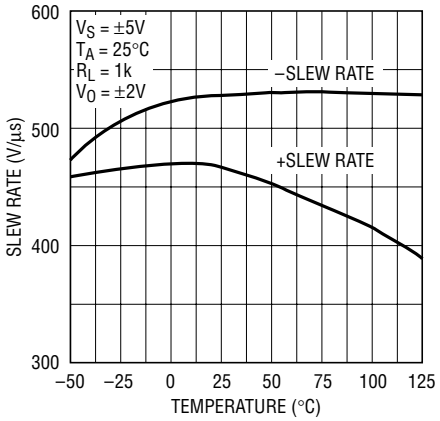
Output Voltage Swing vs Load Resistance



LT1191 • TPC18

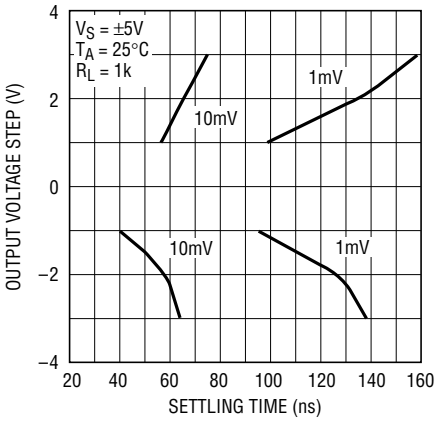
TYPICAL PERFORMANCE CHARACTERISTICS

Slew Rate vs Temperature



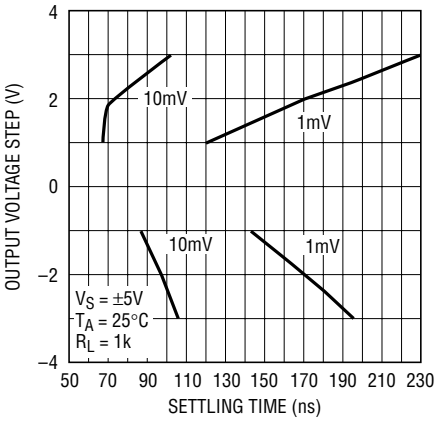
LT1191 • TPC19

Output Voltage Step vs Settling Time, A_V = –1



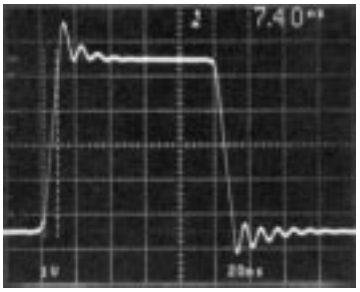
LT1191 • TPC20

Output Voltage Step vs Settling Time, A_V = 1



LT1191 • TPC21

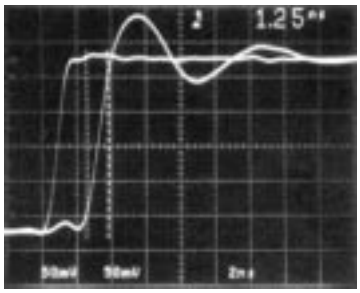
Large-Signal Transient Response



LT1191 • TPC22

A_V = 1, C_L = 10pF SCOPE PROBE

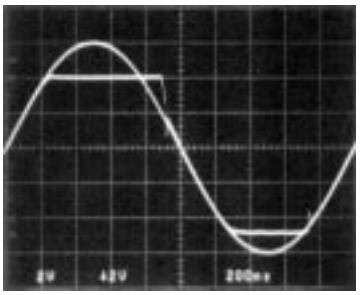
Small-Signal Transient Response



LT1191 • TPC23

A_V = 1, SMALL-SIGNAL RISE TIME, WITH FET PROBES

Output Overload



LT1191 • TPC24

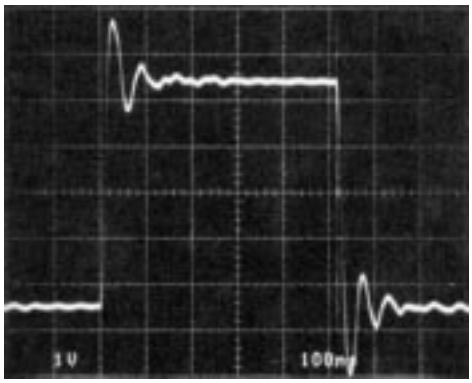
A_V = –1, V_{IN} = 12V_{P-P}

APPLICATIONS INFORMATION

Power Supply Bypassing

The LT1191 is quite tolerant of power supply bypassing. In some applications a 0.1µF ceramic disc capacitor placed 1/2 inch from the amplifier is all that is required. A scope photo of the amplifier output with no supply bypassing is used to demonstrate this bypassing tolerance, R_L = 1kΩ.

No Supply Bypass Capacitors

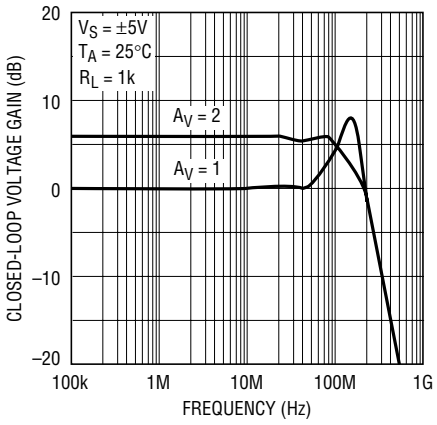


LT1191 • TA04

A_V = –1, IN DEMO BOARD, R_L = 1kΩ

Supply bypassing can also affect the response in the frequency domain. It is possible to see a slight rise in the frequency response at 130MHz depending on the gain configuration, supply bypass, inductance in the supply leads and printed circuit board layout. This can be further minimized by not using a socket.

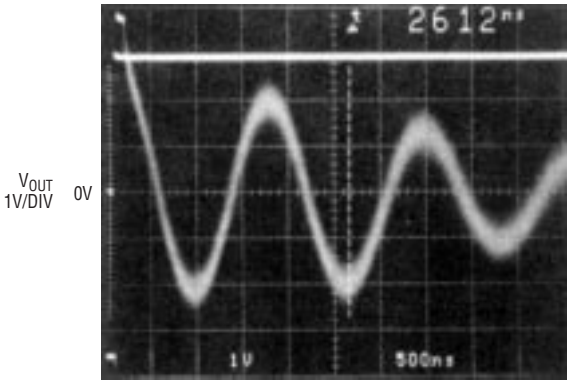
Closed-Loop Voltage Gain vs Frequency



LT1191 • TA05

In most applications, and those requiring good settling time, it is important to use multiple bypass capacitors. A 0.1µF ceramic disc in parallel with a 4.7µF tantalum is recommended. Two oscilloscope photos with different bypass conditions are used to illustrate the settling time characteristics of the amplifier. Note that although the output waveform looks acceptable at 1V/DIV, when amplified to 1mV/DIV the settling time to 2mV is 2.61µs for the 0.1µF bypass; the time drops to 143ns with multiple bypass capacitors.

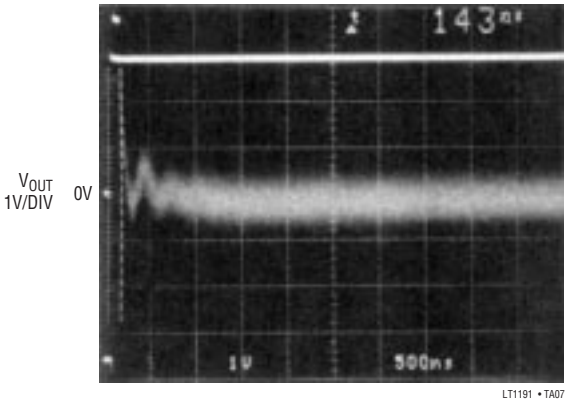
Settling Time Poor Bypass



LT1191 • TA06

SETTLING TIME TO 2mV, A_V = –1
SUPPLY BYPASS CAPACITORS = 0.1µF

Settling Time Good Bypass



LT1191 • TA07

SETTLING TIME TO 2mV, A_V = –1
SUPPLY BYPASS CAPACITORS = 0.1µF + 4.7µF TANTALUM

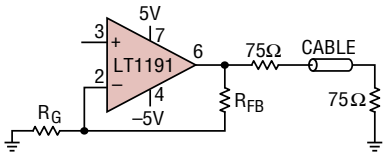
APPLICATIONS INFORMATION

Cable Terminations

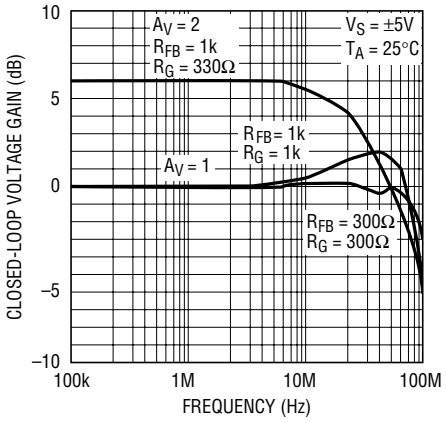
The LT1191 operational amplifier has been optimized as a low cost video cable driver. The ±50mA guaranteed output current enables the LT1191 to easily deliver $7.5V_{P-P}$ into 100Ω, while operating on ±5V supplies or $2.6V_{P-P}$ on a single 5V supply.

When driving a cable it is important to terminate the cable to avoid unwanted reflections. This can be done in one of two ways: single termination or double termination. With single termination, the cable must be terminated at the receiving end (75Ω to ground) to absorb unwanted energy. The best performance can be obtained by double termination (75Ω in series with the output of the amplifier, and 75Ω to ground at the other end of the cable). This termination is preferred because reflected energy is absorbed at each end of the cable. When using the double termination technique it is important to note that the signal is attenuated by a factor of 2, or 6dB. This can be compensated for by taking a gain of 2, or 6dB in the amplifier. The cable driver has a –3dB bandwidth of 100MHz while driving the 150Ω load. Note the response can be improved by lowering the impedance of the feedback elements.

Double Terminated Cable Driver



Cable Driver Voltage Gain vs Frequency

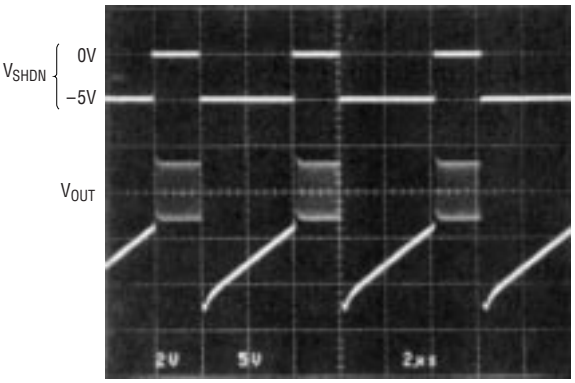


LT1191 • TA08

Using the Shutdown Feature

The LT1191 has a unique feature that allows the amplifier to be shut down for conserving power or for multiplexing several amplifiers onto a common cable. The amplifier will shut down by taking Pin 5 to V^-. In shutdown, the amplifier dissipates 15mW while maintaining a true high impedance output state of 15kΩ in parallel with the feedback resistors. The amplifiers must be used in a noninverting configuration for MUX applications. In inverting configurations the input signal is fed to the output through the feedback components. The following scope photos show that with very high R_L, the output is truly high impedance; the output slowly decays toward ground. Additionally, when the output is loaded with as little as 1kΩ the amplifier shuts off in 400ns. This shutoff can be under the control of HC CMOS operating between 0V and –5V.

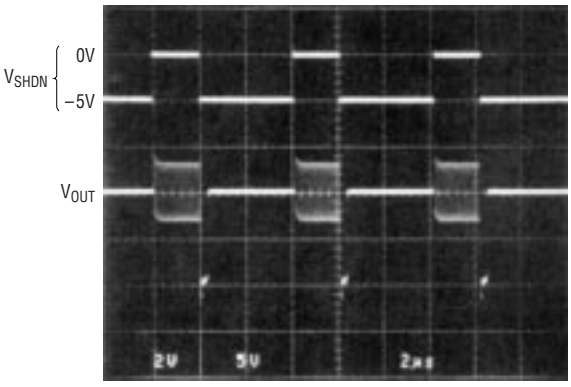
Output Shutdown



LT1191 • TA09

1MHz SINE WAVE GATED OFF WITH SHUTDOWN PIN, $A_V = 1$, $R_L = \infty$

Output Shutdown



LT1191 • TA10

1MHz SINE WAVE GATED OFF WITH SHUTDOWN PIN, $A_V = 1$, $R_L = 1k\Omega$

APPLICATIONS INFORMATION

The ability to maintain shutoff is shown on the curve Shutdown Supply Current vs Temperature in the Typical Performance Characteristics section. At very high elevated temperatures it is important to hold the SHDN pin close to the negative supply to keep the supply current from increasing.

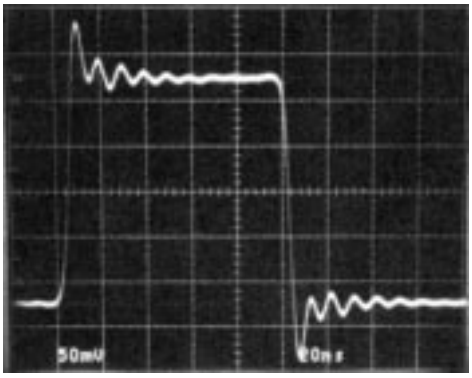
Murphy Circuits

There are several precautions the user should take when using the LT1191 in order to realize its full capability. Although the LT1191 can drive a 30pF load, isolating the capacitance with 10Ω can be helpful. Precautions primarily have to do with driving large capacitive loads.

Other precautions include:

1. Use a ground plane (see Design Note 50, High Frequency Amplifier Evaluation Board).
2. Do not use high source impedances. The input capacitance of 2pF and R_S = 10k, for instance, will give an 8MHz –3dB bandwidth.
3. PC board socket may reduce stability.
4. A feedback resistor of 1k or lower reduces the effects of stray capacitance at the inverting input. (For instance, closed-loop gain of 2 can use R_{FB} = 300Ω and R_G = 300Ω.)

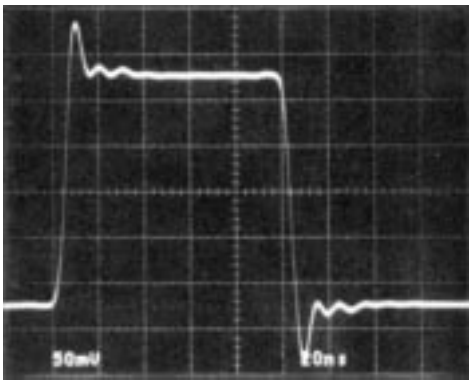
Driving Capacitive Load



LT1191 • TA11

A_V = –1, IN DEMO BOARD, C_L = 30pF

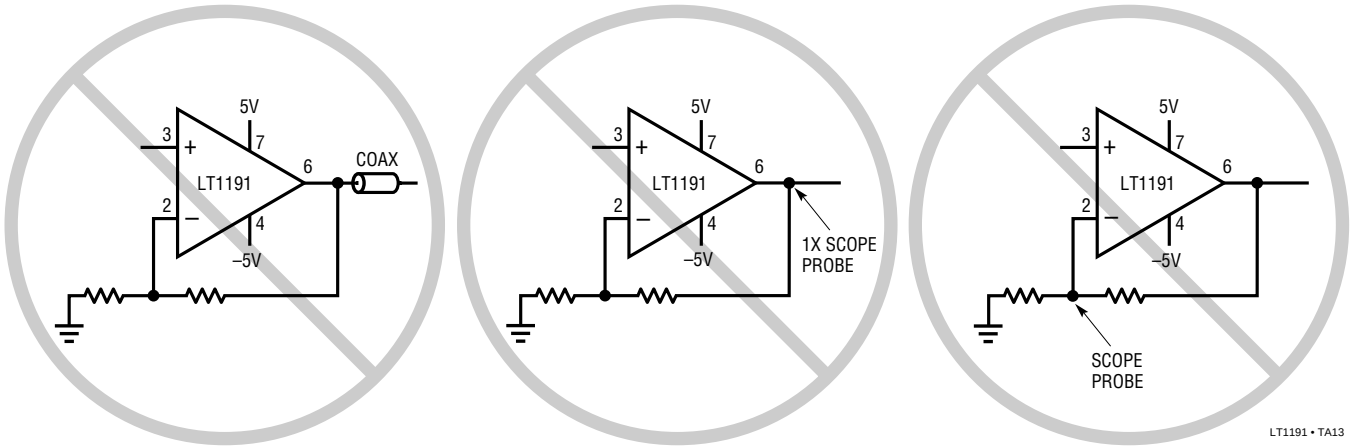
Driving Capacitive Load



LT1191 • TA12

A_V = –1, IN DEMO BOARD, C_L = 30pF
WITH 10Ω ISOLATING RESISTOR

Murphy Circuits



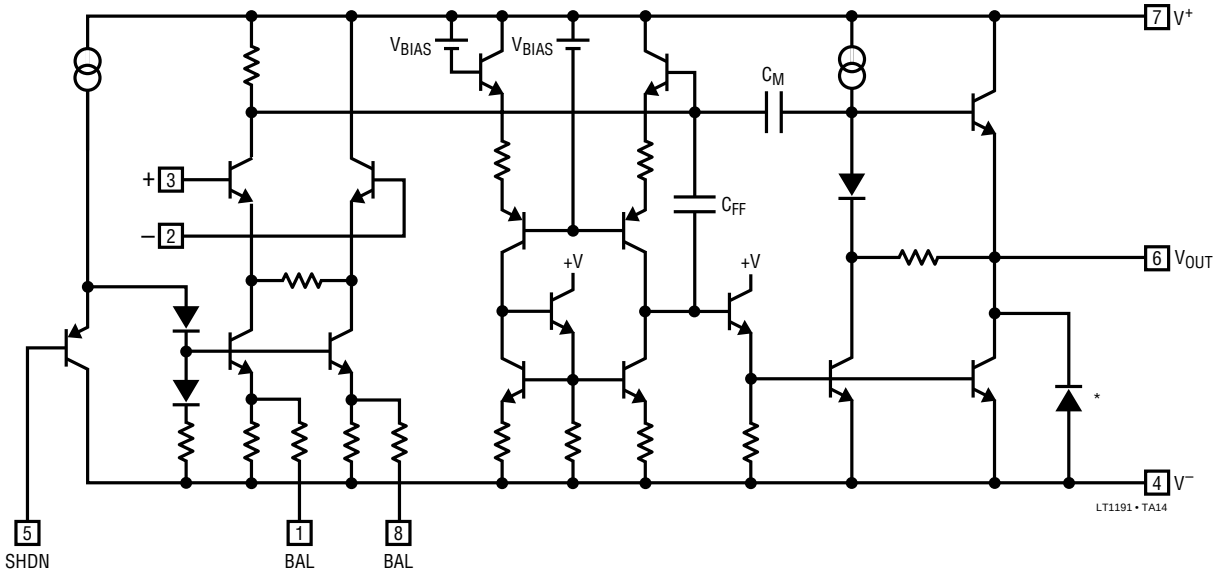
LT1191 • TA13

An Unterminated Cable Is a Large Capacitive Load

A 1X Scope Probe Is a Large Capacitive Load

A Scope Probe on the Inverting Input Reduces Phase Margin

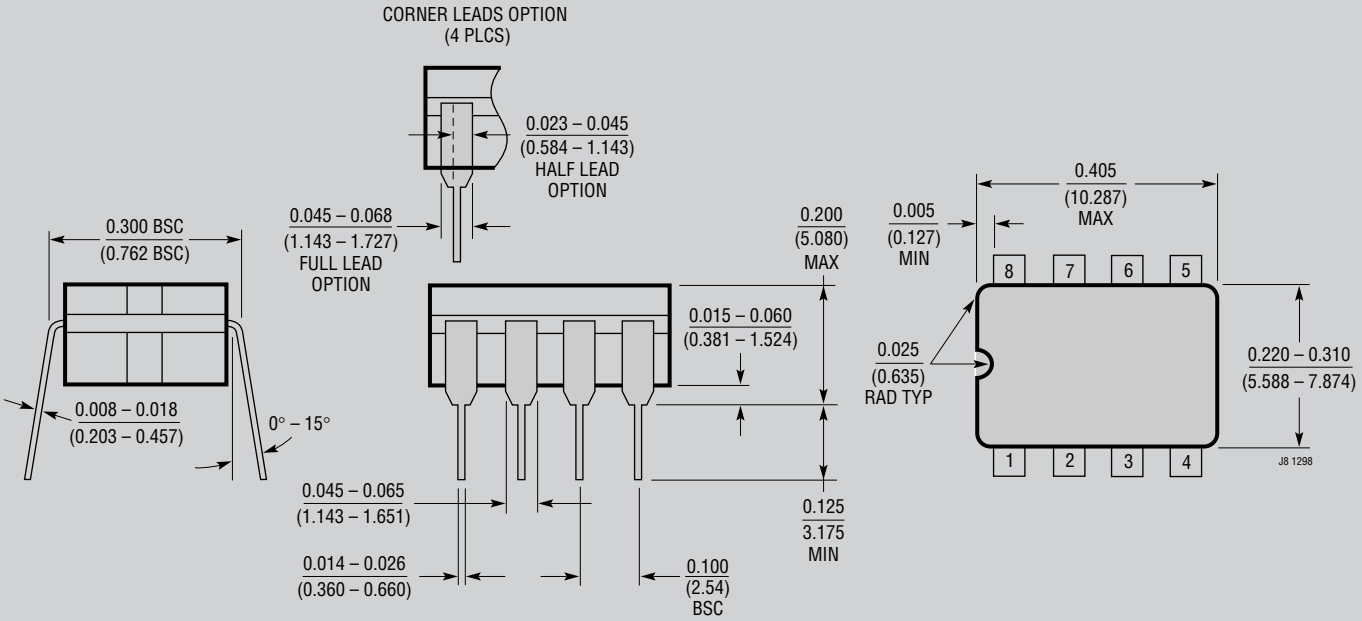
SIMPLIFIED SCHEMATIC



*SUBSTRATE DIODE, DO NOT FORWARD BIAS

PACKAGE DESCRIPTION

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)

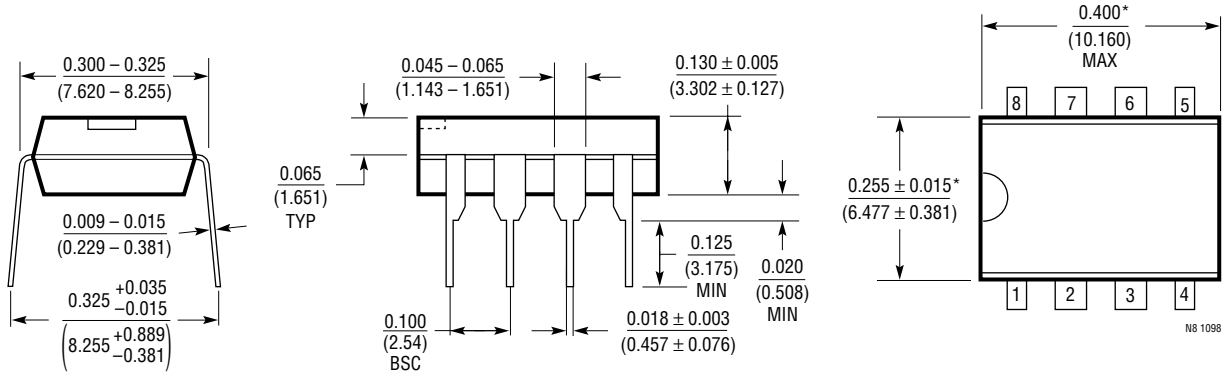


NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE
OR TIN PLATE LEADS

OBSOLETE PACKAGE

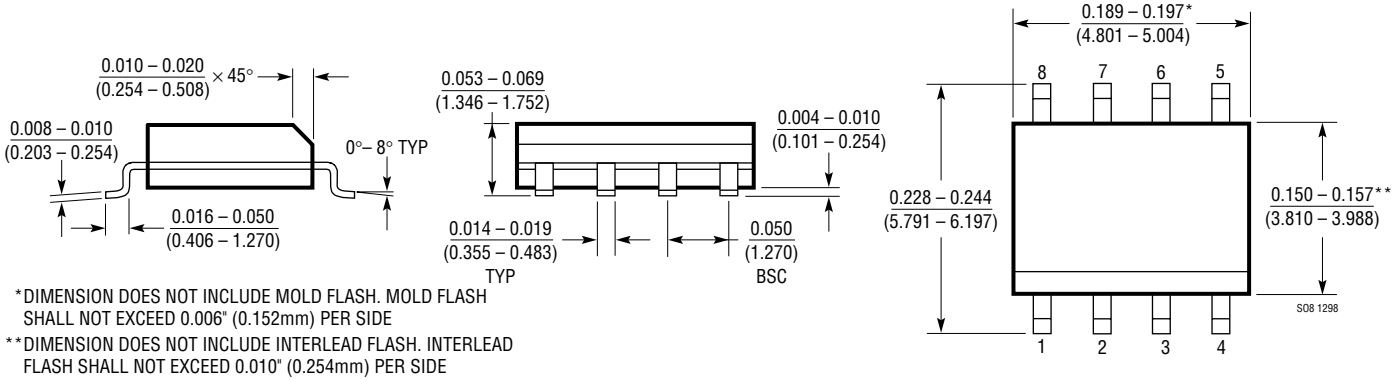
PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1363	High Speed Operational Amplifier	70MHz Gain Bandwidth, 1000V/µs Slew Rate, I_S = 7.5mA Max
LT1813	High Speed Operational Amplifier	100MHz Gain Bandwidth, 750V/µs Slew Rate, I_S = 3.6mA Max

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