

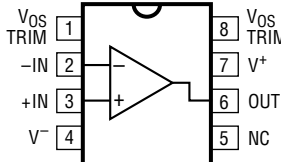
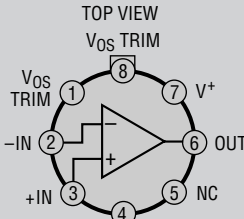
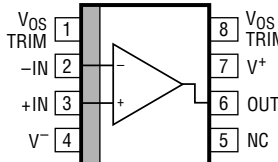
LT1007/LT1037

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage $\pm 22\text{V}$
 Input Voltage Equal to Supply Voltage
 Output Short-Circuit Duration Indefinite
 Differential Input Current (Note 9) $\pm 25\text{mA}$
 Storage Temperature Range -65°C to 150°C

Lead Temperature (Soldering, 10 sec.) 300°C
 Operating Temperature Range
 LT1007/LT1037AC, C 0°C to 70°C
 LT1007/LT1037I -40°C to 85°C
 LT1007/LT1037AM, M (**OBSOLETE**) -55°C to 125°C

PACKAGE/ORDER INFORMATION

TOP VIEW  N8 PACKAGE 8-LEAD PDIP $T_{JMAX} = 100^{\circ}\text{C}$, $\theta_{JA} = 130^{\circ}\text{C/W}$ (N8)	TOP VIEW  V^{OS} TRIM V⁺ V⁻ (CASE) H PACKAGE 8-LEAD TO-5 METAL CAN $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 150^{\circ}\text{C/W}$, $\theta_{JC} = 45^{\circ}\text{C/W}$	TOP VIEW  S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 190^{\circ}\text{C/W}$
ORDER PART NUMBER	ORDER PART NUMBER	ORDER PART NUMBER
LT1007ACN8 LT1037ACN8 LT1007CN8 LT1037CN8 LT1007IN8 LT1037IN8		LT1007CS8 LT1037CS8 LT1007IS8 LT1037IS8
J8 PACKAGE LEAD CERP $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 100^{\circ}\text{C/W}$ (J8) LT1007ACJ8 LT1037ACJ8 LT1007AMJ8 LT1037AMJ8 LT1007CJ8 LT1037CJ8 LT1007MJ8 LT1037MJ8 OBSOLETE PACKAGE Consider the N8 Package for Alternate Source	LT1007ACH LT1037ACH LT1007AMH LT1037AMH LT1007CH LT1037CH LT1007MH LT1037MH OBSOLETE PACKAGE Consider the N8 or S8 Package for Alternate Source	S8 PART MARKING 1007 1037 1007I 1037I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15\text{V}$, $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1007AC/AM LT1037AC/AM			LT1007C/I/M LT1037C/I/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 2)		10	25		20	60	μV
$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	Long Term Input Offset Voltage Stability	(Notes 3, 4)		0.2	1.0		0.2	1.0	$\mu\text{V/Mo}$
I_{OS}	Input Offset Current			7	30		12	50	nA
I_B	Input Bias Current			± 10	± 35		± 15	± 55	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Notes 4, 6)		0.06	0.13		0.06	0.13	μV_{p-p}
	Input Noise Voltage Density	$f_0 = 10\text{Hz}$ (Notes 4, 5) $f_0 = 1000\text{Hz}$ (Note 4)		2.8 2.5	4.5 3.8		2.8 2.5	4.5 3.8	$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f_0 = 10\text{Hz}$ (Notes 4, 7) $f_0 = 1000\text{Hz}$ (Notes 4, 7)		1.5 0.4	4.0 0.6		1.5 0.4	4.0 0.6	$\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$

sn100737 100737fbs

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1007AC/AM LT1037AC/AM			LT1007C/I/M LT1037C/I/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input Resistance, Common Mode		7			5			G Ω
	Input Voltage Range		± 11.0	± 12.5		± 11.0	± 12.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11V$	117	130		110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	110	130		106	126		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 2k$, $V_O = \pm 12V$	7.0	20.0		5.0	20.0		V/ μV
		$R_L \geq 1k$, $V_O = \pm 10V$	5.0	16.0		3.5	16.0		V/ μV
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	3.0	12.0		2.0	12.0		V/ μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k$	± 13.0	± 13.8		± 12.5	± 13.5		V
		$R_L \geq 600\Omega$	± 11.0	± 12.5		± 10.5	± 12.5		V
SR	Slew Rate	LT1007 $R_L \geq 2k$	1.7	2.5		1.7	2.5		V/ μs
		LT1037 $A_{VCL} \geq 5$	11	15		11	15		V/ μs
GBW	Gain Bandwidth Product	LT1007 $f_0 = 100kHz$ (Note 8)	5.0	8.0		5.0	8.0		MHz
		LT1037 $f_0 = 10kHz$ (Note 8) ($A_{VCL} \geq 5$)	45	60		45	60		MHz
Z_O	Open-Loop Output Resistance	$V_O = 0V$, $I_O = 0$	70			70			Ω
P_D	Power Dissipation	LT1007	80			80			mW
		LT1037	80			85			mW

The ● denotes the specifications which apply over the temperature range $0^\circ C \leq T_A \leq 70^\circ C$, $V_S = \pm 15V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1007AC LT1037AC			LT1007C LT1037C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 2)	●	20			35			μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 10)	●	0.2			0.3			$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	10			15			nA
I_B	Input Bias Current		●	± 14			± 20			nA
	Input Voltage Range		●	± 10.5	± 11.8		± 10.5	± 11.8		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	114	126		106	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	106	126		102	120		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 2k$, $V_O = \pm 10V$	●	4.0	18.0		2.5	18.0		V/ μV
		$R_L \geq 1k$, $V_O = \pm 10V$	●	2.5	14.0		2.0	14.0		V/ μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k$	●	± 12.5	± 13.6		± 12.0	± 13.6		V
P_D	Power Dissipation		●	90			90			mW

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1007I/LT1037I			UNITS
				MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 2)	●		40	125	μV
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Input Offset Drift	(Note 10)	●		0.3	1.0	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		●		20	80	nA
I_B	Input Bias Current		●		± 25	± 90	nA
	Input Voltage Range		●	± 10	± 11.7		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.5\text{V}$	●	105	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$	●	101	120		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 2\text{k}$, $V_O = \pm 10\text{V}$	●	2.0	15.0		$\text{V}/\mu\text{V}$
		$R_L \geq 1\text{k}$, $V_O = \pm 10\text{V}$	●	1.5	12.0		$\text{V}/\mu\text{V}$
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2\text{k}$	●	± 12.0	± 13.6		V
P_D	Power Dissipation		●		95	165	mW

The ● denotes the specifications which apply over the temperature range $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1007AM/LT1037AM			LT1007M/LT1037M			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 2)	●		25	60		50	160	μV
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Input Offset Drift	(Note 10)	●		0.2	0.6		0.3	1.0	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		●		15	50		20	85	nA
I_B	Input Bias Current		●		± 20	± 60		± 35	± 95	nA
	Input Voltage Range		●	± 10.3	± 11.5		± 10.3	± 11.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.3\text{V}$	●	112	126		104	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$	●	104	126		100	120		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 2\text{k}$, $V_O = \pm 10\text{V}$	●	3.0	14.0		2.0	14.0		$\text{V}/\mu\text{V}$
		$R_L \geq 1\text{k}$, $V_O = \pm 10\text{V}$	●	2.0	10.0		1.5	10.0		$\text{V}/\mu\text{V}$
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2\text{k}$	●	± 12.5	± 13.5		± 12.0	± 13.5		V
P_D	Power Dissipation		●		100	150		100	170	mW

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power. AM and AC grades are guaranteed fully warmed up.

Note 3: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically $2.5\mu\text{V}$. Refer to typical performance curve.

Note 4: This parameter is tested on a sample basis only.

Note 5: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 6: See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the Applications Information section.

Note 7: See the test circuit for current noise measurement in the Applications Information section.

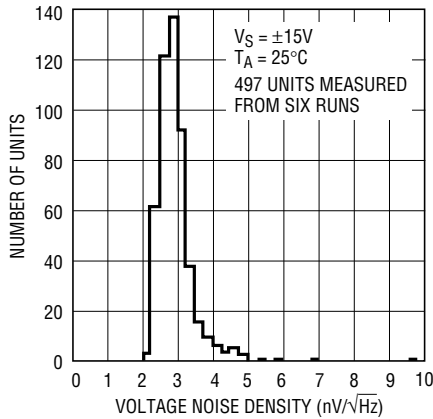
Note 8: This parameter is guaranteed by design and is not tested.

Note 9: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds $\pm 0.7\text{V}$, the input current should be limited to 25mA.

Note 10: The Average Input Offset Drift performance is within the specifications unnullled or when nullled with a pot having a range of $8\text{k}\Omega$ to $20\text{k}\Omega$.

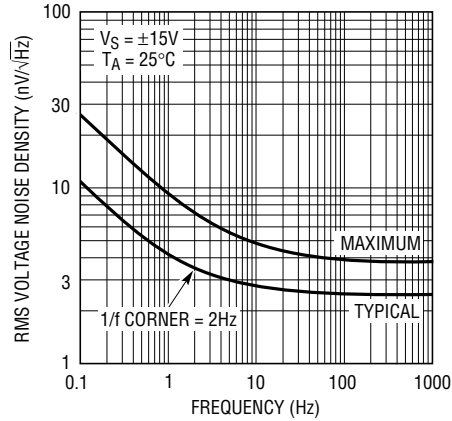
TYPICAL PERFORMANCE CHARACTERISTICS

10Hz Voltage Noise Distribution



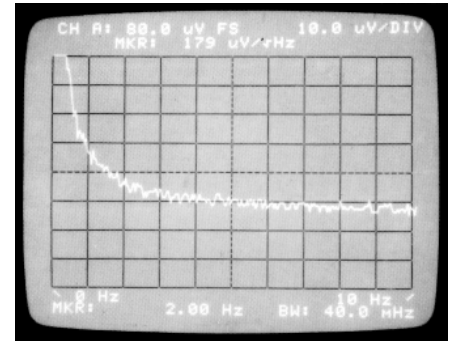
1007/37 G01

Voltage Noise vs Frequency



1007/37 G02

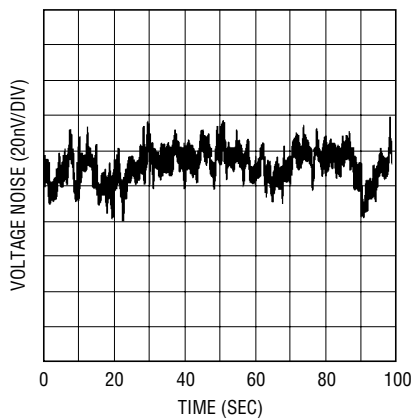
0.02Hz to 10Hz RMS Noise. Gain = 50,000 (Measured on HP3582 Spectrum Analyzer)



$$\text{MARKER AT 2Hz (} = 1/f \text{ CORNER)} = \frac{179 \mu\text{V}/\sqrt{\text{Hz}}}{50,000} = 3.59 \frac{\text{nV}}{\sqrt{\text{Hz}}}$$

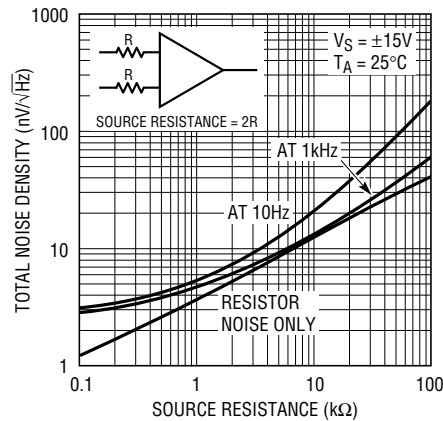
1007/37 G03

0.01Hz to 1Hz Peak-to-Peak Noise



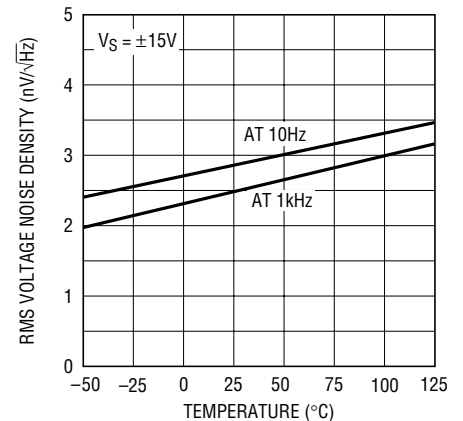
1007/37 G04

Total Noise vs Source Resistance



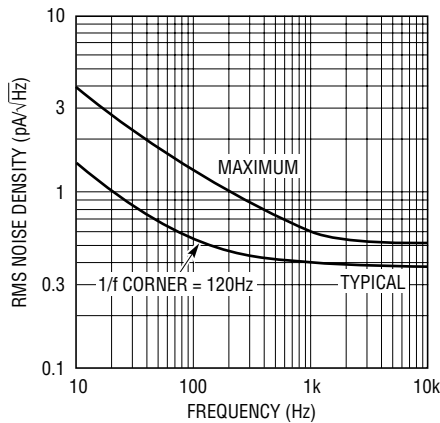
1007/37 G05

Voltage Noise vs Temperature



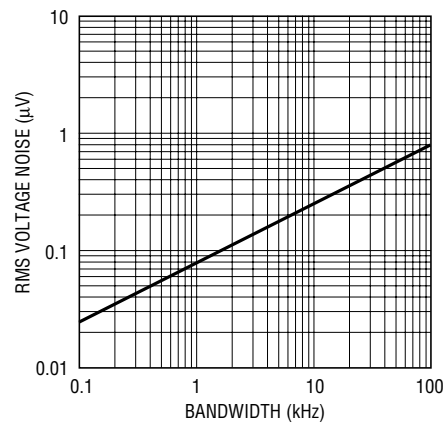
1007/37 G06

Current Noise vs Frequency



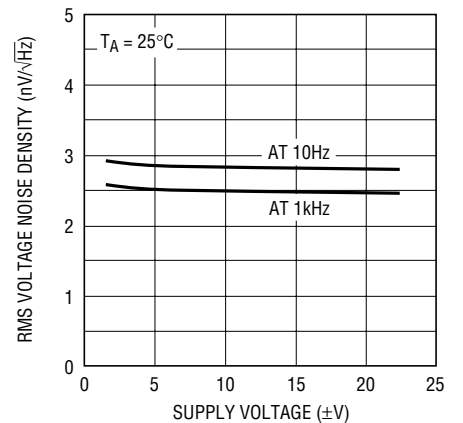
1007/37 G07

Wideband Voltage Noise (0.1Hz to Frequency Indicated)



1007/37 G08

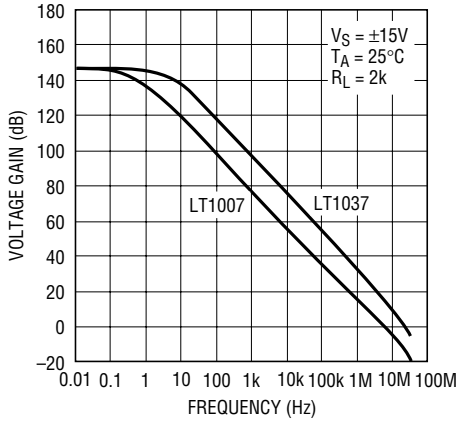
Voltage Noise vs Supply Voltage



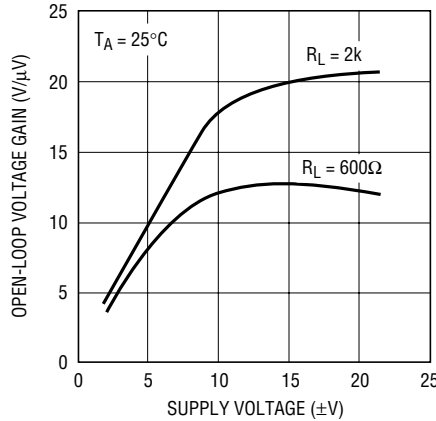
1007/37 G09

TYPICAL PERFORMANCE CHARACTERISTICS

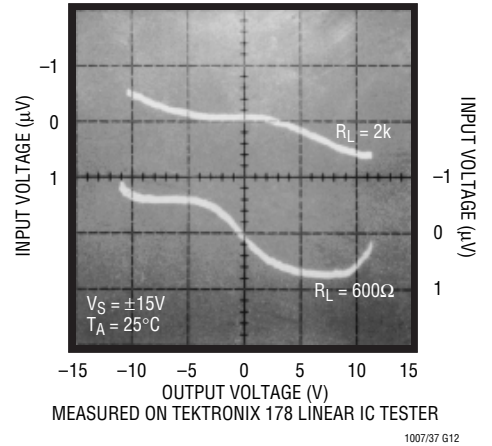
Voltage Gain vs Frequency



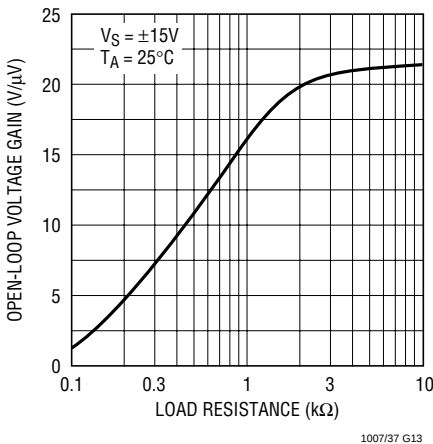
Voltage Gain vs Supply Voltage



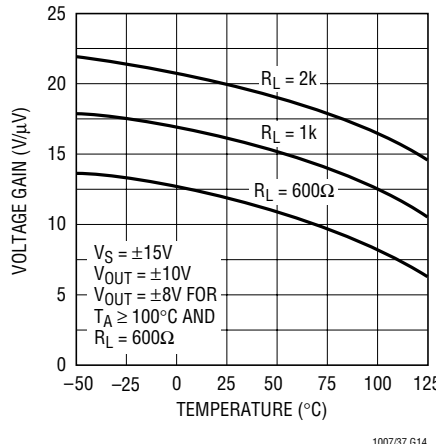
Voltage Gain, $R_L = 2k$ and 600Ω



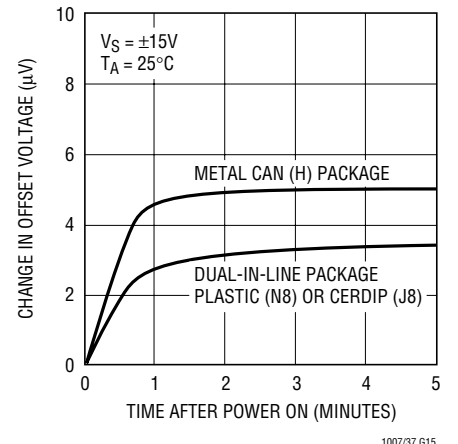
Voltage Gain vs Load Resistance



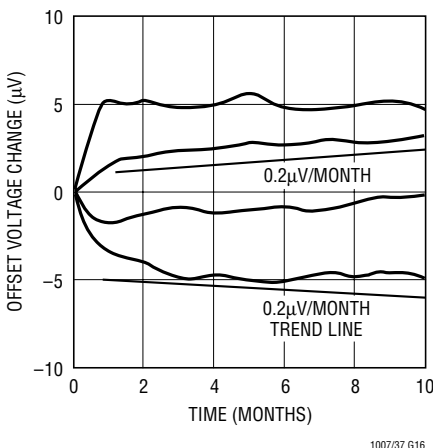
Voltage Gain vs Temperature



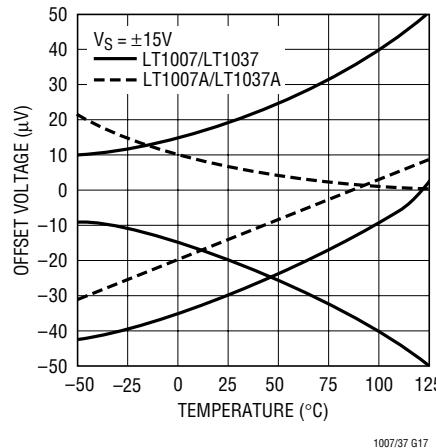
Warm-Up Drift



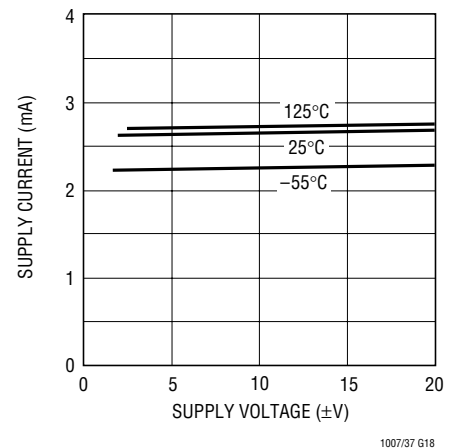
Long Term Stability of Four Representative Units



Offset Voltage Drift with Temperature of Representative Units

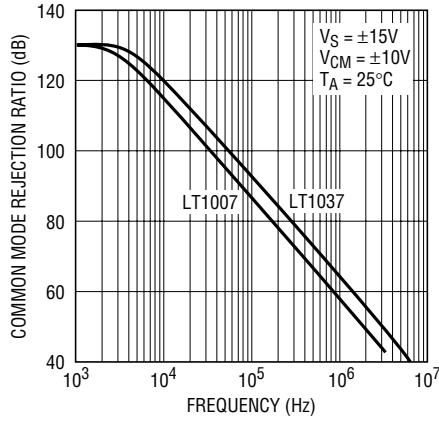


Supply Current vs Supply Voltage



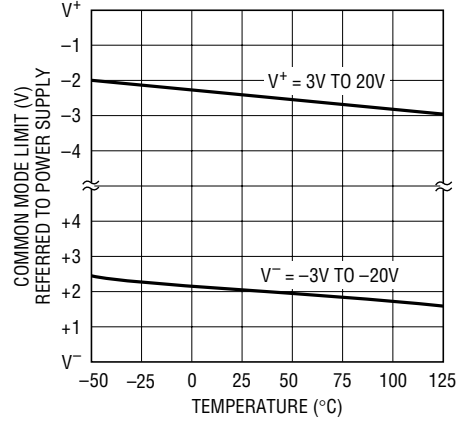
TYPICAL PERFORMANCE CHARACTERISTICS

Common Mode Rejection vs Frequency



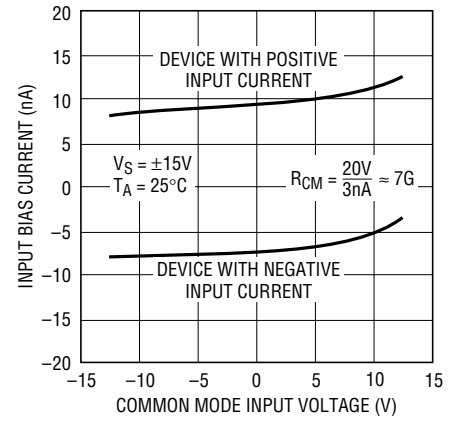
1007/37 G19

Common Mode Limit vs Temperature



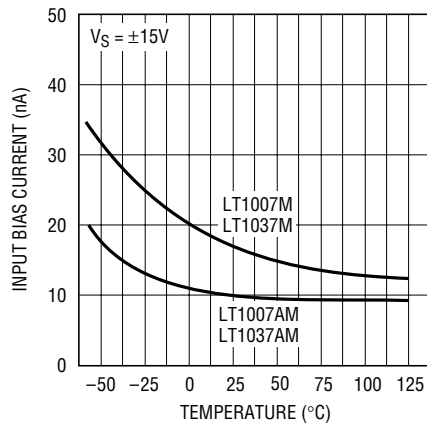
1007/37 G20

Input Bias Current Over the Common Mode Range



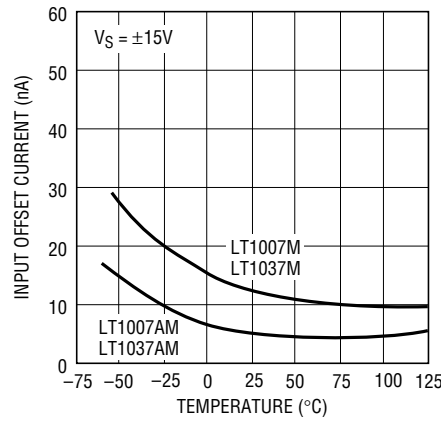
1007/37 G21

Input Bias Current vs Temperature



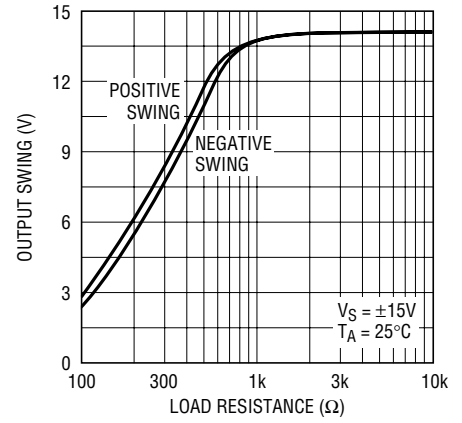
1007/37 G22

Input Offset Current vs Temperature



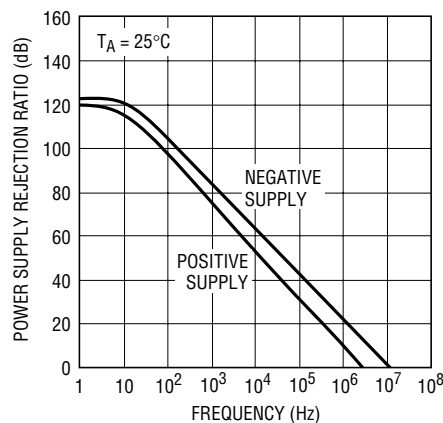
1007/37 G23

Output Swing vs Load Resistance



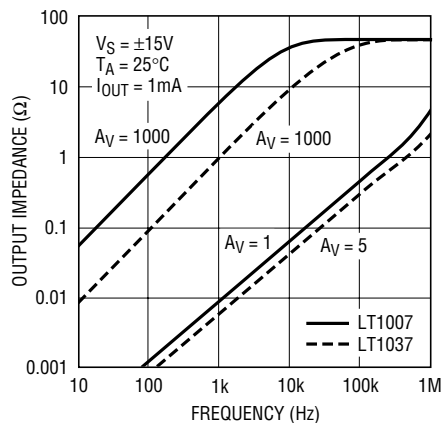
1007/37 G24

PSRR vs Frequency



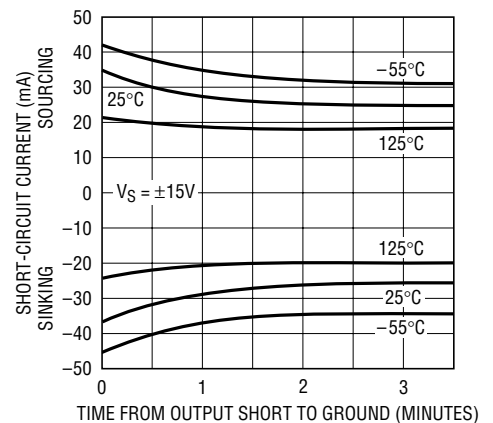
1195 G25

Closed-Loop Output Impedance



1007/37 G26

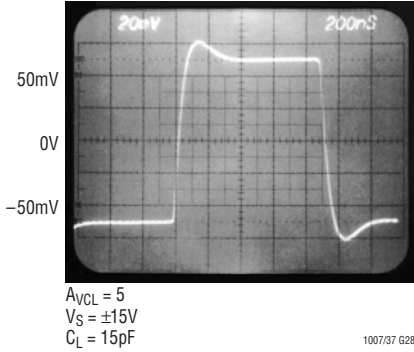
Output Short-Circuit Current vs Time



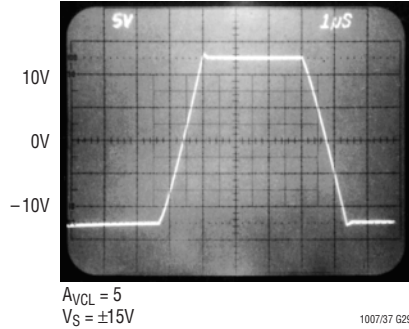
1007/37 G27

TYPICAL PERFORMANCE CHARACTERISTICS

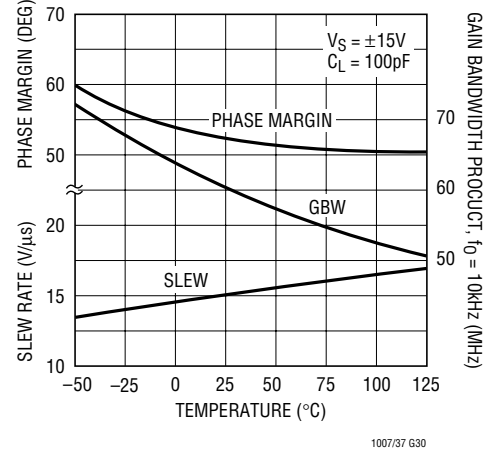
LT1037 Small-Signal Transient Response



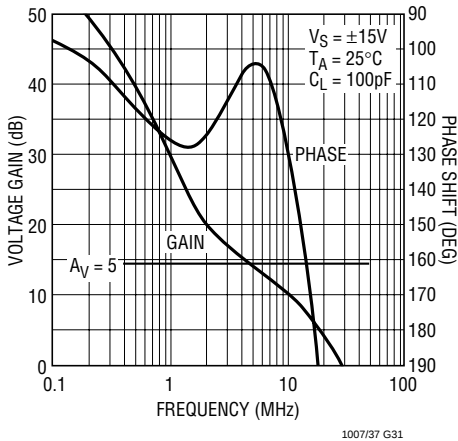
LT1037 Large-Signal Response



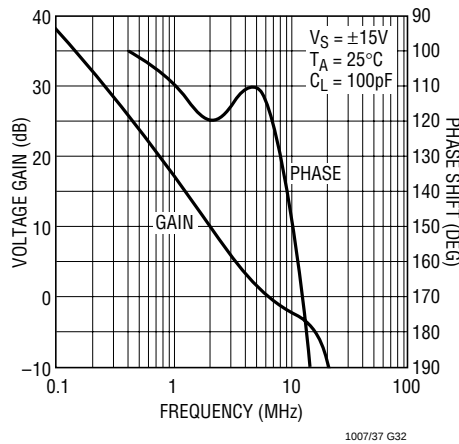
LT1037 Phase Margin, Gain Bandwidth Product, Slew Rate vs Temperature



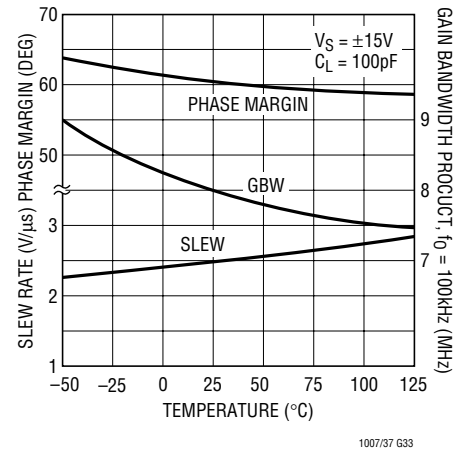
LT1037 Gain, Phase Shift vs Frequency



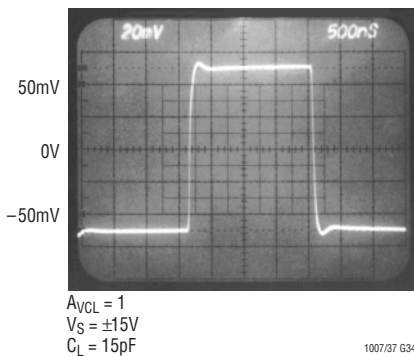
LT1007 Gain, Phase Shift vs Frequency



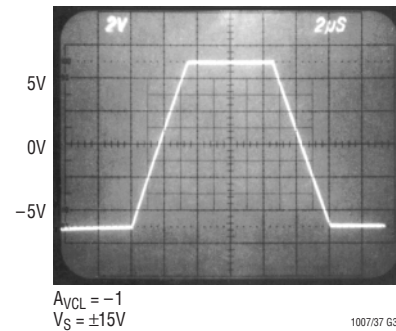
LT1007 Phase Margin, Gain Bandwidth Product, Slew Rate vs Temperature



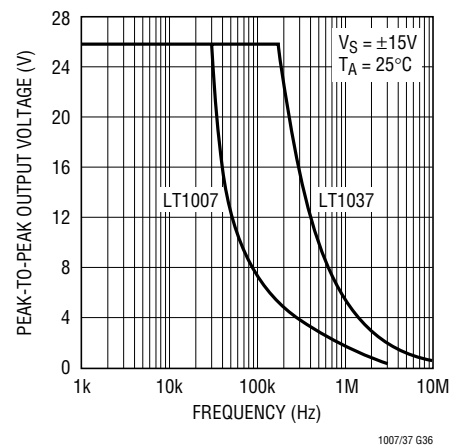
LT1007 Small-Signal Transient Response



LT1007 Large-Signal Response



Maximum Undistorted Output vs Frequency



APPLICATIONS INFORMATION

General

The LT1007/LT1037 series devices may be inserted directly into OP-07, OP-27, OP-37 and 5534 sockets with or without removal of external compensation or nulling components. In addition, the LT1007/LT1037 may be fitted to 741 sockets with the removal or modification of external nulling components.

Offset Voltage Adjustment

The input offset voltage of the LT1007/LT1037 and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, the use of a $10k\Omega$ nulling potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of $(V_{OS}/300)\mu V/^{\circ}C$, e.g., if V_{OS} is adjusted to $300\mu V$, the change in drift will be $1\mu V/^{\circ}C$ (Figure 1).

The adjustment range with a $10k\Omega$ pot is approximately $\pm 2.5mV$. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example has an approximate null range of $\pm 200\mu V$ (Figure 2).

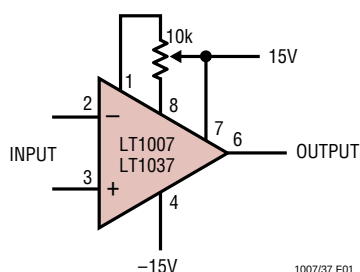


Figure 1. Standard Adjustment

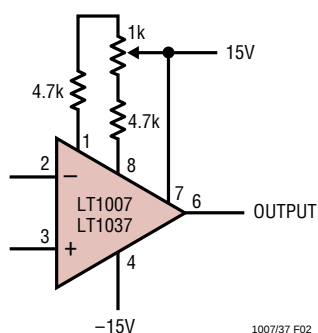


Figure 2. Improved Sensitivity Adjustment

Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

The circuit shown to measure offset voltage is also used as the burn-in configuration for the LT1007/LT1037, with the supply voltages increased to $\pm 20V$ (Figure 3).

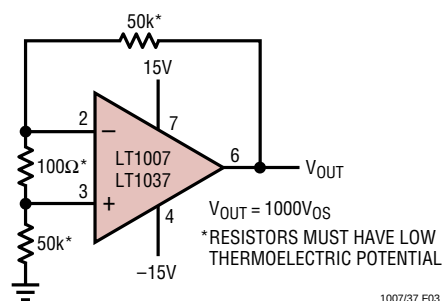


Figure 3. Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature

Unity-Gain Buffer Application (LT1007 Only)

When $R_F \leq 100\Omega$ and the input is driven with a fast, large-signal pulse ($>1V$), the output waveform will look as shown in the pulsed operation diagram (Figure 4).

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_F \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at $10V$) and the amplifier stays in its active mode and a smooth transition will occur.

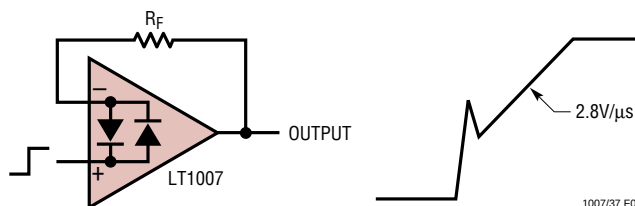


Figure 4. Pulsed Operation

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APPLICATIONS INFORMATION

As with all operational amplifiers when $R_F > 2k$, a pole will be created with R_F and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20pF to 50pF) in parallel with R_F will eliminate this problem.

Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the LT1007/LT1037 is measured in the test circuit shown (Figure 5a). The frequency response of this noise tester (Figure 5b) indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed ten seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 60nV peak-to-peak noise performance of the LT1007/LT1037 requires special test precautions:

1. The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically $3\mu V$ due to its chip temperature increasing $10^\circ C$ to $20^\circ C$ from the moment the power supplies are turned on. In the ten-second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.
2. For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermo-

electric effects in excess of a few nanovolts, which would invalidate the measurements.

3. Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

A noise voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the $1/f$ corner frequency.

Current noise is measured in the circuit shown in Figure 6 and calculated by the following formula:

$$i_n = \frac{\left[(e_{no})^2 - (130nV \cdot 101)^2 \right]^{1/2}}{(1M\Omega)(101)}$$

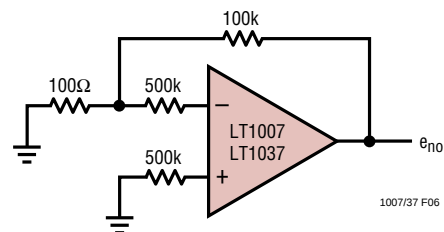


Figure 6

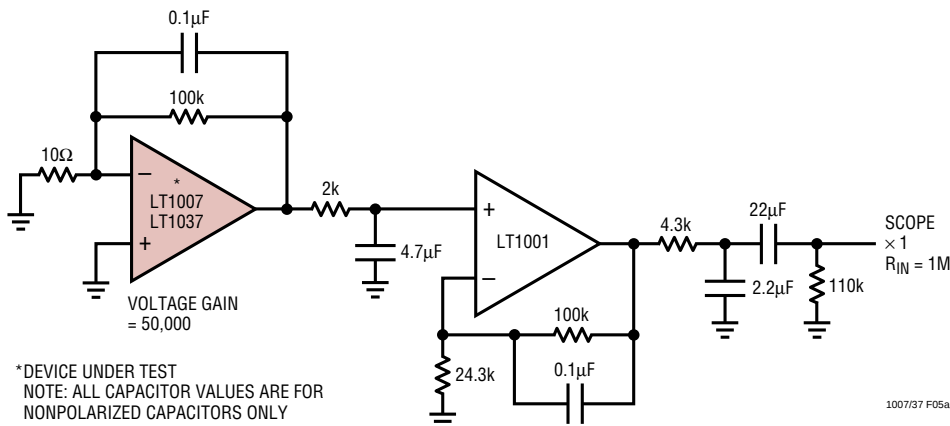


Figure 5a. 0.1Hz to 10Hz Noise Test Circuit

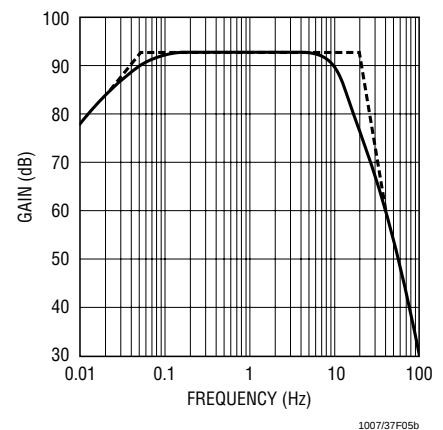


Figure 5b. 0.1Hz to 10Hz Peak-to-Peak Noise Tester Frequency Response

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APPLICATIONS INFORMATION

The LT1007/LT1037 achieve their low noise, in part, by operating the input stage at 120μA versus the typical 10μA of most other op amps. Voltage noise is inversely proportional while current noise is directly proportional to the square root of the input stage current. Therefore, the LT1007/LT1037's current noise will be relatively high. At low frequencies, the low 1/f current noise corner frequency (≈120Hz) minimizes current noise to some extent.

In most practical applications, however, current noise will not limit system performance. This is illustrated in the Total Noise vs Source Resistance plot in the Typical Performance Characteristics section, where:

$$\text{Total Noise} = [(\text{voltage noise})^2 + (\text{current noise} \cdot R_S)^2 + (\text{resistor noise})^2]^{1/2}$$

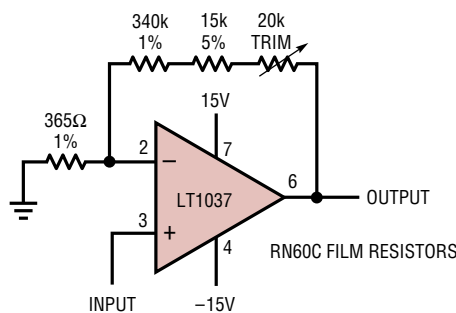
Three regions can be identified as a function of source resistance:

- (i) $R_S \leq 400\Omega$. Voltage noise dominates
- (ii) $400\Omega \leq R_S \leq 50k$ at 1kHz } Resistor noise dominates
- $400\Omega \leq R_S \leq 8k$ at 10Hz }
- (iii) $R_S > 50k$ at 1kHz } Current noise dominates
- $R_S > 8k$ at 10Hz }

Clearly the LT1007/LT1037 should not be used in region (iii), where total system noise is at least six times higher than the voltage noise of the op amp, i.e., the low voltage noise specification is completely wasted.

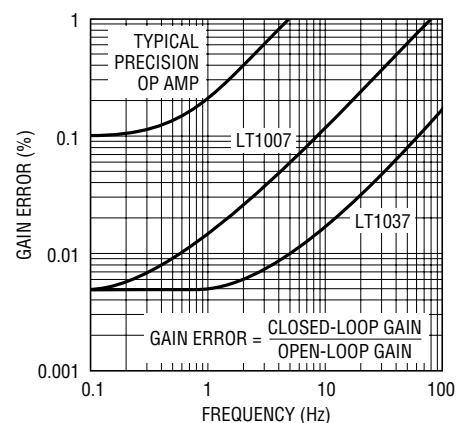
TYPICAL APPLICATIONS

Gain 1000 Amplifier with 0.01% Accuracy, DC to 5Hz



THE HIGH GAIN AND WIDE BANDWIDTH OF THE LT1037 (AND LT1007) IS USEFUL IN LOW FREQUENCY, HIGH CLOSED-LOOP GAIN AMPLIFIER APPLICATIONS. A TYPICAL PRECISION OP AMP MAY HAVE AN OPEN-LOOP GAIN OF ONE MILLION WITH 500kHz BANDWIDTH. AS THE GAIN ERROR PLOT SHOWS, THIS DEVICE IS CAPABLE OF 0.1% AMPLIFYING ACCURACY UP TO 0.3Hz ONLY. EVEN INSTRUMENTATION RANGE SIGNALS CAN VARY AT A FASTER RATE. THE LT1037'S "GAIN PRECISION-BANDWIDTH PRODUCT" IS 200 TIMES HIGHER AS SHOWN.

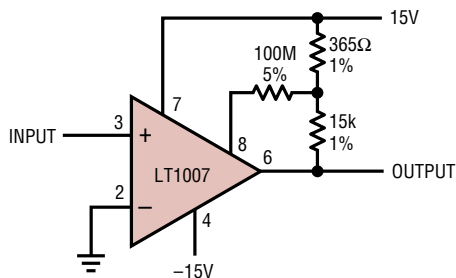
Gain Error vs Frequency
Closed-Loop Gain = 1000



1007/37 TA03

TYPICAL APPLICATIONS

Microvolt Comparator with Hysteresis

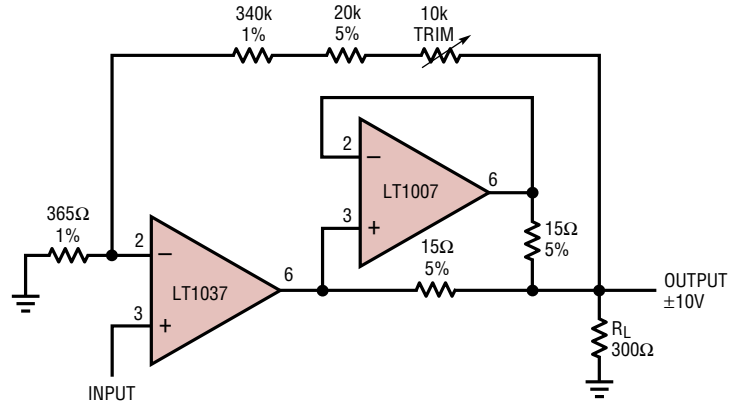


POSITIVE FEEDBACK TO ONE OF THE NULLING TERMINALS CREATES APPROXIMATELY $5\mu\text{V}$ OF HYSTERESIS. OUTPUT CAN SINK 16mA .

INPUT OFFSET VOLTAGE IS TYPICALLY CHANGED LESS THAN $5\mu\text{V}$ DUE TO THE FEEDBACK.

1007/37 TA04

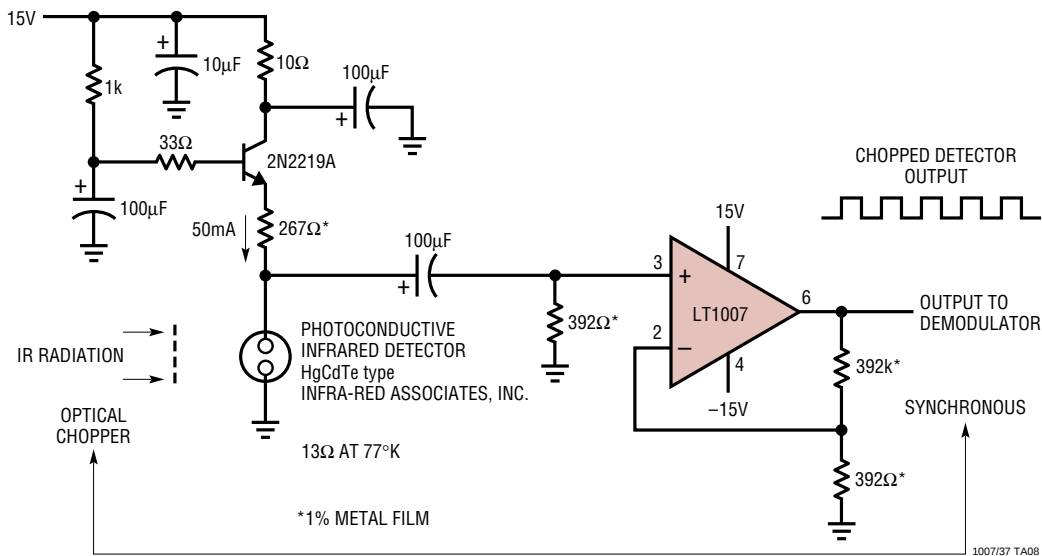
Precision Amplifier Drives 300Ω Load to $\pm 10\text{V}$



THE ADDITION OF THE LT1007 DOUBLES THE AMPLIFIER'S OUTPUT DRIVE TO $\pm 33\text{mA}$. GAIN ACCURACY IS 0.02% , SLIGHTLY DEGRADED COMPARED TO ABOVE BECAUSE OF SELF-HEATING OF THE LT1037 UNDER LOAD.

1007/37 TA05

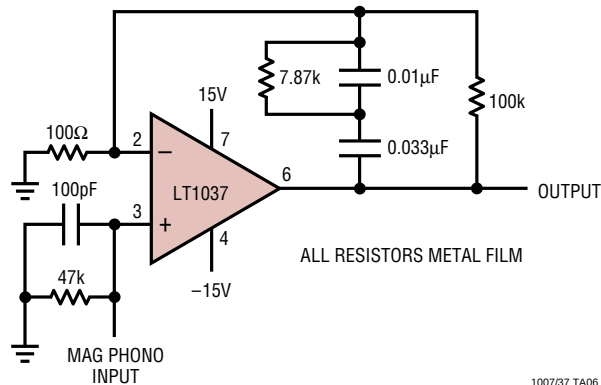
Infrared Detector Preamplifier



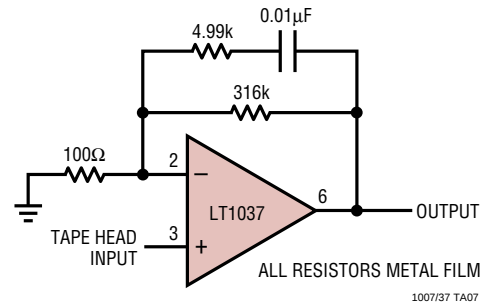
1007/37 TA08

TYPICAL APPLICATIONS

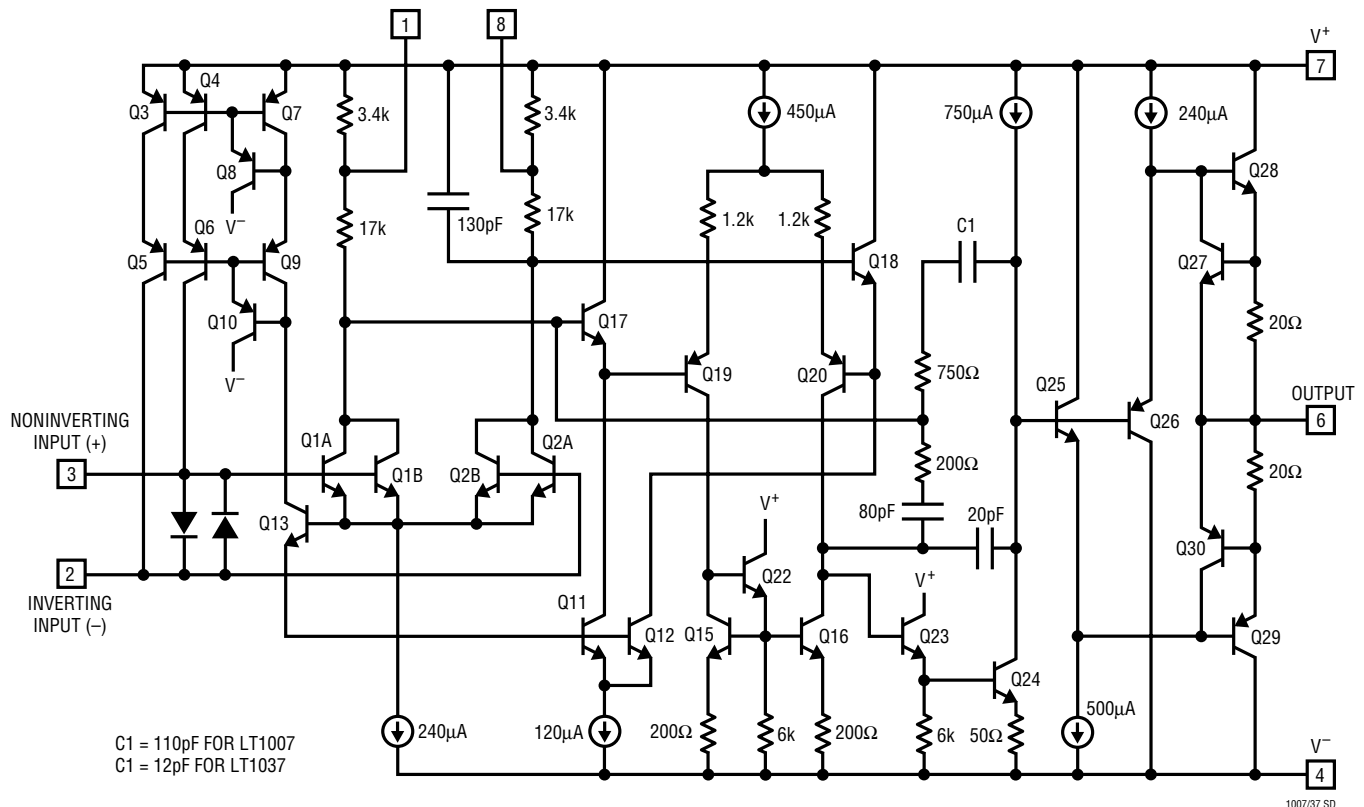
Phono Preamplifier

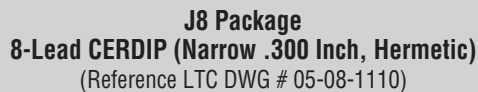


Tape Head Amplifier



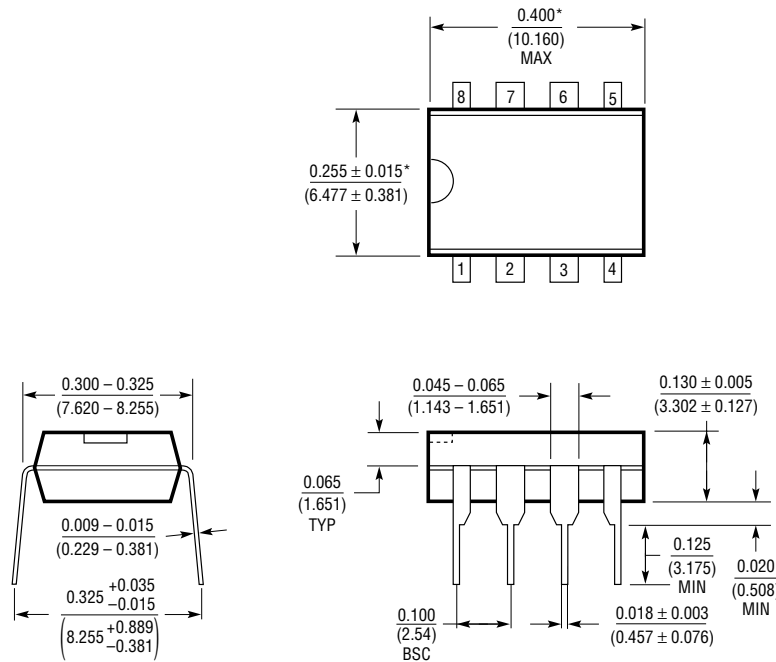
SIMPLIFIED SCHEMATIC





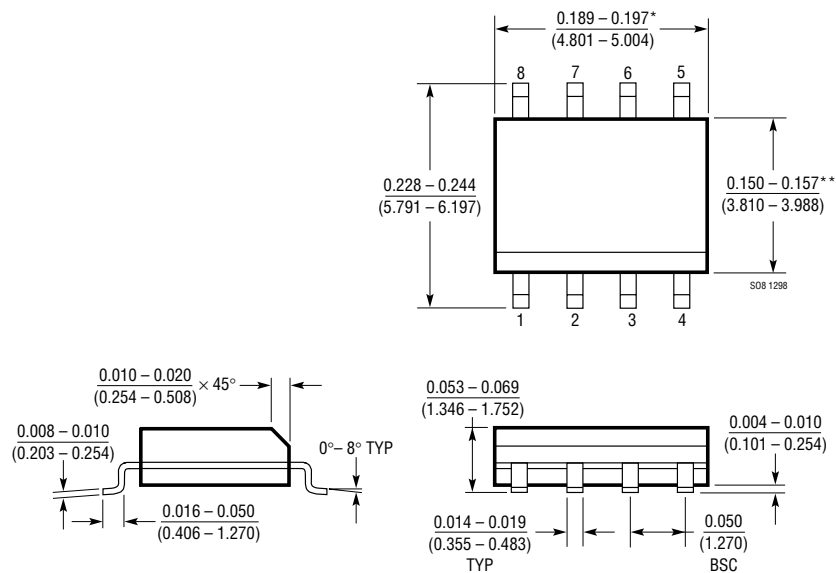
PACKAGE DESCRIPTION

N8 Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



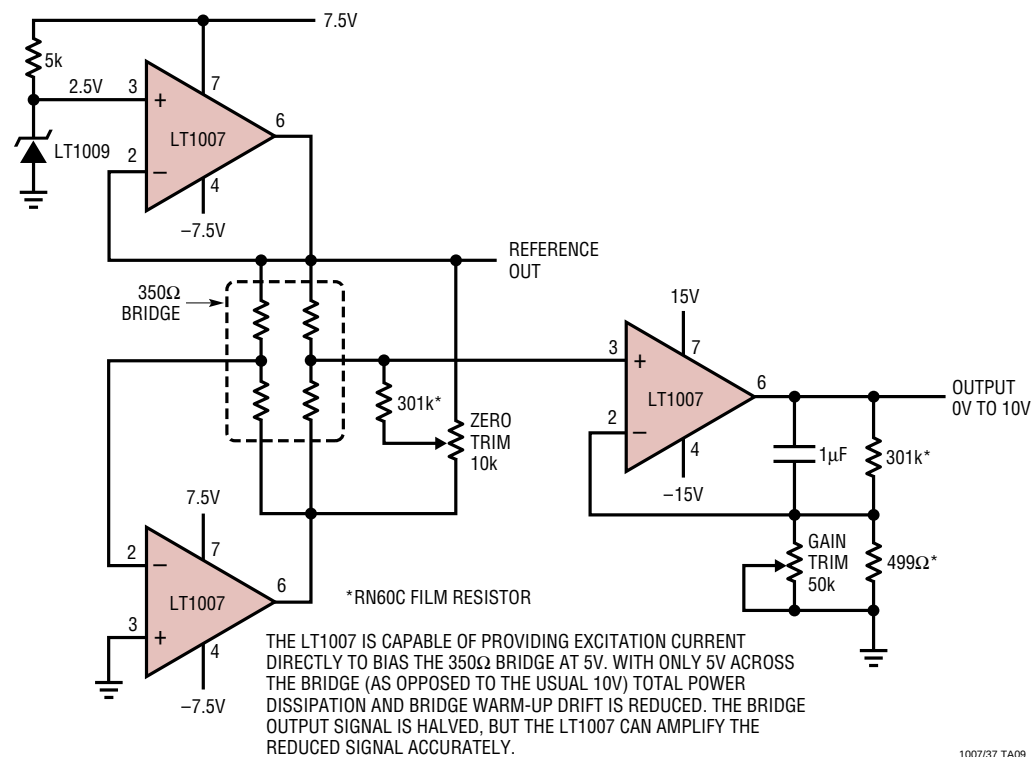
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

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TYPICAL APPLICATION

Strain Gauge Signal Conditioner with Bridge Excitation



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1028	Ultralow Noise Precision Op Amp	Lowest Noise 0.85nV/√Hz
LT1115	Ultralow Noise, Low distortion Audio Op Amp	0.002% THD, Max Noise 1.2mV/√Hz
LT1124/LT1125	Dual/Quad Low Noise, High Speed Precision Op Amps	Similar to LT1007
LT1126/LT1127	Dual/Quad Decompensated Low Noise, High Speed Precision Op Amps	Similar to LT1037
LT1498/LT1499	10MHz, 5V/μs, Dual/Quad Rail-to-Rail Input and Output Precision C-Load™ Op Amps	

C-Load is a trademark of Linear Technology Corporation.