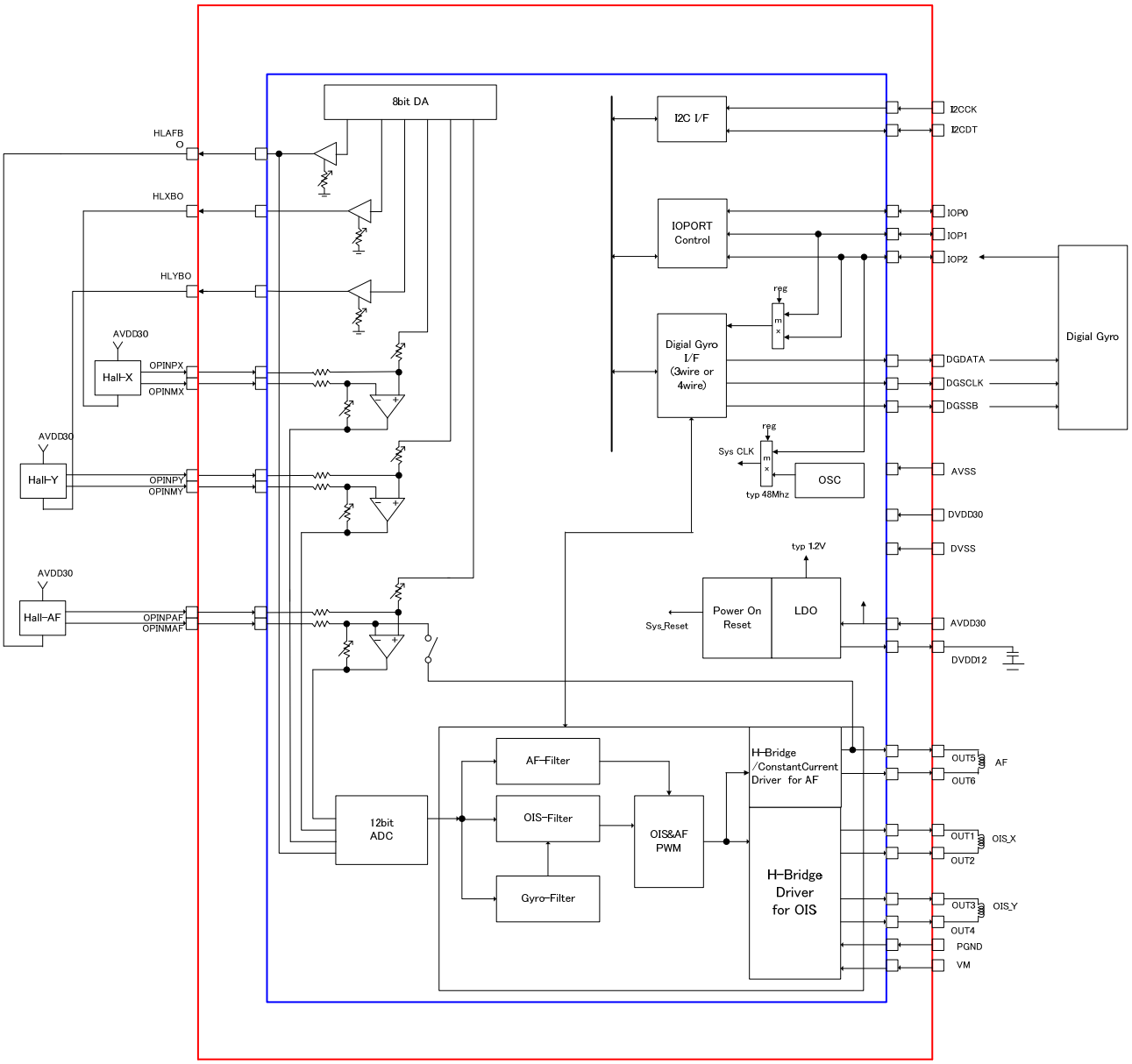
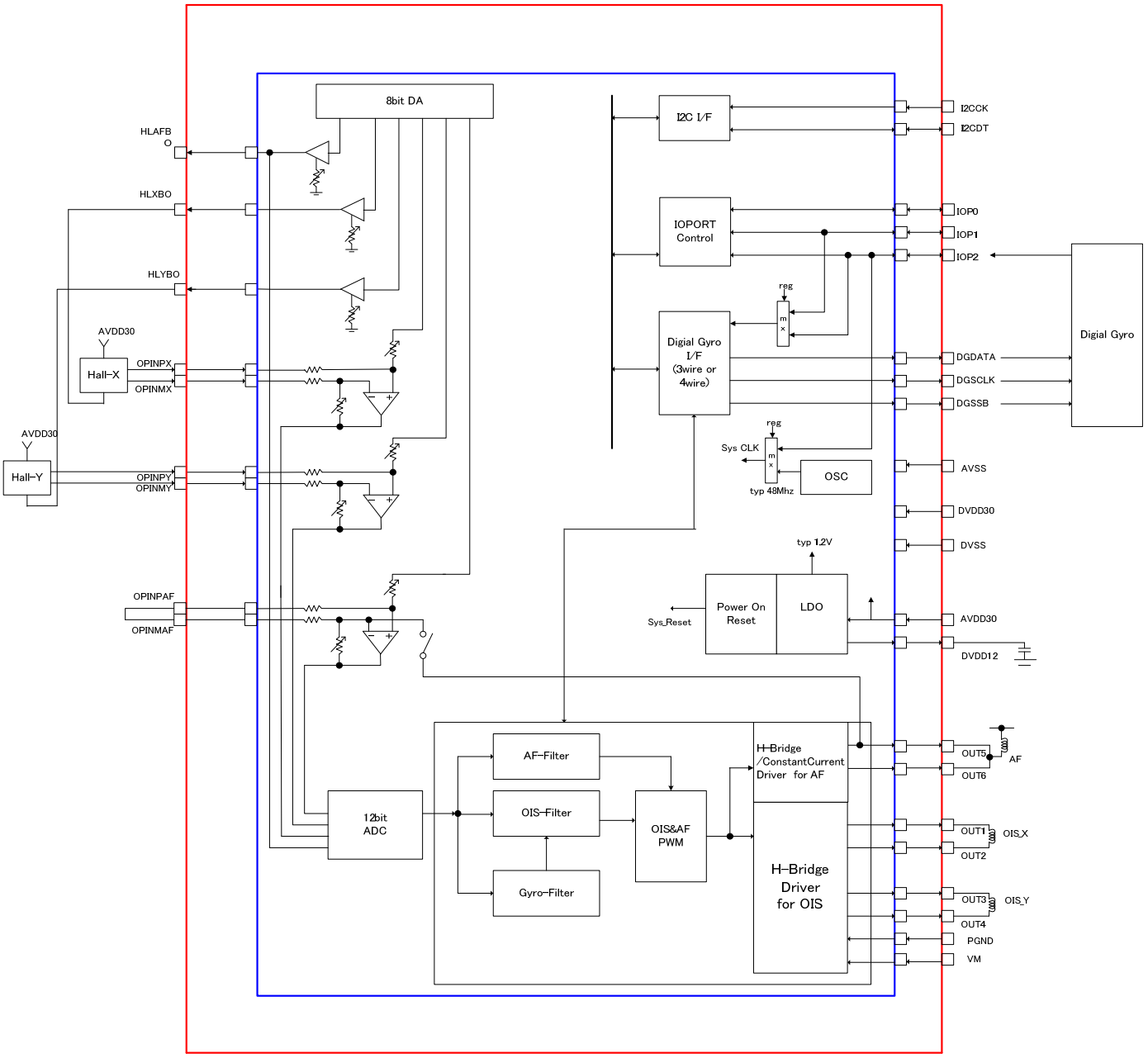
Block Diagram



Example of wiring diagram [Hall, Closed AF] in LC898122AXA

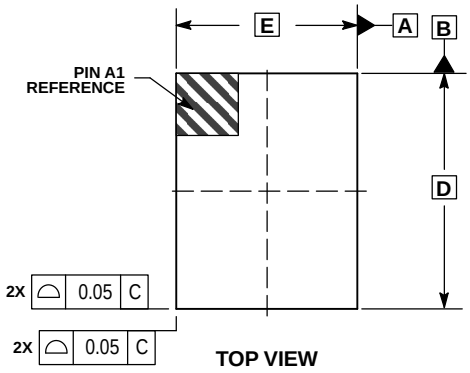


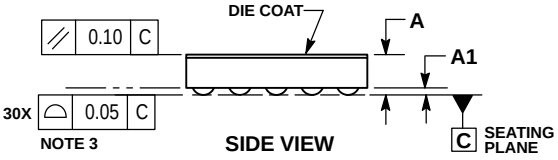
Example of wiring diagram [Hall(OIS), Open AF] in LC898122AXA

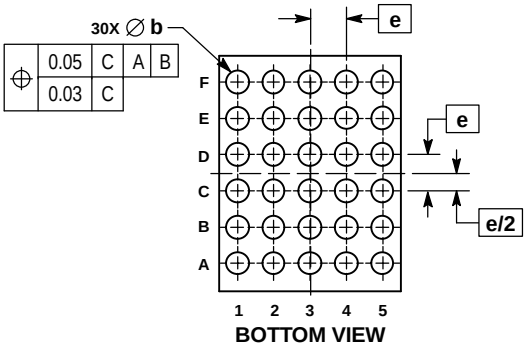
Package Dimensions

unit : mm

WLCSP30, 2.59x1.99
CASE 567HG
ISSUE O



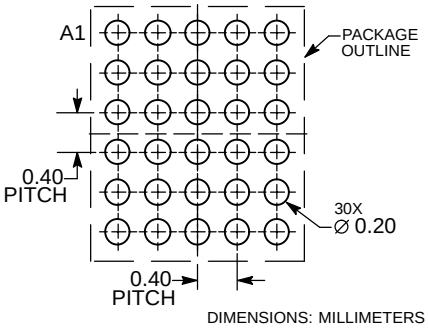




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.45
A1	0.03	0.13
b	0.15	0.25
D	2.59 BSC	
E	1.99 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Assignment

Bottom view

	F	E	D	C	B	A
5	OUT5	OUT4	OUT3	PGND	OUT2	OUT1
4	OUT6	DGDATA	DGSSB	VM	I2CDT	I2CCK
3	HLAFBO	DVSS	DGSCLK	DVDD30	IOP2	IOP1
2	HLYBO	HLXBO	OPINMAF	OPINMX	OPINMY	IOP0
1	OPINPAF	OPINPX	OPINPY	AVSS	AVDD30	DVDD12

Driver
Analog VDD
Analog GND
Digital GND
Digital VDD
Logic Core VDD (Output)

<typ> I : INPUT, O : OUTPUT, B : BIDIRECTION, P : Power

Ball No.	Pin Name	type	Description
A1	DVDD12	P	LDO Power supply out (Logic Core VDD (typ 1.2V))
A2	IOP0	B	General-purpose IOPORT
A3	IOP1	B	General-purpose IOPORT
A4	I2CCK	I	I2C IF clock
A5	OUT1	O	OIS Driver output (H bridge)
B1	AVDD30	P	Analog Power (2.6 to 3.6V)
B2	OPINMY	I	OIS Hall-Y OpAmp input-
B3	IOP2	B	General-purpose IOPORT/ External Clock input (switch from OSC at Register)
B4	I2CDT	B	I2C_IF Data
B5	OUT2	O	OIS Driver output (H bridge)
C1	AVSS	P	Analog GND
C2	OPINMX	I	OIS Hall-X OpAmp input-
C3	DVDD30	P	IO Power (2.6V to 3.6V)
C4	VM	P	Driver Power (2.6V to 3.6V)
C5	PGND	P	Driver GND
D1	OPINPY	I	Hall-Y Bias (Current Drive) for OIS
D2	OPINMAF	I	AF Hall OpAmp input-
D3	DGSCLK	B	Digital Gyro IF clock / General-purpose IOPORT
D4	DGSSB	B	Digital Gyro IF Chip Select / General-purpose IOPORT
D5	OUT3	O	OIS Driver output (H bridge)
E1	OPINPX	I	Hall-X OpAmp input+ for OIS
E2	HLXBO	O	Hall-X Bias (Current Driver) for OIS
E3	DVSS	P	Logic GND
E4	DGDATA	B	Digital Gyro IF Data (3wire : Data in/out, 4wire : Data out)
E5	OUT4	O	OIS Driver output (H bridge)
F1	OPINPAF	I	AF Hall OpAmp input+
F2	HLYBO	O	Hall-Y Bias (current drive) for OIS
F3	HLAFBO	O	Hall Bias (current drive) for AF
F4	OUT6	O	AF Driver output (H bridge/constant current)
F5	OUT5	O	AF Driver output (H bridge/constant current)

Pin Description

<typ> I : INPUT, O : OUTPUT, B : BIDIRECTION, P : Power,GND

	Pin name	typ	Pin Description	function change method (first function in Reset)
I2C IF	I2CCK	I	I2C clock input	
	I2CDT	B	I2C data	
Digital Gyro IF	DGDATA	B	3-wire Digital Gyro I/f Data	Change at Register
		O	4-wire Digital Gyro I/f Data output	
		B	General-purpose IOPORT	
		O	inner signal monitor	
	DGSCLK	O	3-wire /4-wire Digital Gyro SPI I/f clock	Change at Register
		B	General-purpose IOPORT	
		O	inner signal monitor	
	DGSSB	O	3-wire/4-wireDigital Gyro I/f Chip Select	Change at Register
		B	General-purpose IOPORT	
		O	inner signal monitor	
IOPORT	IOP0	B	General-purpose IOPORT	Change at Register
		O	inner signal monitor	
		O	pin for servo evaluation	
	IOP1	B	General-purpose IOPORT	Change at Register
		O	inner signal monitor	
		I	pin for servo evaluation	
		I	4-wire Digital Gyro data input	
	IOP2	B	General –purpose IOPORT (OpenDrain output)	Change at Register
		O	inner signal monitor	
		I	pin for servo evaluation	
		I	4-wire Digital Gyro data input	
		I	External Clock (all block/OIS_PWM/AF_PWM) switch External Clock at register CLKSEL[020Ch] from OSC	
DAC I/F	HLXBO	O	Bias for Hall-X (current drive)	
	HLYBO	O	Bia for Hall-Y (current drive)	
OpAmp	OPINPX	I	Hall-X OpAmp input+ for OIS	
	OPINMX	I	Hall-X OpAmp input- for OIS	
	OPINPY	I	Hall-Y OpAmp input+ for OIS	
	OPINMY	I	Hall-Y OpAmp input- for OIS	
	OPINPAF	I	Hall OpAmp input+ for AF	
	OPINMAF	I	HallOPAmp input- for AF	
Driver I/F	OUT1	O	Driver Saturation-drive H bridge output (1st channel) for OIS	
	OUT2	O	Driver Saturation-drive H bridge output (1st channel) for OIS	
	OUT3	O	Driver Saturation-drive H bridge output (2nd channel) for OIS	
	OUT4	O	Driver Saturation-drive H bridge output (2nd channel) for OIS	
	OUT5	O	Driver Saturation-drive H bridge/constant current output for AF	
	OUT6	O	Driver Saturation-drive H bridge/constant current output for AF	
Power	VM	P	Driver power supply	
	PGND	P	Driver GND	
	AVDD30	P	Analog power supply	
	AGND	P	Analog GND	
	DVDD30	P	IO power supply	
	DVDD12	P	Logic power output (LDO output)	
	DVSS	P	Logic GND	

Electrical Characteristics

Logic

1) Absolute Maximum Rating at V_{SS}= 0V

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}30 max	Ta ≤ 25°C	–0.3 to 4.6	V
	V_{DD}30 max	Ta ≤ 25°C	–0.3 to 4.6	V
Input/Output voltage	V_{AI}30,V_{AO}30	Ta ≤ 25°C	–0.3 to V_{AD}30+0.3	V
	V_{DI}30,V_{DO}30	Ta ≤ 25°C	–0.3 to V_{AD}30+0.3	V
Storage temperature	Tstg		–55 to 125	°C
Operating temperature	Topr		–30 to 85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2) Alowable Operating Ratings at Ta = –30 to 85°C,V_{SS} = 0V

3.0V Power Supply (AVDD30)

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{AD}30	2.6	3.0	3.6	V
Input voltage range	V_{IN}	0	-	3.6	V

3.0V Power Supply (DVDD30)

Paramter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{DD}30	2.6	3.0	3.6	V
Input voltage range	V_{IN}	0	-	V_{DD}30	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3) D.C. Characteristics : Input/Output Vss= 0V, Vdd=2.6 to 3.6V, Vdd2=2.6 to 3.6V, Ta = –30 to 85°C

Parameter	Symbol	Conditions	Min	Typ	Max	unit	Applicable pin
High-level input voltage	VIH	CMOS schmidt	1.48			V	I2CCK, I2CDT, IOP2
Low-level input voltage	VIL				0.37	V	
High-level input voltage	VIH	CMOS supported	1.40				DGDATA, DGSCLK, DGSSB, IOP0, IOP1
Low-level input voltage	VIL				0.51	V	
High-level output voltage	VOH	IOH=–2mA	Vdd-0.4			V	DGDATA, DGSCLK, DGSSB, IOP0, IOP1, IOP2
Low-level output voltage	VOL	IOL= 2mA			0.4	V	
Low-level output voltage	VOL	IOL= 2mA			0.2	V	I2CDT
Analog input voltage	VAI		Vss		Vdd2	V	OPINPX, OPINMX, OPINPY, OPINMY
PullUp resistor	Rup		50		200	KΩ	DGDATA, DGSCLK, DGSSB, IOP0, IOP1, IOP2
PullDown resistor	Rdn		50		220	KΩ	DGDATA, DGSCLK, DGSSB, IOP0, IOP1, IOP2

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Driver

1) Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Symbol
Power supply voltage	VMmax		4.6	V
Output peak current	Iopeak	OUT1 to 4 t ≤ 10ms, ON-duty ≤ 20%	300	mA
		OUT5, OUT6 t ≤ 10ms, ON-duty ≤ 20%	200	mA
Output continuous current	Iomax	OUT1 to 4	220	mA
		OUT5,OUT6	150	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2) Operating Range

Parameter	Symbol	Condition	Ratings	Symbol
Ambient temperature	Topg		–30 to +85	°C
Power supply voltage	VM		2.6 to 3.6	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3) H-Bridge Driver Output at Ta=25°C, VM=3.0V

Parameter	Symbol	Condition	Ratings (Ω)	Symbol
Output ON resistance OUT1 to OUT4	Ronu	Io=220mA(Pch)	2.0	Ω
	Rond	Io=220mA(Nch)	1.0	Ω
Output ON resistance OUT5, OUT6	Ronu	Io=150mA(Pch)	1.0	Ω
	Rond	Io=150mA(Nch)	2.0(*)	Ω

(*) include Constant current detect resistance

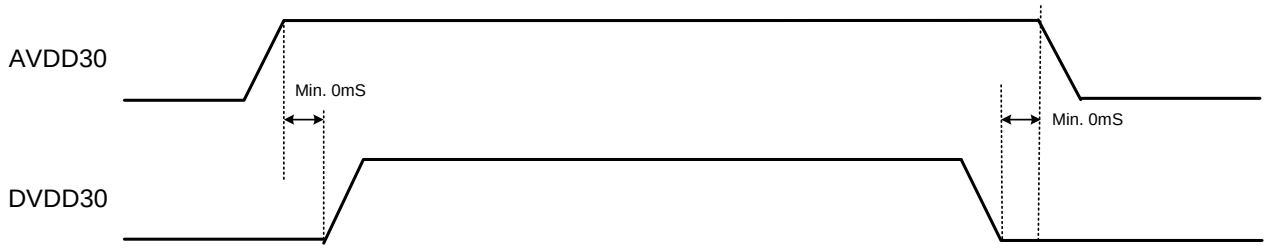
4) Constant Current Open-AF Driver output at Ta=25°C, VM=2.8V

	condition 1	condition 2	output current *1
	DAC code of AF Driver AF_D[9:0]	DAC gain of AF Driver DGAINDAF(0083h[6:4]) (AF_GAIN_D[2:0])	typ
OUT5, OUT6	3FFh (Full Code)	4	150mA

*1 output current is calculated by registance of VCM and
(the drain-source voltage of Nch Driver Tr) + (sense registance voltage).
ex. In the case of "VM=3V" and "output current=100mA"
(the drain-source voltage of Nch Driver Tr) + (sense registance voltage)= max 0.5V.
VCM registance (Rvcm) = (2.8-0.5) / 0.1 = 23Ω

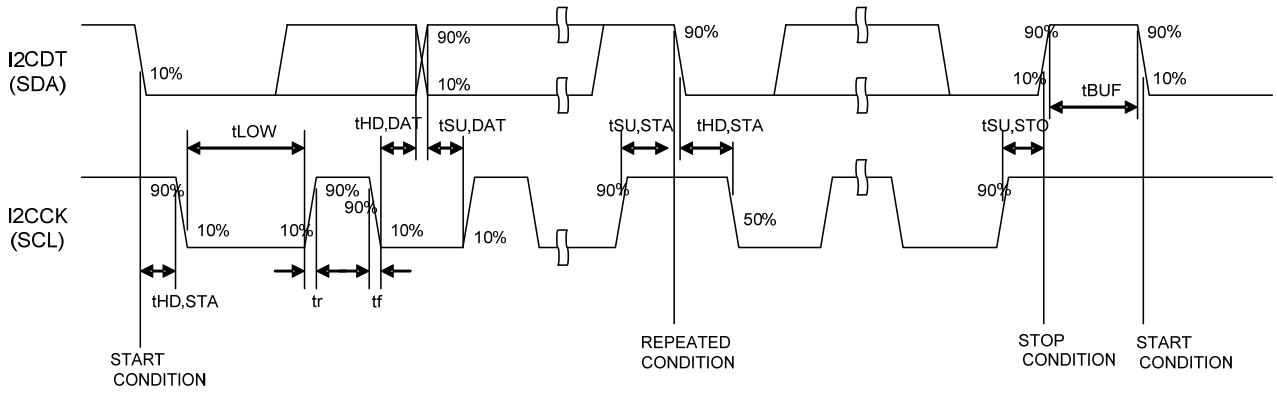
AC Characteristics

Power Sequence



(*) Don't care about injection order of VM

I²C Interface Timing



I²C interface timing definition

Item	Symbol	Pin name	Min	Typ	Max	Units
SCL clock frequency	Fscl	I2CCK			400	KHz
START condition hold time	tHD,STA	I2CCK I2CDT	0.6			µs
SCL clock Low period	tLOW	I2CCK	1.3			µs
SCL clock High period	tHIGH	I2CCK	0.6			µs
Setup time for repetition START condition	tSU,STA	I2CCK I2CDT	0.6			µs
Data hold time	tHD,DAT	I2CCK I2CDT	0 (*1)		0.9	µs
Data setup time	tSU,DAT	I2CCK I2CDT	100			µs
SDA, SCL rising time	tr	I2CCK I2CDT			300	µs
SDA, SCL falling time	tf	I2CCK I2CDT			300	µs
STOP condition setup time	tSU,STO	I2CCK I2CDT	0.6			µs
Bus free time between STOP and START	tBUF	I2CCK I2CDT	1.3			µs

(*1) Although the I²C specification defines a condition that 300 ns of hold time is required internally, LC898122XA is designed for a condition with typ. 30 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC898122AXA-VH	WLCSP30, 2.59x1.99 (Pb-Free / Halogen Free)	5000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF