

LB1863M, LB1869M

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Conditions	Ratings	Unit
$I_{CC\ max}$	Maximum input current	$t \leq 20\ ms$	200	mA
V_{OUT}	Output voltage	LB1863M LB1869M	-0.3 to +85 -0.3 to +60	V
I_{OUT}	Output current		1.5	A
I_{RD}	RD influx current		10	mA
V_{RD}	RD voltage		30	V
$P_d\ max$	Allowable power dissipation	When mounted (on a $20 \times 15 \times 1.5\text{-mm}^3$ glass-epoxy printed circuit board)	800	mW
T_{opr}	Operating temperature		-30 to +80	$^\circ\text{C}$
T_{stg}	Storage temperature		-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ALLOWABLE OPERATING RANGES ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Conditions	Ratings	Unit
I_{CC}	Input Current Range		6.0 to 50	mA
V_{ICM}	Common-mode Input Voltage Range		0 to $V_{IN} - 1.5$	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $I_{CC} = 10\ mA$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OR}	Output Voltage 1	LB1863M	80	-	-	V
		LB1869M	60	-	-	V
$V_{O(SUS)}$	Output Voltage 2	LB1863M: $I_O = 0.1\ A$	65	-	-	V
		LB1869M: $I_O = 0.1\ A$	40	-	-	V
$V_{O(sat)1}$	Output Saturation Voltage	$I_O = 0.5\ A$	-	0.95	1.2	V
$V_{O(sat)2}$		$I_O = 1.0\ A$	-	1.15	1.5	V
V_{IN}	Input Voltage	$I_{CC} = 7.0\ mA$	6.4	6.7	7.0	V
V_{OFF}	Amplifier Input Offset Voltage		-7	0	+7	mV
I_{BA}	Amplifier Input Bias Current		-250	-	-	nA
$V_{RD(sat)}$	RD Output Saturation Voltage	$I_{RD} = 5\ mA$	-	0.1	0.3	V
I_{C1}	Capacitor Discharge Current		2.1	3	3.9	μA
I_{C2}			0.31	0.44	0.59	μA
V_{TH1}	Comparator Input Threshold Voltage		0.77	$0.8\ V_{IN}$	0.83	V
V_{TH2}			0.42	$0.45\ V_{IN}$	0.48	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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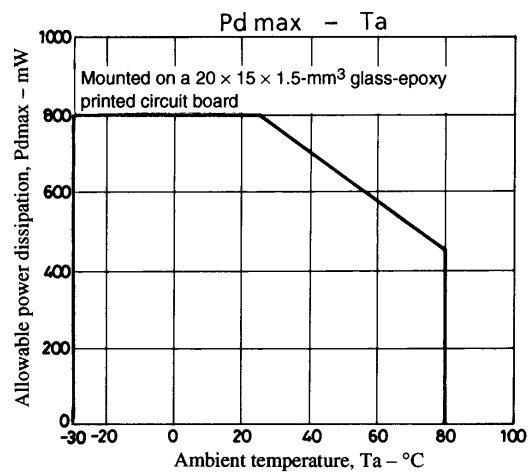
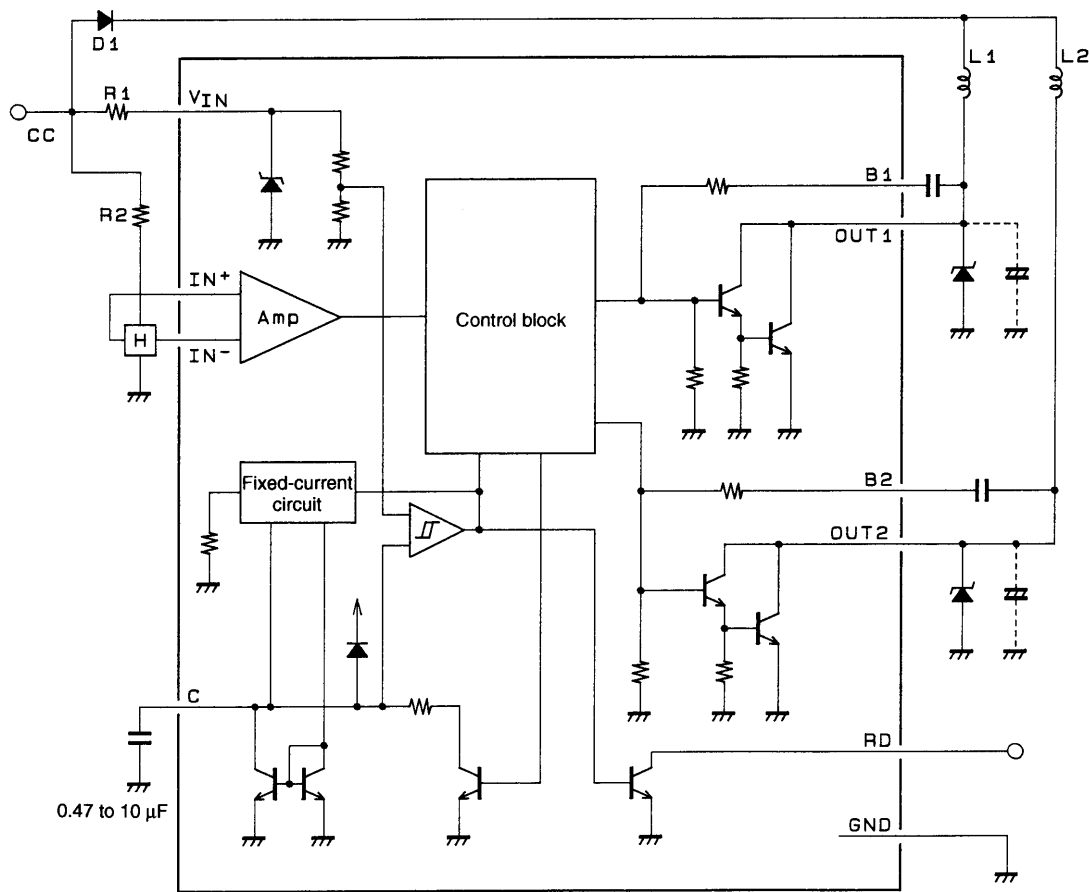


Figure 1. Pd max - TA

BLOCK DIAGRAM



A02886

Figure 2. Block Diagram

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APPLICATION CIRCUIT

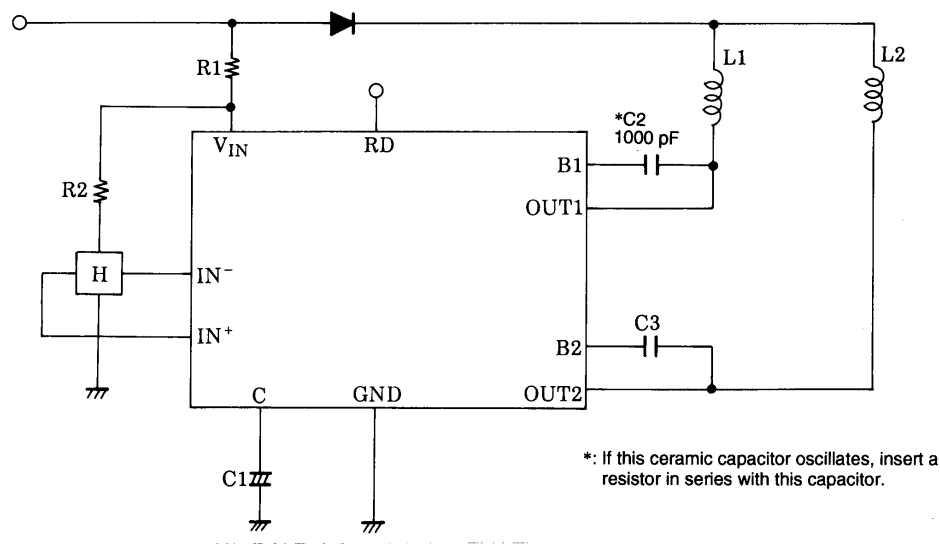


Figure 3. Sample Application Circuit

SAMPLE APPLICATION CIRCUIT OUTPUT WAVEFORMS

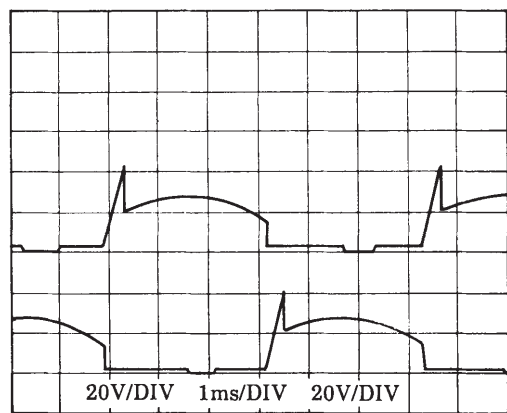


Figure 4. Output Waveforms

TRUTH TABLE

IN+	IN-	C	OUT1	OUT2	RD
H	L	L	H	L	L
L	H		L	H	
H	L	H	H	H	H
L	H		H	H	

DESIGN DOCUMENTATION

(See the Application Circuit Diagram)

1. Power-supply Voltage (V_{IN} Pin)

Since these miniature flat package products supply power to the Hall amplifier block and the control block from an internal parallel regulator, they operate with good stability with respect to kickback currents from the motor and variations in the power-supply voltage. They also provide an adequate ability to withstand surges. The resistor $R1$ between the V_{CC} and V_{IN} pins should be set up so that a current in the range $I_{CC} = 6$ to 50 mA flows into the V_{IN} pin in the fan motor power-supply voltage range.

V_{IN} has a typical value of 6.7 V when I_{CC} is 7 mA. The current flowing into V_{IN} can be calculated with the following formula.

$$I_{CC} = \frac{V_{CC} - V_{IN}}{R1} \quad (\text{eq. 1})$$

- Abnormal voltage considerations

The maximum allowable current for the V_{IN} pin is 200 mA. Therefore, the IC design allows it to withstand voltages up to the plus side abnormal voltage V_{surge} give by formula (2).

$$V_{surge} = V_{IN} + R1 \times 20 \text{ mA} \quad (\text{eq. 2})$$

2. Hall Input Pin Voltages (IN– and IN+ Pins)

The Hall element output voltages to the Hall element input pins must be in the range 0 to $(V_{IN} - 1.5 \text{ V})$. The gain from the Hall input pins to the output pin is over 100 dB. The Hall input amplifier offset voltage is ± 7 mV. This means that the Hall element output must be set up taking this ± 7 mV offset into account.

3. Output Transistors (OUT1 and OUT2 Pins)

Output current: $I_O = 1.5$ A maximum

Output saturation voltage: $V_{Osat} = 1.15$ V/ 1.0 A (typical)

Applications should adopt one of the following three output protection techniques.

- ① If a capacitor is inserted between OUT and ground, use a capacitor with a value up to $C = 10 \mu\text{F}$, and design that value so that the kickback and reverse voltages do not exceed V_{OR} .
- ② If a Zener diode is added, determine a value for the Zener voltage that is lower than $V_{O(SUS)}$. If radio-frequency noise is a problem, insert a capacitor between B1 and B2.
- ③ If a capacitor is inserted between OUT and B1, set the capacitor value so that the kickback voltage is lower than $V_{O(SUS)}$. If oscillation occurs, insert a resistor in series with the capacitor.

4. Output Protection Function (C Pin)

This pin connects the capacitor that forms the automatic recovery circuit. If rotation stops due to, for example, a motor overload, the pin voltage rises and the output stops. The system automatically recovers from stopped to drive mode when the load is set to an appropriate level. The lock detection time can be set by changing the value of the capacitor.

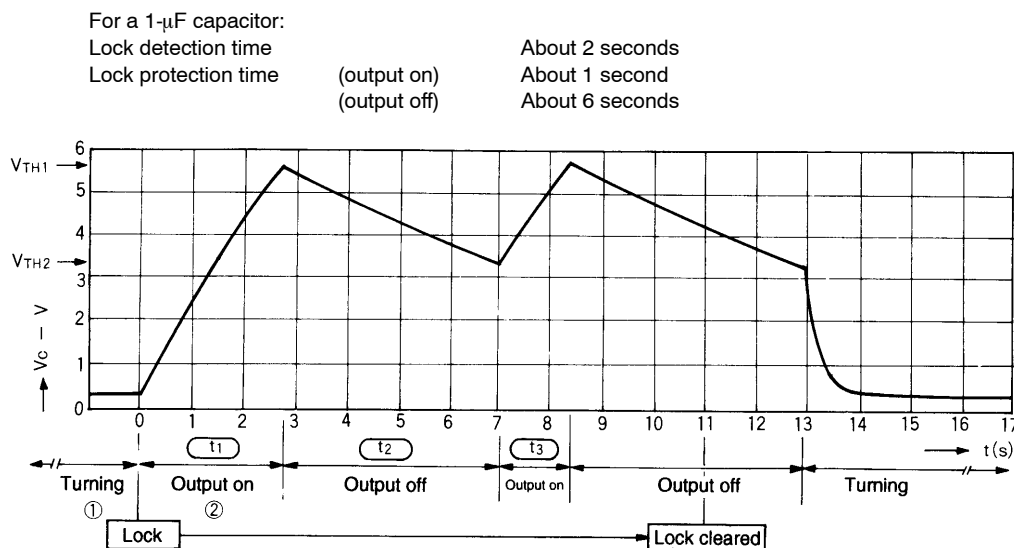


Figure 5. Automatic Recovery Circuit Pin C Voltage

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- ① While the blades are turning, the capacitor is charged with a current of about 3 μA (typical), and C is discharged by pulses that correspond to the motor speed.
 - ② When the blades lock, the capacitor is no longer discharged, and the voltage across the capacitor increases. The output is turned off when that voltage reaches $0.8 \times V_{\text{IN}}$.
 - ③ When the output is turned off, the capacitor is discharged at a current of about 0.44 μA (typical). When the capacitor voltage falls under V_{TH2} , if the lock state is not yet cleared the capacitor continues discharging until V_{TH1} . (Note that the output is turned on at this time.) These operations, i.e. items ② and ③, are repeated with a ton:toff ratio of about 1:6 to protect the motor.
 - ④ If the lock state has been cleared when the capacitor voltage reaches V_{TH2} , motor rotation is started by turning the output on.
5. Rotation Detection Signal (RD Pin)
This is an open collector output, and outputs a low level in drive mode and a high level when the motor is stopped.
 6. Radio-frequency Noise Reduction Function (B1 and B2 Pins)
These are base pins for Darlington pair outputs. Add capacitors of about 0.01 to 0.1 μF if radio-frequency noise is a problem.
 7. Thermal Shutdown Function
Turns off the output in response to coil shorting or IC overheating.

ORDERING INFORMATION

Device	Package	Wire Bond	Shipping† (Qty / Packing)
LB1863M-MPB-E	SOIC14 W / MFP14S (225 mil) (Pb-Free)	Au wire	60 / Fan-Fold
LB1863M-MPB-H	SOIC14 W / MFP14S (225 mil) (Pb-Free / Halogen Free)	Au wire	60 / Fan-Fold
LB1863M-TLM-E	SOIC14 W / MFP14S (225 mil) (Pb-Free)	Au wire	1,000 / Tape & Reel
LB1863M-TLM-H	SOIC14 W / MFP14S (225 mil) (Pb-Free / Halogen Free)	Au wire	1,000 / Tape & Reel
LB1863M-W-AH	SOIC14 W / MFP14S (225 mil) (Pb-Free / Halogen Free)	Cu wire	1,000 / Tape & Reel
LB1869M * Discontinued	SOIC14 W / MFP14S (225 mil) (Pb-Free)	Au wire	- / -

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

MECHANICAL CASE OUTLINE

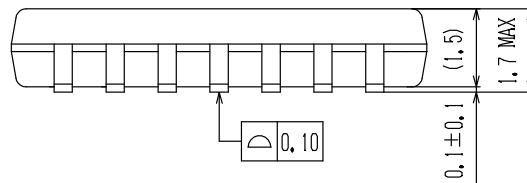
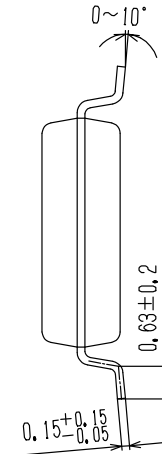
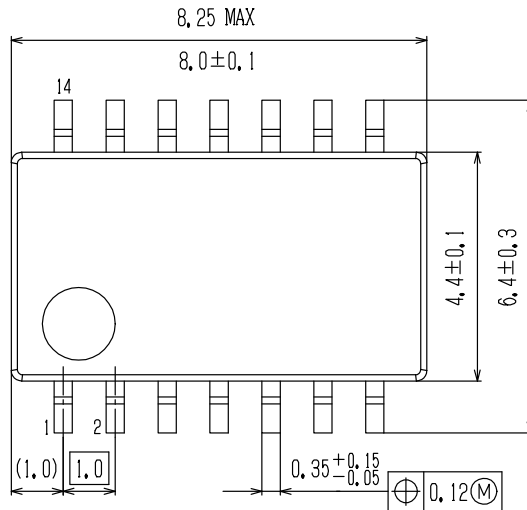
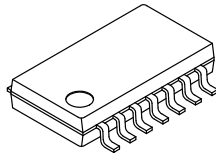
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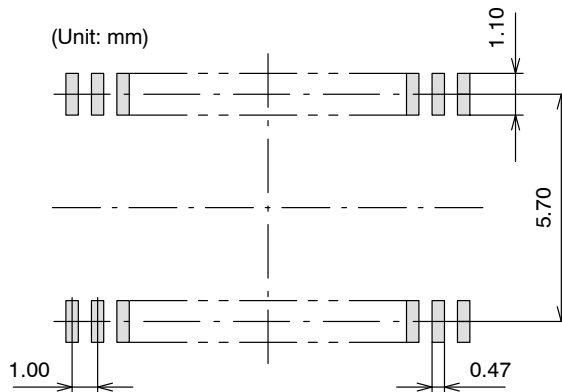
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CASE 751CB
ISSUE A

DATE 25 OCT 2013



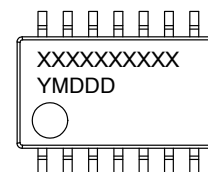
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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