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1 Block diagram and pin information

Figure 1. Block diagram

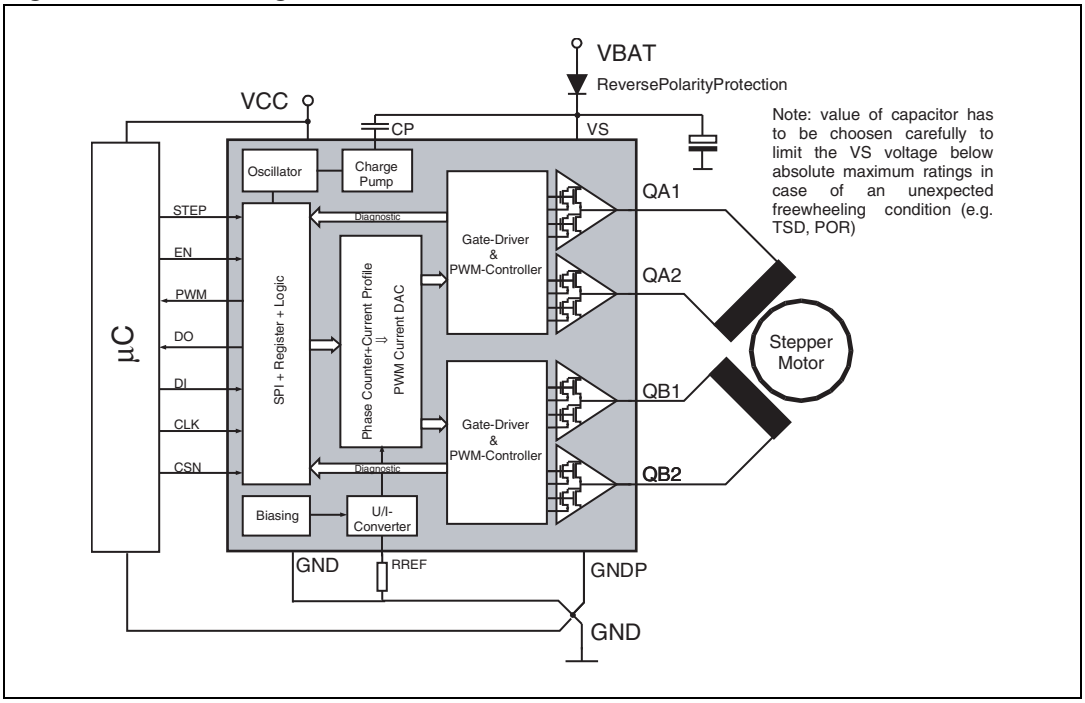
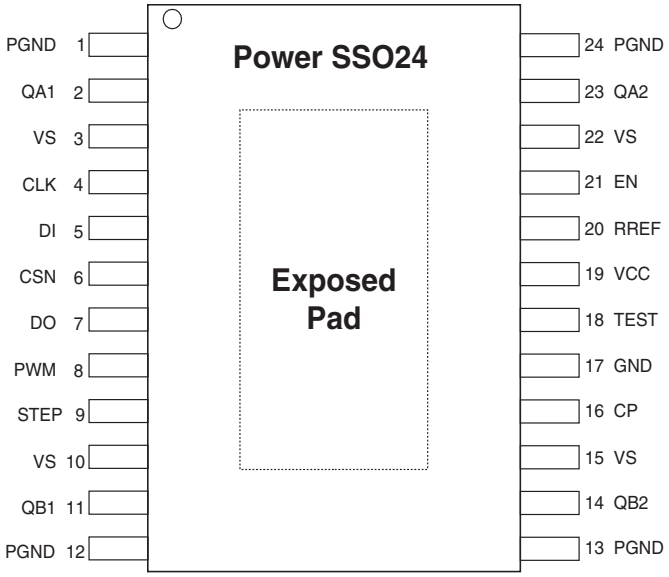


Figure 2. Pin connection (top view)



All pins with the same name must be externally connected!

All pins PGND are internally connected to the heat slug.

Table 2. Pin description

Pin	Symbol	Function
1, 12, 13, 24	PGND	**Power ground:** All pins PGND are internally connected to the heat slug. ***Important:*** All pins of PGND must be externally connected!
3, 10, 15, 22	VS	**Power supply voltage (external reverse protection required):** For EMI reason a ceramic capacitor as close as possible to PGND is recommended. ***Important:*** All pins of VS must be externally connected!
2, 23	QA1,QA2	**Fullbridge-outputs An:** The output is built by a high-side and a low-side switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal reverse diode (bulk-drain-diode: highside driver from output to VS, low-side driver from PGND to output). This output is overcurrent protected.
11, 14	QB1,QB2	**Fullbridge-outputs Bn:** The output is built by a highside and a low-side switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal reverse diode (bulk-drain-diode: highside driver from output to VS, low-side driver from PGND to output). This output is overcurrent protected.
4	CLK	**SPI clock input:** The input requires CMOS logic levels. The CLK input has a pull-down current. It controls the internal shift register of the SPI.
5	DI	**Serial data input:** The input requires CMOS logic levels. The DI input has a pull-down current. It receives serial data from the microcontroller. The data is a 16bit control word and the most significant bit (MSB, bit 0) is transferred first.
6	CSN	**Chip Select Not input** The input requires CMOS logic levels. The CSN input has a pull-up current. The serial data transfer between device and micro controller is enabled by pulling the input CSN to low level.
7	DO	**SPI data output:** The diagnosis data is available via the SPI and it is a tristate-output. The output is CMOS compatible will remain highly resistive, if the chip is not selected by the input CSN (CSN = high)
8	PWM	**PWM output** This CMOS compatible output reflects the current duty cycle of the internal PWM controller of bridge A. It is an high resistance output until VCC has reached minimum voltage ore can switched off via the SPI command.
9	STEP	**Step clock input:** The input requires CMOS logic levels. The STEP input has a pull-down current. It is clock of up and down counter of control register 0. Rising edge starts new PWM cycle to drive motor in next position.
16	CP	**Charge Pump Output:** A ceramic capacitor (e.g.100 nF) to VS can be connected to this pin to buffer the charge-pump voltage.
17	GND	**Ground:** Reference potential besides power ground e.g. for reference resistor RREF. From this pin exist a resistive path via substrate to PGND.
18	TEST	**Test input** The TEST input has a pull-down current. Pin used for production test only. In the application it must be connected to GND.
19	VCC	**Logic supply voltage:** For this input a ceramic capacitor as close as possible to GND is recommended.

Table 2. Pin description (continued)

Pin	Symbol	Function
20	RREF	**Reference Resistor** The reference resistor is used to generate a temperature stable reference current used for current control and internal oscillator. At this output a voltage of about 1.28V is present. The resistor should be chosen that a current of about 200uA will flow through the resistor.
21	EN	**Enable input:** The input requires CMOS logic levels. The EN input has a pull-down resistor. In standby-mode outputs will be switched off and all registers will be cleared. If EN is set to a logic high level then the device will enter the active mode.

2 Device description

2.1 Dual power supply: V_S and V_{CC}

The power supply voltage V_S supplies the half bridges. An internal charge-pump is used to drive the highside switches. The logic supply voltage V_{CC} (stabilized) is used for the logic part and the SPI of the device. Due to the independent logic supply voltage the control and status information will not be lost, if there are temporary spikes or glitches on the power supply voltage. In case of power-on (V_{CC} increases from undervoltage to $V_{POR\ OFF}$ = 2.60 V, typical) the circuit is initialized by an internally generated power-on-reset (POR). If the voltage V_{CC} decreases under the minimum threshold ($V_{POR\ ON}$ = 2.3 V, typical), the outputs are switched to tristate (high impedance) and the internal registers are cleared.

2.2 Standby mode

The EN input has a pull-down resistor. The device is in standby mode if EN input isn't set to a logic high level. All latched data will be cleared and the inputs and outputs are switched to high impedance. In the standby mode the current at VS (VCC) is less than 3 µA (1 µA) for CSN = high (DO in tristate). If EN is set to a logic high level then the device will enter the active mode. In the active mode the charge pump and the supervisor functions are activated.

2.3 Diagnostic functions

All diagnostic functions (overload/-current, open load, power supply over-/undervoltage, temperature warning and thermal shutdown) are internally filtered (t_{GL} = 32 µs, typical) and the condition has to be valid for a minimum time before the corresponding status bit in the status registers will be set. The filters are used to improve the noise immunity of the device. Open load and temperature warning function are intended for information purpose and will not change the state of the bridge drivers. On contrary, the overload/-current and thermal shutdown condition will disable the corresponding driver (overload/-current) or all drivers (thermal shutdown), respectively. The microcontroller has to clear the status bit to reactivate the bridge driver.

2.4 Overvoltage and undervoltage detection

If the power supply voltage Vs rises above the overvoltage threshold $V_{SOV\ OFF}$ (typical 21 V), an overvoltage condition is detected. Programmable by SPI (OVW) the outputs are switched to high impedance state (default after reset) or the overvoltage bit is set without switching the outputs to high impedance. When the voltage Vs drops below the under-voltage threshold $V_{SUV\ OFF}$, the outputs are switched to high impedance state to avoid the operation of the power devices without sufficient gate driving voltage (increased power dissipation). Error condition is latched and the microcontroller needs to clear the status bits to reactivate the drivers.

2.5 Temperature warning and thermal shutdown

If junction temperature rises above $T_{j\,TW}$ a temperature warning flag is set which is detectable via the SPI. If junction temperature increases above the second threshold $T_{j\,SD}$, the thermal shutdown bit will be set and power DMOS transistors of all output stages are switched off to protect the device. In order to reactivate the output stages the junction temperature must decrease below Tj SD -Tj SD HYS and the thermal shutdown bit has to be cleared by the microcontroller.

2.6 Inductive loads

Each half bridge is built by an internally connected highside and a low-side power DMOS transistor. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven without external free-wheeling diodes. In order to reduce the power dissipation during free-wheeling condition the PWM controller will switch-on the output transistor parallel to the freewheeling diode (synchronous rectification).

2.7 Cross-current protection

The four half-brides of the device are cross-current protected by an internal delay time depending on the programmed slew rate. If one driver (LS or HS) is turned-off then activation of the other driver of the same half bridge will be automatically delayed by the cross-current protection time.

2.8 PWM current regulation

An internal current monitor output of each high-side and low-side transistor sources a current image which has a fixed ratio of the instantaneous load current. This current images are compared with the current limit in PWM control. Range of limit can reach from programmed full scale value (register1 DAC Scale) down belonging LSB value of 5 bit DAC (register1 DAC Phase x). The data of the two 5 bit DACs comes form set up in 9 current profiles (register2 to 6). If signal changes to logic high at pin STEP then 2 current profiles are moved in register1 for DAC Phase A and B. Number of profile depends on phase counter reading and direction bit in register0 (*Figure 7*). The bridges are switched on until the load current sensed at HS switch exceeds the limit. Load current comparator signal is used to detect open load or overcurrent condition also.

2.9 Decay modes

During off-time the device will use one of several decay modes programmable by SPI (*Figure 4* top). In slow decay mode HS switches are activated after cross current protection time for synchronous rectification to reduce the power dissipation (*Figure 4* detail A). In fast decay opposite half bridge will switched on after cross current protection time, that is same like change in the direction. For mixed decay the duration of fast decay period before slow decay can be set to a fixed time (*Figure 4* detail B continuous line) or is triggered by under-run of the load current limit (*Figure 4* detail B dashed line), that can be detected at LS switch. The special mode where the actual phase counter value is taken into account to select the decay mode is called auto decay (e.g. in *Figure 3* Micro Stepping DIR=1). If the absolute value of the current limit is higher as during step before then PWM control uses

slow decay mode always. Otherwise one of the fast decay modes is automatic selected for a quick decrease of the load current and so it obtains new lower target value.

2.10 Overcurrent detection

The overcurrent detection circuit monitors the load current in each activated output stage. In HS stage it is in function after detection of current limit during PWM cycle and in LS stage it works permanently. If the load current exceeds the overcurrent detection threshold for at least t_{ISC} = 4 µs, the overcurrent flag is set and the corresponding driver is switched off to reduce the power dissipation and to protect the integrated circuit. Error condition is latched and the microcontroller needs to clear the status bits to reactivate the drivers.

2.11 Open load detection

The open load detection monitors the activity time of the PWM controller and is available for each phase. If the limit of load current is below around 100mA then open load condition is detectable. Open load bit for a bridge is set in the register6 if this low current limit can't reached after at least 15 consecutive PWM cycles.

Table 3. Truth table

DC2	DC1	DC0	I4	I3	I2	I1	I0	max. IOL
0	0	0	0	x	x	x	x	46mA
0	0	1	0	x	x	x	x	68mA
0	1	0	0	0	x	x	x	52mA
0	1	1	0	0	x	x	x	81mA
1	0	0	0	0	0	x	x	53mA
1	0	1	0	0	0	x	x	78mA
1	1	0	0	0	0	0	1	37mA
1	1	1	0	0	0	0	1	44mA

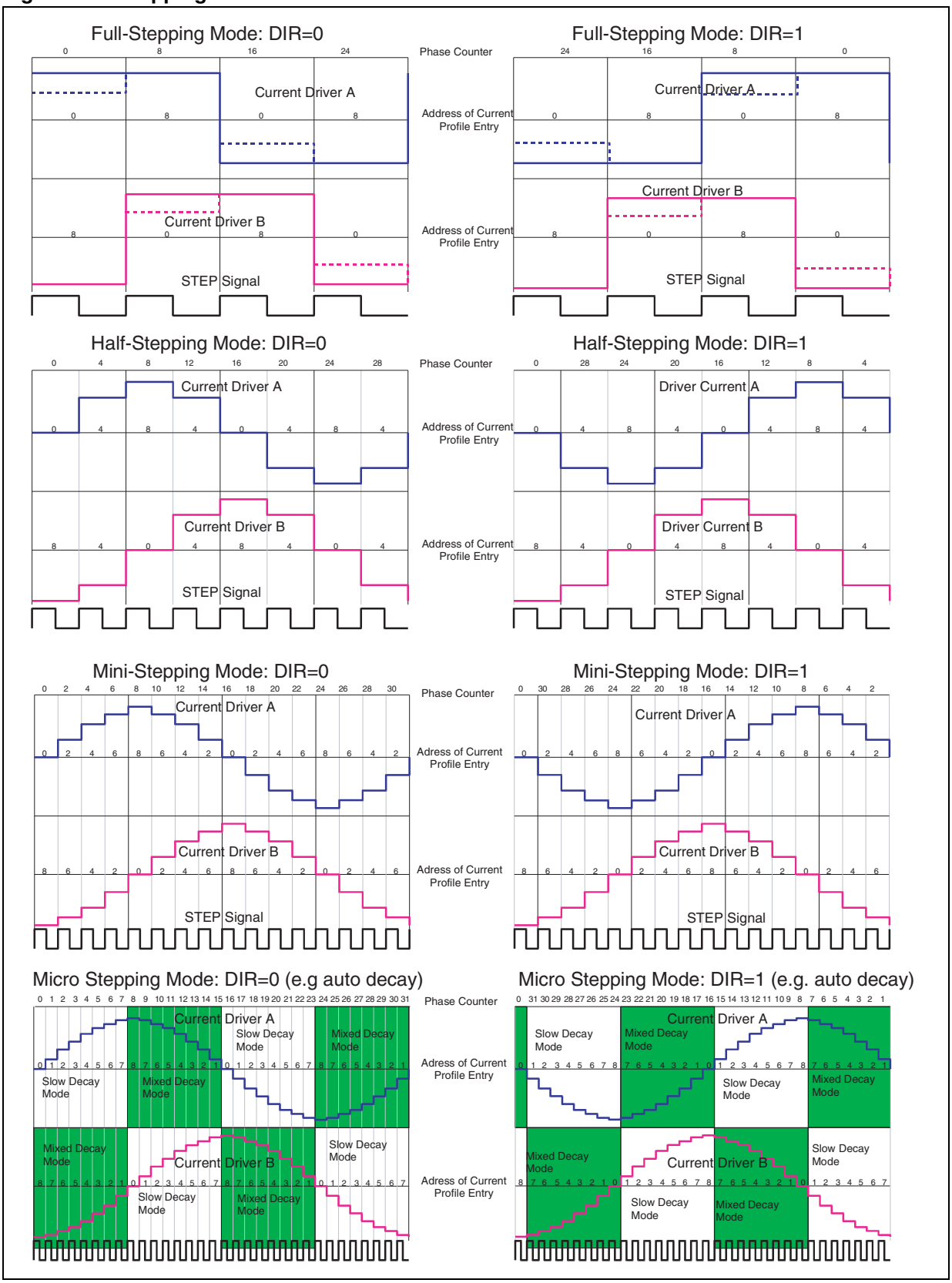
Truth table shows possible profiles for active open load detection. Maximum threshold IOL is shown in left column if x bits are 1 (see also *Figure 7*). Lowest possible limit is e.g. 3.1 mA for DC2=DC1=DC0=0 and it is set only I0=1.

2.12 Stepping modes

One full revolution can consist of four full steps, eight half steps, sixteen mini steps or 32 microsteps.

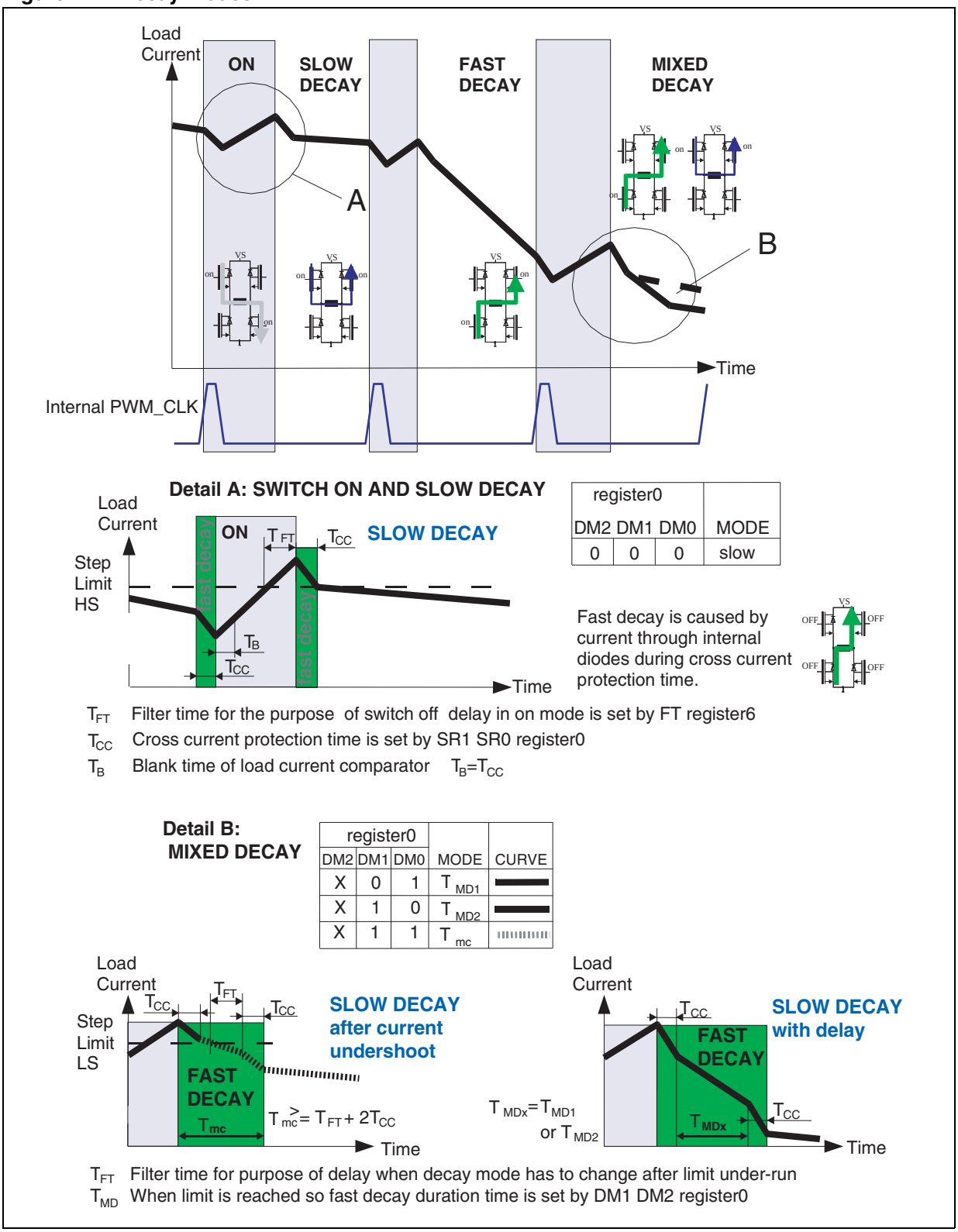
Mode is set up in register 0 and it defines increment size of phase counter. Phase counter value defines address of corresponding current profile. Stepping modes with typical profile values can see in *Figure 3* (e.g. also so called 'Two Phase On' shown in dashed line).

Figure 3. Stepping modes



2.13 Decay modes

Figure 4. Decay modes



3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to 28	V
	single pulse t_{max} < 400 ms	40	V
V_{CC}	Stabilized supply voltage, logic supply	-0.3 to 5.5	V
V_{DI},V_{DO}, V_{CLK} V_{CSN}, V_{STEP} V_{EN}	Digital input / output voltage	-0.3 to V_{CC} + 0.3	V
V_{RREF}	Current reference resistor	-0.3 to V_{CC} + 0.3	V
V_{CP}	Charge pump output	-0.3 to V_S + 11	V
V_{Qxn}	(x=A;B n=1;2) output voltage	-0.3 to V_S + 0.3	V
I_{Qxn}	(x=A;B n=1;2) output current	±2.5	A

Warning: Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit!

3.2 ESD protection

Table 5. ESD protection

Parameter	Value	Unit
All pins	±2 (1)	kV
output pins: Qxn (x=A;B n=1;2)	±4(2)	kV

1. HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A
2. HBM with all unzapped pins grounded

3.3 Thermal data

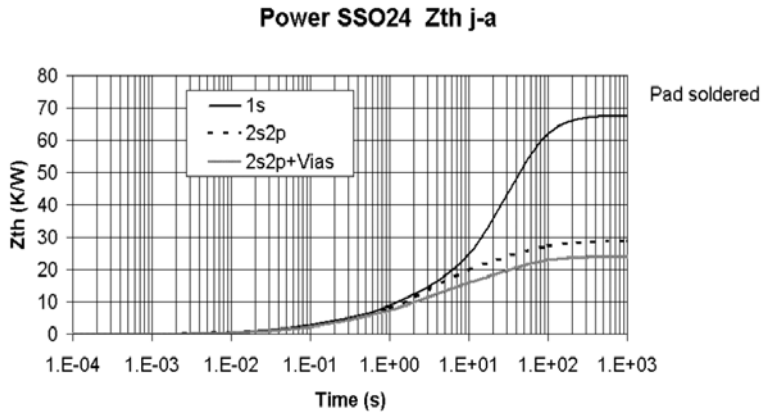
Table 6. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 150	°C

Table 7. Temperature warning and thermal shutdown

Symbol	Parameter		Min.	Typ.	Max.	Unit
$T_{jTW\ ON}$	Temperature warning threshold junction temperature	T_j increasing	-	-	150	°C
$T_{jTW\ OFF}$	Temperature warning threshold junction temperature	-	130	-	-	°C
$T_{jSD\ ON}$	Thermal shutdown threshold junction temperature	-	-	-	170	°C
$T_{jSD\ OFF}$	Thermal shutdown threshold junction temperature	-	150	-	-	°C
$T_{jSD\ HYS}$	Thermal shutdown hysteresis	-	-	5	-	K

Figure 5. Thermal data of the package



Note:
1s 1 signal layer
2s2p 2 signal layers 2 internal planes

3.4 Electrical characteristics

V_S = 7 to 20 V, V_{CC} = 3.0 to 5.3 V, T_j = -40 to 150 °C, I_{REF} = -200 µA, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

3.4.1 Supply

Table 8. Supply

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
I_S	V_S DC supply current in active mode	V_S = 13.5 V, EN=V_{CC} outputs floating		-	7	20	mA
	V_S quiescent supply current	V_S = 13.5 V, TEST, EN = 0V outputs floating	T_j = -40 °C to 25 °C	-	3	10	µA
			T_j = 125 °C	-	6	20	
I_{CC}	V_{CC} DC supply current in active mode	V_{CC} = 5.0 V EN=V_{CC}, DI=CLK=STEP=0V		-	1	3	mA
		V_{CC} = 5.0 V TEST; EN = 0 V; CSN = V_{CC} no clocks outputs floating	T_j = -40 °C to 25 °C	-	1	3	µA
I_{CC}	V_{CC} quiescent supply current	CSN=V_{CC} no clocks outputs floating	T_j = 125 °C	-	2	6	µA
		V_S = 13.5 V, V_{CC} = 5.0 V	T_j = -40 °C to 25 °C	-	4	13	µA
$I_S + I_{CC}$	Sum quiescent supply current	TEST; EN=0 V CSN=V_{CC} no clocks outputs floating	T_j = 125 °C	-	8	26	
t_{setPOR} (1)	V_{CC} on set up time	EN = 5 V, CSN=CLK=0V DO changes from high ohmic to logic level LOW		2	-	-	µs

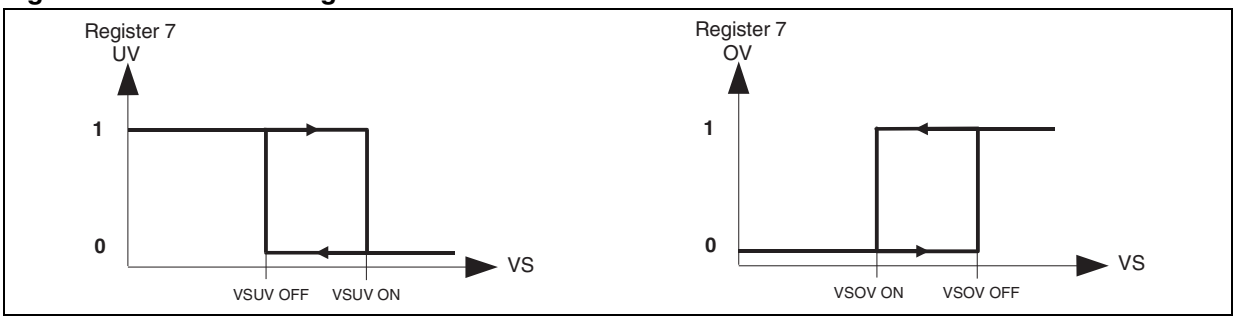
1. This parameter is guaranteed by design.

3.4.2 Over- and undervoltage detection

Table 9. Over- and undervoltage detection

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{SUV\ ON}$	V_S UV-threshold voltage	V_S increasing	-	-	6.90	V
$V_{SUV\ OFF}$	V_S UV-threshold voltage	V_S decreasing	4.8	-	-	V
$V_{SUV\ hyst}$	V_S UV-hysteresis	$V_{SUV\ ON}$ -$V_{SUV\ OFF}$	-	0.3	-	V
$V_{SOV\ OFF}$	V_S OV-threshold voltage	V_S increasing	-	21	25	V
$V_{SOV\ ON}$	V_S OV-threshold voltage	V_S decreasing	18.5	20	-	V
$V_{SOV\ hyst}$	V_S OV-hysteresis	$V_{SOV\ OFF}$ -$V_{SOV\ ON}$	-	0.5	-	V
$V_{POR\ OFF}$	Power-off-reset threshold	V_{CC} increasing	-	2.6	2.9	V
$V_{POR\ ON}$	Power-on-reset threshold	V_{CC} decreasing	2.00	2.3	-	V
$V_{POR\ hyst}$	Power-on-reset hysteresis	$V_{POR\ OFF}$ -$V_{POR\ ON}$	-	0.11	-	V

Figure 6. VS monitoring



3.4.3 Reference current output

Table 10. Reference current output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{REF}	Reference voltage range	I_{REF} = -200 µA	1.05	1.25	1.45	V
$I_{REFshorted}$	Reference current threshold shorted pin REF	register6 bit7 RERR = 1	-	-	-250	µA
$I_{REFopen}$	Reference current threshold open pin REF	register6 bit7 RERR = 1	-150	-	-	µA

The device works properly without the external resistor at pin REF. In this case it doesn't have to fulfill all specified parameters.

3.4.4 Charge pump output

Table 11. Charge pump output

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{CP}	Charge pump output voltage	V_S=7 V	I_{CP}= -100 µA, all switches off at Qxn	11	-	20	V
		V_S=13.5 V		20	-	35	V
		V_S=20 V		30	-	40	V

The ripple of voltage at CP can suppressed using a capacity of e.g.100 nF.

3.4.5 Outputs: Qxn (x = A; B n = 1; 2)

The comparator, which is monitoring current image of HS, is working during ON cycle of PWM control. If load current is higher as set value then the signal ILIMIT is generated and after filter time the bridge is switched off. Test mode gets access to signal ILIMIT and threshold of current can be measured.

Table 12. Outputs: Qxn (x = A; B n =1; 2)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{DSON\ HS}$	On-resistance Qxn to V_S	V_S = 13.5 V, T_j = 25 °C, I_{Qxn} = -1.0 A	-	500	700	mΩ
		V_S = 13.5 V, T_j = 125 °C, I_{Qxn} = -1.0 A	-	750	1000	mΩ
		V_S = 7.0 V, T_j = 25 °C, I_{Qxn} = -1.0 A	-	550	750	mΩ
$R_{DSON\ LS}$	On-resistance Qxn to PGND	V_S = 13.5 V, T_j = 25 °C, I_{Qxn} = + 1.0 A	-	500	700	mΩ
		V_S = 13.5 V, T_j = 125 °C, I_{Qxn} = + 1.0 A	-	750	1000	mΩ
		V_S = 7.0 V, T_j = 25 °C, I_{Qxn} = + 1.0 A	-	550	750	mΩ
$\lvert I_{QxnOC} \rvert$	Output overcurrent limitation to VS or PGND	test mode exclusive of filter time 4µs (*Chapter 2.10*)	1.6	2	-	A
I_{QxnFS_HS}	Value of output current to supply V_S (so called full scale value)1 sourcing from HS switch	Bits: DC2 DC1 DC0=000	60	95	130	mA
		Bits: DC2 DC1 DC0=001	100	140	180	
		Bits: DC2 DC1 DC0=010	180	230	280	
		Bits: DC2 DC1 DC0=011	300	360	420	
		Bits: DC2 DC1 DC0=100	485	550	615	
		Bits: DC2 DC1 DC0=101	720	810	900	
		Bits: DC2 DC1 DC0=110	1000	1150	1300	
		Bits: DC2 DC1 DC0=111	1200	1350	1500	
I_{QxnLIM_HS}	Accuracy of micro steps current limit	-	MIN(1)	-	MAX(1)	mA

1. MIN= 0.92 · I_{QxnLIM} – 0.02 · $\lvert I_{QxnFS\_HS} \rvert$; MAX= 1.08 · I_{QxnLIM} + 0.02 · $\lvert I_{QxnFS\_HS} \rvert$

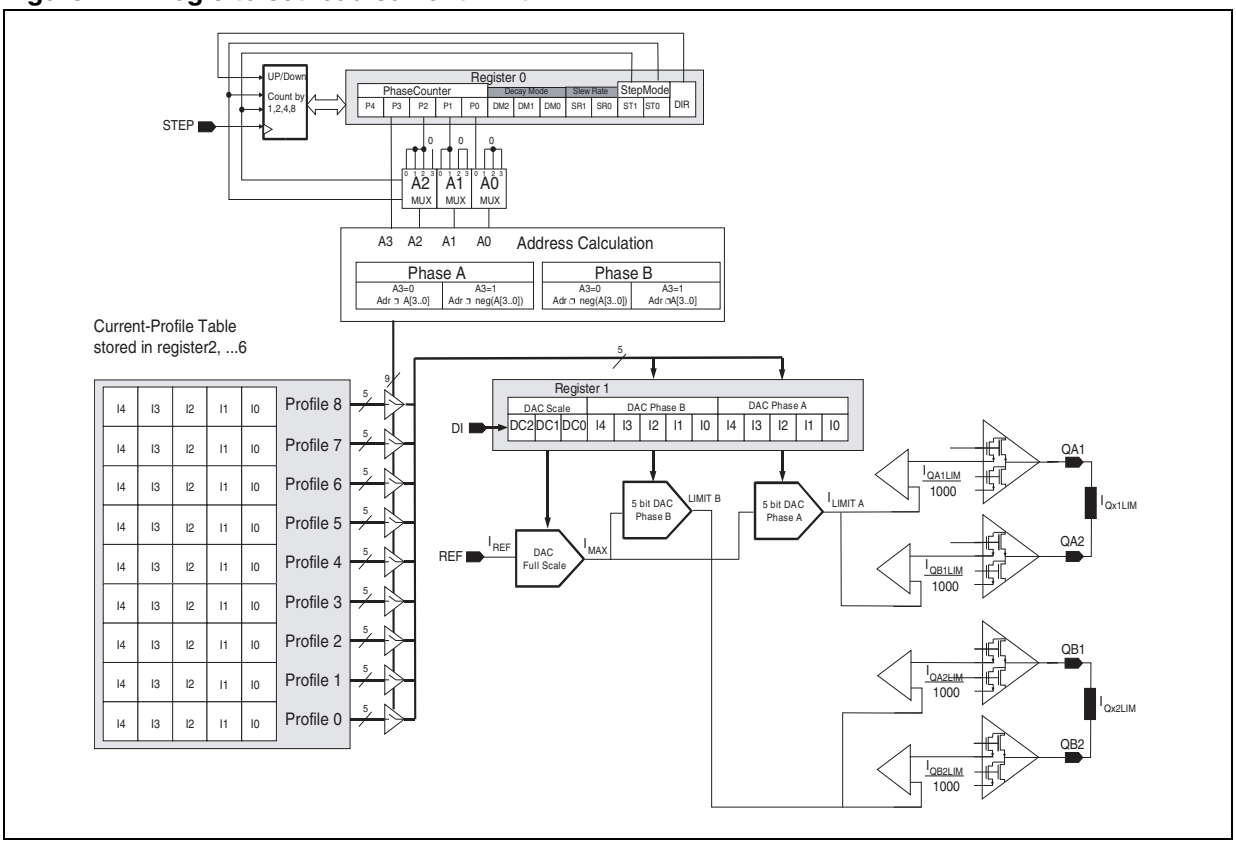
Note: Current profile has to pre set with I4 I3 I2 I1 I0 = 11111 and load to register 1.

Output current limit I_{QxnLIM} is product of full scale current I_{QxnFS_I} (bits DC2 DC1 DC0) and value of DAC Phase A/B (bits I4 I3 I2 I1 I0) in register1.

Values of DAC Phase A and B can read out and depends on set up done before:

1. direction DIR, stepping mode ST1 ST0 and phase counter P4 P3 P2 P1 P0 in register 0 and
2. value of corresponding current profile (for address of current profile entry see also *Figure 3*).

Figure 7. Logic to set load current limit



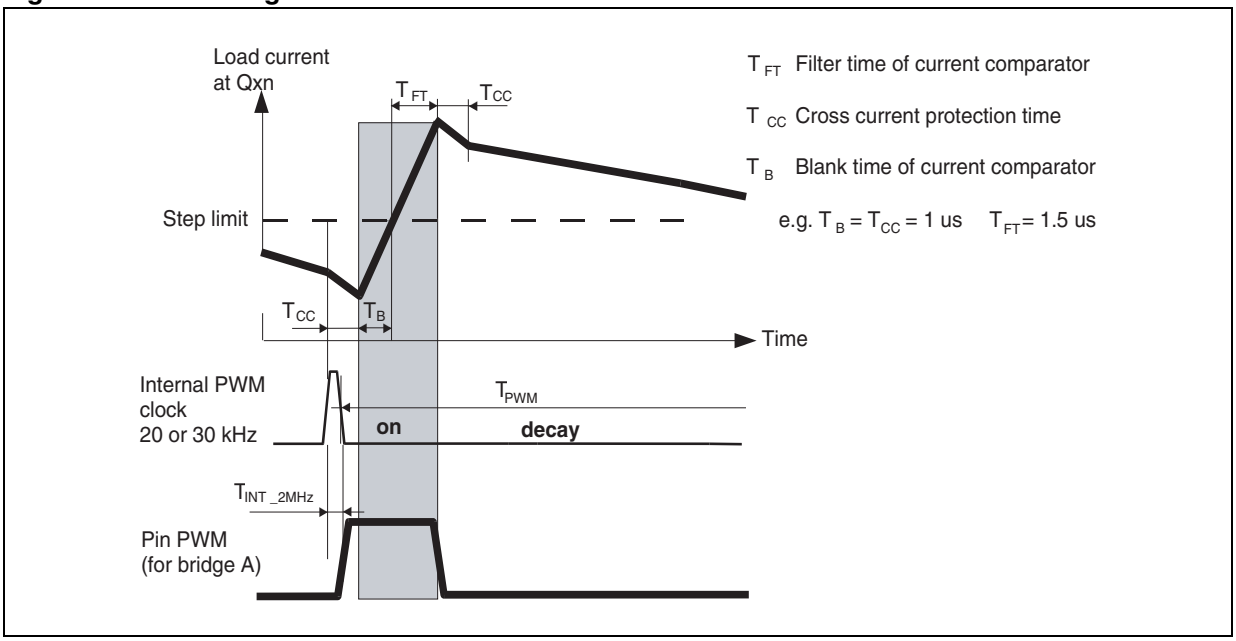
3.4.6 PWM control

Table 13. PWM control (see *Figure 4* and *Figure 7*)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{PWM} (1)	Frequency of PWM cycles	Bit: FRE= 1	-	20.8	-	kHz
		Bit: FRE= 0	-	31.3	-	kHz
T_{MD}(1)	Mixed decay switch off delay time	Bits: DM1 DM0= 0 1	-	4	-	µs
		Bits: DM1 DM0= 1 0	-	8	-	µs
T_{FT}(1)	Glitch filter delay time	Bit: FILTER= 0	-	1.5	-	µs
		Bit: FILTER= 1	-	2.5	-	µs
T_{cc} (1) T_B (1)	Cross current protection time Blank time of comparator	Bits: SR1 SR0= 0 0	-	0.5	-	µs
		Bits: SR1 SR0= 0 1	-	1	-	µs
		Bits: SR1 SR0= 1 0	-	2	-	µs
		Bits: SR1 SR0= 1 1	-	4	-	µs
VSR	Slew rate (dV/dt 30 % - 70 %) @HS switches on resistive load of 10 Ω, VS = 13.5 V	Bits: SR1 SR0= 0 0	-	13	-	V/µs
		Bits: SR1 SR0= 0 1	-	13	-	V/µs
		Bits: SR1 SR0= 1 0	-	6	-	V/µs
		Bits: SR1 SR0= 1 1	-	6	-	V/µs

1. This parameter is guaranteed by design.
Time base is an internal trimmed oscillator of typical 2MHz and it has an accuracy of ±6 %.

Figure 8. Switching on minimum time



4 Functional description of the logic with SPI

4.1 Motor stepping clock input (STEP)

Rising edge of signal STEP is latched. It is synchronized by internal clock. At next start of a new PWM cycle the new values of output current limit are used to drive motor in next position. Before start new motor step this signal has to be low for at least two internal clock periods to reset latch.

4.2 PWM output (PWM)

This output reflects the current duty cycle of the internal PWM controller of bridge A. High level indicates on state to increase current through load and low level is in off state so load current decreases depending on chosen decay mode.

4.3 Serial peripheral interface (SPI)

This device uses a standard 16 bit SPI to communicate with a microcontroller. The SPI can be driven by a microcontroller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0.

For this mode, input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-pin will reflect an internal error flag of the device which is a logical-or of all status bits in the Status Register (reg 7) and in the current profile register 4 (reg 6). The microcontroller can poll the status of the device without the need of a full SPI-communication cycle.

4.4 Chip select not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) will be in high impedance state. A low signal will activate the output driver and a serial communication can be started. The state when CSN is going low until the rising edge of CSN will be called a communication frame.

4.5 Serial data in (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI will be sampled at the rising edge of the CLK signal and latched into an internal 16 bit shift register. The first 3 bit are interpreted as address of the data register. At the rising edge of the CSN signal the contents of the shift register will be transferred to the selected data register. The writing to the register is only enabled if exactly 16 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame will be ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

4.6 Serial data out (DO)

The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the status bit 0 (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

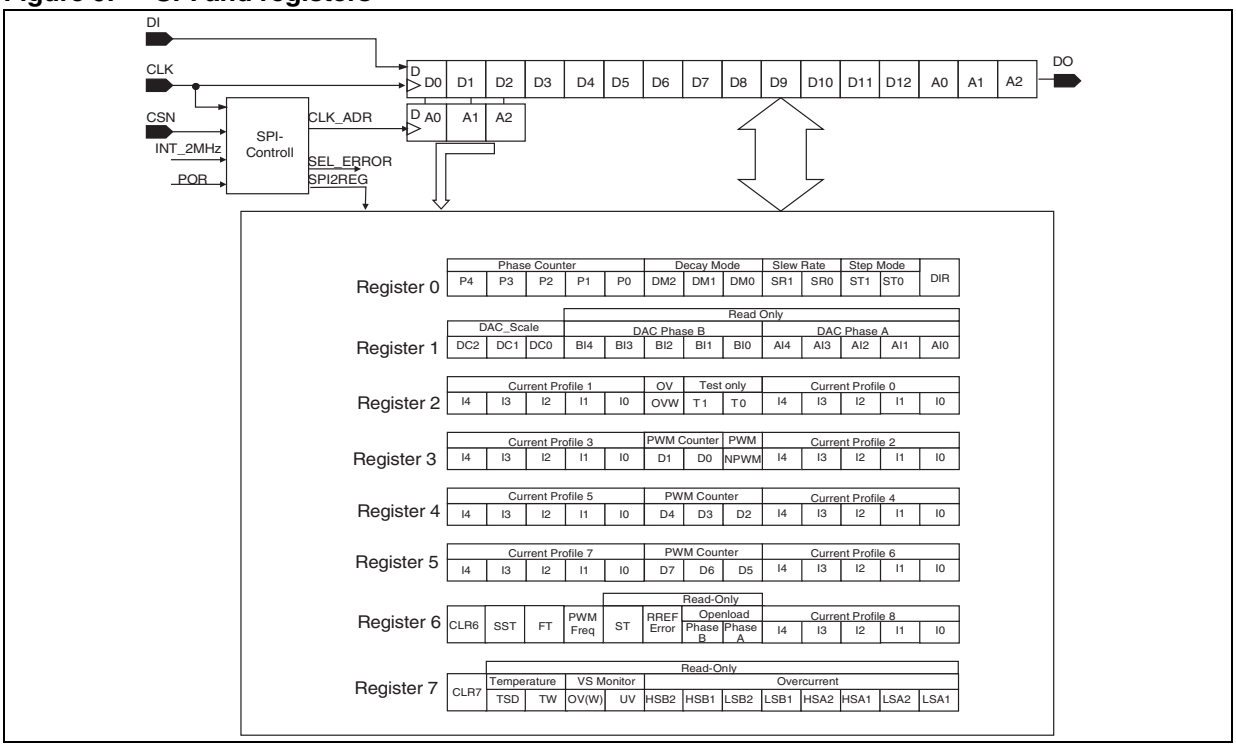
4.7 Serial clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal.

4.8 Data register

The device has eight data registers. The first three bits (bit 0 ... bit 2) at the DI-input are used to select one of the input registers. All bits are first shifted into an input shift register. After the rising edge of CSN the contents of the input shift register will be written to the selected Input Data Register only if a frame of exact 16 data bits are detected. The selected register will be transferred to DO during the current communication frame.

Figure 9. SPI and registers



5 SPI - control and status registers

5.1 Register 0

Table 14. Register 0

Bit	Phase counter					Decay mode			Slew rate		Step mode		DIR
	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	P4	P3	P2	P1	P0	DM2	DM1	DM0	SR1	SR0	ST1	ST0	DIR

The meaning of the different bits is as follows:

DIR	This bit controls direction of motor movement. DIR=1 clockwise DIR=0 counter clockwise.

ST1 ST0	This bits controls step mode of motor movement (*Figure 3*).
00	Micro-stepping
01	Mini-stepping
10	Half-stepping
11	Full-stepping

SR1 SR0	This bit controls slew rate of bridge switches. See also parameter *Table 13*

DM2 DM1 DM0	This bits controls decay mode of output current (*Figure 3*).	
000	Slow decay	
001	Mixed decay, fast decay until T_{MD} > 4 µs	
010	Mixed decay, fast decay until T_{MD} > 8 µs	
011	Mixed decay, fast decay until current undershoot $T_{mc} = T_{FT} + T_{CC}$	
100	Auto decay, fast decay without delay time	Auto decay uses mixed decay automatically to reduce current for next step if required (see *Figure 3* down right).
101	Auto decay, fast decay until T_{MD} > 4 µs	
110	Auto decay, fast decay until T_{MD} > 8 µs	
111	Auto decay, fast decay until current undershoot T_{mc}	

P4 P3 P2 P1 P0	This bits control position of motor, e.g. 00000 step angle is 0°, 01111 step angle is 180 °.

5.2 Register 1

Table 15. Register 1

Bit	DAC scale			DAC phase B					DAC phase A				
	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r w	r w	r w	r	r	r	r	r	r	r	r	r	r
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	DC2	DC1	DC0	BI4	BI3	BI2	BI1	BI0	AI4	AI3	AI2	AI1	AI0

The meaning of the different bits is as follows:

AI4 AI3 AI2 AI1 AI0	These bits control DAC of bridge A.	Value depends on address and the value of corresponding current profile.
BI4 BI3 BI2 BI1 BI0	These bits control DAC of bridge B.	
DC2 DC1 DC0	These bits set full scale range of limit, e.g. 000 for 100 mA or 111 for e.g. 1500 mA	See also parameter *Table 12*.

5.3 Register 2

Table 16. Register 2

Bit	Current profile 1					OV	Test only		Current profile 0				
	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	I4	I3	I2	I1	I0	OVW	T1	T0	I4	I3	I2	I1	I0

The meaning of the different bits is as follows:

I4 I3 I2 I1 I0	These bits are loaded in register1 DAC Phase A or B if needed.	See also parameter *Table 12*
T1 T0	Should be programmed to 0.	-
OVW = 0	In case of an overvoltage event (V-SOV OFF) the outputs are switched to high impedance state and the Vs Monitor bit OV is set.	-
OVW = 1	In case of an overvoltage event (V-SOV OFF) the Vs Monitor bit OV is set. The status of the outputs are unchanged.	-

5.4 Register 3

Table 17. Register 3

Bit	Current profile 3					PWM counter		PWM	Current profile 2				
	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	I4	I3	I2	I1	I0	D1	D0	NPWM	I4	I3	I2	I1	I0

The meaning of the different bits is as follows:

I4 I3 I2 I1 I0	These bits are loaded in register1 DAC Phase A or B if needed.	See also parameter *Table 12*
D1 D0	These bits are for threshold value in counter of active time during signal PWM.	-
NPWM	This bit switches internal PWM signal of bridge A to pin PWM if it is set to 0, otherwise pin is in high resistance status.	-

5.5 Register 4 and 5

Table 18. Register 4 and 5

Bit	Current profile 5 (7)					PWM counter			Current profile 4 (6)				
	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	I4	I3	I2	I1	I0	D4(7)	D3(6)	D2(5)	I4	I3	I2	I1	I0

The meaning of the different bits is as follows:

I4 I3 I2 I1 I0	These bits are loaded needed. in register1 DAC Phase A or B if needed.	See also parameter *Table 12*
D4 D3 D2 (register4)	These bits are for threshold value in counter of active time during signal PWM. LSB and next value are set in register3 by D0 and D1.	-
D7 D6 D5 (register5)		

5.6 Register 6

Table 19. Register 6

	CLR	ST (PWM)	Filter	Freq.	ST	REF ERR	Open load		Current profile 8				
Bit	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Access	r w	r w	r w	r w	r	r	r	r	r w	r w	r w	r w	r w
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	CLR6	SST	FT	PWM Freq.	ST	RREF Error	Phase B	Phase A	I4	I3	I2	I1	I0

The meaning of the different bits is as follows:

I4 I3 I2 I1 I0	These bits are loaded in register1 DAC Phase A or B if needed	See also parameter *Table 12*
Phase B Phase A	These bits indicate open load at bridges	
RREF Error	This bit indicates if reference current is OK (150 µA <I_{REF} < 250 µA), then is RERR=0.	
ST	This bit indicates stall detection.	
PWM Freq.	This bit sets frequency of PWM cycle. FRE=1 frequency 20 kHz, FRE=0 frequency 30 kHz	
FT	This bit sets filter time in glitch filter. FT=0 T_F =1.5 µs, FT=1 T_F = 2.5 µs	
SST	This bit specifies output PWM to reflect same logical level like bit ST.	
CLR6	This bit resets all read only bits to 0 in register 6.	

5.7 Register 7

Table 20. Register 7

	CLR	Temperature		VS monitor		Overcurrent							
Bit	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Access	r w	r	r	r	r	r	r	r	r	r	r	r	r
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	CLR7	TSD	TW	OV(W)	UV	HSB2	HSB1	LSB2	LSB1	HSA2	HSA1	LSA2	LSA1

The meaning of the different bits is as follows:

bit7 ... bit0	These bits indicate overcurrent in each low side or highside power transistor.
1	overcurrent failure I > 2 A
OV(W) UV	These bits indicates failure at VS (See also parameter *Table 9*)
01	Voltage at pin VS is too low.
10	Voltage at pin VS is too high.
TSD TW	These bits indicates temperature failure (See also parameter *Table 7*)
01	Only for information set at temperature warning threshold.
10	In case of thermal shutdown all bridges are switched off. It has to reset by bit CLR7.
CLR7	This bit resets all bits to 0 in register 7.

5.8 Auxiliary logic blocks

5.8.1 Fault condition

Logical level at pin D0 represents fault condition. It is valid from first high to low edge of signal CLK up to transfer of data bit D12. Fault bit is an logical OR of:

Control and status register 6 bit 5 and 6 for open load, bit 7 reference current failure (RERR) and

Control and status register 7 bit 0 to bit 7 for overcurrent, bit 8 and 9 failure at VS (UV,OV) and

bit 10 and bit 11 during high temperature (TW,TSD)

5.8.2 SPI communication monitoring

At the rising edge of the CSN signal the contents of the shift register will be transferred to the selected data register. A counter monitors proper SPI communication. It counts rising edges at pin CLK. The writing to the register is only enabled if exactly 16 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame will be ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame. SPI communication can be checked by loading a command twice and then answer at pin DO must be same.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

5.8.3 PWM monitoring for stall detection

Control registers 4, 5, and 3 contain bits D0-D7, use for setting a stall detection threshold. The value in this set of bits determine the minimum time for current rise over one quadrant of motor driving. D7-D0 is compared with the sum of the rise times over one quadrant. When the sum is less than the value stored in D7-D0 the ST bit (register 6 bit 8) is set to a logic “1”.

The PWM pin reflects the PWM control signal of the load current in bridge A. This is so after power on when the SST bit (register 6, bit11) is reset to a logic “0”. If this bit is set to a logical “1” then status of the ST bit 8 is mirrored to pin PWM. This provides stall detection without the need of reading register 6 through the SPI bus.

6 Logic with SPI - electrical characteristics

VS = 7 to 20 V, VCC = 3.0 to 5.3 V, EN=VCC, T_j = -40 to 150 °C, I_{REF} = -200 µA, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

6.1 Inputs: CSN, CLK, STEP, EN and DI

Table 21. Inputs: CSN, CLK, STEP, EN and DI

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{in\ L}$	input low level	-	0.3*VCC	0.4*VCC	-	V
$V_{in\ H}$	input high level	-	-	0.6*VCC	0.7*VCC	V
$V_{in\ Hyst}$	input hysteresis	-	-	0.1*VCC	-	V
$I_{CSN\ in}$	pull up current at input CSN	V_{CSN} = VCC -1.5 V,	-50	-25	-10	µA
$I_{CLK\ in}$	pull down current at input CLK	V_{CLK} = 1.5 V	10	25	50	µA
$I_{DI\ in}$	pull down current at input DI	V_{DI} = 1.5 V	10	25	50	µA
$I_{STEP\ in}$	pull down current at input STEP	V_{STEP} = 1.5 V	10	25	50	µA
$R_{EN\ in}$	resistance at input EN to GND	$V_{EN\ in}$ = VCC	110		510	kΩ
C_{in} (1)	input capacitance at input CSN, CLK, DI and PWM	0 V < VCC < 5.3 V	-	10	15	pF

1. Parameter guaranteed by design.

6.2 DI timing

Table 22. DI timing (see *Figure 11* and *Figure 13*) (1)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{CLK}	Clock period	VCC = 5 V	250	-	-	ns
t_{CLKH}	Clock high time	VCC = 5 V	100	-	-	ns
t_{CLKL}	Clock low time	VCC = 5 V	100	-	-	ns
$t_{set\ CSN}$	CSN set up time, CSN low before rising edge of CLK	VCC = 5 V	100	-	-	ns
$t_{set\ CLK}$	CLK set up time, CLK high before rising edge of CSN	VCC = 5 V	100	-	-	ns
$t_{set\ DI}$	DI set up time	VCC = 5 V	50	-	-	ns
$t_{hold\ DI}$	DI hold time	VCC = 5 V	50	-	-	ns
$t_{r\ in}$	Rise time of input signal DI, CLK, CSN	VCC = 5 V	-	-	25	ns
$t_{f\ in}$	Fall time of input signal DI, CLK, CSN	VCC = 5 V	-	-	25	ns

1. DI timing parameters tested in production by a passed/failed test:
T_j=-40°C/+25°C: SPI communication @5MHz; T_j=+125°C: SPI communication @4.25MHz

6.3 Outputs: DO, PWM

Table 23. Outputs: DO, PWM

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DOoutL} $V_{PWMoutL}$	Output low level	VCC = 5 V, I_D = 2 mA	-	0.2	0.4	V
V_{DOoutH} $V_{PWMoutH}$	output high level	VCC = 5 V, I_D = -2 mA	VCC - 0.4	VCC - 0.2	-	V
$I_{DOoutLK}$	Tristate leakage current	V_{CSN} = VCC, 0 V < V_{DO} < VCC	-10	-	10	µA
$I_{PWMoutLK}$	Tristate leakage current	Register3bit5=1 (NPWM) 0 V < V_{PWM} < VCC	-10	-	10	µA
C_{out} (1)	Tristate input capacitance	V_{CSN} = VCC, 0 V < VCC < 5.3 V	-	10	15	pF

6.4 Output: DO timing

Table 24. Output: DO timing (see *Figure 12* and *Figure 13*)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{r\ DO}$	DO rise time	C_L = 100 pF, I_{load} = -1 mA	-	50	100	ns
$t_{f\ DO}$	DO fall time	C_L = 100 pF, I_{load} = 1 mA	-	50	100	ns
$t_{en\ DO\ tri\ L}$	DO enable time from tristate to low level	C_L = 100 pF, I_{load} = 1 mA pull-up load to VCC	-	50	250	ns
$t_{dis\ DO\ L\ tri}$	DO disable time from low level to tristate	C_L = 100 pF, I_{load} = 4 mA pull-up load to VCC	-	50	250	ns
$t_{en\ DO\ tri\ H}$	DO enable time from tristate to high level	C_L = 100 pF, I_{load} = -1 mA pull-down load to GND	-	50	250	ns
$t_{dis\ DO\ H\ tri}$	DO disable time from high level to tristate	C_L = 100 pF, I_{load} = -4 mA pull-down load to GND	-	50	250	ns
$t_{d\ DO}$	DO delay time	V_{DO} < 0.3 VCC, V_{DO} > 0.7 VCC, C_L = 100 pF	-	50	250	ns

6.5 CSN timing

Table 25. CSN timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{CSN\_HI,min}$ (1)	CSN high time, active mode	Transfer of SPI-command to Input Register	2	-	-	µs

1. Parameter guaranteed by design.

6.6 STEP timing

Table 26. STEP timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{STEPmin}$ (1)	STEP low or high time	-	2	-	-	µs

1. Parameter guaranteed by design.

Figure 10. Transfer timing diagram

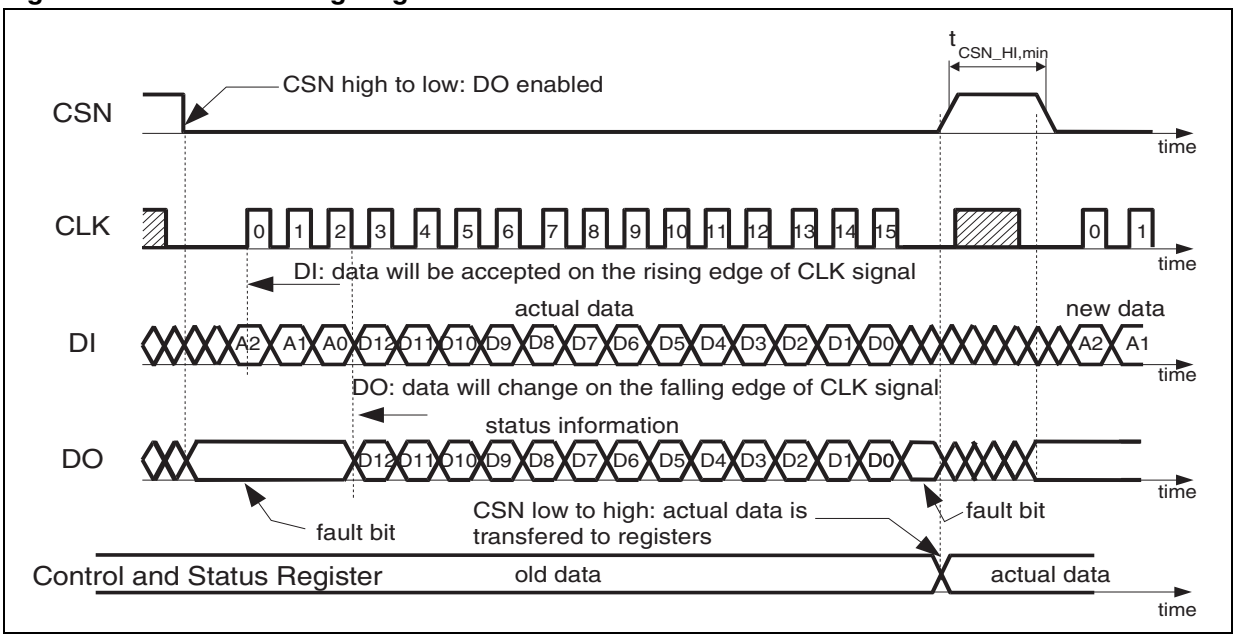


Figure 11. Input timing

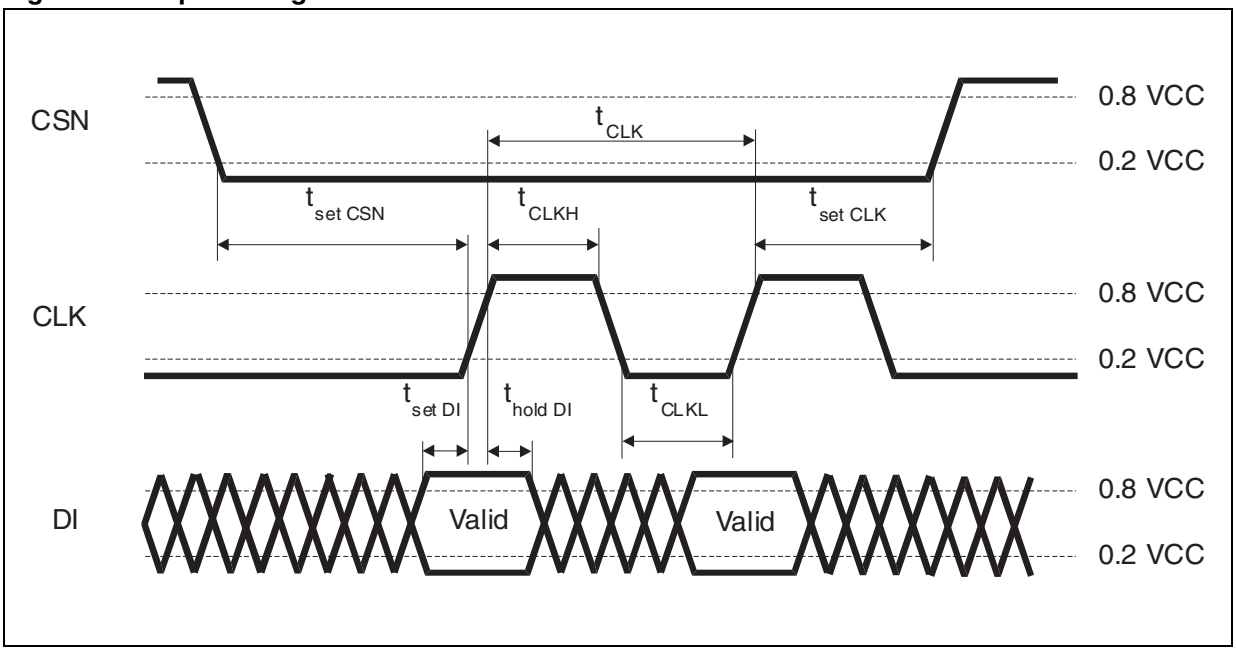


Figure 12. SPI - DO valid data delay time and valid time

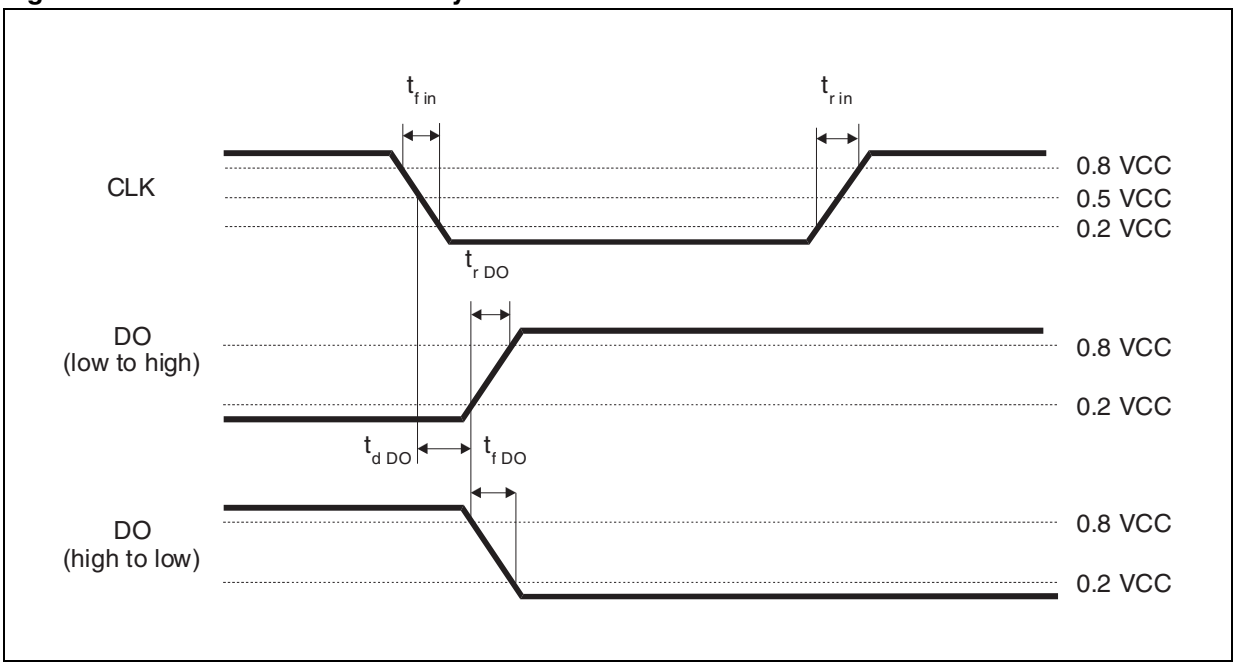


Figure 13. DO enable and disable time

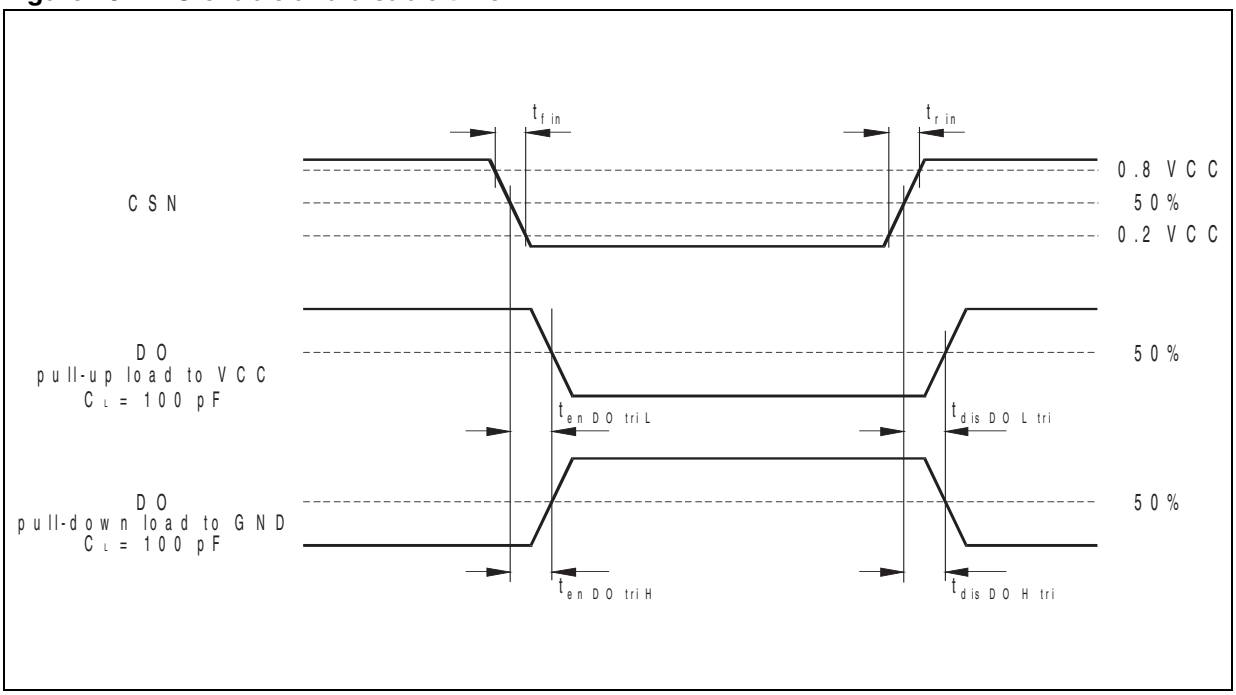
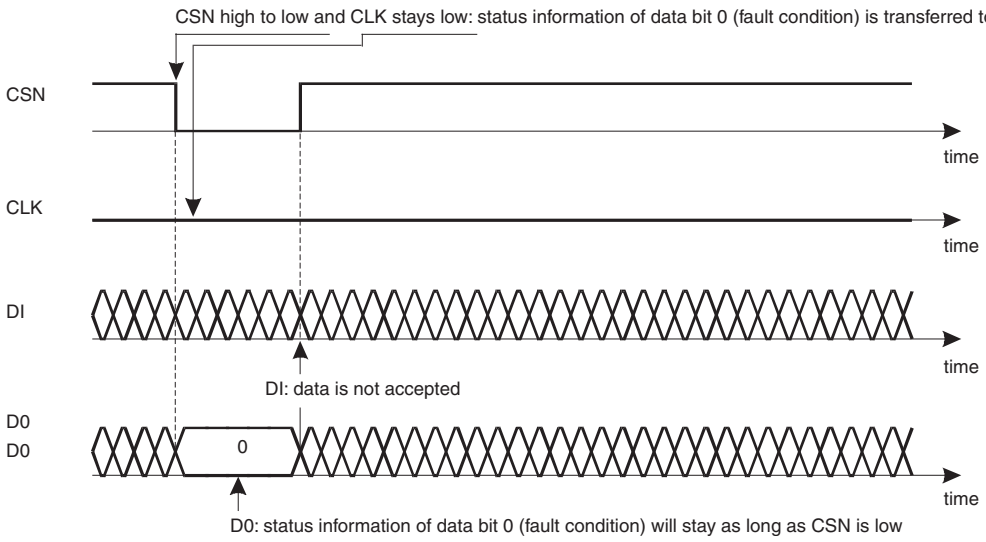


Figure 14. Timing of status bit 0 (fault condition)



7 Appendix

7.1 Stall detection

The L9942 contains logic blocks designed to detect a motor stall caused by excessive mechanical load.During a motor stall condition the load current rises much faster than during normal operation. The L9942 measures this time and compares it to a programmed value.
This is done by summing the PWM on times for one full quadrant. For a full wave stepping this is just one value (step 0). For microstepping this includes 8 separate values added together, one for each step. This measurement is only done on phase A during the quadrants where the current is increasing naturally (quadrants 1 and 3 of *Figure 15*); e.g. stall detection is active during phase counter values 1 to 8 and 17 to 24 for DIR=0. During the quadrants where the current is decreasing fast decay recirculation interferes with accurate measurement of this time. If the sum of the PWM on time is less than a programmed threshold stored in D0-D7, stall is detected and indicated as a logic “1” in the stall (ST) bit found in register 6 bit 8 (*Figure 15* bottom). If bit 11 of register 6 is set to logical “1” then the ST bit is mirrored to the PWM pin providing detection externally.The register values DT7-DT0 store the threshold value in 16us intervals. These bits can be found interstitially in register 3 (D0, D1), register4 (D2, D3, D4) and register5 (D5, D6, D7).

Care should be taken when deciding the threshold timing. Motor current slew rates are dependant on the driving voltage, the actual speed of the motor, the back EMF of the motor as well as the motor and the inductance. Be sure to set your threshold well away from what can be seen in normal operation at any temperature.

7.2 Step clock input

The Step clock input allows to run one device in micro-step mode, or several devices simultaneously with cost effective 8 bit µController. In case of the L9942, the SPI communication link provides only the settings for motor operation mode. Motor commutation as high duty process is outsourced to a parallel driven pin. Without this step clock input, the SPI command would also have to clock the motor, leading to a high SPI speed. For full micro-step operation or simultaneous motor drive, an 8 bit µController could be rapidly overloaded.

7.3 Load current control and detection of overcurrent (shortages at outputs)

The L9942 controls load current in the two full bridges by using a pulls with modulation (PWM) regulator. The mirrored output current of active HS switch is compared with a programmed reference current (e.g. in figure A2 HSA1 and HSB2). Bridge is switched off if current has exceeded the programmed limit value. A second comparator of the related LS switch uses the mirrored load current to detect an overcurrent to ground during ON state of bridges (e.g. in *Figure 16* LSA2 and LSB1). The event of shortage from output to supply voltage VS is detectable, but short current between outputs is limited through PWM controller and so an overcurrent failure will not occur.
Load currents decrease more or less fast during OFF state of bridges depending on selected decay mode. Slow decay mode is released by activating the HS switches of the

bridge and current comparator has as new reference the overcurrent limit. A shortage to ground can be detected, but not between the outputs.
Is it recommended to use the different fast decay modes too, especially in period if the load current has to reduce from step to step. The duration of fast decay can set by fixed time ore that it depends on the comparator signal utilizing the second current mirror at LS switch. There can be monitored the undershoot of bridge current during OFF state.
Fast decay can be seen as switching the bridge in opposite direction, if it is compared to ON state before. The load current control at HS switch is not used, but the comparator is still active. The reference value is changed to overcurrent limit and a shortage to ground or now between the outputs too will result in a signal. The internal filter time of at least 4 us will inhibit the signal in many applications. Then you can use the mode “auto decay without any delay time“ (On *Section 5.1* mode 100). On *page 12* you can find in the lower part of *Figure 3* the phase counter values, when fast decay as only part of mixed decay is used and the shortages can be detected during a longer time. After this it is signalized in register 7 as overcurrent in HS switch (e.g. in *Figure 17* HSA1).

Figure 15. Stall detection

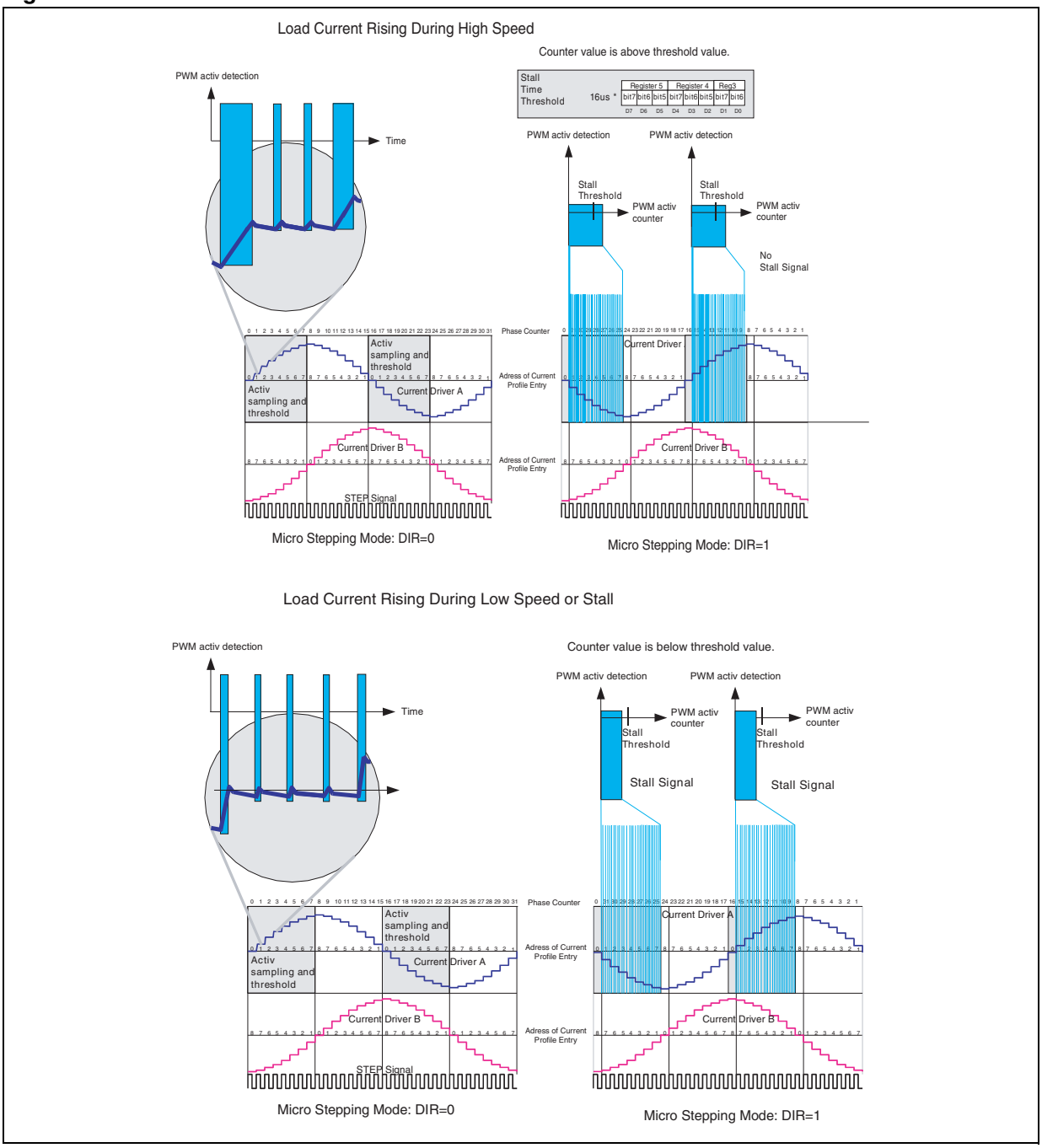


Figure 16. Reference generation for PWM control (switch on)

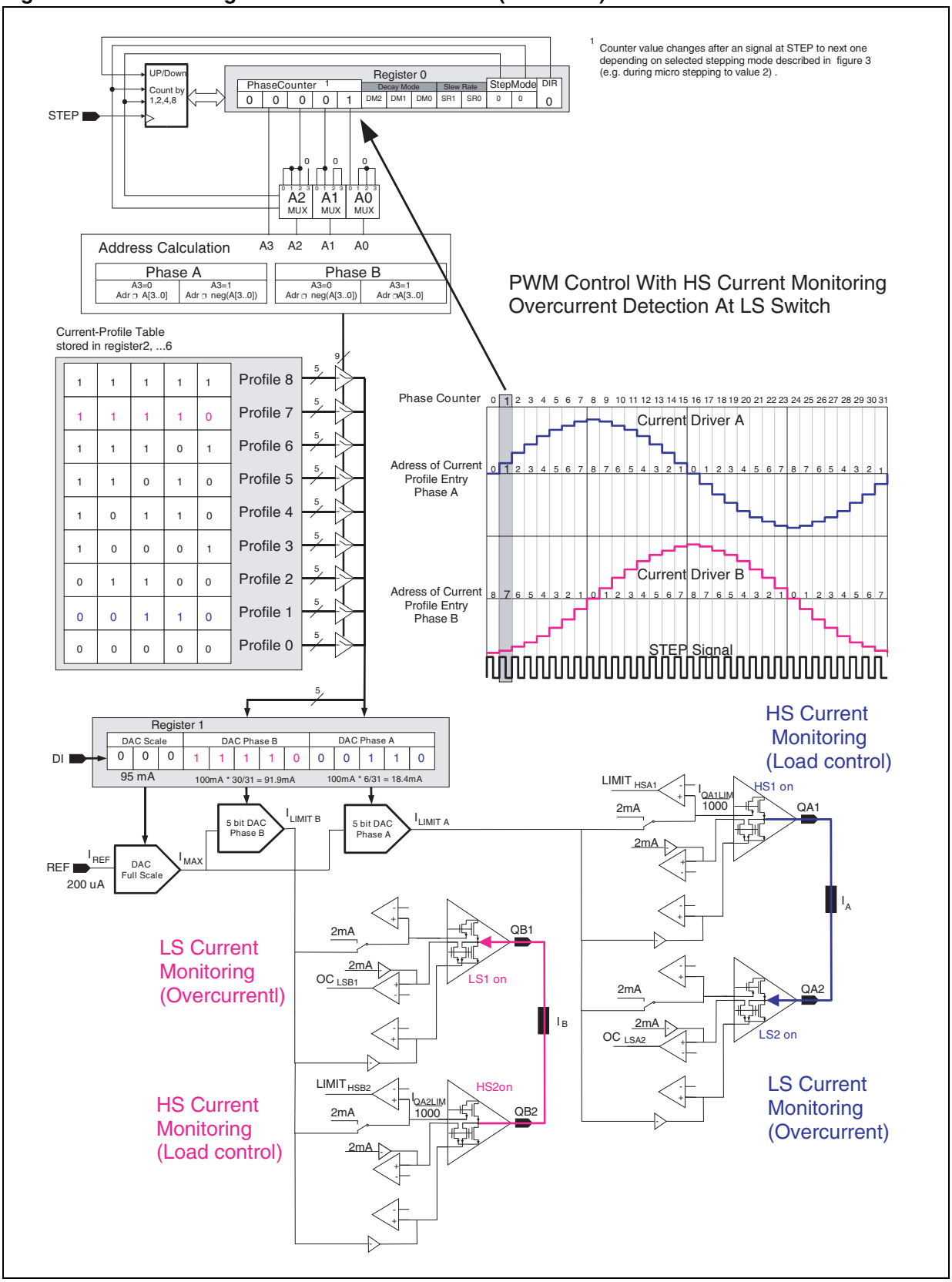
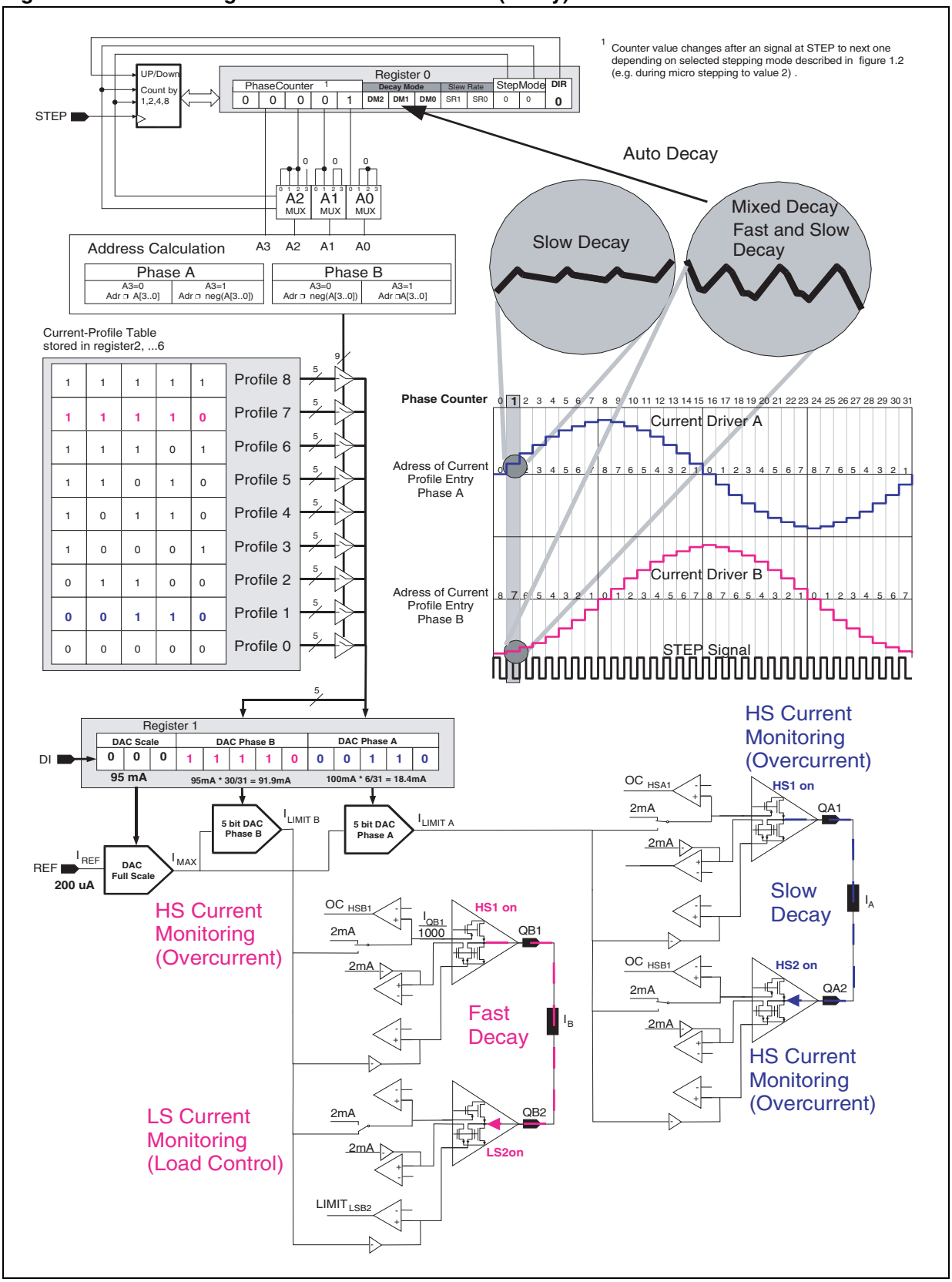


Figure 17. Reference generation for PWM control (decay)



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

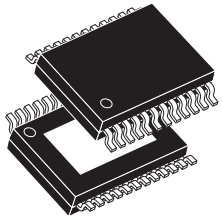
ECOPACK® is an ST trademark.

Figure 18. PowerSSO24 mechanical data and package dimensions

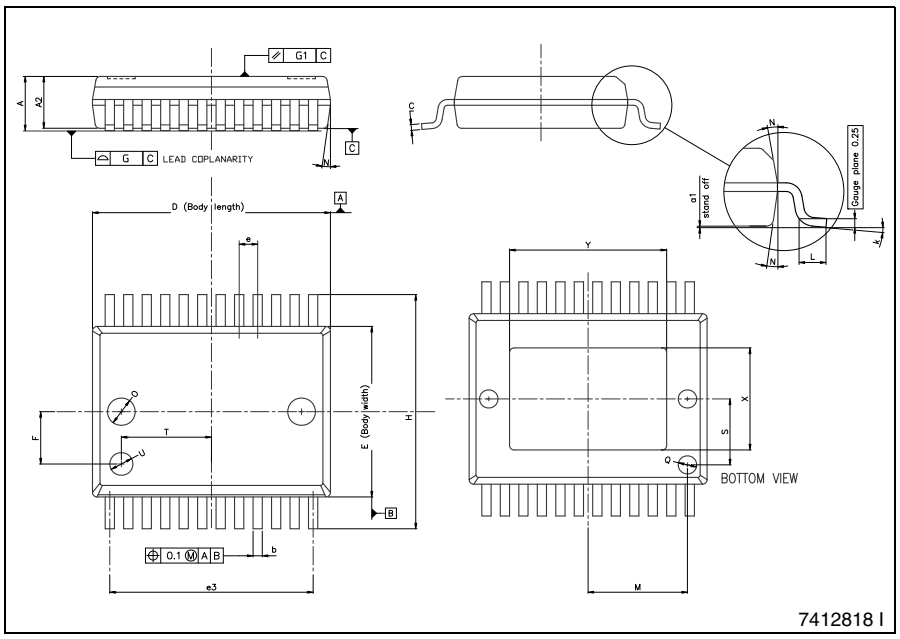
Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.45			0.0965
A2	2.15		2.35	0.084		0.0925
a1	0		0.10	0		0.003
b	0.33		0.51	0.013		0.020
c	0.23		0.32	0.009		0.012
D (1)	10.10		10.50	0.398		0.413
E (1)	7.40		7.60	0.291		0.299
e		0.80			0.031	
e3		8.80			0.346	
F		2.30			0.090	
G			0.10			0.004
G1			0.06			0.002
H	10.10		10.50	0.398		0.413
h			0.40			0.016
k	0° (min.), 8° (max.)					
L	0.55		0.85	0.0217		0.0335
O		1.20				0.047
Q		0.80				0.031
S		2.90				0.114
T		3.65				0.143
U		1.0				0.039
N	10° (max)					
X	4.10		4.70	0.161		0.185
Y	6.50 4.90(4)		7.10 5.50(4)	0.256 0.192(4)		0.279 0.216(4)

(1) "D and E1" do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006")
(2) No intrusion allowed inwards the leads.
(3) Flash or bleeds on exposed die pad shall not exceed 0.4 mm per side
(4) Variation for small window leadframe option.

OUTLINE AND MECHANICAL DATA



PowerSSO24 (Exposed pad down)



9 Revision history

Table 27. Document revision history

Date	Revision	Changes
10-Nov-2005	1	Initial release.
04-May-2006	2	Feature list updated. Part numbers updated.
21-Sep-2006	3	Feature list updated. *Table 21 on page 28* updated.
09-Jul-2007	4	Updated the order codes (see *Table 1: Device summary on page 1*). Changed the status from Preliminary data to Datasheet.
02-Feb-2009	5	Updated the following tables: *2*, *9*, *14*, *15*, *16*, *17*, *18*, *19* and *20*. Updated the following chapters: *2.4*, *5.1*, *5.2*, *5.3*, *5.4*, *5.5*, *5.6* and *5.7*.
15-May-2009	6	Updated *Figure 18: PowerSSO24 mechanical data and package dimensions on page 38*.
19-Sep-2013	7	Updated Disclaimer.

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